

High-Speed CMOS Logic Quad D-Type Flip-Flop, Three-State

Features

- Three-State Buffered Outputs
- Gated Input and Output Enables
- Fanout (Over Temperature Range)
 - Standard Outputs 10 LSTTL Loads
 - Bus Driver Outputs 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
 - 2V to 6V Operation
 - High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} at $V_{CC} = 5V$
- HCT Types
 - 4.5V to 5.5V Operation
 - Direct LSTTL Input Logic Compatibility, $V_{IL} = 0.8V$ (Max), $V_{IH} = 2V$ (Min)
 - CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL} , V_{OH}

Description

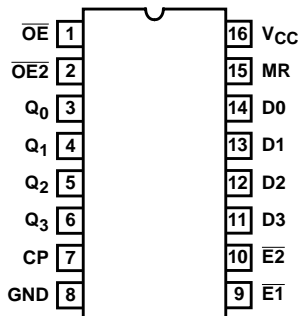
The 'HC173 and 'HCT173 high speed three-state quad D-type flip-flops are fabricated with silicon gate CMOS technology. They possess the low power consumption of standard CMOS Integrated circuits, and can operate at speeds comparable to the equivalent low power Schottky devices. The buffered outputs can drive 15 LSTTL loads. The large output drive capability and three-state feature make these parts ideally suited for interfacing with bus lines in bus oriented systems.

The four D-type flip-flops operate synchronously from a common clock. The outputs are in the three-state mode when either of the two output disable pins are at the logic "1" level. The input ENABLES allow the flip-flops to remain in their present states without having to disrupt the clock. If either of the 2 input ENABLES are taken to a logic "1" level, the Q outputs are fed back to the inputs, forcing the flip-flops to remain in the same state. Reset is enabled by taking the MASTER RESET (MR) input to a logic "1" level. The data outputs change state on the positive going edge of the clock.

The 'HCT173 logic family is functionally, as well as pin compatible with the standard LS logic family.

Pinout

CD54HC173, CD54HCT173
(CERDIP)
CD74HC173
(PDIP, SOIC, SOP, TSSOP)
CD74HCT173
(PDIP, SOIC)
TOP VIEW

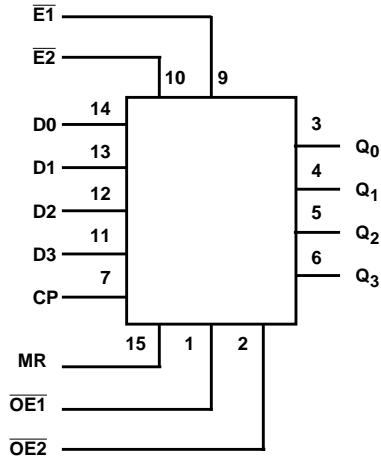


Ordering Information

| PART NUMBER | TEMP. RANGE (°C) | PACKAGE |
|---------------|------------------|--------------|
| CD54HC173F3A | -55 to 125 | 16 Ld CERDIP |
| CD54HCT173F3A | -55 to 125 | 16 Ld CERDIP |
| CD74HC173E | -55 to 125 | 16 Ld PDIP |
| CD74HC173M | -55 to 125 | 16 Ld SOIC |
| CD74HC173MT | -55 to 125 | 16 Ld SOIC |
| CD74HC173M96 | -55 to 125 | 16 Ld SOIC |
| CD74HC173NSR | -55 to 125 | 16 Ld SOP |
| CD74HC173PW | -55 to 125 | 16 Ld TSSOP |
| CD74HC173PWR | -55 to 125 | 16 Ld TSSOP |
| CD74HC173PWT | -55 to 125 | 16 Ld TSSOP |
| CD74HCT173E | -55 to 125 | 16 Ld PDIP |
| CD74HCT173M | -55 to 125 | 16 Ld SOIC |
| CD74HCT173MT | -55 to 125 | 16 Ld SOIC |
| CD74HCT173M96 | -55 to 125 | 16 Ld SOIC |

NOTE: When ordering, use the entire part number. The suffixes 96 and R denote tape and reel. The suffix T denotes a small-quantity reel of 250.

Functional Diagram



TRUTH TABLE

| INPUTS | | | | DATA D | OUTPUT Q _n |
|--------|----|-----------------|-----------------|-----------|--------------------------|
| MR | CP | DATA ENABLE | | | |
| | | $\overline{E1}$ | $\overline{E2}$ | | |
| H | X | X | X | X | L |
| L | L | X | X | X | Q ₀ |
| L | ↑ | H | X | X | Q ₀ |
| L | ↑ | X | H | X | Q ₀ |
| L | ↑ | L | L | L | L |
| L | ↑ | L | L | H | H |

H= High Voltage Level

L = Low Voltage Level

X= Irrelevant

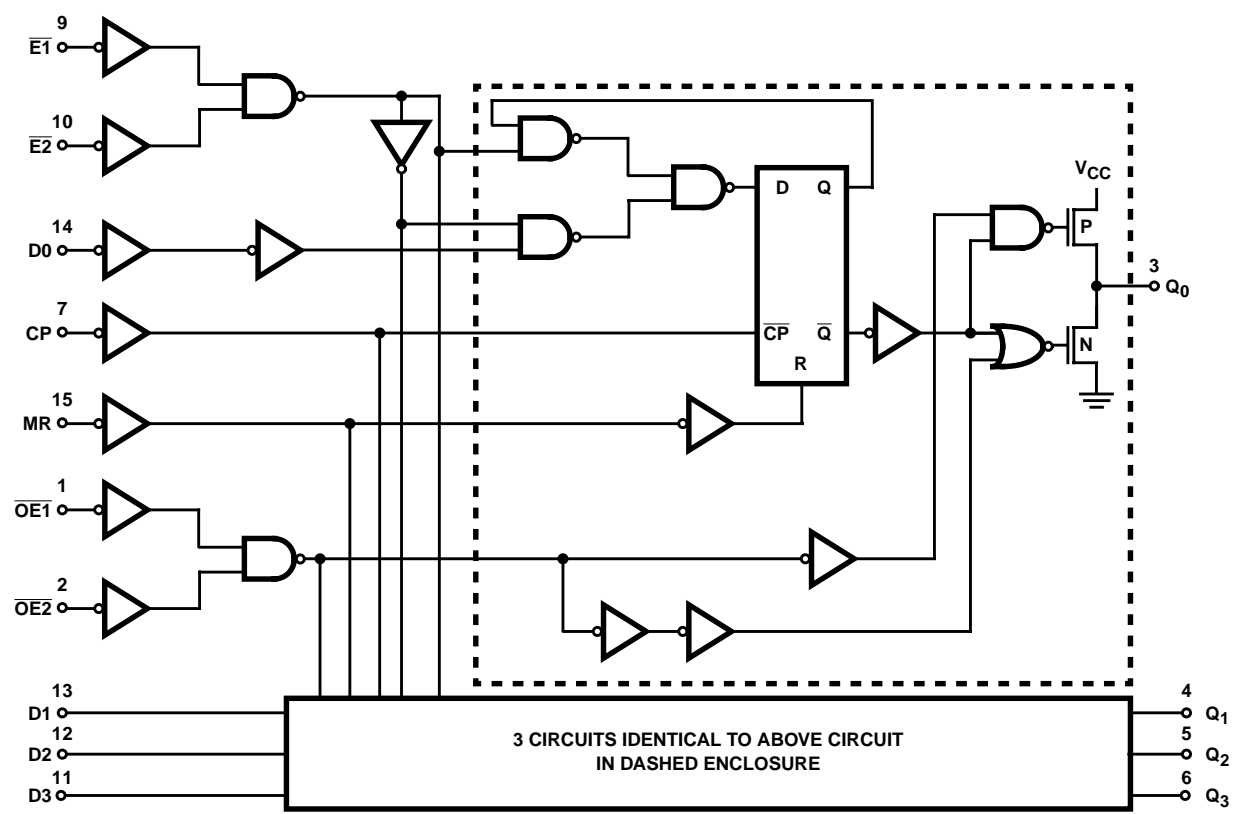
↑= Transition from Low to High Level

Q₀= Level Before the Indicated Steady-State Input Conditions Were Established

NOTE:

1. When either OE1 or OE2 (or both) is (are) high, the output is disabled to the high-impedance state, however, sequential operation of the flip-flops is not affected.

Logic Diagram



CD54HC173, CD74HC173, CD54HCT173, CD74HCT173

Absolute Maximum Ratings

| | |
|--|-------------|
| DC Supply Voltage, V_{CC} | -0.5V to 7V |
| DC Input Diode Current, I_{IK} | |
| For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ | $\pm 20mA$ |
| DC Output Diode Current, I_{OK} | |
| For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ | $\pm 20mA$ |
| DC Output Source or Sink Current per Output Pin, I_O | |
| For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ | $\pm 25mA$ |
| DC V_{CC} or Ground Current, I_{CC} | $\pm 70mA$ |

Thermal Information

| | |
|--|----------------|
| Package Thermal Impedance, θ_{JA} (see Note 2): | |
| E (PDIP) Package | 67°C/W |
| M (SOIC) Package | 73°C/W |
| NS (SOP) Package | 64°C/W |
| PW (TSSOP) Package | 108°C/W |
| Maximum Junction Temperature | 150°C |
| Maximum Storage Temperature Range | -65°C to 150°C |
| Maximum Lead Temperature (Soldering 10s) | 300°C |
| (SOIC - Lead Tips Only) | |

Operating Conditions

| | |
|--|----------------|
| Temperature Range (T_A) | -55°C to 125°C |
| Supply Voltage Range, V_{CC} | |
| HC Types | .2V to 6V |
| HCT Types | 4.5V to 5.5V |
| DC Input or Output Voltage, V_I, V_O | 0V to V_{CC} |
| Input Rise and Fall Time | |
| 2V | 1000ns (Max) |
| 4.5V | 500ns (Max) |
| 6V | 400ns (Max) |

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

| PARAMETER | SYMBOL | TEST CONDITIONS | | V_{CC} (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|----------|-------------------------|------------|--------------|------|-----|-----------|---------------|---------|----------------|---------|---------|
| | | V_I (V) | I_O (mA) | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| HC TYPES | | | | | | | | | | | | |
| High Level Input Voltage | V_{IH} | - | - | 2 | 1.5 | - | - | 1.5 | - | 1.5 | - | V |
| | | | | 4.5 | 3.15 | - | - | 3.15 | - | 3.15 | - | V |
| | | | | 6 | 4.2 | - | - | 4.2 | - | 4.2 | - | V |
| Low Level Input Voltage | V_{IL} | - | - | 2 | - | - | 0.5 | - | 0.5 | - | 0.5 | V |
| | | | | 4.5 | - | - | 1.35 | - | 1.35 | - | 1.35 | V |
| | | | | 6 | - | - | 1.8 | - | 1.8 | - | 1.8 | V |
| High Level Output Voltage CMOS Loads | V_{OH} | V_{IH} or V_{IL} | -0.02 | 2 | 1.9 | - | - | 1.9 | - | 1.9 | - | V |
| | | | -0.02 | 4.5 | 4.4 | - | - | 4.4 | - | 4.4 | - | V |
| | | | -0.02 | 6 | 5.9 | - | - | 5.9 | - | 5.9 | - | V |
| | | | -6 | 4.5 | 3.98 | - | - | 3.84 | - | 3.7 | - | V |
| High Level Output Voltage TTL Loads | | | -7.8 | 6 | 5.48 | - | - | 5.34 | - | 5.2 | - | V |
| Low Level Output Voltage CMOS Loads | V_{OL} | V_{IH} or V_{IL} | 0.02 | 2 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 0.02 | 4.5 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 0.02 | 6 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 6 | 4.5 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| Low Level Output Voltage TTL Loads | | | 7.8 | 6 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| Input Leakage Current | I_I | V_{CC} or GND | - | 6 | - | - | ± 0.1 | - | ± 1 | - | ± 1 | μA |
| Quiescent Device Current | I_{CC} | V_{CC} or GND | 0 | 6 | - | - | 8 | - | 80 | - | 160 | μA |

CD54HC173, CD74HC173, CD54HCT173, CD74HCT173

DC Electrical Specifications (Continued)

| PARAMETER | SYMBOL | TEST CONDITIONS | | V _{CC} (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|--|------------------------------|------------------------------------|---------------------|---------------------|------|-----|------|---------------|------|----------------|-----|-------|
| | | V _I (V) | I _O (mA) | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| Three-State Leakage Current | I _{OZ} | V _{IL} or V _{IH} | - | 6 | - | - | ±0.5 | - | ±0.5 | - | ±10 | μA |
| HCT TYPES | | | | | | | | | | | | |
| High Level Input Voltage | V _{IH} | - | - | 4.5 to 5.5 | 2 | - | - | 2 | - | 2 | - | V |
| Low Level Input Voltage | V _{IL} | - | - | 4.5 to 5.5 | - | - | 0.8 | - | 0.8 | - | 0.8 | V |
| High Level Output Voltage CMOS Loads | V _{OH} | V _{IH} or V _{IL} | -0.02 | 4.5 | 4.4 | - | - | 4.4 | - | 4.4 | - | V |
| High Level Output Voltage TTL Loads | | | -6 | 4.5 | 3.98 | - | - | 3.84 | - | 3.7 | - | V |
| Low Level Output Voltage CMOS Loads | V _{OL} | V _{IH} or V _{IL} | 0.02 | 4.5 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| Low Level Output Voltage TTL Loads | | | 6 | 4.5 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| Input Leakage Current | I _I | V _{CC} to GND | 0 | 5.5 | - | - | ±0.1 | - | ±1 | - | ±1 | μA |
| Quiescent Device Current | I _{CC} | V _{CC} or GND | 0 | 5.5 | - | - | 8 | - | 80 | - | 160 | μA |
| Additional Quiescent Device Current Per Input Pin: 1 Unit Load | ΔI _{CC} (Note 3) | V _{CC} -2.1 | - | 4.5 to 5.5 | - | 100 | 360 | - | 450 | - | 490 | μA |
| Three-State Leakage Current | I _{OZ} | V _{IL} or V _{IH} | - | 5.5 | - | - | ±0.5 | - | ±5.0 | - | ±10 | μA |

NOTE:

3. For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

| INPUT | UNIT LOADS |
|-----------------------------|------------|
| D0-D3 | 0.15 |
| $\bar{E}1$ and $\bar{E}2$ | 0.15 |
| CP | 0.25 |
| MR | 0.2 |
| $\bar{OE}1$ and $\bar{OE}2$ | 0.5 |

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Specifications table, e.g., 360μA max at 25°C.

CD54HC173, CD74HC173, CD54HCT173, CD74HCT173

Switching Specifications Input $t_r, t_f = 6\text{ns}$

| PARAMETER | SYMBOL | TEST CONDITIONS | V_{CC} (V) | 25°C | | -40°C TO 85°C | -55°C TO 125°C | UNITS |
|---|--|---------------------|--------------|------|-----|---------------|----------------|-------|
| | | | | TYP | MAX | MAX | MAX | |
| HC TYPES | | | | | | | | |
| Propagation Delay, Clock to Output | t_{PLH}, t_{PHL} | $C_L = 50\text{pF}$ | 2 | - | 200 | 250 | 300 | ns |
| | | | 4.5 | - | 40 | 50 | 60 | ns |
| | | $C_L = 15\text{pF}$ | 5 | 17 | - | - | - | ns |
| | | $C_L = 50\text{pF}$ | 6 | - | 34 | 43 | 51 | ns |
| Propagation Delay, MR to Output | t_{PHL} | $C_L = 50\text{pF}$ | 2 | - | 175 | 220 | 265 | ns |
| | | | 4.5 | - | 35 | 44 | 53 | ns |
| | | $C_L = 15\text{pF}$ | 5 | 12 | - | - | - | ns |
| | | $C_L = 50\text{pF}$ | 6 | - | 30 | 37 | 45 | ns |
| Propagation Delay Output Enable to Q (Figure 6) | t_{PLZ}, t_{PHZ} t_{PZL}, t_{PZH} | $C_L = 50\text{pF}$ | 2 | - | 150 | 190 | 225 | ns |
| | | $C_L = 50\text{pF}$ | 4.5 | - | 30 | 38 | 45 | ns |
| | | $C_L = 15\text{pF}$ | 5 | 12 | - | - | - | ns |
| | | $C_L = 50\text{pF}$ | 6 | - | 26 | 33 | 38 | ns |
| Output Transition Times | t_{TLH}, t_{THL} | $C_L = 50\text{pF}$ | 2 | - | 60 | 75 | 90 | ns |
| | | | 4.5 | - | 12 | 15 | 18 | ns |
| | | | 6 | - | 10 | 13 | 15 | ns |
| Maximum Clock Frequency | f_{MAX} | $C_L = 15\text{pF}$ | 5 | 60 | - | - | - | MHz |
| Input Capacitance | C_{IN} | - | - | - | 10 | 10 | 10 | pF |
| Three-State Output Capacitance | C_O | - | - | - | 10 | 10 | 10 | pF |
| Power Dissipation Capacitance (Notes 4, 5) | C_{PD} | - | 5 | 29 | - | - | - | pF |
| HCT TYPES | | | | | | | | |
| Propagation Delay, Clock to Output | t_{PLH}, t_{PHL} | $C_L = 50\text{pF}$ | 4.5 | - | 40 | 50 | 60 | ns |
| | | $C_L = 15\text{pF}$ | 5 | 17 | - | - | - | ns |
| Propagation Delay, MR to Output | t_{PHL} | $C_L = 50\text{pF}$ | 4.5 | - | 44 | 55 | 66 | ns |
| | | $C_L = 15\text{pF}$ | 5 | 18 | - | - | - | ns |
| Propagation Delay Output Enable to Q (Figure 6) | t_{PZL}, t_{PZH} | $C_L = 50\text{pF}$ | 2 | - | 150 | 190 | 225 | ns |
| | | $C_L = 50\text{pF}$ | 4.5 | - | 30 | 38 | 45 | ns |
| | | $C_L = 15\text{pF}$ | 5 | 14 | - | - | - | ns |
| | | $C_L = 50\text{pF}$ | 6 | - | 26 | 33 | 38 | ns |
| Output Transition Times | t_{TLH}, t_{THL} | $C_L = 50\text{pF}$ | 4.5 | - | 15 | 19 | 22 | ns |
| Maximum Clock Frequency | f_{MAX} | $C_L = 15\text{pF}$ | 5 | 60 | - | - | - | MHz |
| Input Capacitance | C_{IN} | - | - | - | 10 | 10 | 10 | pF |
| Power Dissipation Capacitance (Notes 4, 5) | C_{PD} | - | 5 | 34 | - | - | - | pF |

NOTES:

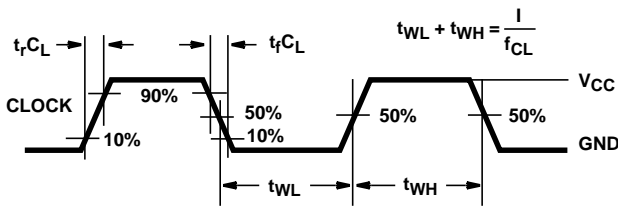
- C_{PD} is used to determine the dynamic power consumption, per package.
- $P_D = V_{CC}^2 f_i + \sum (C_L V_{CC}^2 + f_O)$ where f_i = Input Frequency, f_O = Output Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

CD54HC173, CD74HC173, CD54HCT173, CD74HCT173

Prerequisite For Switching Specifications

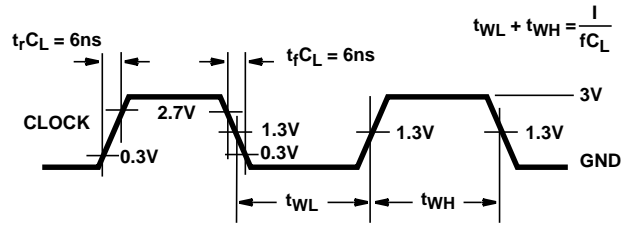
| PARAMETER | SYMBOL | V _{CC} (V) | 25°C | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|---|------------------|---------------------|------|-----|---------------|-----|----------------|-----|-------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| HC TYPES | | | | | | | | | |
| Maximum Clock Frequency | f _{MAX} | 2 | 6 | - | 5 | - | 4 | - | MHz |
| | | 4.5 | 30 | - | 24 | - | 20 | - | MHz |
| | | 6 | 35 | - | 28 | - | 24 | - | MHz |
| MR Pulse Width | t _w | 2 | 80 | - | 100 | - | 120 | - | ns |
| | | 4.5 | 16 | - | 20 | - | 24 | - | ns |
| | | 6 | 14 | - | 17 | - | 20 | - | ns |
| Clock Pulse Width | t _w | 2 | 80 | - | 100 | - | 120 | - | ns |
| | | 4.5 | 16 | - | 20 | - | 24 | - | ns |
| | | 6 | 14 | - | 17 | - | 20 | - | ns |
| Set-up Time, Data to Clock and \bar{E} to Clock | t _{SU} | 2 | 60 | - | 75 | - | 90 | - | ns |
| | | 4.5 | 12 | - | 15 | - | 18 | - | ns |
| | | 6 | 10 | - | 13 | - | 15 | - | ns |
| Hold Time, Data to Clock | t _H | 2 | 3 | - | 3 | - | 3 | - | ns |
| | | 4.5 | 3 | - | 3 | - | 3 | - | ns |
| | | 6 | 3 | - | 3 | - | 3 | - | ns |
| Hold Time, \bar{E} to Clock | t _H | 2 | 0 | - | 0 | - | 0 | - | ns |
| | | 4.5 | 0 | - | 0 | - | 0 | - | ns |
| | | 6 | 0 | - | 0 | - | 0 | - | ns |
| Removal Time, MR to Clock | t _{REM} | 2 | 60 | - | 75 | - | 90 | - | ns |
| | | 4.5 | 12 | - | 15 | - | 18 | - | ns |
| | | 6 | 10 | - | 13 | - | 15 | - | ns |
| HCT TYPES | | | | | | | | | |
| Maximum Clock Frequency | f _{MAX} | 4.5 | 20 | - | 16 | - | 13 | - | MHz |
| MR Pulse Width | t _w | 4.5 | 15 | - | 19 | - | 22 | - | ns |
| Clock Pulse Width | t _w | 4.5 | 25 | - | 31 | - | 38 | - | ns |
| Set-up Time, \bar{E} to Clock | t _{SU} | 4.5 | 12 | - | 15 | - | 18 | - | ns |
| Set-up Time, Data to Clock | t _{SU} | 4.5 | 18 | - | 23 | - | 27 | - | ns |
| Hold Time, Data to Clock | t _H | 4.5 | 0 | - | 0 | - | 0 | - | ns |
| Hold Time, \bar{E} to Clock | t _H | 4.5 | 0 | - | 0 | - | 0 | - | ns |
| Removal Time, MR to Clock | t _{REM} | 4.5 | 12 | - | 15 | - | 18 | - | ns |

Test Circuits and Waveforms



NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX} , input duty cycle = 50%.

FIGURE 1. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH



NOTE: Outputs should be switching from 10% V_{CC} to 90% V_{CC} in accordance with device truth table. For f_{MAX} , input duty cycle = 50%.

FIGURE 2. HCT CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH

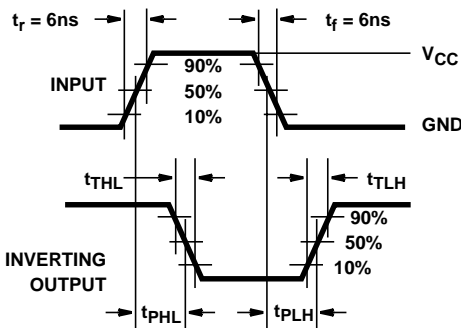


FIGURE 3. HC AND HCU TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

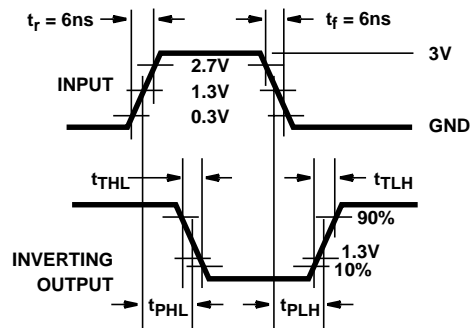


FIGURE 4. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

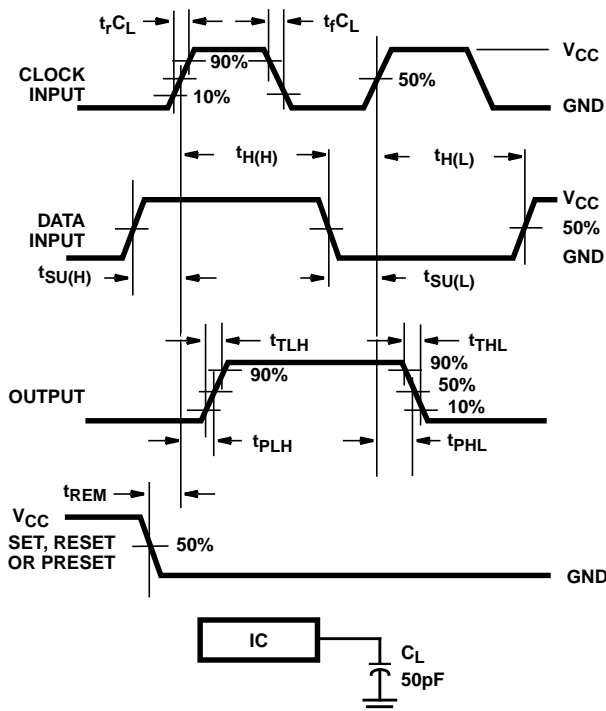


FIGURE 5. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

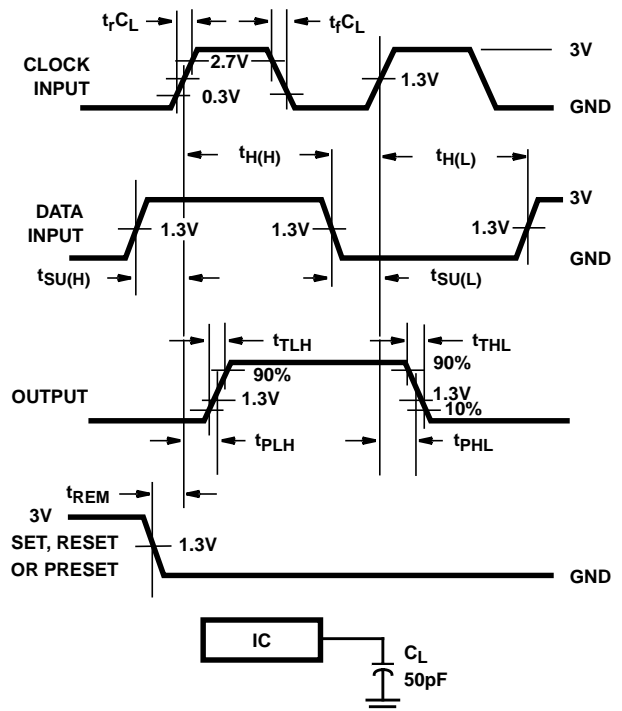


FIGURE 6. HCT SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

Test Circuits and Waveforms (Continued)

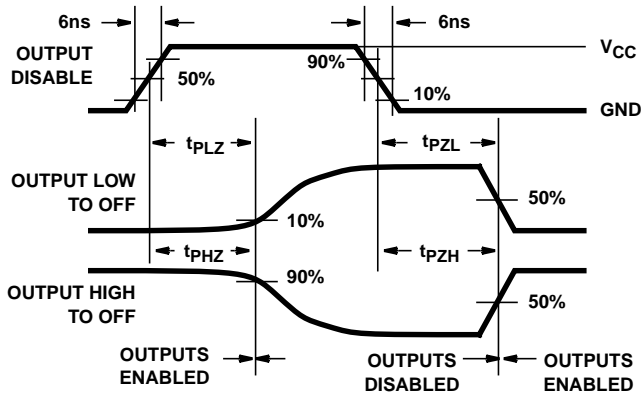


FIGURE 7. HC THREE-STATE PROPAGATION DELAY WAVEFORM

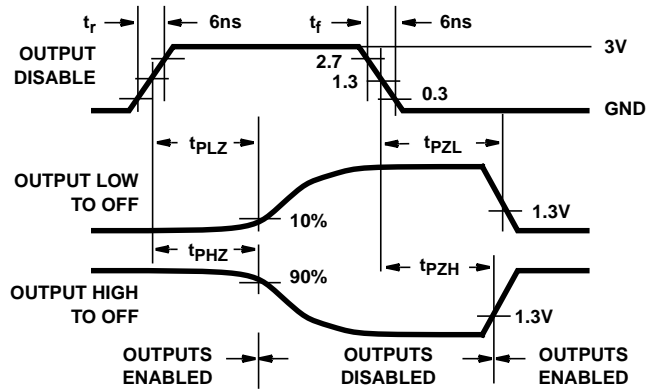


FIGURE 8. HCT THREE-STATE PROPAGATION DELAY WAVEFORM



NOTE: Open drain waveforms t_{PLZ} and t_{PZH} are the same as those for three-state shown on the left. The test circuit is Output $R_L = 1k\Omega$ to V_{CC} , $C_L = 50pF$.

FIGURE 9. HC AND HCT THREE-STATE PROPAGATION DELAY TEST CIRCUIT

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/ Ball Finish | MSL Peak Temp ⁽³⁾ | Samples (Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|----------------------------|----------------------|------------------------------|-----------------------------|
| 5962-8682501EA | ACTIVE | CDIP | J | 16 | 1 | TBD | Call TI | Call TI | |
| 5962-8875901EA | ACTIVE | CDIP | J | 16 | 1 | TBD | Call TI | Call TI | |
| CD54HC173F | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | |
| CD54HC173F3A | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | |
| CD54HCT173F3A | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | |
| CD74HC173E | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | |
| CD74HC173EE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | |
| CD74HC173M | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| CD74HC173M96 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| CD74HC173M96E4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| CD74HC173M96G4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| CD74HC173ME4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| CD74HC173MG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| CD74HC173MT | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| CD74HC173MTE4 | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| CD74HC173MTG4 | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| CD74HC173PW | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| CD74HC173PWE4 | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| CD74HC173PWG4 | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| CD74HC173PWR | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/ Ball Finish | MSL Peak Temp ⁽³⁾ | Samples (Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|----------------------|------------------------------|-----------------------------|
| CD74HC173PWRE4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| CD74HC173PWRG4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| CD74HC173PWT | ACTIVE | TSSOP | PW | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| CD74HC173PWTE4 | ACTIVE | TSSOP | PW | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| CD74HC173PWTG4 | ACTIVE | TSSOP | PW | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| CD74HCT173E | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | |
| CD74HCT173EE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | |
| CD74HCT173M | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| CD74HCT173M96 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| CD74HCT173M96E4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| CD74HCT173M96G4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| CD74HCT173ME4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| CD74HCT173MG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| CD74HCT173MT | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| CD74HCT173MTE4 | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| CD74HCT173MTG4 | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF CD54HC173, CD54HCT173, CD74HC173, CD74HCT173 :

● Catalog: [CD74HC173](#), [CD74HCT173](#)

● Military: [CD54HC173](#), [CD54HCT173](#)

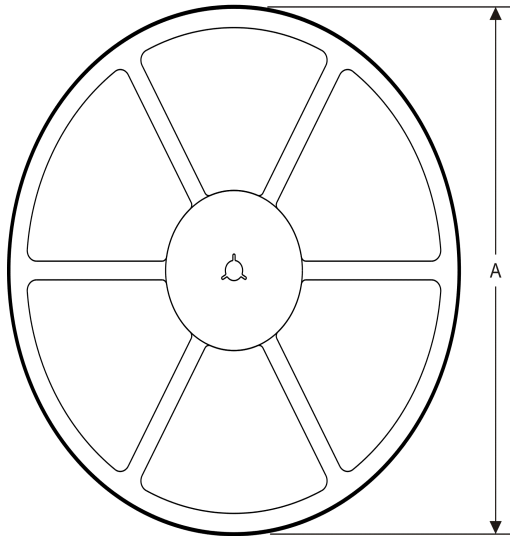
NOTE: Qualified Version Definitions:

● Catalog - TI's standard catalog product

● Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

TAPE AND REEL INFORMATION

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD74HC173M96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| CD74HC173PWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| CD74HC173PWT | TSSOP | PW | 16 | 250 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| CD74HCT173M96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD74HC173M96 | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| CD74HC173PWR | TSSOP | PW | 16 | 2000 | 367.0 | 367.0 | 35.0 |
| CD74HC173PWT | TSSOP | PW | 16 | 250 | 367.0 | 367.0 | 35.0 |
| CD74HCT173M96 | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - (C) Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - (D) The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040064-4/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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