# ATA8203/ATA8204/ATA8205

## Industrial UHF ASK/FSK Receiver

**DATASHEET**

## Features

- Frequency receiving range of (3 versions)
  - $f_0$ = 312.5MHz to 317.5MHz or
  - $f_0$ = 431.5MHz to 436.5MHz or
  - $f_0$ = 868MHz to 870MHz
- 30dB image rejection
- Receiving bandwidth
  - $B_{IF}$ = 300kHz for 315MHz/433MHz version
  - $B_{IF}$ = 600kHz for 868MHz version
- Fully integrated LC-VCO and PLL loop filter
- Very high sensitivity with power matched LNA
  - Atmel® ATA8203/ATA8204:
    - –107dBm, FSK, BR_0 (1.0Kbit/s to 1.8Kbit/s), Manchester, BER 10E-3
    - –113dBm, ASK, BR_0 (1.0Kbit/s to 1.8Kbit/s), Manchester, BER 10E-3
  - Atmel ATA8205:
    - –105dBm, FSK, BR_0 (1.0Kbit/s to 1.8Kbit/s), Manchester, BER 10E-3
    - –111dBm, ASK, BR_0 (1.0Kbit/s to 1.8Kbit/s), Manchester, BER 10E-3
- High system IIP3
  - –18dBm at 868MHz
  - –23dBm at 433MHz
  - –24dBm at 315MHz
- System 1-dB compression point
  - –27.7dBm at 868MHz
  - –32.7dBm at 433MHz
  - –33.7dBm at 315MHz
- High large-signal capability at GSM band (blocking –33dBm at +10MHz, IIP3 = –24dBm at +20MHz)
- Logarithmic RSSI output
- XTO start-up with negative resistor of 1.5kΩ
- 5V to 20V automotive compatible data interface
- Data clock available for manchester and bi-phase-coded signals
- Programmable digital noise suppression
- Low power consumption due to configurable polling

- Temperature range –40°C to +85°C
- ESD protection 2kV HBM, All pins
- Communication to microcontroller possible using a single bi-directional data line
- Low-cost solution due to high integration level with minimum external circuitry requirements
- Supply voltage range 4.5V to 5.5V

## Benefits

- Low BOM list due to high integration
- Use of low-cost 13MHz crystal
- Lowest average current consumption for application due to self polling feature
- Reuse of Atmel ATA5743 software
- World-wide coverage with one PCB due to 3 versions are pin compatible

# 1. Description

The Atmel® ATA8203/ATA8204/ATA8205 is a multi-chip PLL receiver device supplied in an SSO20 package. It has been specially developed for the demands of RF low-cost data transmission systems with data rates from 1Kbit/s to 10Kbit/s in Manchester or Bi-phase code. Its main applications are in the areas of aftermarket keyless entry systems, and tire pressure monitoring systems, telemetering, consumer/industrial remote control applications, home entertainment, access control systems, and security technology systems. It can be used in the frequency receiving range of $f_0$ = 312.5MHz to 317.5MHz, $f_0$ = 431.5MHz to 436.5MHz or $f_0$ = 868MHz to 870MHz for ASK or FSK data transmission. All the statements made below refer to 315MHz, 433MHz and 868.3MHz applications.

**Figure 1-1. System Block Diagram**

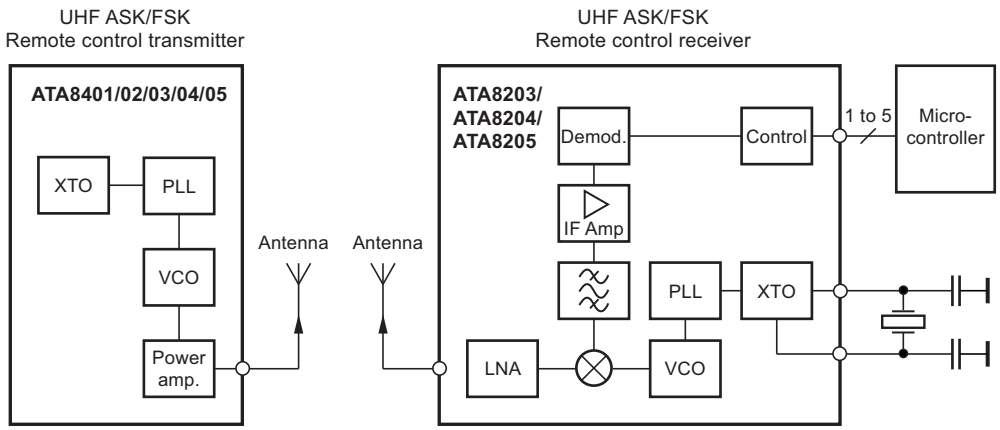
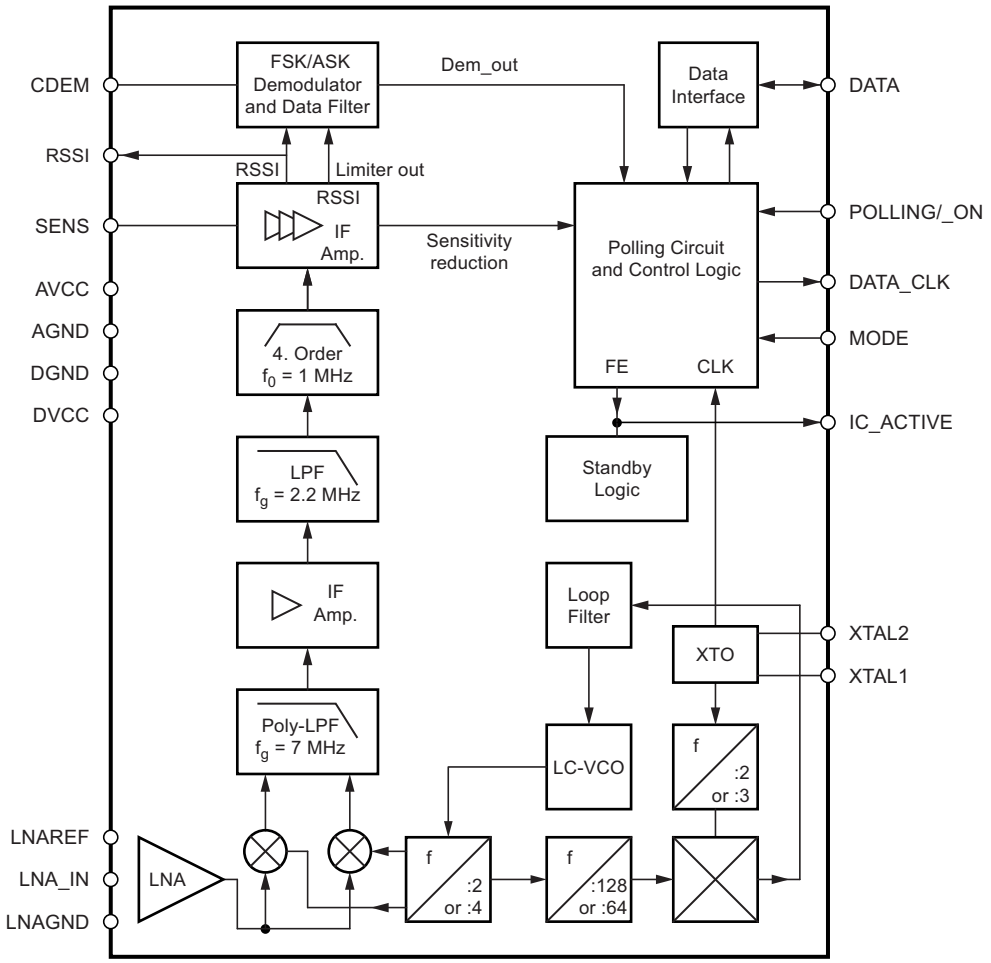


**Figure 1-2. Block Diagram**



# 2. Pin Configuration

**Figure 2-1. Pinning SSO20**

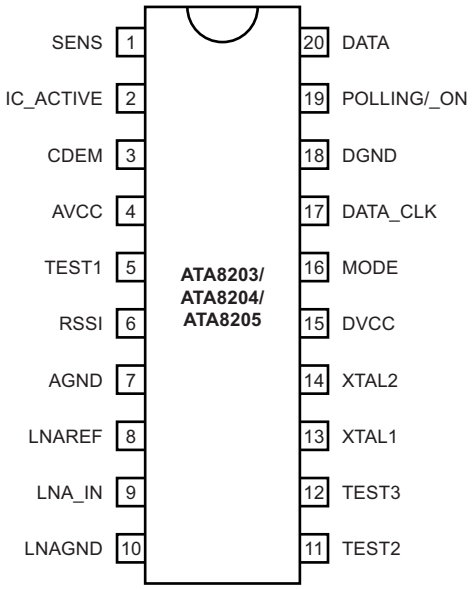



**Table 2-1. Pin Description**

| Pin | Symbol | Function |
|---|---|---|
| 1 | SENS | Sensitivity-control resistor |
| 2 | IC_ACTIVE | IC condition indicator: Low = sleep mode, High = active mode |
| 3 | CDEM | Lower cut-off frequency data filter |
| 4 | AVCC | Analog power supply |
| 5 | TEST 1 | Test pin, during operation at GND |
| 6 | RSSI | RSSI output |
| 7 | AGND | Analog ground |
| 8 | LNAREF | High-frequency reference node LNA and mixer |
| 9 | LNA_IN | RF input |
| 10 | LNAGND | DC ground LNA and mixer |
| 11 | TEST 2 | Do not connect during operating |
| 12 | TEST 3 | Test pin, during operation at GND |
| 13 | XTAL1 | Crystal oscillator XTAL connection 1 |
| 14 | XTAL2 | Crystal oscillator XTAL connection 2 |
| 15 | DVCC | Digital power supply |
| 16 | MODE | Selecting 315MHz/other versions<br>Low: 315MHz version (Atmel ATA8203)<br>High: 433MHz/868MHz versions (Atmel ATA8204/ATA8205) |
| 17 | DATA_CLK | Bit clock of data stream |
| 18 | DGND | Digital ground |
| 19 | POLLING/_ON | Selects polling or receiving mode; Low: receiving mode, High: polling mode |
| 20 | DATA | Data output/configuration input |

# 3. RF Front-end

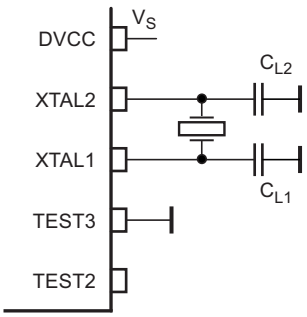
The RF front-end of the receiver is a low-IF heterodyne configuration that converts the input signal into about 1MHz IF signal with a typical image rejection of 30dB. According to Figure Figure 1-2 on page 4 the front-end consists of an LNA (Low Noise Amplifier), LO (Local Oscillator), I/Q mixer, polyphase low-pass filter and an IF amplifier.

The PLL generates the drive frequency $f_{LO}$ for the mixer using a fully integrated synthesizer with integrated low noise LC-VCO (Voltage Controlled Oscillator) and PLL-loop filter. The XTO (crystal oscillator) generates the reference frequency $f_{REF} = f_{XTO}/2$ (868MHz and 433MHz versions) or $f_{REF} = f_{XTO}/3$ (315MHz version). The integrated LC-VCO generates two or four times the mixer drive frequency $f_{VCO}$. The I/Q signals for the mixer are generated with a divide by two or four circuit ($f_{LO} = f_{VCO}/2$ for 868MHz version, $f_{LO} = f_{VCO}/4$ for 433MHz and 315MHz versions). $f_{VCO}$ is divided by a factor of 128 or 64 and feeds into a phase frequency detector and is compared with $f_{REF}$. The output of the phase frequency detector is fed into an integrated loop filter and thereby generates the control voltage for the VCO. If $f_{LO}$ is determined, $f_{XTO}$ can be calculated using the following formula: $f_{REF} = f_{LO}/128$ for 868MHz band, $f_{REF} = f_{LO}/64$ for 433MHz bands, $f_{REF} = f_{LO}/64$ for 315MHz bands.

The XTO is a two-pin oscillator that operates at the series resonance of the quartz crystal with high current but low voltage signal, so that there is only a small voltage at the crystal oscillator frequency at pins XTAL1 and XTAL2. According to Figure 3-1, the crystal should be connected to GND with two capacitors $C_{L1}$ and $C_{L2}$ from XTAL1 and XTAL2 respectively. The value of these capacitors are recommended by the crystal supplier. Due to an inductive impedance at steady state oscillation and some PCB parasitics, a lower value of $C_{L1}$ and $C_{L2}$ is normally necessary.

The value of $C_{Lx}$ should be optimized for the individual board layout to achieve the exact value of $f_{XTO}$ and hence of $f_{LO}$. (The best way is to use a crystal with known load resonance frequency to find the right value for this capacitor.) When designing the system in terms of receiving bandwidth and local oscillator accuracy, the accuracy of the crystal and the XTO must be considered.

**Figure 3-1. XTO Peripherals**




The nominal frequency $f_{LO}$ is determined by the RF input frequency $f_{RF}$ and the IF frequency $f_{IF}$ using the following formula (low-side injection):

$f_{LO} = f_{RF} - f_{IF}$

To determine $f_{LO}$, the construction of the IF filter must be considered. The nominal IF frequency is $f_{IF}$ = 950kHz. To achieve a good accuracy of the filter corner frequencies, the filter is tuned by the crystal frequency $f_{XTO}$. This means that there is a fixed relationship between $f_{IF}$ and $f_{LO}$.

$f_{IF} = f_{LO}/318$ for the 315MHz band (Atmel® ATA8203)
$f_{IF} = f_{LO}/438$ for the 433.92MHz band (Atmel ATA8204)
$f_{IF} = f_{LO}/915$ for the 868.3MHz band (Atmel ATA8205)

The relationship is designed to achieve the nominal IF frequency of:

$f_{IF}$ = 987Hz for the 315MHz and $B_{IF}$ = 300kHz (Atmel ATA8203)
$f_{IF}$ = 987kHz for the 433.92MHz and $B_{IF}$ = 300kHz (Atmel ATA8204)
$f_{IF}$ = 947.8kHz for the 868.3MHz and $B_{IF}$ = 600kHz (Atmel ATA8205)

The RF input either from an antenna or from an RF generator must be transformed to the RF input pin LNA_IN. The input impedance of this pin is provided in the electrical parameters. The parasitic board inductances and capacitances influence the input matching. The RF receiver Atmel ATA8203/ATA8204/ATA8205 exhibits its highest sensitivity if the LNA is power matched. Because of this, matching to a SAW filter, a 50Ω or an antenna is easier.

Figure 14-1 on page 30 “Application Circuit” shows a typical input matching network for $f_{RF}$ = 315MHz, $f_{RF}$ = 433.92MHz or $f_{RF}$ = 868.3MHz to 50Ω. The input matching network shown in Table 14-2 on page 30 is the reference network for the parameters given in the electrical characteristics.

# 4. Analog Signal Processing

## 4.1 IF Filter

The signals coming from the RF front-end are filtered by the fully integrated 4th-order IF filter. The IF center frequency is:

$f_{IF}$ = 987kHz for the 315 MHz and $B_{IF}$ = 300kHz (Atmel® ATA8203)
$f_{IF}$ = 987kHz for the 433.92 MHz and $B_{IF}$ = 300kHz (Atmel ATA8204)
$f_{IF}$ = 947.9kHz for the 868.3 MHz and $B_{IF}$ = 600kHz (Atmel ATA8205)

The nominal bandwidth is 300 kHz for ATA8203 and ATA8204 and 600 kHz for ATA8205.

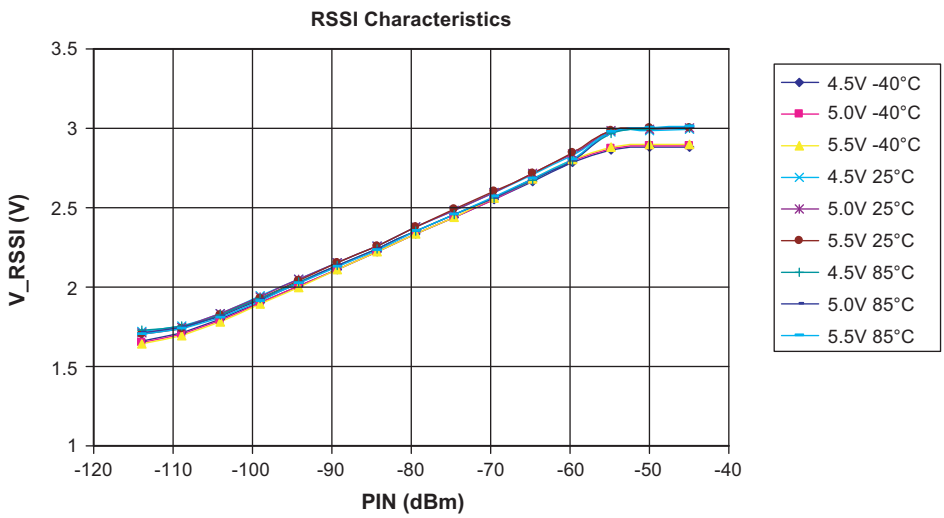
## 4.2 Limiting RSSI Amplifier

The subsequent RSSI amplifier enhances the output signal of the IF amplifier before it is fed into the demodulator. The dynamic range of this amplifier is $\Delta R_{RSSI}$ = 60dB. If the RSSI amplifier is operated within its linear range, the best S/N ratio is maintained in ASK mode. If the dynamic range is exceeded by the transmitter signal, the S/N ratio is defined by the ratio of the maximum RSSI output voltage and the RSSI output voltage due to a disturber. The dynamic range of the RSSI amplifier is exceeded if the RF input signal is approximately 60 dB higher compared to the RF input signal at full sensitivity.

The S/N ratio is not affected by the dynamic range of the RSSI amplifier in FSK mode because only the hard limited signal from a high-gain limiting amplifier is used by the demodulator.

The output voltage of the RSSI amplifier (VRSSI) is available at pin RSSI. Using the RSSI output signal, the signal strength of different transmitters can be distinguished. The usable input power range $P_{Ref}$ is –100dBm to –55dBm.

**Figure 4-1. RSSI Characteristics Atmel ATA8204**




The output voltage of the RSSI amplifier is internally compared to a threshold voltage $V_{Th_red}$. $V_{Th_red}$ is determined by the value of the external resistor $R_{Sens}$. $R_{Sens}$ is connected between pin SENS and GND or $V_S$. The output of the comparator is fed into the digital control logic. By this means, it is possible to operate the receiver at a lower sensitivity.

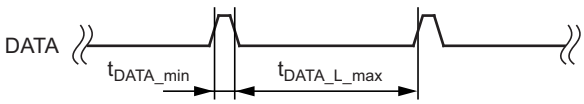
If $R_{Sens}$ is connected to GND, the receiver switches to full sensitivity. It is also possible to connect the pin SENS directly to GND to get the maximum sensitivity.

If $R_{Sens}$ is connected to $V_S$, the receiver operates at a lower sensitivity. The reduced sensitivity is defined by the value of $R_{Sens}$, and the maximum sensitivity is defined by the signal-to-noise ratio of the LNA input. The reduced sensitivity depends on the signal strength at the output of the RSSI amplifier.

Since different RF input networks may exhibit slightly different values for the LNA gain, the sensitivity values given in the electrical characteristics refer to a specific input matching. This matching is described and illustrated in Section 14. “Data Interface” on page 30.

$R_{Sens}$ can be connected to $V_S$ or GND using a microcontroller. The receiver can be switched from full sensitivity to reduced sensitivity or vice versa at any time. In polling mode, the receiver does not wake up if the RF input signal does not exceed the selected sensitivity. If the receiver is already active, the data stream at pin DATA disappears when the input signal is lower than defined by the reduced sensitivity. Instead of the data stream, the pattern according to Figure 4-2 “Steady L State Limited DATA Output Pattern” is issued at pin DATA to indicate that the receiver is still active (see Figure 13-2 on page 28 “Data Interface”).

**Figure 4-2. Steady L State Limited DATA Output Pattern**




## 4.3 FSK/ASK Demodulator and Data Filter

The signal coming from the RSSI amplifier is converted into the raw data signal by the ASK/FSK demodulator. The operating mode of the demodulator is set using the bit ASK/_FSK in the OPMODE register. Logic L sets the demodulator to FSK, applying H to ASK mode.

In ASK mode an automatic threshold control circuit (ATC) is employed to set the detection reference voltage to a value where a good signal to noise ratio is achieved. This circuit also implements the effective suppression of any kind of in-band noise signals or competing transmitters. If the S/N (ratio to suppress in-band noise signals) exceeds about 10dB the data signal can be detected properly. However, better values are found for many modulation schemes of the competing transmitter.

The FSK demodulator is intended to be used for an FSK deviation of 10kHz ≤ Δf ≤ 100kHz. The data signal in FSK mode can be detected if the S/N (ratio to suppress in-band noise signals) exceeds about 2dB. This value is valid for all modulation schemes of a disturber signal.

The output signal of the demodulator is filtered by the data filter before it is fed into the digital signal processing circuit. The data filter improves the S/N ratio as its pass-band can be adopted to the characteristics of the data signal. The data filter consists of a 1st order high-pass and a 2nd order low-pass filter.

The high-pass filter cut-off frequency is defined by an external capacitor connected to pin CDEM. The cut-off frequency of the high-pass filter is defined by the following formula:

$$\mathrm{fcu_DF} = \frac{1}{2 \times \pi \times 30\ \mathrm{k}\Omega \times \mathrm{CDEM}}$$

In self-polling mode the data filter must settle very rapidly to achieve a low current consumption. Therefore, CDEM cannot be increased to very high values if self-polling is used. On the other hand, CDEM must be large enough to meet the data filter requirements according to the data signal. Recommended values for CDEM are given in the electrical characteristics.

The cut-off frequency of the low-pass filter is defined by the selected baud-rate range (BR_Range). The BR_Range is defined in the OPMODE register (refer to Section 11. “Configuring the Receiver” on page 23). The BR_Range must be set in accordance to the baud-rate used.

The Atmel® ATA8203/ATA8204/ATA8205 is designed to operate with data coding where the DC level of the data signal is 50%. This is valid for Manchester and Bi-phase coding. If other modulation schemes are used, the DC level should always remain within the range of $V_{DC_min}$ = 33% and $V_{DC_max}$ = 66%. The sensitivity may be reduced by up to 2dB in that condition.

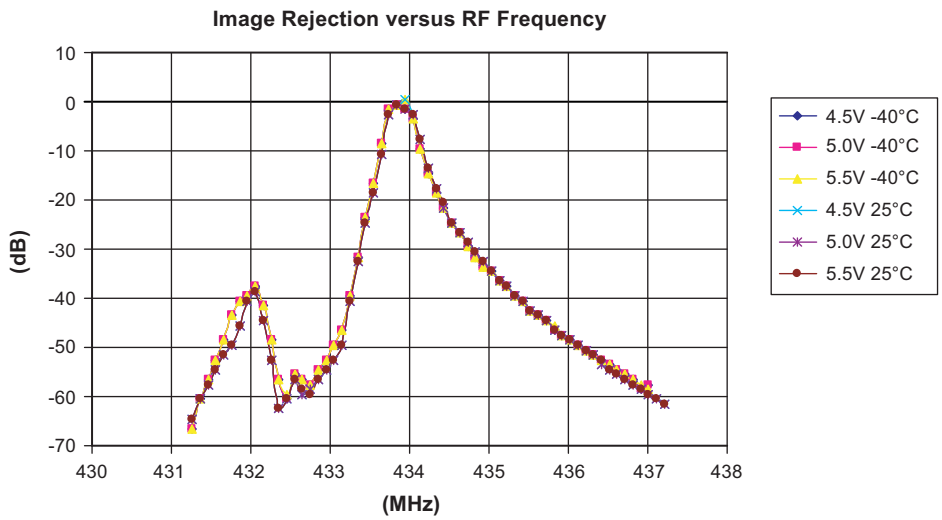
Each BR_Range is also defined by a minimum and a maximum edge-to-edge time ($t_{ee_sig}$). These limits are defined in the electrical characteristics. They should not be exceeded to maintain full sensitivity of the receiver.

# 5. Receiving Characteristics

The RF receiver Atmel® ATA8203/ATA8204/ATA8205 can be operated with and without a SAW front-end filter. In a typical automotive application, a SAW filter is used to achieve better selectivity and large signal capability. The receiving frequency response without a SAW front-end filter is illustrated in Figure 5-1 “Narrow Band Receiving Frequency Response ATA8204”. This example relates to ASK mode. FSK mode exhibits a similar behavior. The plots are printed relatively to the maximum sensitivity. If a SAW filter is used, an insertion loss of about 3dB must be considered, but the overall selectivity is much better.

When designing the system in terms of receiving bandwidth, the LO deviation must be considered as it also determines the IF center frequency. The total LO deviation is calculated, to be the sum of the deviation of the crystal and the XTO deviation of the Atmel ATA8203/ATA8204/ATA8205. Low-cost crystals are specified to be within ±90ppm over tolerance, temperature, and aging. The XTO deviation of the Atmel ATA8203/ATA8204/ATA8205 is an additional deviation due to the XTO circuit. This deviation is specified to be ±10ppm worst case for a crystal with CM = 7fF. If a crystal of ±90ppm is used, the total deviation is ±100ppm in that case. Note that the receiving bandwidth and the IF-filter bandwidth are equivalent in ASK mode but not in FSK mode.

**Figure 5-1. Narrow Band Receiving Frequency Response ATA8204**




# 6. Polling Circuit and Control Logic

The receiver is designed to consume less than 1 mA while being sensitive to signals from a corresponding transmitter. This is achieved using the polling circuit. This circuit enables the signal path periodically for a short time. During this time the bit-check logic verifies the presence of a valid transmitter signal. Only if a valid signal is detected, the receiver remains active and transfers the data to the connected microcontroller. If there is no valid signal present, the receiver is in sleep mode most of the time resulting in low current consumption. This condition is called polling mode. A connected microcontroller is disabled during that time.

All relevant parameters of the polling logic can be configured by the connected microcontroller. This flexibility enables the user to meet the specifications in terms of current consumption, system response time, data rate etc.

The receiver is very flexible with regards to the number of connection wires to the microcontroller. It can be either operated by a single bi-directional line to save ports to the connected microcontroller or it can be operated by up to five uni-directional ports.

# 7. Basic Clock Cycle of the Digital Circuitry

The complete timing of the digital circuitry and the analog filtering is derived from one clock. This clock cycle $T_{Clk}$ is derived from the crystal oscillator (XTO) in combination with a divide by 28 or 30 circuit. According to Section 3. “RF Front-end” on page 6, the frequency of the crystal oscillator ($f_{XTO}$) is defined by the RF input signal ($f_{RFin}$) which also defines the operating frequency of the local oscillator ($f_{LO}$). The basic clock cycle for Atmel® ATA8204 and Atmel ATA8205 is $T_{Clk}$ 28/$f_{XTO}$ giving $T_{Clk}$ = 2.066µs for $f_{RF}$ = 868.3MHz and $T_{Clk}$ = 2.069µs for $f_{RF}$ = 433.92MHz. For Atmel ATA8203 the basic clock cycle is $T_{Clk}$ = 30/$f_{REF}$ giving $T_{Clk}$ = 2.0382µs for $f_{RF}$ = 315MHz.

$T_{Clk}$ controls the following application-relevant parameters:

- Timing of the polling circuit including bit check
- Timing of the analog and digital signal processing
- Timing of the register programming
- Frequency of the reset marker
- IF filter center frequency (fIF0)

Most applications are dominated by three transmission frequencies: $f_{Transmit}$ = 315MHz is mainly used in USA, $f_{Transmit}$ = 868.3MHz and 433.92MHz in Europe. All timings are based on $T_{Clk}$. For the aforementioned frequencies, $T_{Clk}$ is given as:

- Application 315MHz band ($f_{XTO}$ = 14.71875MHz, $f_{LO}$ = 314.13MHz, $T_{Clk}$ = 2.0382µs)
- Application 868.3MHz band ($f_{XTO}$ = 13.55234MHz, $f_{LO}$ = 867.35MHz, $T_{Clk}$ = 2.066µs)
- Application 433.92MHz band ($f_{XTO}$ = 13.52875MHz, $f_{LO}$ = 432.93MHz, $T_{Clk}$ = 2.0696µs)

For calculation of $T_{Clk}$ for applications using other frequency bands, see table in Section 18. “Electrical Characteristics Atmel ATA8204, ATA8205” on page 35.

The clock cycle of some function blocks depends on the selected baud-rate range (BR_Range), which is defined in the OPMODE register. This clock cycle $T_{XClk}$ is defined by the following formulas:

| | | |
|---|---|---|
| BR_Range = | BR_Range0: | $T_{XClk} = 8 \times T_{Clk}$ |
| | BR_Range1: | $T_{XClk} = 4 \times T_{Clk}$ |
| | BR_Range2: | $T_{XClk} = 2 \times T_{Clk}$ |
| | BR_Range3: | $T_{XClk} = 1 \times T_{Clk}$ |

# 8. Polling Mode

According to Figure 8-1 on page 12, the receiver stays in polling mode in a continuous cycle of three different modes. In sleep mode the signal processing circuitry is disabled for the time period $T_{Sleep}$ while consuming low current of $I_S = I_{Soff}$. During the start-up period, $T_{Startup}$, all signal processing circuits are enabled and settled. In the following bit-check mode, the incoming data stream is analyzed bit-by-bit and compared with a valid transmitter signal. If no valid signal is present, the receiver is set back to sleep mode after the period $T_{Bit\text{-}check}$. This period varies according to each check as it is a statistical process. An average value for $T_{Bitcheck}$ is given in the electrical characteristics. During $T_{Startup}$ and $T_{Bit\text{-}check}$, the current consumption is $I_S = I_{Son}$. The condition of the receiver is indicated on pin IC_ACTIVE. The average current consumption in polling mode is dependent on the duty cycle of the active mode and can be calculated as:

$$I_{Spoll} = \frac{I_{Soff} \times T_{Sleep} + I_{Son} \times (T_{Startup} + T_{Bit\text{-}check})}{T_{Sleep} + T_{Startup} + T_{Bit\text{-}check}}$$

During $T_{Sleep}$ and $T_{Startup}$, the receiver is not sensitive to a transmitter signal. To guarantee the reception of a transmitted command, the transmitter must start the telegram with an adequate preburst. The required length of the preburst depends on the polling parameters $T_{Sleep}$, $T_{Startup}$, $T_{Bit\text{-}check}$ and the start-up time of a connected microcontroller, $T_{Start_microcontroller}$. Thus, $T_{Bit\text{-}check}$ depends on the actual bit rate and the number of bits ($N_{Bit\text{-}check}$) to be tested.

The following formula indicates how to calculate the preburst length.

$$T_{Preburst} \geq T_{Sleep} + T_{Startup} + T_{Bit\text{-}check} + T_{Start_microcontroller}$$

## 8.1 Sleep Mode

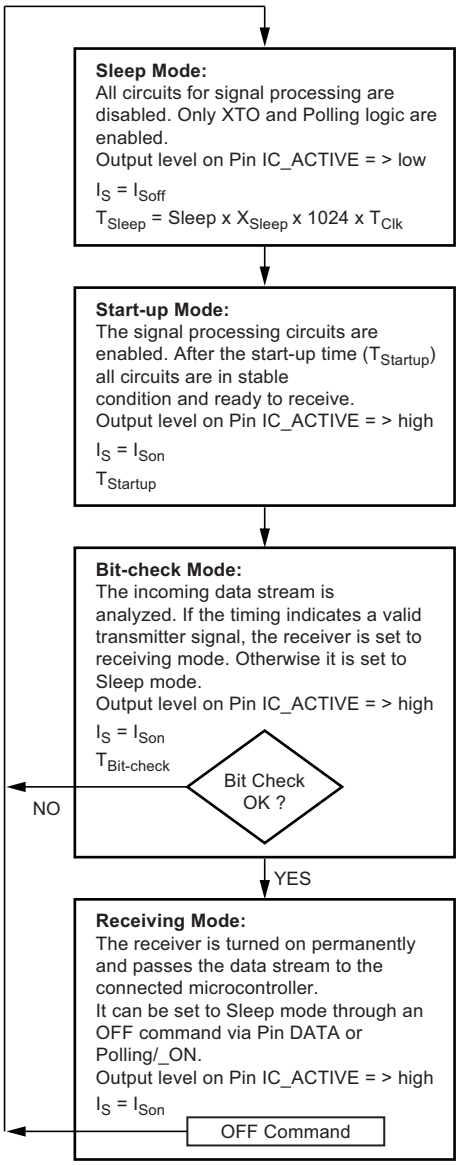
The length of period $T_{Sleep}$ is defined by the 5-bit word Sleep of the OPMODE register, the extension factor $X_{Sleep}$ (according to Table 11-8 on page 25), and the basic clock cycle $T_{Clk}$. It is calculated to be:

$$T_{Sleep} = \text{Sleep} \times X_{Sleep} \times 1024 \times T_{Clk}$$

The maximum value of $T_{Sleep}$ is about 60 ms if $X_{Sleep}$ is set to 1. The time resolution is about 2 ms in that case. The sleep time can be extended to almost half a second by setting $X_{Sleep}$ to 8. $X_{Sleep}$ can be set to 8 by bit $X_{SleepStd}$ to “1”.

Setting the configuration word Sleep to its maximal value puts the receiver into a permanent sleep mode. The receiver remains in this state until another value for Sleep is programmed into the OPMODE register. This is particularily useful when several devices share a single data line. (It can also be used for microcontroller polling: using pin POLLING/_ON, the receiver can be switched on and off.)

**Figure 8-1. Polling Mode Flow Chart**




Sleep: 5-bit word defined by Sleep 0 to Sleep 4 in OPMODE register

$X_{Sleep}$: Extension factor defined by XSleepStd according to Table 11-8

$T_{Clk}$: Basic clock cycle defined by $f_{XTO}$ and Pin MODE

$T_{Startup}$: Is defined by the selected baud rate range and TClk. The baud-rate range is defined by Baud 0 and Baud 1 in the OPMODE register.

$T_{Bit-check}$: Depends on the result of the bit check

If the bit check is ok, $T_{Bit-check}$ depends on the number of bits to be checked ($N_{Bit-check}$) and on the data rate used.

If the bit check fails, the average time period for that check depends on the selected baud-rate range and on $T_{Clk}$. The baud-rate range is defined by Baud 0 and Baud 1 in the OPMODE register.

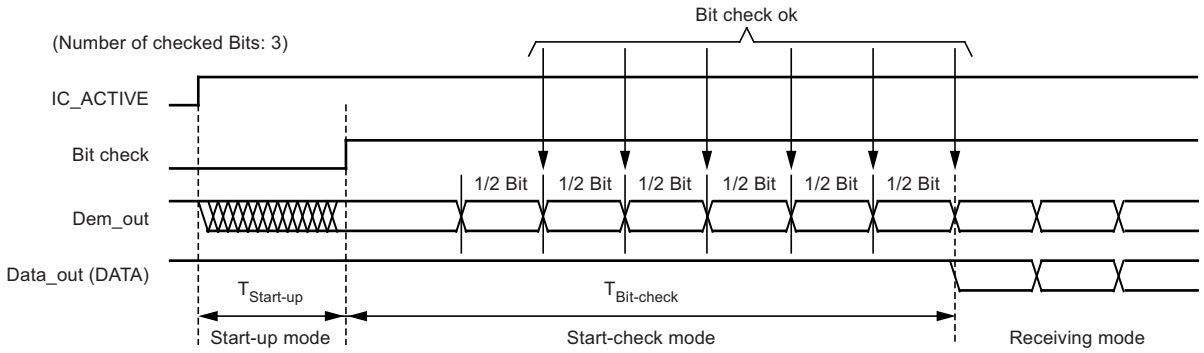
## 8.2 Bit-check Mode

In bit-check mode the incoming data stream is examined to distinguish between a valid signal from a corresponding transmitter and signals due to noise. This is done by subsequent time frame checks where the distances between 2 signal edges are continuously compared to a programmable time window. The maximum number of these edge-to-edge tests, before the receiver switches to receiving mode, is also programmable.

## 8.3 Configuring the Bit Check

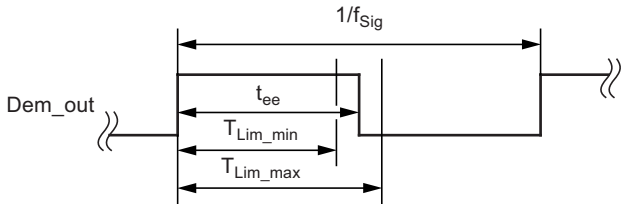
Assuming a modulation scheme that contains two edges per bit, two time frame checks verify one bit. This is valid for Manchester, Bi-phase, and most other modulation schemes. The maximum count of bits to be checked can be set to 0, 3, 6, or 9 bits using the variable $N_{Bit\text{-}check}$ in the OPMODE register. This implies 0, 6, 12, and 18 edge-to-edge checks respectively. If $N_{Bit\text{-}check}$ is set to a higher value, the receiver is less likely to switch to receiving mode due to noise. In the presence of a valid transmitter signal, the bit check takes less time if $N_{Bit\text{-}check}$ is set to a lower value. In polling mode, the bit-check time is not dependent on NBit-check. Figure 8-2 shows an example where three bits are tested successfully and the data signal is transferred to pin DATA.

**Figure 8-2. Timing Diagram for Complete Successful Bit Check**




According to Figure 8-3, the time window for the bit check is defined by two separate time limits. If the edge-to-edge time $t_{ee}$ is in between the lower bit-check limit $T_{Lim_min}$ and the upper bit-check limit $T_{Lim_max}$, the check continues. If $t_{ee}$ is smaller than $T_{Lim_min}$ or $t_{ee}$ exceeds $T_{Lim_max}$, the bit check is terminated and the receiver switches to sleep mode.

**Figure 8-3. Valid Time Window for Bit Check**




For best noise immunity using a low span between $T_{Lim_min}$ and $T_{Lim_max}$ is recommended. This is achieved using a fixed frequency at a 50% duty cycle for the transmitter preburst. A “11111...” or a “10101...” sequence in Manchester or Bi-phase is suitable for this. A good compromise between receiver sensitivity and susceptibility to noise is a time window of ±30% regarding the expected edge-to-edge time $t_{ee}$. Using pre-burst patterns that contain various edge-to-edge time periods, the bit-check limits must be programmed according to the required span.

The bit-check limits are determined by means of the formula below.

$T_{Lim_min} = Lim_min \times T_{XClk}$
$T_{Lim_max} = (Lim_max - 1) \times T_{XClk}$

Lim_min and Lim_max are defined by a 5-bit word each within the LIMIT register.

Using above formulas, Lim_min and Lim_max can be determined according to the required $T_{Lim_min}$, $T_{Lim_max}$ and $T_{XClk}$. The time resolution defining $T_{Lim_min}$ and $T_{Lim_max}$ is $T_{XClk}$. The minimum edge-to-edge time $t_{ee}$ ($t_{DATA_L_min}$, $t_{DATA_H_min}$) is defined according to the Section 8.6 “Digital Signal Processing” on page 15. The lower limit should be set to Lim_min ≥ 10. The maximum value of the upper limit is Lim_max = 63.

If the calculated value for Lim_min is < 19, it is recommended to check 6 or 9 bits ($N_{Bit\text{-}check}$) to prevent switching to receiving mode due to noise.

Figure 8-4, Figure 8-5, and Figure 8-6 illustrate the bit check for the bit-check limits Lim_min = 14 and Lim_max = 24. When the IC is enabled, the signal processing circuits are enabled during $T_{Startup}$. The output of the ASK/FSK demodulator (Dem_out) is undefined during that period. When the bit check becomes active, the bit-check counter is clocked with the cycle $T_{XClk}$.

Figure 8-4 shows how the bit check proceeds if the bit-check counter value CV_Lim is within the limits defined by Lim_min and Lim_max at the occurrence of a signal edge. In Figure 8-5 the bit check fails as the value CV_Lim is lower than the limit Lim_min. The bit check also fails if CV_Lim reaches Lim_max. This is illustrated in Figure 8-6.

**Figure 8-4. Timing Diagram During Bit Check**

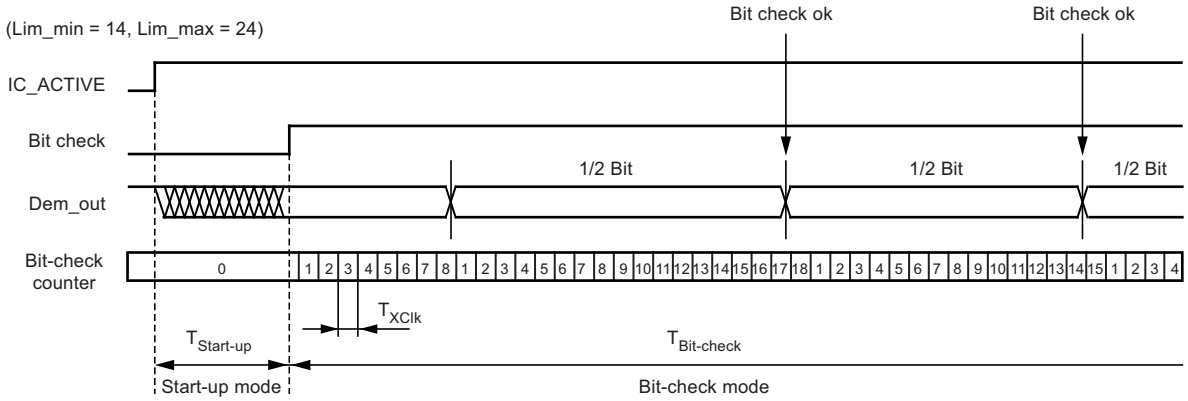



**Figure 8-5. Timing Diagram for Failed Bit Check (Condition: CV_Lim < Lim_min)**

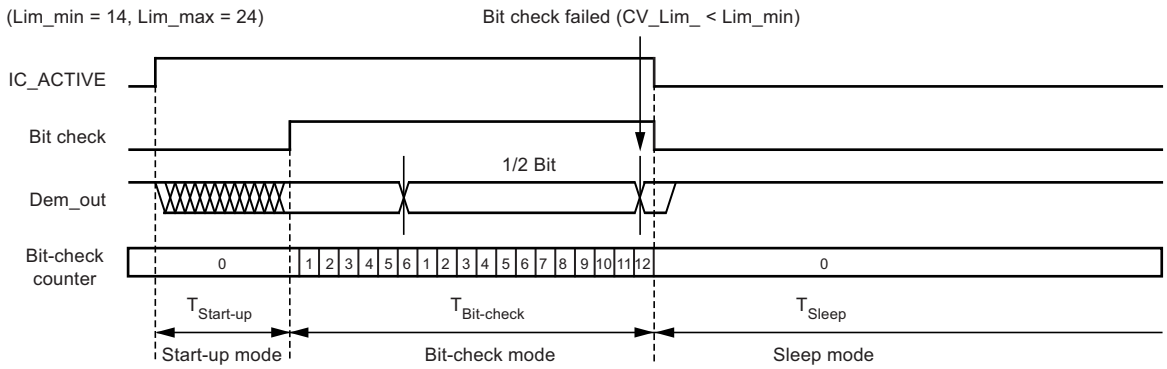
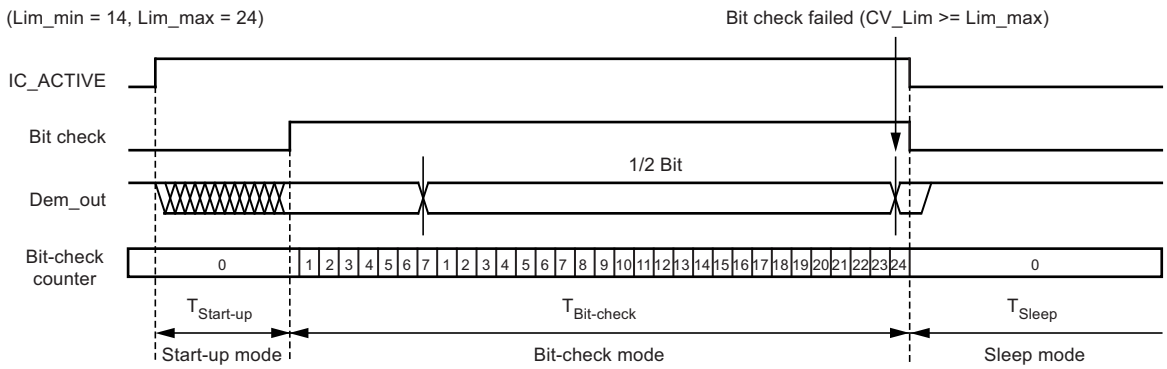



**Figure 8-6. Timing Diagram for Failed Bit Check (Condition: CV_Lim ≥ Lim_max)**



## 8.4 Duration of the Bit Check

If no transmitter signal is present during the bit check, the output of the ASK/FSK demodulator delivers random signals. The bit check is a statistical process and $T_{Bit\text{-}check}$ varies for each check. Therefore, an average value for $T_{Bit\text{-}check}$ is given in the electrical characteristics. $T_{Bit\text{-}check}$ depends on the selected baud-rate range and on $T_{Clk}$. A higher baud-rate range causes a lower value for $T_{Bit\text{-}check}$ resulting in a lower current consumption in polling mode.

In the presence of a valid transmitter signal, $T_{Bit\text{-}check}$ is dependent on the frequency of that signal, $f_{Sig}$, and the count of the checked bits, $N_{Bit\text{-}check}$. A higher value for $N_{Bit\text{-}check}$ thereby results in a longer period for $T_{Bit\text{-}check}$ requiring a higher value for the transmitter pre-burst $T_{Preburst}$.

## 8.5 Receiving Mode

If the bit check was successful for all bits specified by $N_{Bit\text{-}check}$, the receiver switches to receiving mode. According to Figure 8-2 on page 13, the internal data signal is switched to pin DATA in that case, and the data clock is available after the start bit has been detected (see Figure 9-1 on page 18). A connected microcontroller can be woken up by the negative edge at pin DATA or by the data clock at pin DATA_CLK. The receiver stays in that condition until it is switched back to polling mode explicitly.

## 8.6 Digital Signal Processing

The data from the ASK/FSK demodulator (Dem_out) is digitally processed in different ways and as a result converted into the output signal data. This processing depends on the selected baud-rate range (BR_Range). Figure 8-7 illustrates how Dem_out is synchronized by the extended clock cycle $T_{XClk}$. This clock is also used for the bit-check counter. Data can change its state only after $T_{XClk}$ has elapsed. The edge-to-edge time period $t_{ee}$ of the Data signal as a result is always an integral multiple of $T_{XClk}$.

The minimum time period between two edges of the data signal is limited to $t_{ee} \geq T_{DATA_min}$. This implies an efficient suppression of spikes at the DATA output. At the same time it limits the maximum frequency of edges at DATA. This eases the interrupt handling of a connected microcontroller.

The maximum time period for DATA to stay low is limited to $T_{DATA_L_max}$. This function is employed to ensure a finite response time in programming or switching off the receiver via pin DATA. $T_{DATA_L_max}$ is therefore longer than the maximum time period indicated by the transmitter data stream. Figure 8-9 on page 16 gives an example where Dem_out remains Low after the receiver has switched to receiving mode.

**Figure 8-7. Synchronization of the Demodulator Output**

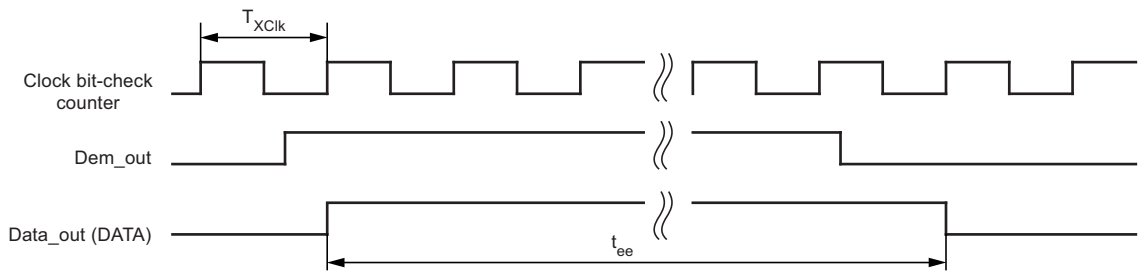



**Figure 8-8. Debouncing of the Demodulator Output**

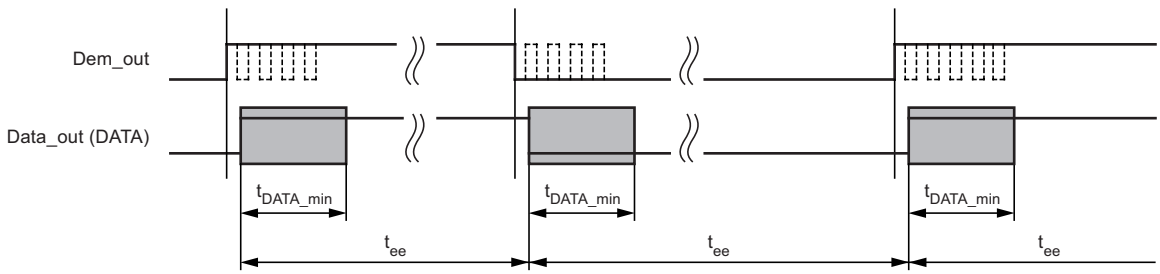
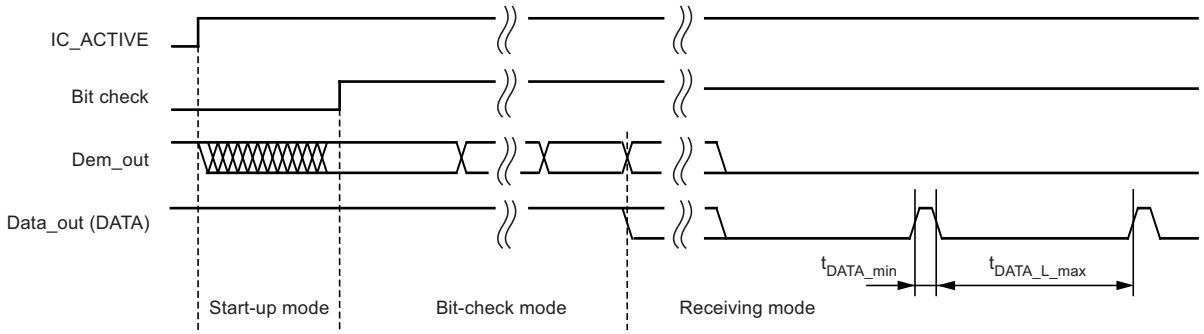


**Figure 8-9. Steady L State Limited DATA Output Pattern After Transmission**




After the end of a data transmission, the receiver remains active. Depending of the bit Noise_Disable in the OPMODE register, the output signal at pin DATA is high or random noise pulses appear at pin DATA (see Section 10. “Digital Noise Suppression” on page 21). The edge-to-edge time period $t_{ee}$ of the majority of these noise pulses is equal or slightly higher than $T_{DATA_min}$.

## 8.7 Switching the Receiver Back to Sleep Mode

The receiver can be set back to polling mode via pin DATA or via pin POLLING/_ON.

When using pin DATA, this pin must be pulled to low by the connected microcontroller for the period t1. Figure 8-10 illustrates the timing of the OFF command (see Figure 13-2 on page 28). The minimum value of t1 depends on the BR_Range. The maximum value for t1 is not limited; however, exceeding the specified value to prevent erasing the reset marker is not recommended. Note also that an internal reset for the OPMODE and the LIMIT register is generated if t1 exceeds the specified values. This item is explained in more detail in the Section 11. “Configuring the Receiver” on page 23. Setting the receiver to sleep mode via DATA is achieved by programming bit 1 to “1” during the register configuration. Only one sync pulse (t3) is issued.

The duration of the OFF command is determined by the sum of t1, t2, and t10. The sleep time $T_{Sleep}$ elapses after the OFF command. Note that the capacitive load at pin DATA is limited (see Section 14. “Data Interface” on page 30).

**Figure 8-10. Timing Diagram of the OFF Command using Pin DATA**

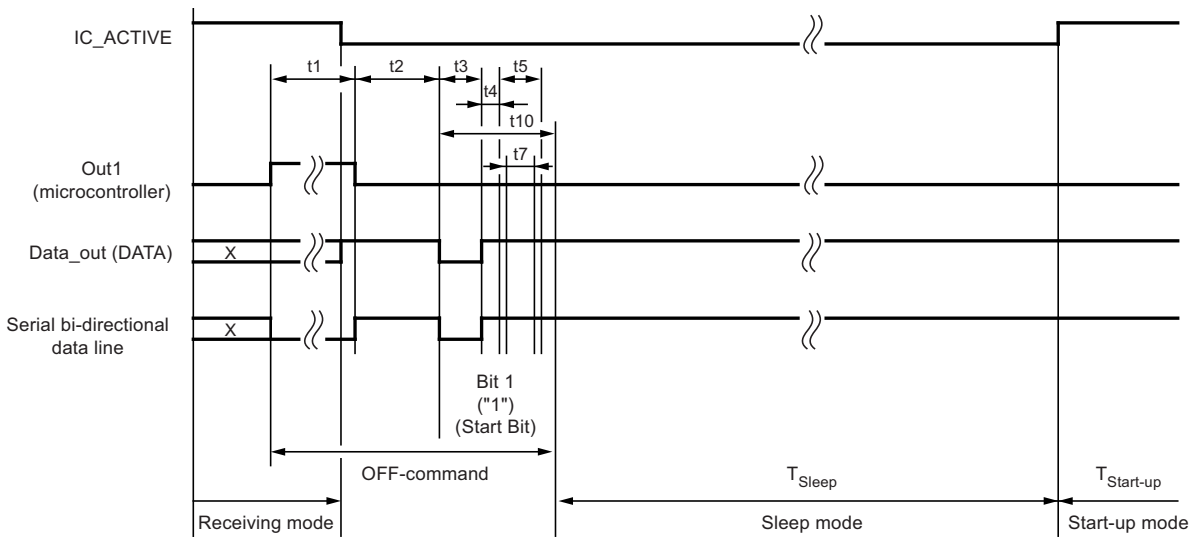


**Figure 8-11. Timing Diagram of the OFF Command using Pin POLLING/_ON**

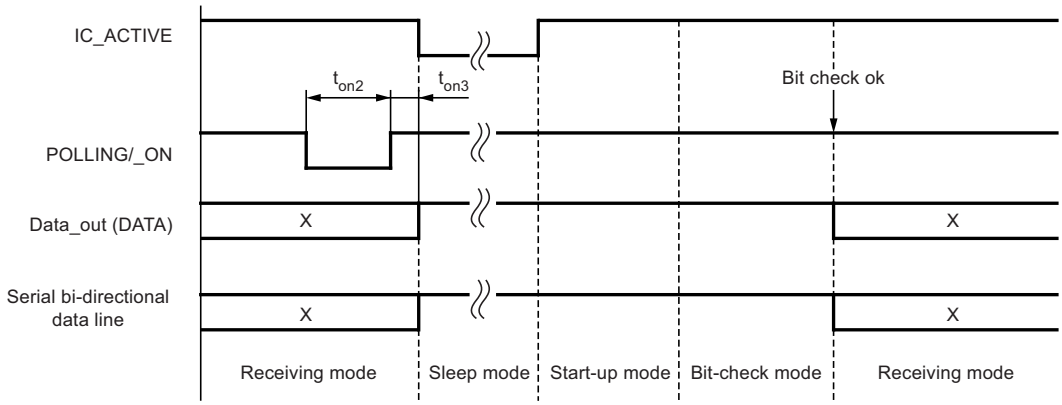



**Figure 8-12. Activating the Receiving Mode using Pin POLLING/_ON**

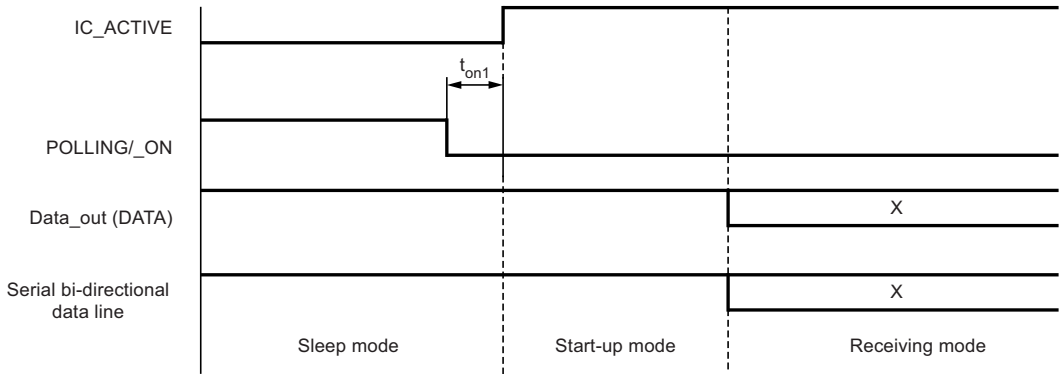



Figure 8-11 “Timing Diagram of the OFF Command using Pin POLLING/_ON” illustrates how to set the receiver back to polling mode using pin POLLING/_ON. The pin POLLING/_ON must be held to low for the time period $t_{on2}$. After the positive edge on pin POLLING/_ON and the delay $t_{on3}$, the polling mode is active and the sleep time $T_{Sleep}$ elapses.

Using the POLLING/_ON command is faster than using pin DATA; however, this requires the use of an additional connection to the microcontroller.

Figure 8-12 “Activating the Receiving Mode using Pin “POLLING/_ON” illustrates how to set the receiver to receiving mode using the pin POLLING/_ON. The pin POLLING/_ON must be held to low. After the delay $t_{on1}$, the receiver changes from sleep mode to start-up mode regardless of the programmed values for $T_{Sleep}$ and $N_{Bit\text{-}check}$. As long as POLLING/_ON is held to low, the values for $T_{Sleep}$ and $N_{Bit\text{-}check}$ is ignored, but not deleted (see Section 10. “Digital Noise Suppression” on page 21).

If the receiver is polled exclusively by a microcontroller, $T_{Sleep}$ must be programmed to 31 (permanent sleep mode). In this case the receiver remains in sleep mode as long as POLLING/_ON is held to high.

# 9. Data Clock

The pin DATA_CLK makes a data shift clock available to sample the data stream into a shift register. Using this data clock, a microcontroller can easily synchronize the data stream. This clock can only be used for Manchester and Bi-phase coded signals.

## 9.1 Generation of the Data Clock

After a successful bit check, the receiver switches from polling mode to receiving mode and the data stream is available at pin DATA. In receiving mode, the data clock control logic (Manchester/Bi-phase demodulator) is active and examines the incoming data stream. This is done, as with the bit check, by subsequent time frame checks where the distance between two edges is continuously compared to a programmable time window. As illustrated in Figure 9-1 on page 18, only two distances between two edges in Manchester and Bi-phase coded signals are valid (T and 2T).

The limits for T are the same as used with the bit check. They can be programmed in the LIMIT-register (Lim_min and Lim_max, see Table 11-10 on page 26 and Table 11-11 on page 26).

The limits for 2T are calculated as follows:

Lower limit of 2T: Lim_min_2T = (Lim_min + Lim_max) – (Lim_max – Lim_min)/2

Upper limit of 2T: Lim_max_2T= (Lim_min + Lim_max) + (Lim_max – Lim_min)/2

(If the result for 'Lim_min_2T' or 'Lim_max_2T' is not an integer value, it is rounded up.)

The data clock is available, after the data clock control logic has detected the distance 2T (Start bit) and is issued with the delay $t_{Delay}$ after the edge on pin DATA (see Figure 9-1 on page 18).

If the data clock control logic detects a timing or logical error (Manchester code violation), as illustrated in Figure 9-2 on page 19 and Figure 9-3 on page 19, it stops the output of the data clock. The receiver remains in receiving mode and starts with the bit check. If the bit check was successful and the start bit has been detected, the data clock control logic starts again with the generation of the data clock (see Figure 9-4 on page 19).

Use the function of the data clock only in conjunction with the bit check 3, 6 or 9 is recommended. If the bit check is set to 0 or the receiver is set to receiving mode using the pin POLLING/_ON, the data clock is available if the data clock control logic has detected the distance 2T (Start bit).

Note that for Bi-phase-coded signals, the data clock is issued at the end of the bit.

**Figure 9-1. Timing Diagram of the Data Clock**

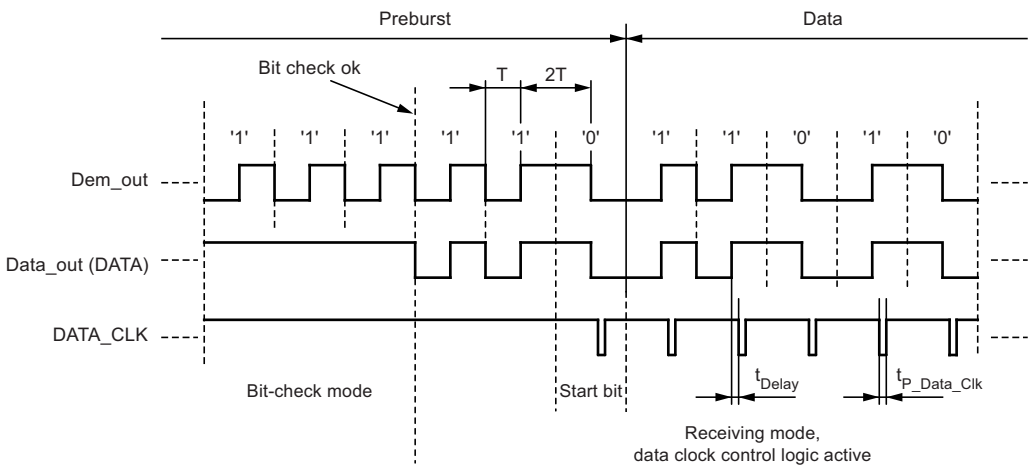


**Figure 9-2. Data Clock Disappears Because of a Timing Error**

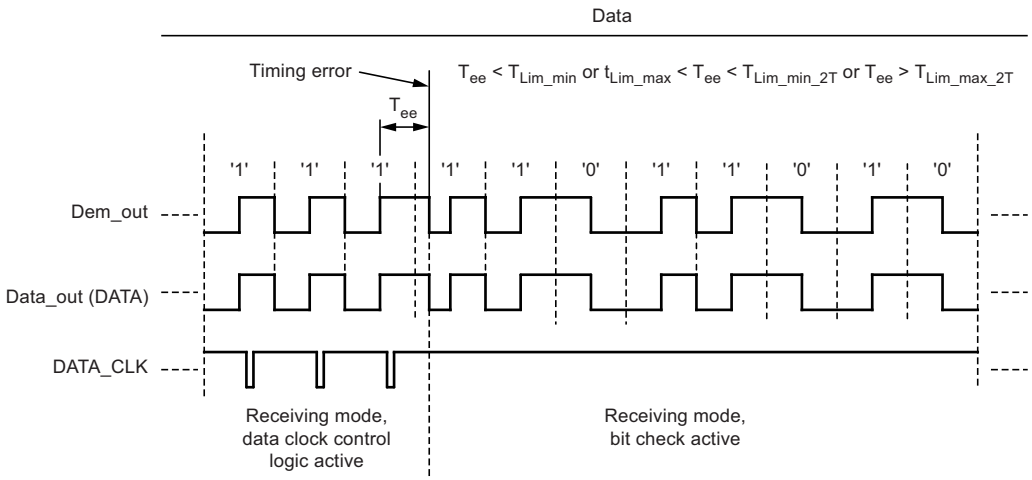



**Figure 9-3. Data Clock Disappears Because of a Logical Error**

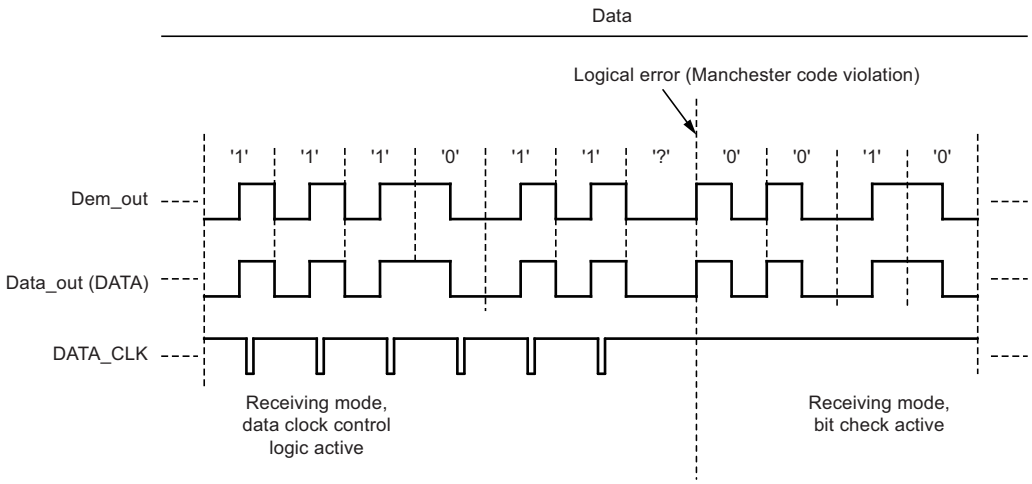
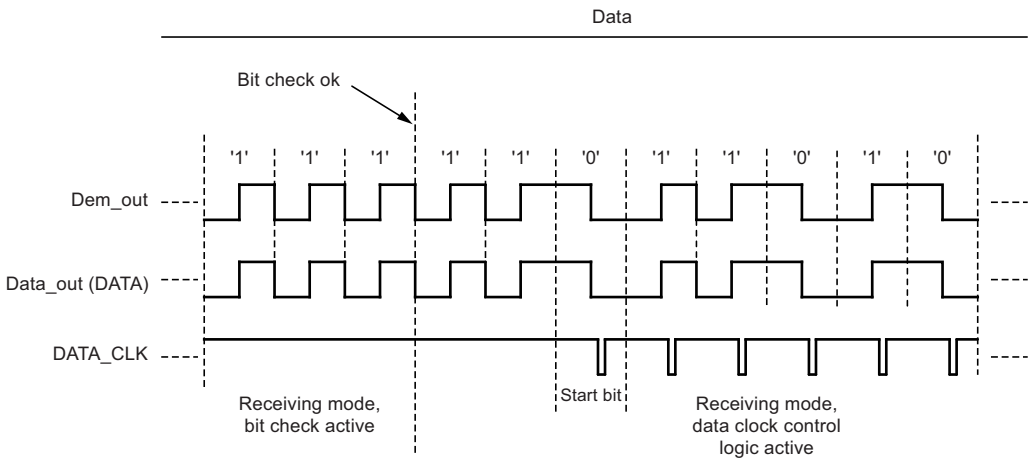



**Figure 9-4. Output of the Data Clock After a Successful Bit Check**




The delay of the data clock is calculated as follows: $t_{Delay} = t_{Delay1} + t_{Delay2}$

$t_{Delay1}$ is the delay between the internal signals Data_Out and Data_In. For the rising edge, $t_{Delay1}$ depends on the capacitive load $C_L$ at pin DATA and the external pull-up resistor $R_{pup}$. For the falling edge, $t_{Delay1}$ depends additionally on the external voltage $V_X$ (see Figure 9-5, Figure 9-6 on page 20 and Figure 13-2 on page 28). When the level of Data_In is equal to the level of Data_Out, the data clock is issued after an additional delay $t_{Delay2}$.

Note that the capacitive load at pin DATA is limited. If the maximum tolerated capacitive load at pin DATA is exceeded, the data clock disappears (see Section 14. “Data Interface” on page 30).

**Figure 9-5. Timing Characteristic of the Data Clock (Rising Edge on Pin DATA)**

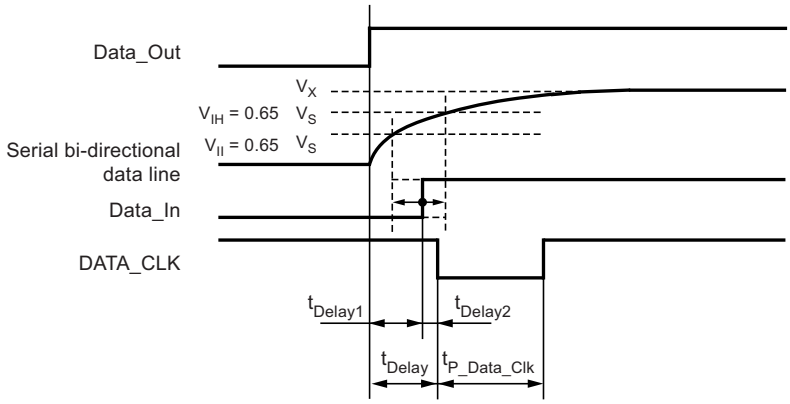
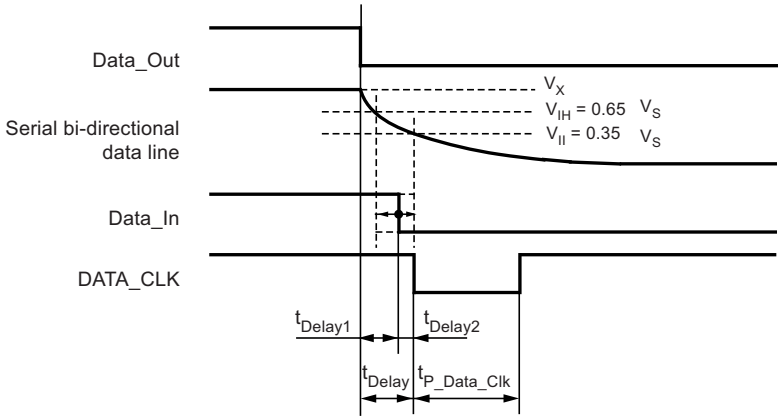



**Figure 9-6. Timing Characteristic of the Data Clock (Falling Edge of the Pin DATA)**



# 10. Digital Noise Suppression

After a data transmission, digital noise appears on the data output (see Figure 10-1 “Output of Digital Noise at the End of the Data Stream”). To prevent digital noise keeping the connected microcontroller busy, it can be suppressed in two different ways:

- Automatic Noise Suppression
- Controlled Noise Suppression by the Microcontroller

## 10.1 Automatic Noise Suppression

The receiver changes to bit-check mode at the end of a valid data stream if the bit Noise_Disable (Table 11-9 on page 25) in the OPMODE register is set to 1 (default). The digital noise is suppressed, and the level at pin DATA is high. The receiver changes back to receiving mode, if the bit check was successful.

This method of noise suppression is recommended if the data stream is Manchester or Bi-phase coded and is active after power on.

Figure 10-3 “Occurrence of a Pulse at the End of the Data Stream” illustrates the behavior of the data output at the end of a data stream. If the last period of the data stream is a high period (rising edge to falling edge), a pulse occurs on pin DATA. The length of the pulse depends on the selected baud-rate range.

**Figure 10-1. Output of Digital Noise at the End of the Data Stream**

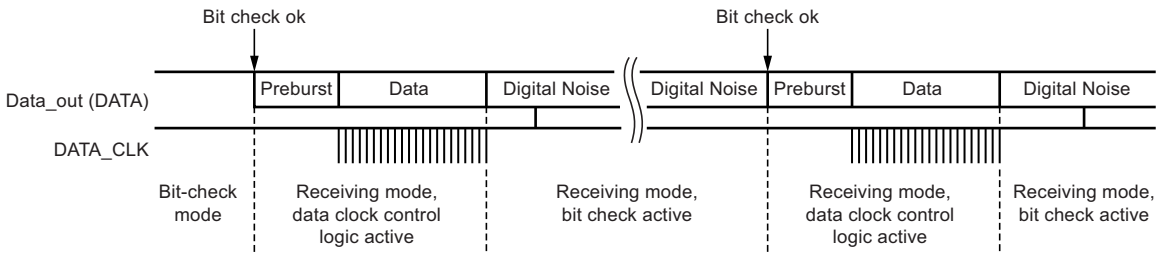



**Figure 10-2. Automatic Noise Suppression**

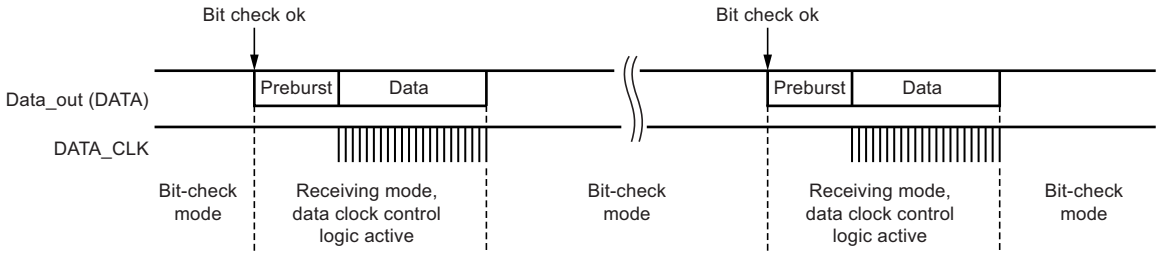
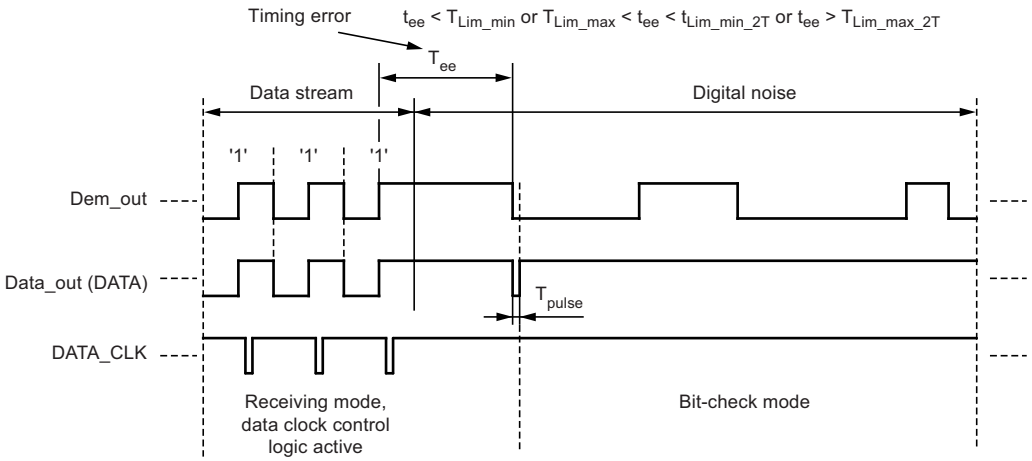


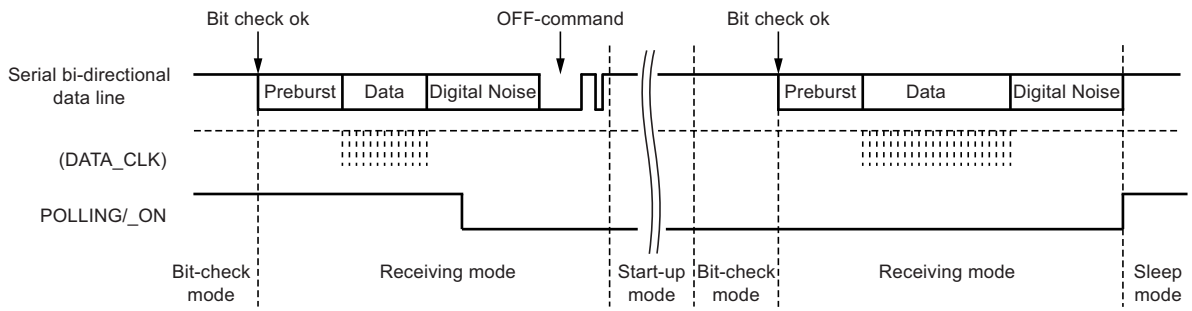
**Figure 10-3. Occurrence of a Pulse at the End of the Data Stream**




## 10.2 Controlled Noise Suppression by the Microcontroller

Digital noise appears at the end of a valid data stream if the bit Noise_Disable (see Table 11-9 on page 25) in the OPMODE register is set to 0. To suppress the noise, the pin POLLING/_ON must be set to low. The receiver remains in receiving mode. The OFF command then causes a change to start-up mode. The programmed sleep time (see Table 11-7 on page 25) is not executed because the level at pin POLLING/_ON is low; however, the bit check is active in this case. The OFF command also activates the bit check if the pin POLLING/_ON is held to low. The receiver changes back to receiving mode if the bit check was successful. To activate the polling mode at the end of the data transmission, the pin POLLING/_ON must be set to high. This way of suppressing the noise is recommended if the data stream is not Manchester or Bi-phase coded.

**Figure 10-4. Controlled Noise Suppression**



# 11. Configuring the Receiver

The Atmel® ATA8203/ATA8204/ATA8205 receiver is configured using two 12-bit RAM registers called OPMODE and LIMIT. The registers can be programmed by means of the bidirectional DATA port. If the register content has changed due to a voltage drop, this condition is indicated by a the output pattern called reset marker (RM). If this occurs, the receiver must be reprogrammed. After a Power-On Reset (POR), the registers are set to default mode. If the receiver is operated in default mode, there is no need to program the registers. Table 11-3 on page 23 shows the structure of the registers. According to Table 11-1, bit 1 defines whether the receiver is set back to polling mode using the OFF command (see "Receiving Mode" on page 15) or whether it is programmed. Bit 2 represents the register address. It selects the appropriate register to be programmed. For high programming reliability, bit 15 (Stop bit), at the end of the programming operation, must be set to 0.

**Table 11-1. Effect of Bit 1 and Bit 2 on Programming the Registers**

| Bit 1 | Bit 2 | Action |
|---|---|---|
| 1 | x | The receiver is set back to polling mode (OFF command) |
| 0 | 1 | The OPMODE register is programmed |
| 0 | 0 | The LIMIT register is programmed |

**Table 11-2. Effect of Bit 15 on Programming the Register**

| Bit 15 | Action |
|---|---|
| 0 | The values are written into the register (OPMODE or LIMIT) |
| 1 | The values are not written into the register |

**Table 11-3. Effect of the Configuration Words within the Registers**

| Bit 1 | Bit 2 | Bit 3 | Bit 4 | Bit 5 | Bit 6 | Bit 7 | Bit 8 | Bit 9 | Bit 10 | Bit 11 | Bit 12 | Bit 13 | Bit 14 | Bit 15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OFF command | | | | | | | | | | | | | | |
| 1 | – | – | – | – | – | – | – | – | – | – | – | – | – | – |
| – | | OPMODE register | | | | | | | | | | | | – |
| 0 | 1 | BR_Range | | $N_{Bit\text{-}check}$ | | Modu-lation | Sleep | | | | | $X_{Sleep}$ | Noise Suppression | 0 |
| | | Baud1 | Baud0 | BitChk1 | BitChk0 | ASK/ _FSK | Sleep4 | Sleep3 | Sleep2 | Sleep1 | Sleep0 | $X_{SleepStd}$ | Noise_ Disable | |
| Default values of Bit 3...14 | | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | – |
| – | | LIMIT register | | | | | | | | | | | | – |
| 0 | 0 | Lim_min | | | | | | Lim_max | | | | | | – |
| | | Lim_ min5 | Lim_ min4 | Lim_ min3 | Lim_ min2 | Lim_ min1 | Lim_ min0 | Lim_ max5 | Lim_ max4 | Lim_ max3 | Lim_ max2 | Lim_ max1 | Lim_ max0 | 0 |
| Default values of Bit 3...14 | | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | – |

The following tables illustrate the effect of the individual configuration words. The default configuration is highlighted for each word.

BR_Range sets the appropriate baud-rate range and simultaneously defines XLim. XLim is used to define the bit-check limits $T_{Lim_min}$ and $T_{Lim_max}$ as shown in Table 11-10 on page 26 and Table 11-11 on page 26.

**Table 11-4. Effect of the configuration word BR_Range**

| BR_Range | | |
|---|---|---|
| **Baud1** | **Baud0** | **Baud-rate Range/Extension Factor for Bit-check Limits (XLim)** |
| 0 | 0 | BR_Range0<br>(BR_Range0 = 1.0Kbit/s to 1.8Kbit/s)<br>XLim = 8 (default) |
| 0 | 1 | BR_Range1<br>(BR_Range1 = 1.8Kbit/s to 3.2Kbit/s)<br>XLim = 4 |
| 1 | 0 | BR_Range2<br>(BR_Range2 = 3.2Kbit/s to 5.6Kbit/s)<br>XLim = 2 |
| 1 | 1 | BR_Range3<br>(BR_Range3 = 5.6Kbit/s to 10Kbit/s)<br>XLim = 1 |

**Table 11-5. Effect of the Configuration word $N_{Bit\text{-}check}$**

| $N_{Bit\text{-}check}$ | | |
|---|---|---|
| **BitChk1** | **BitChk0** | **Number of Bits to be Checked** |
| 0 | 0 | 0 |
| 0 | 1 | 3 (default) |
| 1 | 0 | 6 |
| 1 | 1 | 9 |

**Table 11-6. Effect of the Configuration Bit Modulation**

| Modulation | Selected Modulation |
|---|---|
| ASK/_FSK | – |
| 0 | FSK (default) |
| 1 | ASK |

**Table 11-7. Effect of the Configuration Word Sleep**

| Sleep | | | | | Start Value for Sleep Counter ($T_{Sleep}$ = Sleep × $X_{Sleep}$ × 1024 × $T_{Clk}$) |
|---|---|---|---|---|---|
| Sleep4 | Sleep3 | Sleep2 | Sleep1 | Sleep0 | |
| 0 | 0 | 0 | 0 | 0 | 0 (Receiver polls continuously until a valid signal occurs) |
| 0 | 0 | 0 | 0 | 1 | If $X_{Sleep}$ = 1<br>$T_{Sleep}$ = 2.11ms for $f_{RF}$ = 868.3MHz,<br>$T_{Sleep}$ = 2.12ms for $f_{RF}$ = 433.92MHz<br>$T_{Sleep}$ = 2.08ms for $f_{RF}$ = 315MHz |
| 0 | 0 | 0 | 1 | 0 | 2 |
| 0 | 0 | 0 | 1 | 1 | 3 |
| ... | ... | ... | ... | ... | ... |
| 0 | 0 | 1 | 1 | 0 | If $X_{Sleep}$ = 1<br>$T_{Sleep}$ = 12.69ms for $f_{RF}$ = 868.3MHz,<br>$T_{Sleep}$ = 12.71ms for $f_{RF}$ = 433.92MHz<br>$T_{Sleep}$ = 12.52ms for $f_{RF}$ = 315MHz |
| ... | ... | ... | ... | ... | ... |
| 1 | 1 | 1 | 0 | 1 | 29 |
| 1 | 1 | 1 | 1 | 0 | 30 |
| 1 | 1 | 1 | 1 | 1 | 31 (permanent sleep mode) |

**Table 11-8. Effect of the Configuration Bit XSleep**

| $X_{Sleep}$ | Extension Factor for Sleep Time ($T_{Sleep}$ = Sleep × $X_{Sleep}$ × 1024 × $T_{Clk}$) |
|---|---|
| $X_{SleepStd}$ | |
| 0 | 1 (default) |
| 1 | 8 |

**Table 11-9. Effect of the Configuration Bit Noise Suppression**

| Noise Suppression | |
|---|---|
| Noise_Disable | Suppression of the Digital Noise at Pin DATA |
| 0 | Noise suppression is inactive |
| 1 | Noise suppression is active (default) |

**Table 11-10. Effect of the Configuration Word Lim_min**

| Lim_min[1] (Lim_min < 10 is not Applicable) | | | | | | Lower Limit Value for Bit Check |
|---|---|---|---|---|---|---|
| Lim_min5 | Lim_min4 | Lim_min3 | Lim_min2 | Lim_min1 | Lim_min0 | ($T_{Lim_min}$ = Lim_min × XLim × $T_{Clk}$) |
| 0 | 0 | 1 | 0 | 1 | 0 | 10 |
| 0 | 0 | 1 | 0 | 1 | 1 | 11 |
| 0 | 0 | 1 | 1 | 0 | 0 | 12 |
| .. | .. | .. | .. | .. | .. | |
| 0 | 1 | 0 | 1 | 0 | 1 | 21 (default, BR_Range0)<br>($T_{Lim_min}$ = 347µs for $f_{RF}$ = 868.3MHz<br>$T_{Lim_min}$ = 347µs for $f_{RF}$ = 433.92MHz<br>$T_{Lim_min}$ = 342µs for $f_{RF}$ = 315MHz) |
| .. | .. | .. | .. | .. | .. | |
| 1 | 1 | 1 | 1 | 0 | 1 | 61 |
| 1 | 1 | 1 | 1 | 1 | 0 | 62 |
| 1 | 1 | 1 | 1 | 1 | 1 | 63 |

Note: 1. Lim_min is also used to determine the margins of the data clock control logic (see Section 9. “Data Clock” on page 18).

**Table 11-11. Effect of the Configuration Word Lim_max**

| Lim_max[1] (Lim_max < 12 is not applicable) | | | | | | Upper Limit Value for Bit Check |
|---|---|---|---|---|---|---|
| Lim_max5 | Lim_max4 | Lim_max3 | Lim_max2 | Lim_max1 | Lim_max0 | (TLim_max = (Lim_max – 1) × XLim × $T_{Clk}$) |
| 0 | 0 | 1 | 1 | 0 | 0 | 12 |
| 0 | 0 | 1 | 1 | 0 | 1 | 13 |
| 0 | 0 | 1 | 1 | 1 | 0 | 14 |
| .. | .. | .. | .. | .. | .. | |
| 1 | 0 | 1 | 0 | 0 | 1 | 41 (default, BR_Range0)<br>($T_{Lim_max}$ = 66µs for $f_{RF}$ = 868.3MHz<br>$T_{Lim_max}$ = 662µs for $f_{RF}$ = 433.92MHz<br>$T_{Lim_max}$ = 652µs for $f_{RF}$ = 315MHz) |
| .. | .. | .. | .. | .. | .. | |
| 1 | 1 | 1 | 1 | 0 | 1 | 61 |
| 1 | 1 | 1 | 1 | 1 | 0 | 62 |
| 1 | 1 | 1 | 1 | 1 | 1 | 63 |

Note: 1. Lim_max is also used to determine the margins of the data clock control logic (see Section 9. “Data Clock” on page 18).

# 12. Conservation of the Register Information

The Atmel® ATA8203/ATA8204/ATA8205 uses an integrated power-on reset and brown-out detection circuitry as a mechanism to preserve the RAM register information.

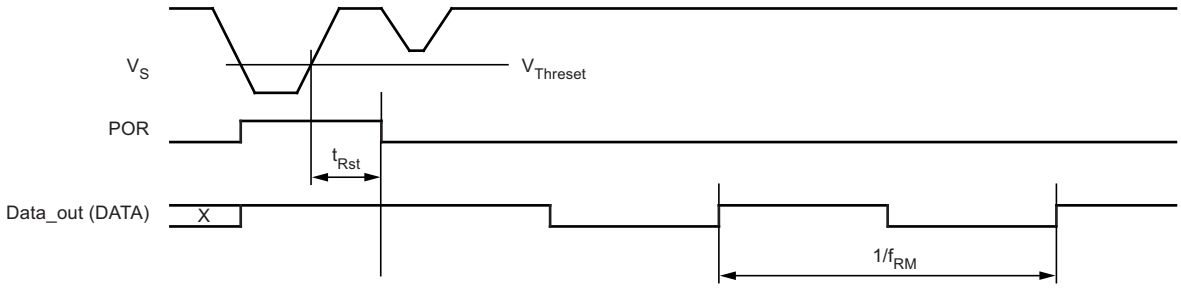
According to Figure 12-1, a power-on reset (POR) is generated if the supply voltage $V_S$ drops below the threshold voltage $V_{ThReset}$. The default parameters are programmed into the configuration registers in that condition. The POR is cancelled after the minimum reset period $t_{Rst}$ when $V_S$ exceeds $V_{ThReset}$. A POR is also generated when the supply voltage of the receiver is turned on.

To indicate that condition, the receiver displays a reset marker (RM) at pin DATA after a reset. The RM is represented by the fixed frequency $f_{RM}$ at a 50% duty-cycle. RM can be cancelled using a low pulse t1 at pin DATA. The RM has the following characteristics:

- $f_{RM}$ is lower than the lowest feasible frequency of a data signal. Due to this, RM cannot be misinterpreted by the connected microcontroller.
- If the receiver is set back to polling mode using pin DATA, RM cannot be cancelled accidentally if t1 is applied as described in the proposal in Section 13. “Programming the Configuration Register” on page 28.

Using this conservation mechanism, the receiver cannot lose its register information without communicating this condition using the reset marker RM.

**Figure 12-1. Generation of the Power-on Reset**



# 13. Programming the Configuration Register

**Figure 13-1. Timing of the Register Programming**

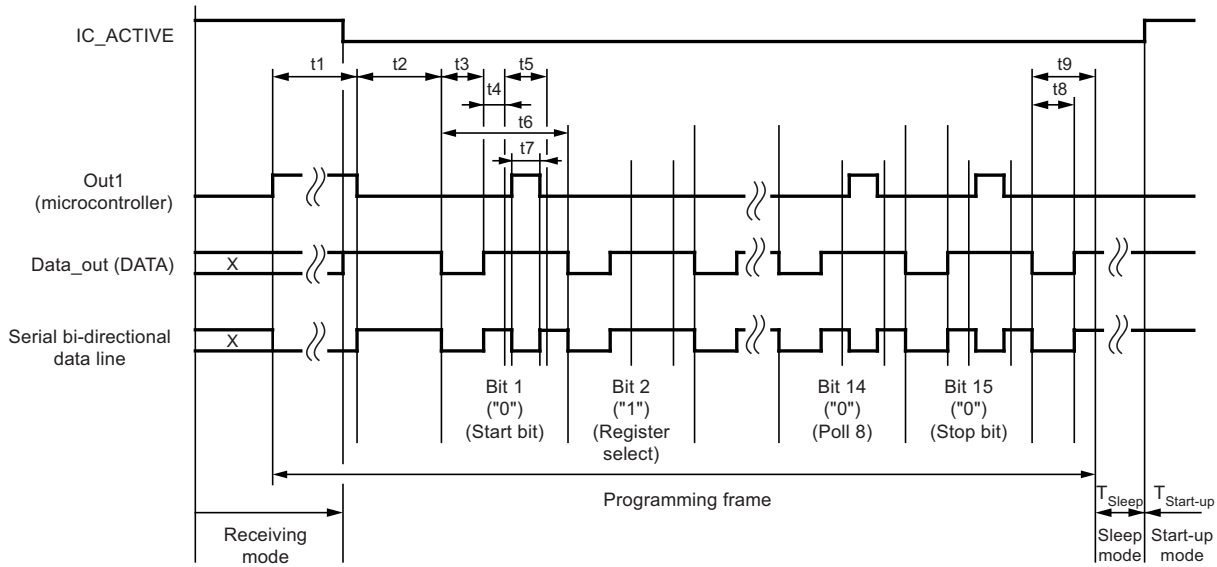
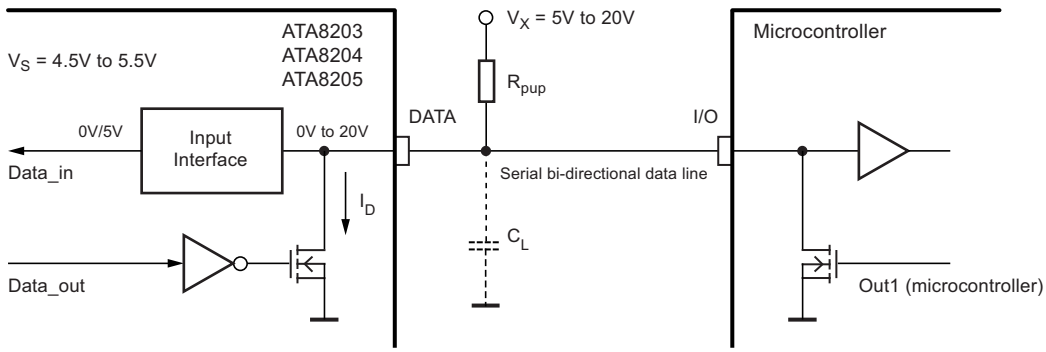



**Figure 13-2. Data Interface**




The configuration registers are serially programmed using the bi-directional data line as shown in Figure 13-1 and Figure 13-2.

To start programming, the serial data line DATA is pulled to low by the microcontroller for the time period t1. When DATA has been released, the receiver becomes the master device. When the programming delay period t2 has elapsed, the receiver emits 15 subsequent synchronization pulses with the pulse length t3. After each of these pulses, a programming window occurs. The delay until the program window starts is determined by t4, the duration is defined by t5. The individual bits are set within the programming window. If the microcontroller pulls down pin DATA for the time period t7 during t5, the corresponding bit is set to “0”. If no programming pulse t7 is issued, this bit is set to “1”. All 15 bits are programmed this way. The time frame to program a bit is defined by t6.

Bit 15 is followed by the equivalent time window t9. During this window, the equivalence acknowledge pulse t8 (E_Ack) occurs if the just programmed mode word is equivalent to the mode word that was already stored in that register. E_Ack should be used to verify that the mode word was correctly transferred to the register. The register must be programmed twice in that case.

A register can be programmed when the receiver is in both sleep-mode and active mode. During programming, the LNA, LO, low-pass filter, IF-amplifier, and the FSK/MSK demodulator are disabled. The t1 pulse is used to start the programming or to switch the receiver back to polling mode (OFF command). (The receiver is switched back to polling mode with the OFF command if bit 1 is set to „1“.) The following convention should be considered for the length of the programming start pulse t1:

Using a t1 value of t1 (min) < t1 < 5632 TClk (where t1 (min) is the minimum specified value for the relevant BR_Range) when the receiver is active i.e., not in reset mode initiates the programming or OFF command. However, if this t1 value is used when the receiver is in reset mode, programming or OFF command is NOT initiated and RM remains present at pin DATA. Note, the RM cannot be deleted when using this t1 value.

Using a t1 value of t1 > 7936 ´ TClk, programming or OFF command is initiated when the receiver is in both reset mode and active mode. The registers PMODE and LIMIT are set to the default values and the RM is deleted, if present. This t1 values can be used if the connected microcontroller detects an RM. Additionally, this t1 value can generally be used if the receiver operates in default mode.

Note that the capacitive load at pin DATA is limited.

# 14. Data Interface

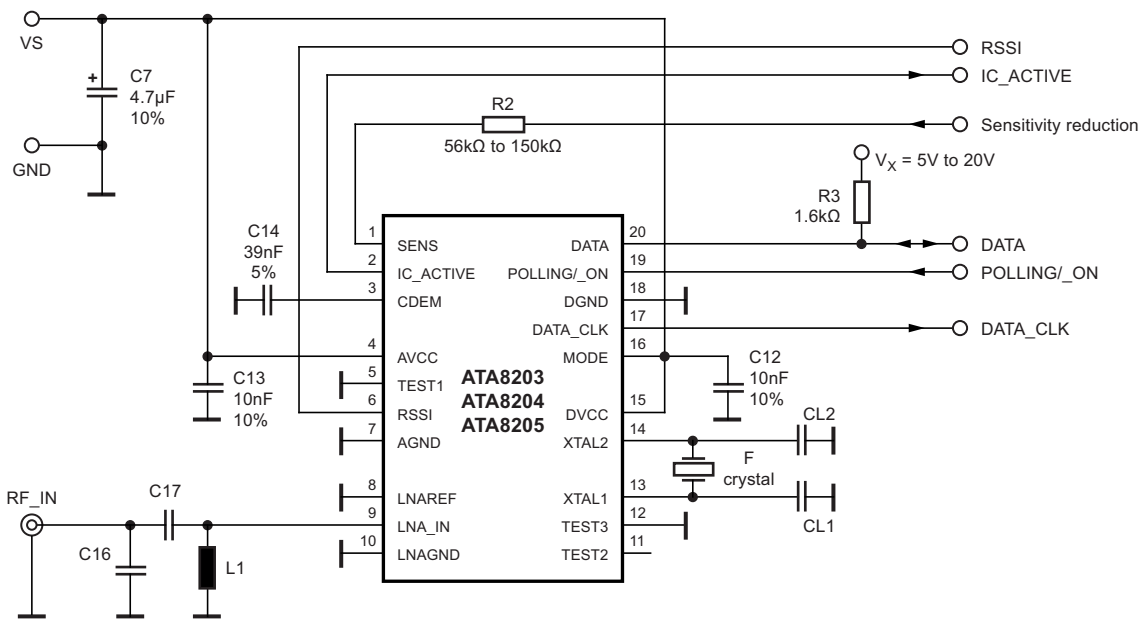
The data interface (see Figure 13-2 on page 28) is designed for automotive requirements. It can be connected using the pull-up resistor $R_{pup}$ up to 20V and is short-circuit-protected.

The applicable pull-up resistor $R_{pup}$ depends on the load capacity $C_L$ at pin DATA and the selected BR_range (see Table 14-1).

**Table 14-1. Applicable $R_{pup}$**

| - | BR_range | Applicable $R_{pup}$ |
|---|---|---|
| $C_L \leq 1nF$ | B0 | 1.6kΩ to 47kΩ |
| | B1 | 1.6kΩ to 22kΩ |
| | B2 | 1.6 Ω to 12kΩ |
| | B3 | 1.6kΩ to 5.6kΩ |
| $C_L \leq 100pF$ | B0 | 1.6kΩ to 470kΩ |
| | B1 | 1.6kΩ to 220kΩ |
| | B2 | 1.6kΩ to 120kΩ |
| | B3 | 1.6kΩ to 56kΩ |

**Figure 14-1. Application Circuit: $f_{RF}$ = 315MHz(1), 433.92MHz or 868MHz without SAW Filter**




Note: For 315MHz application pin MODE must be connected to GND.

**Table 14-2. Input Matching to 50Ω**

| RF Frequency (MHz) | LNA Matching | | | Crystal Frequency $f_{XTAL}$ (MHz) |
|---|---|---|---|---|
| | C16 (pF) | C17 (pF) | L1 (nH) | |
| 315 | Not connected | 3 | 39 | 14.71875 |
| 433.92 | Not connected | 3 | 20 | 13.52875 |
| 868.3 | 1 | 3 | 6.8 | 13.55234 |

## 15. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

| Parameters | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|
| Supply voltage | $V_S$ | | 6 | V |
| Power dissipation | $P_{tot}$ | | 1000 | mW |
| Junction temperature | $T_j$ | | 150 | °C |
| Storage temperature | $T_{stg}$ | –55 | +125 | °C |
| Ambient temperature | $T_{amb}$ | –40 | +85 | °C |
| Maximum input level, input matched to 50Ω | $P_{in_max}$ | | 10 | dBm |

## 16. Thermal Resistance

| Parameters | Symbol | Value | Unit |
|---|---|---|---|
| Junction ambient | $R_{thJA}$ | 100 | K/W |

# 17. Electrical Characteristics Atmel ATA8203

All parameters refer to GND, $T_{amb}$ = 25°C, $V_S$ = 5V, $f_0$ = 315MHz unless otherwise specified.

| No. | Parameter | Test Conditions | Symbol | $f_{RF}$ = 315MHz 14.71875MHz Oscillator | | | | | | Variable Oscillator | | | Unit | Type* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | | |
| 1 | Basic Clock Cycle of the Digital Circuitry | | | | | | | | | | | | | |
| 1.1 | Basic clock cycle | | $T_{Clk}$ | 2.0382 | | 2.0382 | | | | $30/f_{XTO}$ | | $30/f_{XTO}$ | µs | A |
| 1.2 | Extended basic clock cycle | BR_Range0<br>BR_Range1<br>BR_Range2<br>BR_Range3 | $T_{XClk}$ | 16.3057<br>8.1528<br>4.0764<br>2.0382 | | 16.3057<br>8.1528<br>4.0764<br>2.0382 | | | | $8 \times T_{Clk}$<br>$4 \times T_{Clk}$<br>$2 \times T_{Clk}$<br>$1 \times T_{Clk}$ | | $8 \times T_{Clk}$<br>$4 \times T_{Clk}$<br>$2 \times T_{Clk}$<br>$1 \times T_{Clk}$ | µs<br>µs<br>µs<br>µs | A |
| 2 | Polling Mode | | | | | | | | | | | | | |
| 2.1 | Sleep time (see Figure 8-1, Figure 8-10 and Figure 13-1) | Sleep and XSleep are defined in the OPMODE register | $T_{Sleep}$ | Sleep × $X_{Sleep}$ × 1024 × 2.0382 | | Sleep × $X_{Sleep}$ × 1024 × 2.0382 | | | | Sleep × $X_{Sleep}$ × 1024 × $T_{Clk}$ | | Sleep × $X_{Sleep}$ × 1024 × $T_{Clk}$ | ms | A |
| 2.2 | Start-up time (see Figure 8-1 and Figure 8-4) | BR_Range0<br>BR_Range1<br>BR_Range2<br>BR_Range3 | $T_{Startup}$ | 1827<br>1044<br>1044<br>653 | | 1827<br>1044<br>1044<br>653 | | | | 896.5<br>512.5<br>512.5<br>320.5<br>× $T_{Clk}$ | | 896.5<br>512.5<br>512.5<br>320.5<br>× $T_{Clk}$ | µs<br>µs<br>µs<br>µs<br>µs | A |
| 2.3 | Time for bit check (see Figure 8-1 | Average bit-check time while polling, no RF applied (see Figure 8-5 and Figure 8-6)<br>BR_Range0<br>BR_Range1<br>BR_Range2<br>BR_Range3 | $T_{Bit\text{-}check}$ | | 0.45<br>0.24<br>0.14<br>0.08 | | | | | | 0.45<br>0.24<br>0.14<br>0.08 | | ms<br>ms<br>ms<br>ms | C |
| 2.4 | Time for bit check (see Figure 8-1 | Bit-check time for a valid input signal $f_{Sig}$ (see Figure 8-5)<br>$N_{Bit\text{-}check}$ = 0<br>$N_{Bit\text{-}check}$ = 3<br>$N_{Bit\text{-}check}$ = 6<br>$N_{Bit\text{-}check}$ = 9 | $T_{Bit\text{-}check}$ | $1 \times T_{XClk}$<br>$3/f_{Sig}$<br>$6/f_{Sig}$<br>$9/f_{Sig}$ | | $1 \times T_{XClk}$<br>$3.5/f_{Sig}$<br>$6.5/f_{Sig}$<br>$9.5/f_{Sig}$ | | | | $1 \times T_{XClk}$<br>$3/f_{Sig}$<br>$6/f_{Sig}$<br>$9/f_{Sig}$ | | $1 \times T_{Clk}$<br>$3.5/f_{Sig}$<br>$6.5/f_{Sig}$<br>$9.5/f_{Sig}$ | ms<br>ms<br>ms<br>ms | C |
| 3 | Receiving Mode | | | | | | | | | | | | | |
| 3.1 | Intermediate frequency | | $f_{IF}$ | | 987 | | | | | $f_{IF} = f_{LO}/318$ | | | kHz | A |
| 3.2 | Baud-rate range | BR_Range0<br>BR_Range1<br>BR_Range2<br>BR_Range3 | BR_Range | 1.0<br>1.8<br>3.2<br>5.6 | | 1.8<br>3.2<br>5.6<br>10.0 | | | | BR_Range0 × 2 µs/$T_{Clk}$<br>BR_Range1 × 2 µs/$T_{Clk}$<br>BR_Range2 × 2 µs/$T_{Clk}$<br>BR_Range3 × 2 µs/$T_{Clk}$ | | | Kbit/s<br>Kbit/s<br>Kbit/s<br>Kbit/s | A |

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

## 17. Electrical Characteristics Atmel ATA8203 (Continued)

All parameters refer to GND, $T_{amb}$ = 25°C, $V_S$ = 5V, $f_0$ = 315MHz unless otherwise specified.

| No. | Parameter | Test Conditions | Symbol | $f_{RF}$ = 315MHz 14.71875MHz Oscillator | | | | | | Variable Oscillator | | | Unit | Type* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | | |
| 3.3 | Minimum time period between edges at pin DATA (see Figure 4-2 and Figure 8-8, Figure 8-9) (With the exception of parameter $T_{Pulse}$) | BR_Range =<br>BR_Range0<br>BR_Range1<br>BR_Range2<br>BR_Range3 | $t_{DATA_min}$ | 163.06<br>81.53<br>40.76<br>20.38 | | 163.06<br>81.53<br>40.76<br>20.38 | | | | $10 \times T_{XClk}$<br>$10 \times T_{XClk}$<br>$10 \times T_{XClk}$<br>$10 \times T_{XClk}$ | | $10 \times T_{XClk}$<br>$10 \times T_{XClk}$<br>$10 \times T_{XClk}$<br>$10 \times T_{XClk}$ | µs<br>µs<br>µs<br>µs | A |
| 3.4 | Maximum Low period at pin DATA (see Figure 4-2) | BR_Range =<br>BR_Range0<br>BR_Range1<br>BR_Range2<br>BR_Range3 | $t_{DATA_L_max}$ | 2120<br>1060<br>530<br>265 | | 2120<br>1060<br>530<br>265 | | | | $130 \times T_{XClk}$<br>$130 \times T_{XClk}$<br>$130 \times T_{XClk}$<br>$130 \times T_{XClk}$ | | $130 \times T_{XClk}$<br>$130 \times T_{XClk}$<br>$130 \times T_{XClk}$<br>$130 \times T_{XClk}$ | µs<br>µs<br>µs<br>µs | A |
| 3.5 | Delay to activate the start-up mode (see Figure 8-12) | | Ton1 | 19.36 | | 21.4 | | | | $9.5 \times T_{Clk}$ | | $10.5 \times T_{Clk}$ | µs | A |
| 3.6 | OFF command at pin POLLING/_ON (see Figure 8-11) | | Ton2 | 16.3 | | | | | | $8 \times T_{Clk}$ | | | µs | A |
| 3.7 | Delay to activate the sleep mode (see Figure 8-11) | | Ton3 | 17.32 | | 19.36 | | | | $8.5 \times T_{Clk}$ | | $9.5 \times T_{Clk}$ | µs | A |
| 3.8 | Pulse on pin DATA at the end of a data stream (see Figure 10-3) | BR_Range =<br>BR_Range0<br>BR_Range1<br>BR_Range2<br>BR_Range3 | $T_{Pulse}$ | 16.3<br>8.15<br>4.07<br>2.04 | | 16.3<br>8.15<br>4.07<br>2.04 | | | | $8 \times T_{Clk}$<br>$4 \times T_{Clk}$<br>$2 \times T_{Clk}$<br>$1 \times T_{Clk}$ | | $8 \times T_{Clk}$<br>$4 \times T_{Clk}$<br>$2 \times T_{Clk}$<br>$1 \times T_{Clk}$ | µs<br>µs<br>µs<br>µs | C |

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

## 17. Electrical Characteristics Atmel ATA8203 (Continued)

All parameters refer to GND, $T_{amb}$ = 25°C, $V_S$ = 5V, $f_0$ = 315MHz unless otherwise specified.

| No. | Parameter | Test Conditions | Symbol | $f_{RF}$ = 315MHz 14.71875MHz Oscillator | | | | | | Variable Oscillator | | | Unit | Type* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | | |
| 4 | Configuration of the Receiver (see Figure 12-1 and Figure 13-1) | | | | | | | | | | | | | |
| 4.1 | Frequency of the reset marker | Frequency is stable within 50ms after POR | $f_{RM}$ | 119.78 | | 119.78 | | | | 1/ (4096 × $T_{Clk}$) | | 1/ (4096 × $T_{Clk}$) | Hz | A |
| 4.2 | Programmin g start pulse | BR_Range = BR_Range0<br>BR_Range1<br>BR_Range2<br>BR_Range3<br>after POR | t1 | 3310<br>2242<br>1708<br>1441<br>16175 | | 11479<br>11479<br>11479<br>11479 | | | | 1624 × $T_{Clk}$<br>1100 × $T_{Clk}$<br>838 × $T_{Clk}$<br>707 × $T_{Clk}$<br>7936 × $T_{Clk}$ | | 5632 × $T_{Clk}$<br>5632 × $T_{Clk}$<br>5632 × $T_{Clk}$<br>5632 × $T_{Clk}$ | µs<br>µs<br>µs<br>µs<br>µs | A |
| 4.3 | Programmin g delay period | | t2 | 783 | | 785 | | | | 384.5 × $T_{Clk}$ | | 385.5 × $T_{Clk}$ | µs | A |
| 4.4 | Synchroniza - tion pulse | | t3 | 261 | | 261 | | | | 128 × $T_{Clk}$ | | 128 × $T_{Clk}$ | µs | A |
| 4.5 | Delay until of the program window starts | | t4 | 129 | | 129 | | | | 63.5 × $T_{Clk}$ | | 63.5 × $T_{Clk}$ | µs | A |
| 4.6 | Programmin g window | | t5 | 522 | | 522 | | | | 256 × $T_{Clk}$ | | 256 × $T_{Clk}$ | µs | A |
| 4.7 | Time frame of a bit | | t6 | 1044 | | 1044 | | | | 512 × $T_{Clk}$ | | 512 × $T_{Clk}$ | µs | A |
| 4.8 | Programmin g pulse | | t7 | 130.5 | | 522 | | | | 64 × $T_{Clk}$ | | 256 × $T_{Clk}$ | µs | C |
| 4.9 | Equivalent acknowledg e pulse: E_Ack | | t8 | 261 | | 261 | | | | 128 × $T_{Clk}$ | | 128 × $T_{Clk}$ | µs | A |
| 4.10 | Equivalent time window | | t9 | 526 | | 526 | | | | 258 × $T_{Clk}$ | | 258 × $T_{Clk}$ | µs | A |
| 4.11 | OFF-bit programmin g window | | t10 | 916 | | 916 | | | | 449.5 × $T_{Clk}$ | | 449.5 × $T_{Clk}$ | µs | A |
| 5 | Data Clock (see Figure 9-1 and Figure 9-6) | | | | | | | | | | | | | |
| 5.1 | Minimum delay time between edge at DATA and DATA_CLK | BR_Range = BR_Range0<br>BR_Range1<br>BR_Range2<br>BR_Range3 | $t_{Delay2}$ | 0<br>0<br>0<br>0 | | 16.3057<br>8.1528<br>4.0764<br>2.0382 | | | | 0<br>0<br>0<br>0 | | 1 × $T_{XClk}$<br>1 × $T_{XClk}$<br>1 × $T_{XClk}$<br>1 × $T_{XClk}$ | µs<br>µs<br>µs<br>µs | C |
| 5.2 | Pulse width of negative pulse at pin DATA_CLK | BR_Range = BR_Range0<br>BR_Range1<br>BR_Range2<br>BR_Range3 | $t_{P_DATA_CLK}$ | 65.2<br>32.6<br>16.3<br>8.15 | | 65.2<br>32.6<br>16.3<br>8.15 | | | | 4 × $T_{XClk}$<br>4 × $T_{XClk}$<br>4 × $T_{XClk}$<br>4 × $T_{XClk}$ | | 4 × $T_{XClk}$<br>4 × $T_{XClk}$<br>4 × $T_{XClk}$<br>4 × $T_{XClk}$ | µs<br>µs<br>µs<br>µs | A |

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

# 18. Electrical Characteristics Atmel ATA8204, ATA8205

All parameters refer to GND, $T_{amb}$ = 25°C, $V_S$ = 5V, $f_0$ = 433.92MHz and $f_0$ = 868.3MHz unless otherwise specified.

| No. | Parameter | Test Conditions | Symbol | $f_{RF}$ = 433.92MHz 13.52875MHz Oscillator | | | $f_{RF}$ = 868.3MHz, 13.55234MHz Oscillator | | | Variable Oscillator | | | Unit | Type* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | | |
| 6 | Basic Clock Cycle of the Digital Circuitry | | | | | | | | | | | | | |
| 6.1 | Basic clock cycle | | $T_{Clk}$ | 2.0696 | | 2.0696 | 2.066 | | 2.066 | $28/f_{XTO}$ | | $28/f_{XTO}$ | µs | A |
| 6.2 | Extended basic clock cycle | BR_Range0<br>BR_Range1<br>BR_Range2<br>BR_Range3 | $T_{XClk}$ | 16.557<br>8.278<br>4.139<br>2.069 | | 16.557<br>8.278<br>4.139<br>2.069 | 16.528<br>8.264<br>4.132<br>2.066 | | 16.528<br>8.264<br>4.132<br>2.066 | $8 \times T_{Clk}$<br>$4 \times T_{Clk}$<br>$2 \times T_{Clk}$<br>$1 \times T_{Clk}$ | | $8 \times T_{Clk}$<br>$4 \times T_{Clk}$<br>$2 \times T_{Clk}$<br>$1 \times T_{Clk}$ | µs<br>µs<br>µs<br>µs | A |
| 7 | Polling Mode | | | | | | | | | | | | | |
| 7.1 | Sleep time (see Figure 8-1, Figure 8-10 and Figure 13-1) | Sleep and XSleep are defined in the OPMODE register | $T_{Sleep}$ | Sleep × $X_{Sleep}$ × 1024 × 2.0696 | | Sleep × $X_{Sleep}$ × 1024 × 2.0696 | Sleep × $X_{Sleep}$ × 1024 × 2.066 | | Sleep × $X_{Sleep}$ × 1024 × 2.066 | Sleep × $X_{Sleep}$ × 1024 × $T_{Clk}$ | | Sleep × $X_{Sleep}$ × 1024 × $T_{Clk}$ | ms | A |
| 7.2 | Start-up time (see Figure 8-1 and Figure 8-4) | BR_Range0<br>BR_Range1<br>BR_Range2<br>BR_Range3 | $T_{Startup}$ | 1855<br>1060<br>1060<br>663 | | 1855<br>1060<br>1060<br>663 | 1852<br>1058<br>1058<br>662 | | 1852<br>1058<br>1058<br>662 | 896.5<br>512.5<br>512.5<br>320.5<br>× $T_{Clk}$ | | 896.5<br>512.5<br>512.5<br>320.5<br>× $T_{Clk}$ | µs<br>µs<br>µs<br>µs<br>µs | A |
| 7.3 | Time for bit check (see Figure 8-1 | Average bit-check time while polling, no RF applied (see Figure 8-8 on page 15 and Figure 8-9 on page 16)<br>BR_Range0<br>BR_Range1<br>BR_Range2<br>BR_Range3 | $T_{Bit\text{-}check}$ | | 0.45<br>0.24<br>0.14<br>0.08 | | | 0.45<br>0.24<br>0.14<br>0.08 | | | 0.45<br>0.24<br>0.14<br>0.08 | | ms<br>ms<br>ms<br>ms | C |
| 7.4 | Time for bit check (see Figure 8-1 | Bit-check time for a valid input signal $f_{Sig}$ (see Figure 8-5 on page 14)<br>$N_{Bit\text{-}check}$ = 0<br>$N_{Bit\text{-}check}$ = 3<br>$N_{Bit\text{-}check}$ = 6<br>$N_{Bit\text{-}check}$ = 9 | $T_{Bit\text{-}check}$ | $1 \times T_{XClk}$<br>$3/f_{Sig}$<br>$6/f_{Sig}$<br>$9/f_{Sig}$ | | $1 \times T_{XClk}$<br>$3.5/f_{Sig}$<br>$6.5/f_{Sig}$<br>$9.5/f_{Sig}$ | $1 \times T_{XClk}$<br>$3/f_{Sig}$<br>$6/f_{Sig}$<br>$9/f_{Sig}$ | | $1 \times T_{XClk}$<br>$3.5/f_{Sig}$<br>$6.5/f_{Sig}$<br>$9.5/f_{Sig}$ | $1 \times T_{XClk}$<br>$3/f_{Sig}$<br>$6/f_{Sig}$<br>$9/f_{Sig}$ | | $1 \times T_{Clk}$<br>$3.5/f_{Sig}$<br>$6.5/f_{Sig}$<br>$9.5/f_{Sig}$ | ms<br>ms<br>ms<br>ms | C |
| 8 | Receiving Mode | | | | | | | | | | | | | |
| 8.1 | Intermediate frequency | | $f_{IF}$ | | 987 | | | 947.9 | | $f_{IF} = f_{LO}/438$ for the 433.92MHz band (ATA8204)<br>$f_{IF} = f_{LO}/915$ for the 868.3MHz band (ATA8205) | | | kHz | A |
| 8.2 | Baud-rate range | BR_Range0<br>BR_Range1<br>BR_Range2<br>BR_Range3 | BR_Range | 1.0<br>1.8<br>3.2<br>5.6 | | 1.8<br>3.2<br>5.6<br>10.0 | 1.0<br>1.8<br>3.2<br>5.6 | | 1.8<br>3.2<br>5.6<br>10.0 | BR_Range0 × 2 µs/$T_{Clk}$<br>BR_Range1 × 2 µs/$T_{Clk}$<br>BR_Range2 × 2 µs/$T_{Clk}$<br>BR_Range3 × 2 µs/$T_{Clk}$ | | | Kbit/s<br>Kbit/s<br>Kbit/s<br>Kbit/s | A |

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

## 18. Electrical Characteristics Atmel ATA8204, ATA8205 (Continued)

All parameters refer to GND, $T_{amb}$ = 25°C, $V_S$ = 5V, $f_0$ = 433.92MHz and $f_0$ = 868.3MHz unless otherwise specified.

| No. | Parameter | Test Conditions | Symbol | $f_{RF}$ = 433.92MHz 13.52875MHz Oscillator | | | $f_{RF}$ = 868.3MHz, 13.55234MHz Oscillator | | | Variable Oscillator | | | Unit | Type* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | | |
| 8.3 | Minimum time period between edges at pin DATA (see Figure 4-2 and Figure 8-8, Figure 8-9) (With the exception of parameter $T_{Pulse}$) | BR_Range =<br>BR_Range0<br>BR_Range1<br>BR_Range2<br>BR_Range3 | $t_{DATA_min}$ | <br>165.5<br>82.8<br>41.4<br>20.7 | | <br>165.5<br>82.8<br>41.4<br>20.7 | <br>165.3<br>82.6<br>41.3<br>20.6 | | <br>165.3<br>82.6<br>41.3<br>20.6 | <br>$10 \times T_{XClk}$<br>$10 \times T_{XClk}$<br>$10 \times T_{XClk}$<br>$10 \times T_{XClk}$ | | <br>$10 \times T_{XClk}$<br>$10 \times T_{XClk}$<br>$10 \times T_{XClk}$<br>$10 \times T_{XClk}$ | <br>µs<br>µs<br>µs<br>µs | A |
| 8.4 | Maximum Low period at pin DATA (see Figure 4-2) | BR_Range =<br>BR_Range0<br>BR_Range1<br>BR_Range2<br>BR_Range3 | $t_{DATA_L_max}$ | <br>2152<br>1076<br>538<br>269 | | <br>2152<br>1076<br>538<br>269 | <br>2148<br>1074<br>537<br>268.5 | | <br>2148<br>1074<br>537<br>268.5 | <br>$130 \times T_{XClk}$<br>$130 \times T_{XClk}$<br>$130 \times T_{XClk}$<br>$130 \times T_{XClk}$ | | <br>$130 \times T_{XClk}$<br>$130 \times T_{XClk}$<br>$130 \times T_{XClk}$<br>$130 \times T_{XClk}$ | <br>µs<br>µs<br>µs<br>µs | A |
| 8.5 | Delay to activate the start-up mode (see Figure 8-12) | | Ton1 | 19.6 | | 21.7 | 19.6 | | 21.7 | $9.5 \times T_{Clk}$ | | $10.5 \times T_{Clk}$ | µs | A |
| 8.6 | OFF command at pin POLLING/_ON (see Figure 8-11) | | Ton2 | 16.5 | | | 16.5 | | | $8 \times T_{Clk}$ | | | µs | A |
| 8.7 | Delay to activate the sleep mode (see Figure 8-11) | | Ton3 | 17.6 | | 19.6 | 17.6 | | 19.6 | $8.5 \times T_{Clk}$ | | $9.5 \times T_{Clk}$ | µs | A |
| 8.8 | Pulse on pin DATA at the end of a data stream (see Figure 10-3) | BR_Range =<br>BR_Range0<br>BR_Range1<br>BR_Range2<br>BR_Range3 | $T_{Pulse}$ | <br>16.557<br>8.278<br>4.139<br>2.069 | | <br>16.557<br>8.278<br>4.139<br>2.069 | <br>16.528<br>8.264<br>4.132<br>2.066 | | <br>16.528<br>8.264<br>4.132<br>2.066 | <br>$8 \times T_{Clk}$<br>$4 \times T_{Clk}$<br>$2 \times T_{Clk}$<br>$1 \times T_{Clk}$ | | <br>$8 \times T_{Clk}$<br>$4 \times T_{Clk}$<br>$2 \times T_{Clk}$<br>$1 \times T_{Clk}$ | <br>µs<br>µs<br>µs<br>µs | C |

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

# 18. Electrical Characteristics Atmel ATA8204, ATA8205 (Continued)

All parameters refer to GND, $T_{amb}$ = 25°C, $V_S$ = 5V, $f_0$ = 433.92MHz and $f_0$ = 868.3MHz unless otherwise specified.

| No. | Parameter | Test Conditions | Symbol | $f_{RF}$ = 433.92MHz 13.52875MHz Oscillator | | | $f_{RF}$ = 868.3MHz, 13.55234MHz Oscillator | | | Variable Oscillator | | | Unit | Type* |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | | |
| 9 | Configuration of the Receiver (see Figure 12-1 and Figure 13-1) | | | | | | | | | | | | | |
| 9.1 | Frequency of the reset marker | Frequency is stable within 50ms after POR | $f_{RM}$ | 117.9 | | 117.9 | 118.2 | | 118.2 | 1/ (4096 × $T_{Clk}$) | | 1/ (4096 × $T_{Clk}$) | Hz | A |
| 9.2 | Programming start pulse | BR_Range = BR_Range0<br>BR_Range1<br>BR_Range2<br>BR_Range3<br>after POR | t1 | 3361<br>2276<br>1734<br>1463<br>16425 | | 11656<br>11656<br>11656<br>11656 | 3355<br>2272<br>1731<br>1460 | | 11636<br>11636<br>11636<br>11636 | 1624 × $T_{Clk}$<br>1100 × $T_{Clk}$<br>838 × $T_{Clk}$<br>707 × $T_{Clk}$<br>7936 × $T_{Clk}$ | | 5632 × $T_{Clk}$<br>5632 × $T_{Clk}$<br>5632 × $T_{Clk}$<br>5632 × $T_{Clk}$ | µs<br>µs<br>µs<br>µs<br>µs | A |
| 9.3 | Programming delay period | | t2 | 796 | | 798 | 794 | | 796 | 384.5 × $T_{Clk}$ | | 385.5 × $T_{Clk}$ | µs | A |
| 9.4 | Synchronization pulse | | t3 | 265 | | 265 | 264 | | 264 | 128 × $T_{Clk}$ | | 128 × $T_{Clk}$ | µs | A |
| 9.5 | Delay until of the program window starts | | t4 | 131 | | 131 | 131 | | 131 | 63.5 × $T_{Clk}$ | | 63.5 × $T_{Clk}$ | µs | A |
| 9.6 | Programming window | | t5 | 530 | | 530 | 529 | | 529 | 256 × $T_{Clk}$ | | 256 × $T_{Clk}$ | µs | A |
| 9.7 | Time frame of a bit | | t6 | 1060 | | 1060 | 1058 | | 1058 | 512 × $T_{Clk}$ | | 512 × $T_{Clk}$ | µs | A |
| 9.8 | Programming pulse | | t7 | 132 | | 530 | 132 | | 529 | 64 × $T_{Clk}$ | | 256 × $T_{Clk}$ | µs | C |
| 9.9 | Equivalent acknowledge pulse: E_Ack | | t8 | 265 | | 265 | 264 | | 264 | 128 × $T_{Clk}$ | | 128 × $T_{Clk}$ | µs | A |
| 9.10 | Equivalent time window | | t9 | 534 | | 534 | 533 | | 533 | 258 × $T_{Clk}$ | | 258 × $T_{Clk}$ | µs | A |
| 9.11 | OFF-bit programming window | | t10 | 930 | | 930 | 929 | | 929 | 449.5 × $T_{Clk}$ | | 449.5 × $T_{Clk}$ | µs | A |
| 10 | Data Clock (see Figure 9-1 and Figure 9-6) | | | | | | | | | | | | | |
| 10.1 | Minimum delay time between edge at DATA and DATA_CLK | BR_Range = BR_Range0<br>BR_Range1<br>BR_Range2<br>BR_Range3 | $t_{Delay2}$ | 0<br>0<br>0<br>0 | | 16.557<br>8.278<br>4.139<br>2.069 | 0<br>0<br>0<br>0 | | 16.528<br>8.264<br>4.132<br>2.066 | 0<br>0<br>0<br>0 | | 1 × $T_{XClk}$<br>1 × $T_{XClk}$<br>1 × $T_{XClk}$<br>1 × $T_{XClk}$ | µs<br>µs<br>µs<br>µs | C |
| 10.2 | Pulse width of negative pulse at pin DATA_CLK | BR_Range = BR_Range0<br>BR_Range1<br>BR_Range2<br>BR_Range3 | $t_{P_DATA_CLK}$ | 66.2<br>33.1<br>16.5<br>8.3 | | 62.2<br>33.1<br>16.5<br>8.3 | 66.1<br>33.0<br>16.5<br>8.25 | | 66.1<br>33.0<br>16.5<br>8.25 | 4 × $T_{XClk}$<br>4 × $T_{XClk}$<br>4 × $T_{XClk}$<br>4 × $T_{XClk}$ | | 4 × $T_{XClk}$<br>4 × $T_{XClk}$<br>4 × $T_{XClk}$<br>4 × $T_{XClk}$ | µs<br>µs<br>µs<br>µs | A |

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

# 19. Electrical Characteristics Atmel ATA8203, ATA8204, ATA8205

All parameters refer to GND, $T_{amb}$ = 25°C, $V_S$ = 5V, $f_0$ = 868.3MHz, $f_0$ = 433.92MHz and $f_0$ = 315MHz, unless otherwise specified.

| No. | Parameters | Test Conditions | Symbol | Min. | Typ. | Max. | Unit | Type* |
|---|---|---|---|---|---|---|---|---|
| 11 | Current Consumption | | | | | | | |
| 11.1 | Current consumption | Sleep mode<br>(XTO and polling logic active) | $IS_{off}$ | | 170 | 290 | µA | A |
| | | IC active (start-up-, bit-check-, receiving mode) Pin DATA = H<br>FSK<br>ASK | $IS_{on}$ | | <br>8.5<br>8.0 | <br>11.0<br>10.4 | <br>mA<br>mA | A |
| 12 | LNA, Mixer, Polyphase Low-pass and IF Amplifier (Input Matched According to Figure 14-1 on page 30 Referred to RFIN) | | | | | | | |
| 12.1 | Third-order intercept point | LNA/mixer/IF amplifier<br>868MHz<br>433MHz<br>315MHz | IIP3 | | <br>–18<br>–23<br>–24 | | dBm | C |
| 12.2 | LO spurious emission | Required according to I-ETS 300220 | $IS_{LORF}$ | | –70 | –57 | dBm | A |
| 12.3 | System noise figure | With power matching \|S11\| < –10dB | NF | | 5 | | dB | B |
| 12.4 | LNA_IN input impedance | At 868.3MHz<br>AT 433.92MHz<br>At 315MHz | $Zi_{LNA_IN}$ | | (14.15 – j73.53)<br>(19.3 – j113.3)<br>(26.97 – j158.7) | | Ω<br>Ω<br>Ω | C |
| 12.5 | 1 dB compression point | At 868.3MHz<br>AT 433.92MHz<br>At 315MHz | $IP_{1db}$ | | –27.7<br>–32.7<br>–33.7 | | dBm | C |
| 12.6 | Image rejection | Within the complete image band | | 20 | 30 | | dB | A |
| 12.7 | Maximum input level | BER ≤ $10^{-3}$,<br>FSK mode<br>ASK mode | $P_{in_max}$ | | | <br>–10<br>–10 | <br>dBm<br>dBm | C |
| 13 | Local Oscillator | | | | | | | |
| 13.1 | Operating frequency range VCO | ATA8205<br>ATA8204<br>ATA8203 | $f_{VCO}$ | 868<br>431.5<br>312.5 | | 870<br>436.5<br>317.5 | MHz<br>MHz<br>MHz | A |
| 13.2 | Phase noise local oscillator | $f_{osc}$ = 868.3MHz at 10MHz<br>$f_{osc}$ = 433.92MHz at 10MHz<br>$f_{osc}$ = 315MHz at 10MHz | L (fm) | | –140<br>–143<br>–143 | –130<br>–133<br>–133 | dBC/Hz | B |
| 13.3 | Spurious of the VCO | At $\pm f_{XTO}$ | | | –55 | –45 | dBC | B |
| 13.4 | XTO pulling | XTO pulling,<br>appropriate load capacitance must be connected to XTAL, crystal CL1 and CL2<br>$f_{XTAL}$ = 14.71875MHz (315MHz band)<br>$f_{XTAL}$ = 13.52875MHz (433MHz band)<br>$f_{XTAL}$ = 13.55234MHz (868MHz band) | $f_{XTO}$ | –10ppm | $f_{XTAL}$ | +10ppm | MHz | B |
| 13.5 | Series resonance resistor of the crystal | Parameter of the supplied crystal | $R_S$ | | | 120 | Ω | B |

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

All parameters refer to GND, $T_{amb}$ = 25°C, $V_S$ = 5V, $f_0$ = 868.3MHz, $f_0$ = 433.92MHz and $f_0$ = 315MHz, unless otherwise specified.

| No. | Parameters | Test Conditions | Symbol | Min. | Typ. | Max. | Unit | Type* |
|---|---|---|---|---|---|---|---|---|
| 13.6 | Static capacitance at pin XTAL1 to GND | Parameter of the supplied crystal and board parasitics | $C_{L1}$ | –5% | 18 | +5% | pF | B |
| 13.7 | Static capacitance at pin XTAL2 to GND | Parameter of the supplied crystal and board parasitics | $C_{L2}$ | –5% | 18 | +5% | pF | B |
| 13.8 | Crystal series resistor Rm at start-up | $C_0$ < 1.8pF, $C_L$ = 9pF<br>$f_{XTAL}$ = 14.71875MHz | | | 1.5 | | kΩ | B |
| | | $C_0$ < 2.0pF, $C_L$ = 9pF<br>$f_{XTAL}$ = 13.52875MHz<br>$f_{XTAL}$ = 13.55234MHz | | | 1.5 | | kΩ | B |
| 14 | Analog Signal Processing (Input Matched According to Figure 14-1 on page 30 Referred to RFIN) | | | | | | | |
| 14.1 | Input sensitivity ASK 300 kHz IF Filter (ATA8203/ATA8204) | ASK (level of carrier)<br>BER ≤ $10^{-3}$, 100% Mod<br>$f_{in}$ = 315MHz/433.92MHz<br>$V_S$ = 5V, $T_{amb}$ = 25°C<br>$f_{IF}$ = 987kHz | $P_{Ref_ASK}$ | | | | | |
| | | BR_Range0 | | –111 | –113 | –115 | dBm | B |
| | | BR_Range1 | | –109.5 | –111.5 | –113.5 | dBm | B |
| | | BR_Range2 | | –109 | –111 | –113 | dBm | B |
| | | BR_Range3 | | –107 | –109 | –111 | dBm | B |
| 14.2 | Input sensitivity ASK 600 kHz IF Filter (ATA8205) | ASK (level of carrier)<br>BER ≤ $10^{-3}$, 100% Mod<br>$f_{in}$ = 868.3MHz<br>$V_S$ = 5V, $T_{amb}$ = 25°C<br>$f_{IF}$ = 948kHz | $P_{Ref_ASK}$ | | | | | |
| | | BR_Range0 | | –109 | –111 | –113 | dBm | B |
| | | BR_Range1 | | –107.5 | –109.5 | –111.5 | dBm | B |
| | | BR_Range2 | | –107 | –109 | –111 | dBm | B |
| | | BR_Range3 | | –105 | –107 | –109 | dBm | B |
| 14.3 | Sensitivity variation ASK for the full operating range compared to $T_{amb}$ = 25°C, $V_S$ = 5V (ATA8203/ATA8204/ATA8205) | 300kHz and 600kHz<br>$f_{in}$ = 315MHz/433.92MHz/868.3MHz<br>$P_{ASK} = P_{Ref_ASK} + \Delta P_{Ref}$ | $\Delta P_{Ref}$ | +2.5 | | –1.5 | dB | B |
| 14.4 | Sensitivity variation ASK for full operating range including IF filter compared to $T_{amb}$ = 25°C, $V_S$ = 5V | 300 kHz version (ATA8203/ATA8204)<br>$f_{in}$ = 315MHz/433.92MHz<br>$f_{IF}$ = 987kHz<br>$f_{IF}$ = –110kHz to +110kHz<br>$f_{IF}$ = –140kHz to +140kHz<br>$P_{ASK} = P_{Ref_ASK} + \Delta P_{Ref}$ | $\Delta P_{Ref}$ | +7.5<br>+9.5 | | –1.5<br>–1.5 | dB<br>dB | B |
| | | 600kHz version (ATA8205)<br>$f_{in}$ = 868.3MHz<br>$f_{IF}$ = 948kHz<br>$f_{IF}$ = –210kHz to +210kHz<br>$f_{IF}$ = –270kHz to +270kHz<br>$P_{ASK} = P_{Ref_ASK} + \Delta P_{Ref}$ | $\Delta P_{Ref}$ | +6.5<br>+8.5 | | –1.5<br>–1.5 | dB<br>dB | B |

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

## 19. Electrical Characteristics Atmel ATA8203, ATA8204, ATA8205 (Continued)

All parameters refer to GND, $T_{amb}$ = 25°C, $V_S$ = 5V, $f_0$ = 868.3MHz, $f_0$ = 433.92MHz and $f_0$ = 315MHz, unless otherwise specified.

| No. | Parameters | Test Conditions | Symbol | Min. | Typ. | Max. | Unit | Type* |
|---|---|---|---|---|---|---|---|---|
| 14.5 | Input sensitivity FSK 300kHz IF filter (ATA8203/ATA8204) | BER ≤ $10^{-3}$<br>$f_{in}$ = 315MHz/433.92MHz<br>$V_S$ = 5V, $T_{amb}$ = 25°C<br>$f_{IF}$ = 987kHz | | | | | | |
| | | BR_Range0<br>df = ±16kHz<br>df = ±10kHz to ±30kHz | $P_{Ref_FSK}$ | –104<br>–102 | –107 | –108.5<br>–108.5 | dBm<br>dBm | B |
| | | BR_Range1<br>df = ±16kHz<br>df = ±10kHz to ±30kHz | $P_{Ref_FSK}$ | –102<br>–100 | –105 | –106.5<br>–106.5 | dBm<br>dBm | B |
| | | BR_Range2<br>df = ±16kHz<br>df = ±10kHz to ±30kHz | $P_{Ref_FSK}$ | –100.5<br>–98.5 | –103.5 | –105<br>–105 | dBm<br>dBm | B |
| | | BR_Range3<br>df = ±16kHz<br>df = ±10kHz to ±30kHz | $P_{Ref_FSK}$ | –98.5<br>–96.5 | –101.5 | –103<br>–103 | dBm<br>dBm | B |
| 14.6 | Input sensitivity FSK 600kHz IF filter (ATA8205) | BER ≤ $10^{-3}$<br>$f_{in}$ = 868.3MHz<br>$V_S$ = 5V, $T_{amb}$ = 25°C<br>$f_{IF}$ = 948kHz | | | | | | |
| | | BR_Range0<br>df = ±16kHz to ±28kHz<br>df = ±10kHz to ±100kHz | $P_{Ref_FSK}$ | –102<br>–100 | –105 | –106.5<br>–106.5 | dBm<br>dBm | B |
| | | BR_Range1<br>df = ±16kHz ±28kHz<br>df = ±10kHz to ±100kHz | $P_{Ref_FSK}$ | –100<br>–98 | –103 | –104.5<br>–104.5 | dBm<br>dBm | B |
| | | BR_Range2<br>df = ±18kHz ±31kHz<br>df = ±13kHz to ±100kHz | $P_{Ref_FSK}$ | –98.5<br>–96.5 | –101.5 | –103<br>–103 | dBm<br>dBm | B |
| | | BR_Range3<br>df = ±25kHz ±44kHz<br>df = ±20kHz to ±100kHz | $P_{Ref_FSK}$ | –96.5<br>–94.5 | –99.5 | –101<br>–101 | dBm<br>dBm | B |
| 14.7 | Sensitivity variation FSK for the full operating range compared to $T_{amb}$ = 25°C, $V_S$ = 5V (ATA8203/ATA8204/ATA8205) | 300kHz and 600kHz versions<br>$f_{in}$ = 315MHz/433.92MHz/868.3MHz<br>$P_{FSK} = P_{Ref_FSK} + \Delta P_{Ref}$ | $\Delta P_{Ref}$ | +3 | | –1.5 | dB | B |

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

## 19. Electrical Characteristics Atmel ATA8203, ATA8204, ATA8205 (Continued)

All parameters refer to GND, $T_{amb}$ = 25°C, $V_S$ = 5V, $f_0$ = 868.3MHz, $f_0$ = 433.92MHz and $f_0$ = 315MHz, unless otherwise specified.

| No. | Parameters | Test Conditions | Symbol | Min. | Typ. | Max. | Unit | Type* |
|---|---|---|---|---|---|---|---|---|
| 14.8 | Sensitivity variation FSK for the full operating range including IF filter compared to $T_{amb}$ = 25°C, $V_S$ = 5V | 300kHz version (ATA8203/ATA8204)<br>$f_{in}$ = 315MHz/433.92MHz<br>$f_{IF}$ = 987kHz<br>$f_{IF}$ = –110kHz to +110kHz<br>$f_{IF}$ = –140kHz to +140kHz<br>$f_{IF}$ = –180kHz to +180kHz<br>$P_{FSK} = P_{Ref_FSK} + \Delta P_{Ref}$ | $\Delta P_{Ref}$ | +8<br>+10<br>+13 | | –2<br>–2<br>–2 | dB<br>dB<br>dB | B |
| | | 600kHz version (ATA8205)<br>$f_{in}$ = 868.3MHz<br>$f_{IF}$ = 948kHz<br>$f_{IF}$ = –150kHz to +150kHz<br>$f_{IF}$ = –200kHz to +200kHz<br>$f_{IF}$ = –260kHz to +150kHz<br>$P_{FSK} = P_{Ref_FSK} + \Delta P_{Ref}$ | $\Delta P_{Ref}$ | +7<br>+9<br>+12 | | –2<br>–2<br>–2 | dB<br>dB<br>dB | B |
| 14.9 | S/N ratio to suppress in-band noise signals. Noise signals may have any modulation scheme | ASK mode<br>FSK mode | $SNR_{ASK}$<br>$SNR_{FSK}$ | | 10<br>2 | 12<br>3 | dB<br>dB | C |
| 14.10 | Dynamic range RSSI amplifier | | $\Delta R_{RSSI}$ | | 60 | | dB | A |
| 14.11 | RSSI output voltage range | | $V_{RSSI}$ | 1 | | 3.5 | V | A |
| 14.12 | RSSI gain | | $G_{RSSI}$ | | 20 | | mV/dB | A |
| 14.13 | Lower cut-off frequency of the data filter | $f_{cu_DF} = \frac{1}{2 \times \pi \times 30\ k\Omega \times CDEM}$<br>CDEM = 33nF | fcu_DF | 0.11 | 0.16 | 0.20 | kHz | B |
| 14.14 | Recommended CDEM for best performance | BR_Range0 (default)<br>BR_Range1<br>BR_Range2<br>BR_Range3 | CDEM | | 39<br>22<br>12<br>8.2 | | nF<br>nF<br>nF<br>nF | C |
| 14.15 | Edge-to-edge time period of the input data signal for full sensitivity | BR_Range0 (default)<br>BR_Range1<br>BR_Range2<br>BR_Range3 | $t_{ee_sig}$ | 270<br>156<br>89<br>50 | | 1000<br>560<br>320<br>180 | ms<br>ms<br>ms<br>ms | C |
| 14.16 | Upper cut-off frequency data filter | Upper cut-off frequency programmable in 4 ranges using a serial mode word<br>BR_Range0 (default)<br>BR_Range1<br>BR_Range2<br>BR_Range3 | fu | 2.8<br>4.8<br>8.0<br>15.0 | 3.4<br>6.0<br>10.0<br>19.0 | 4.0<br>7.2<br>12.0<br>23.0 | kHz<br>kHz<br>kHz<br>kHz | B |
| 14.17 | Reduced sensitivity | 300kHz version (ATA8203/ATA8204)<br>$R_{Sense}$ connected from pin SENS to $V_S$, input matched according to Figure 14-1 “Application Circuit,<br>$f_{in}$ = 315MHz/433.92MHz,<br>$V_S$ = 5V, $T_{amb}$ = +25°C | | | | | dBm (peak level) | |
| | | $R_{Sense}$ = 56kΩ | $P_{Ref_Red}$ | –71 | –79 | –86 | dBm | B |
| | | $R_{Sense}$ = 100kΩ | $P_{Ref_Red}$ | –80 | –88 | –96 | dBm | B |

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

## 19. Electrical Characteristics Atmel ATA8203, ATA8204, ATA8205 (Continued)

All parameters refer to GND, $T_{amb}$ = 25°C, $V_S$ = 5V, $f_0$ = 868.3MHz, $f_0$ = 433.92MHz and $f_0$ = 315MHz, unless otherwise specified.

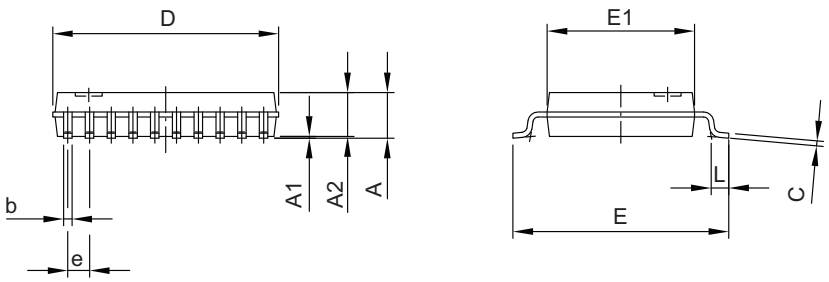
| No. | Parameters | Test Conditions | Symbol | Min. | Typ. | Max. | Unit | Type* |
|---|---|---|---|---|---|---|---|---|
| 14.18 | Reduced sensitivity | 600kHz version (ATA8205)<br>$R_{Sense}$ connected from pin SENS to $V_S$, input matched according to Figure 14-1 "Application Circuit,<br>$f_{in}$ = 868.3MHz,<br>$V_S$ = 5V, $T_{amb}$ = +25°C | | | | | dBm (peak level) | |
| | | $R_{Sense}$ = 56kΩ | $P_{Ref_Red}$ | –60 | –68 | –76 | dBm | B |
| | | $R_{Sense}$ = 100kΩ | $P_{Ref_Red}$ | –69 | –77 | –85 | dBm | B |
| 14.19 | Reduced sensitivity variation over full operating range | $R_{Sense}$ = 56kΩ<br>$R_{Sense}$ = 100kΩ<br>$P_{Red} = P_{Ref_Red} + \Delta P_{Red}$ | $\Delta P_{Red}$ | 5<br>5 | 0<br>0 | 0<br>0 | dB<br>dB | C |
| 14.20 | Reduced sensitivity variation for different values of $R_{Sense}$ | Values relative to $R_{Sense}$ = 56kΩ<br>$R_{Sense}$ = 56kΩ<br>$R_{Sense}$ = 68kΩ<br>$R_{Sense}$ = 82kΩ<br>$R_{Sense}$ = 100kΩ | $\Delta P_{Red}$ | | 0<br>–3.5<br>–6.0<br>–9.0 | | dB<br>dB<br>dB<br>dB | C |
| 14.21 | Threshold voltage for reset | | $V_{ThRESET}$ | 1.95 | 2.8 | 3.75 | V | A |
| 15 | Digital Ports | | | | | | | |
| 15.1 | Data output<br>- Saturation voltage Low<br><br>- max voltage at pin DATA<br>- quiescent current<br>- short-circuit current<br>- ambient temp. in case of permanent short-circuit<br>Data input<br>- Input voltage Low<br>- Input voltage High | $I_{ol} \leq$ 12mA<br>$I_{ol}$ = 2mA<br><br>$V_{oh}$ = 20V<br>$V_{ol}$ = 0.8V to 20V<br>$V_{oh}$ = 0V to 20V | $V_{ol}$<br>$V_{ol}$<br>$V_{oh}$<br>$I_{qu}$<br>$I_{ol_lim}$<br>$t_{amb_sc}$<br><br>$V_{Il}$<br>$V_{ich}$ | 13<br><br>$0.65 \times V_S$ | 0.35<br>0.08<br><br>30 | 0.8<br>0.3<br>20<br>20<br>45<br>85<br><br>$0.35 \times V_S$ | V<br>V<br>V<br>µA<br>mA<br>°C<br><br>V<br>V | A |
| 15.2 | DATA_CLK output<br>- Saturation voltage Low<br>- Saturation voltage High | IDATA_CLK = 1mA<br>IDATA_CLK = –1mA | $V_{ol}$<br>$V_{oh}$ | $V_S$ – 0.4V | 0.1<br>$V_S$ – 0.15V | 0.4 | V<br>V | A |
| 15.3 | IC_ACTIVE output<br>- Saturation voltage Low<br>- Saturation voltage High | IIC_ACTIVE = 1mA<br>IIC_ACTIVE = –1mA | $V_{ol}$<br>$V_{oh}$ | $V_S$ – 0.4 V | 0.1<br>$V_S$ – 0.15V | 0.4 | V<br>V | A |
| 15.4 | POLLING/_ON input<br>- Low level input voltage<br>- High level input voltage | Receiving mode<br>Polling mode | $V_{Il}$<br>$V_{Ih}$ | <br>$0.8 \times V_S$ | | $0.2 \times V_S$ | V<br>V | A |
| 15.5 | MODE pin<br>- High level input voltage | Test input must always be set to High | $V_{Ih}$ | $0.8 \times V_S$ | | | V | A |
| 15.6 | TEST 1 pin<br>- Low level input voltage | Test input must always be set to Low | $V_{Il}$ | | | $0.2 \times V_S$ | V | A |

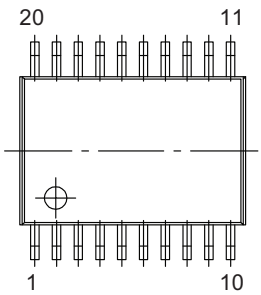
*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

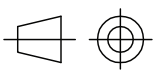
## 20. Ordering Information

| Extended Type Number | Package | Remarks |
|---|---|---|
| ATA8203P3C-TKQW | SSO20 | 315MHz version, MOQ 4000 |
| ATA8204P3C-TKQW | SSO20 | 433MHz version, MOQ 4000 |
| ATA8205P6C-TKQW | SSO20 | 868MHz version, MOQ 4000 |

## 21. Package Information



technical drawings according to DIN specifications

Dimensions in mm

| COMMON DIMENSIONS (Unit of Measure = mm) | | | | |
|---|---|---|---|---|
| **Symbol** | **MIN** | **NOM** | **MAX** | **NOTE** |
| A | 0.9 | 1.0 | 1.1 | |
| A1 | 0.05 | 0.1 | 0.15 | |
| A2 | 0.85 | 0.9 | 0.95 | |
| D | 6.4 | 6.5 | 6.6 | |
| E | 6.3 | 6.4 | 6.5 | |
| E1 | 4.3 | 4.4 | 4.5 | |
| L | 0.5 | 0.6 | 0.7 | |
| C | 0.1 | 0.15 | 0.2 | |
| b | 0.2 | 0.25 | 0.3 | |
| e | | 0.65 BSC | | |

04/16/14

| | TITLE | GPC | DRAWING NO. | REV. |
|---|---|---|---|---|
| Atmel **Package Drawing Contact:** packagedrawings@atmel.com | **Package: SSO20** 4.4mm | | 6.543-5182.01-4 | 1 |

# 22. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

| Revision No. | History |
|---|---|
| 9121D-INDCO-09/14 | • Section 20 “Ordering Information” on page 44 updated<br>• Section 21 “Package Information” on page 44 updated |
| 9121C-INDCO-12/12 | • Section 20 “Ordering Information” on page 43 changed |
| 9121B-INDCO-04/09 | • Figure 1-1 “System Block Diagram” on page 2 changed |

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