HEX INVERTERS WITH OPEN DRAIN OUTPUTS

Description

The 74LVC06A provides six independent open-drain inverter buffers. The device is designed for operation with a power supply range of 1.65V to 5.5V. The inputs are tolerant to 5.5V allowing this device to be used in a mixed voltage environment. The device is fully specified for partial power down applications using IOFF. The IOFF circuitry disables the output preventing damaging current backflow when the device is powered down. The outputs can be connected to implement active-low wired-OR or active-high wired-AND functions.

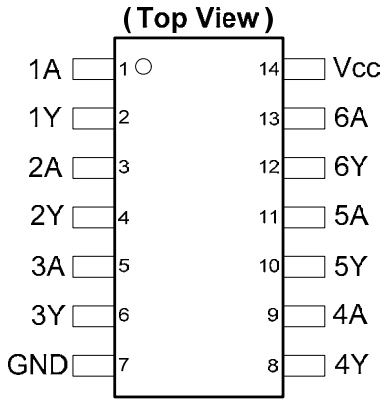
The gates perform the positive Boolean function:

$Y = \overline{A}$

Features

- Wide Supply Voltage Range from 1.65V to 5.5V
- Sinks 24mA at V_{CC} = 3.3V
- CMOS Low Power Consumption
- IOFF Supports Partial-Power-Down Mode Operation
- Inputs or Outputs Accept Up to 5.5V
- Inputs Can be Driven by 3.3V or 5.5V Allowing for Voltage Translation Applications.
- ESD Protection Exceeds JESD 22
  - 200-V Machine Model (A115-A)
  - 2000-V Human Body Model (A114-A)
  - Exceeds 1000-V Charged Device Model (C101C)
- Latch-Up Exceeds 250mA per JESD 78, Class II
- Range of Package Options SO-14 and TSSOP-14
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

Pin Assignments



SO-14 / TSSOP-14

Applications

- Voltage Level Shifting
- General Purpose Logic
- Power Down Signal Isolation
- Wide array of products such as:
  - PCs, networking, notebooks, ultrabooks, netbooks
  - Computer peripherals, hard drives, CD/DVD ROM
  - TV, DVD, DVR, set top box

Notes: 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

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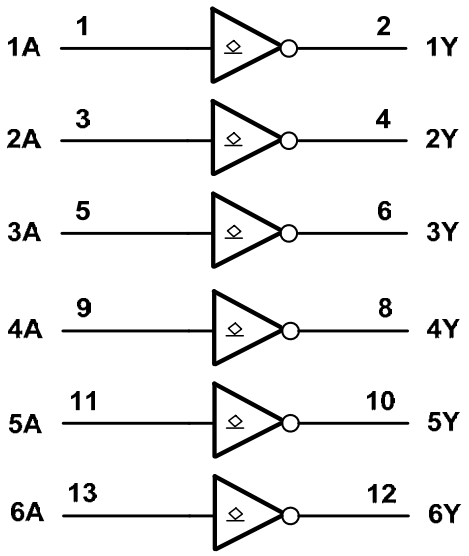
Pin Descriptions

Pin Number	Pin Name	Description
1	1A	Data Input
2	1Y	Data Output
3	2A	Data Input
4	2Y	Data Output
5	3A	Data Input
6	3Y	Data Output
7	GND	Ground
8	4Y	Data Output
9	4A	Data Input
10	5Y	Data Output
11	5A	Data Input
12	6Y	Data Output
13	6A	Data Input
14	V_{CC}	Supply Voltage

Logic Diagram



Function Table

Inputs	Outputs
A	**Y**
H	L
L	Z

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Absolute Maximum Ratings (Note 4) (@T_A = +25°C, unless otherwise specified.)

Symbol	Description	Rating	Unit
ESD HBM	Human Body Model ESD Protection	2	KV
ESD CDM	Charged Device Model ESD Protection	1	KV
ESD MM	Machine Model ESD Protection	200	V
V_{CC}	Supply Voltage Range	-0.5 to +6.5	V
V_I	Input Voltage Range	-0.5 to +6.5	V
V_O	Voltage applied to output in high impedance or I_{OFF} state	-0.5 to +6.5	V
V_O	Voltage applied to output in high or low state	-0.3 to V_{CC} +0.5	V
I_{IK}	Input Clamp Current $V_I < 0$	-50	mA
I_{OK}	Output Clamp Current $V_O < 0$	-50	mA
I_O	Continuous Output Current	50	mA
	Continuous current through Vdd or GND	±100	mA
T_J	Operating Junction Temperature	-40 to +150	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_{TOT}	Total Power Dissipation	500	mW

Note: 4. Stresses beyond the absolute maximum may result in immediate failure or reduced reliability. These are stress values and device operation should be within recommend values.

Recommended Operating Conditions (Note 5) (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage		1.65	5.5	V
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	Active Mode	0	V_{CC}	V
		V_{CC} = 0V; Power Down Mode	0	5.5	V
Δt/ΔV	Input transition rise or fall rate	V_{CC} = 1.65V to 2.7V		20	ns/V
		V_{CC} = 2.7V to 5.5V		10	
T_A	Operating free-air temperature		-40	+125	°C

Notes: 5. Unused inputs should be held at V_{CC} or Ground.

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Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Test Conditions	V_{CC}	T_A = -40°C to +85°C		T_A = -40°C to +125°C		Unit
				Min	Max	Min	Max	
V_{IH}	High-level Input Voltage		1.65V to 1.95V	0.65 X V_{CC}		0.65 X V_{CC}		V
			2.3V to 2.7V	1.7		1.6		
			2.7V to 3.6V	2.0		2.0		
			4.5V to 5.5V	0.7 X V_{CC}		2.0		
V_{IL}	Low-level input voltage		1.65V to 1.95V		0.35 X V_{CC}		0.35 X V_{CC}	V
			2.3V to 2.7V		0.7		0.7	
			2.7V to 3.6V		0.8		0.8	
			4.5V to 5.5V		0.3 X V_{CC}		0.3 X V_{CC}	
V_{OL}	Low-level Output Voltage	I_{OL} = 100μA	1.65V to 5.5V		0.2		0.3	V
		I_{OL} = 4mA	1.65V		0.45		0.6	
		I_{OL} = 8mA	2.3V		0.70		0.85	
		I_{OL} = 12mA	2.7V		0.40		0.6	
			3.0V		0.55		0.6	
		I_{OL} = 24mA	3.0V		0.55		0.6	
		I_{OL}= 32mA	4.5V		0.55		0.6	
I_{OZ}	Z State Leakage Current	V_O = GND or 5.5V	3.6V		±10		±20	μA
I_I	Input Current	V_I =GND to 5.5V	3.6V		± 5		± 20	μA
I_{OFF}	Power Down Leakage Current	V_I or V_O = 0V to 3.6V	0		10		20	μA
I_{CC}	Supply Current	V_I = GND or V_{CC} I_O=0	3.6V		10		40	μA

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Switching Characteristics

Symbol	Parameter	Test Conditions	V_{CC}	T_A = +25°C			-40°C to +85°C		-40°C to +125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
t_{PLZ} /t_{PZL}	Propagation Delay A_N to Y_N	Figure 1	1.65V to1.95V	0.3	2.9	5.3	0.3	5.6	0.3	7.6	ns
			2.3V to 2.7V	0.3	2.6	4.1	0.3	4.7	0.3	5.5	
			2.7V	0.3	2.5	4.0	0.3	4.5	0.3	5.0	
			3V to 3.6V	0.3	2.3	3.5	0.3	3.7	0.3	5.0	
			4.5V to 5.5V	0.3	1.7	2.5	0.3	3.4	0.3	4.5	

Operating Characteristics (@T_A = +25°C, unless otherwise specified.)

Parameter		Test Conditions	V_{CC} = 1.8V	V_{CC} = 2.5V	V_{CC} = 3.3V	V_{CC} = 5V	Unit
			Typ	Typ	Typ	Typ	
C_{pd}	Power dissipation capacitance per gate	f = 10 MHz	7.0	7.5	8.0	8.6	pF
C_I	Input Capacitance	V_I = V_{CC} – or GND	4	4	4	4	pF

Package Characteristics

Symbol	Parameter	Test Conditions	V_{CC}	Min	Typ	Max	Unit
θ_{JA}	Thermal Resistance Junction-to-Ambient	SO-14	(Note 6)		TBD		°C/W
		TSSOP-14			159		
θ_{JC}	Thermal Resistance Junction-to-Case	SO-14	(Note 6)		TBD		°C/W
		TSSOP-14			25		

Note: 6. Test condition for SO-14 and TSSOP-14: Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.

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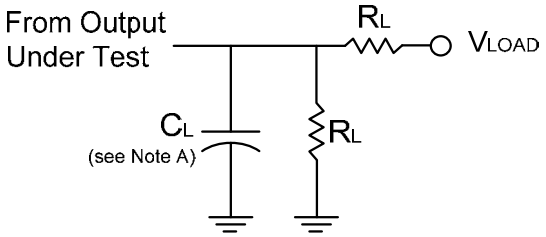
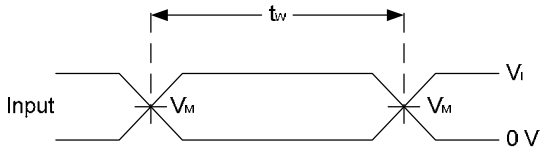
Parameter Measuement Information

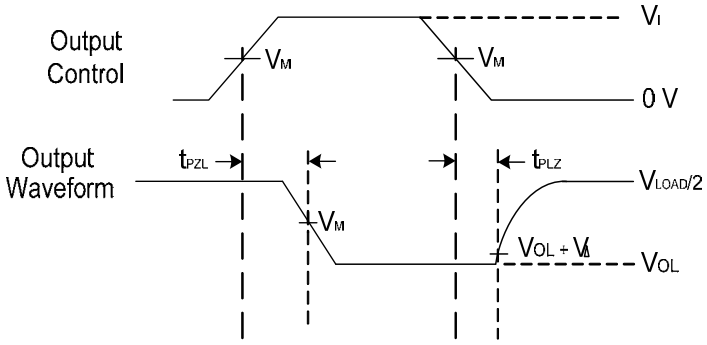


TEST	Condition
t_{PLZ} (see Note E)	V_{LOAD}
t_{PZL}(see Note D)	V_{LOAD}

V_{CC}	Inputs		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8V±0.15V	V_{CC}	≤2ns	$V_{CC}/2$	2 X V_{CC}	30pF	1KΩ	0.15V
2.5V±0.2V	V_{CC}	≤2ns	$V_{CC}/2$	2 X V_{CC}	30pF	500Ω	0.15V
2.7V	2.7V	≤2ns	1.5V	6V	50pF	500Ω	0.3V
3.3V±0.3V	3V	≤2.5ns	1.5V	6V	50pF	500Ω	0.3V
5V±0.5V	V_{CC}	≤2.5ns	$V_{CC}/2$	2 X V_{CC}	50pF	500Ω	0.3V



Voltage Waveform
Pulse Duration



Voltage Waveform
Propagation Delay Times

Notes: A. Includes test lead and test apparatus capacitance.
B. All pulses are supplied at pulse repetition rate ≤ 10 MHz.
C. The inputs are measured one at a time with one transition per measurement.
D. t_{PZL} is measured at V_M.
E. t_{PLZ} is measured at V_{OL} +V_Δ.

Figure 1. Load Circuit and Voltage Waveforms

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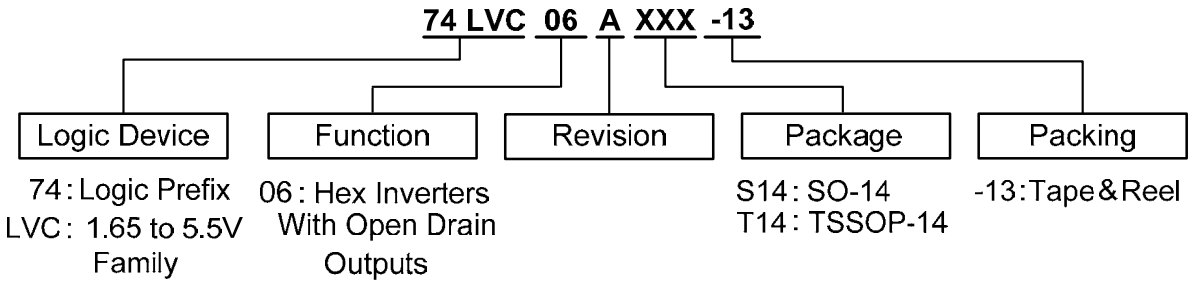
Ordering Information

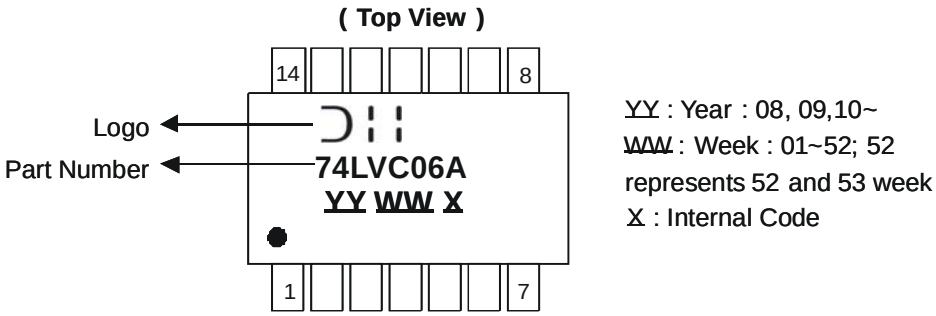


Device	Package Code	Packaging (Note 7)	13" Tape and Reel	
			Quantity	Part Number Suffix
74LVC06AS14-13	S14	SO-14	2500/Tape & Reel	-13
74LVC06AT14-13	T14	TSSOP-14	2500/Tape & Reel	-13

Notes: 7. The taping orientation and tape details can be found at http://www.diodes.com/datasheets/ap02007.pdf

Marking Information

(1) SO-14, TSSOP-14



Part Number	Package
74LVC06AS14	SO-14
74LVC06AT14	TSSOP-14

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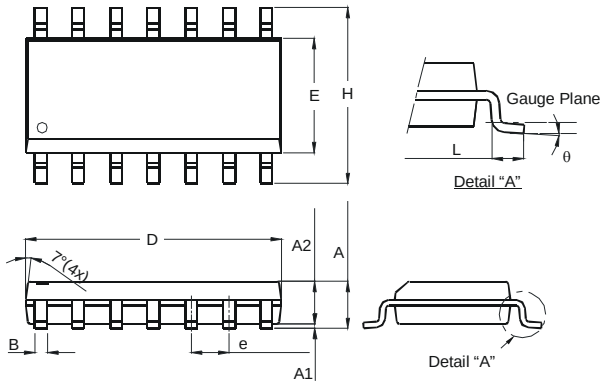
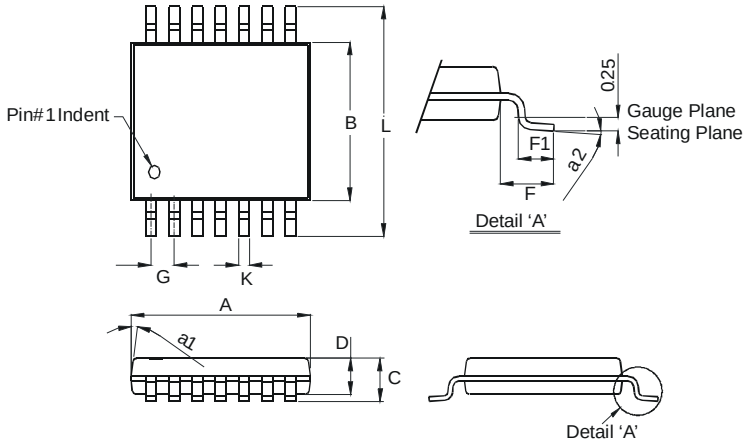
Package Outline Dimensions (All dimensions in mm.)

Package Type: SO-14



SO-14		
Dim	**Min**	**Max**
A	1.47	1.73
A1	0.10	0.25
A2	1.45 Typ	
B	0.33	0.51
D	8.53	8.74
E	3.80	3.99
e	1.27 Typ	
H	5.80	6.20
L	0.38	1.27
θ	0°	8°
All Dimensions in mm		

Package Type: TSSOP-14



TSSOP-14		
Dim	**Min**	**Max**
a1	7° (4X)	
a2	0°	8°
A	4.9	5.10
B	4.30	4.50
C	—	1.2
D	0.8	1.05
F	1.00 Typ	
F1	0.45	0.75
G	0.65 Typ	
K	0.19	0.30
L	6.40 Typ	
All Dimensions in mm		

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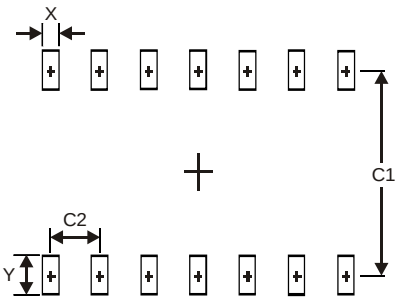
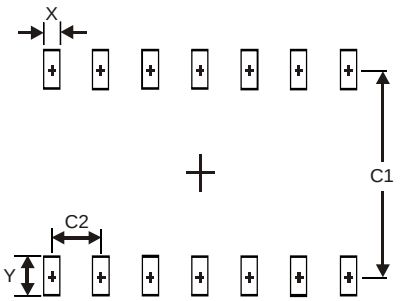
Suggested Pad Layout

Package Type: SO-14



Dimensions	Value (in mm)
X	0.60
Y	1.50
C1	5.4
C2	1.27

Package Type: TSSOP-14



Dimensions	Value (in mm)
X	0.45
Y	1.45
C1	5.9
C2	0.65

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