



HIGH-SPEED 3.3V 64K x 18 SYNCHRONOUS PIPELINED DUAL-PORT STATIC RAM WITH 3.3V OR 2.5V INTERFACE

IDT70V3389S

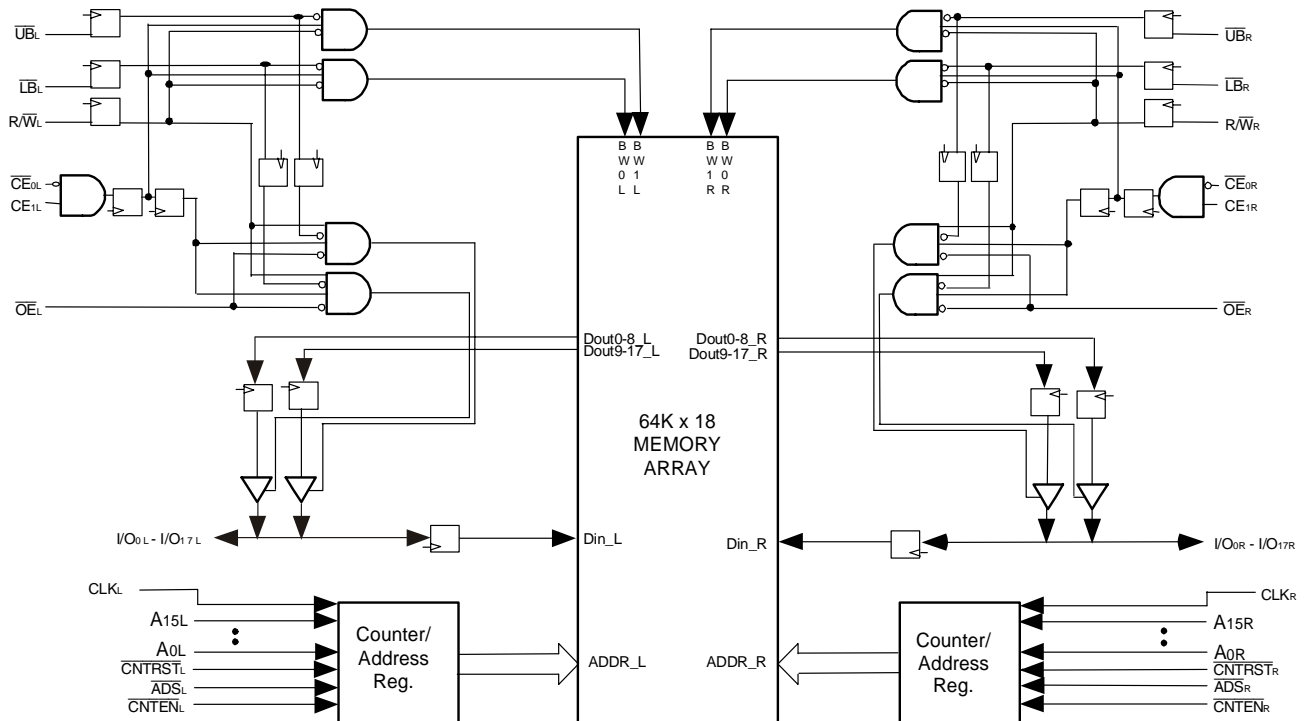
LEAD FINISH (SnPb) ARE IN EOL PROCESS - LAST TIME BUY EXPIRES JUNE 15, 2018

Features

- ◆ True Dual-Port memory cells which allow simultaneous access of the same memory location
- ◆ High-speed clock to data access
 - Commercial: 4.2/5/6ns (max.)
 - Industrial: 5ns (max)
- ◆ Pipelined output mode
- ◆ Counter enable and reset features
- ◆ Dual chip enables allow for depth expansion without additional logic
- ◆ Full synchronous operation on both ports
 - 7.5ns cycle time, 133MHz operation (9.6 Gbps bandwidth)
 - Fast 4.2ns clock to data out
 - 1.8ns setup to clock and 0.7ns hold on all control, data, and address inputs @ 133MHz

- Data input, address, byte enable and control registers
- Self-timed write allows fast cycle time
- ◆ Separate byte controls for multiplexed bus and bus matching compatibility
- ◆ LVTTTL-compatible, single 3.3V ($\pm 150\text{mV}$) power supply for core
- ◆ LVTTTL-compatible, selectable 3.3V ($\pm 150\text{mV}$)/2.5V ($\pm 125\text{mV}$) power supply for I/Os and control signals on each port
- ◆ Industrial temperature range (-40°C to $+85^{\circ}\text{C}$) is available for selected speeds
- ◆ Available in a 128-pin Thin Quad Plastic Flatpack (TQFP), 208-pin fine pitch Ball Grid Array, and 256-pin Ball Grid Array
- ◆ Green parts available, see ordering information

Functional Block Diagram



4832 tbl 01

FEBRUARY 2018

Description:

The IDT70V3389 is a high-speed 64K x 18 bit synchronous Dual-Port RAM. The memory array utilizes Dual-Port memory cells to allow simultaneous access of any address from both ports. Registers on control, data, and address inputs provide minimal setup and hold times. The timing latitude provided by this approach allows systems to be designed with very short cycle times. With an input data register, the IDT70V3389 has been optimized for applications having unidirectional or bidirectional data flow

in bursts. An automatic power down feature, controlled by \overline{CE}_0 and CE_1 , permits the on-chip circuitry of each port to enter a very low standby power mode.

The 70V3389 can support an operating voltage of either 3.3V or 2.5V on one or both ports, controllable by the OPT pins. The power supply for the core of the device (VDD) remains at 3.3V.

Pin Configuration^(1,2,3,4)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
12/12/01	I/O _{9L}	NC	V _{SS}	NC	NC	NC	A _{12L}	A _{8L}	NC	V _{DD}	CLK _L	\overline{CNTEN}_L	A _{4L}	A _{0L}	OPT _L	NC	V _{SS}	A
	NC	V _{SS}	NC	V _{SS}	NC	A _{13L}	A _{9L}	NC	\overline{CE}_{0L}	V _{SS}	\overline{ADS}_L	A _{5L}	A _{1L}	V _{SS}	V _{DDQR}	I/O _{8L}	NC	B
	V _{DDQL}	I/O _{9R}	V _{DDQR}	V _{DD}	NC	A _{14L}	A _{10L}	\overline{UB}_L	CE _{1L}	V _{SS}	R \overline{W}_L	A _{6L}	A _{2L}	V _{DD}	I/O _{8R}	NC	V _{SS}	C
	NC	V _{SS}	I/O _{10L}	NC	A _{15L}	A _{11L}	A _{7L}	\overline{LB}_L	V _{DD}	\overline{OE}_L	\overline{CNTRST}_L	A _{3L}	V _{DD}	NC	V _{DDQL}	I/O _{7L}	I/O _{7R}	D
	I/O _{11L}	NC	V _{DDQR}	I/O _{10R}	<p style="text-align: center;">70V3389BF BF-208⁽⁵⁾ 208-Pin fpBGA Top View⁽⁶⁾</p>								I/O _{6L}	NC	V _{SS}	NC	E	
	V _{DDQL}	I/O _{11R}	NC	V _{SS}									V _{SS}	I/O _{6R}	NC	V _{DDQR}	F	
	NC	V _{SS}	I/O _{12L}	NC									NC	V _{DDQL}	I/O _{5L}	NC	G	
	V _{DD}	NC	V _{DDQR}	I/O _{12R}									V _{DD}	NC	V _{SS}	I/O _{5R}	H	
	V _{DDQL}	V _{DD}	V _{SS}	V _{SS}									V _{SS}	V _{DD}	V _{SS}	V _{DDQR}	J	
	I/O _{14R}	V _{SS}	I/O _{13R}	V _{SS}									I/O _{3R}	V _{DDQL}	I/O _{4R}	V _{SS}	K	
	NC	I/O _{14L}	V _{DDQR}	I/O _{13L}									NC	I/O _{3L}	V _{SS}	I/O _{4L}	L	
	V _{DDQL}	NC	I/O _{15R}	V _{SS}									V _{SS}	NC	I/O _{2R}	V _{DDQR}	M	
	NC	V _{SS}	NC	I/O _{15L}									I/O _{1R}	V _{DDQL}	NC	I/O _{2L}	N	
	I/O _{16R}	I/O _{16L}	V _{DDQR}	NC									NC	NC	A _{12R}	A _{8R}	NC	V _{DD}
	V _{SS}	NC	I/O _{17R}	NC	NC	A _{13R}	A _{9R}	NC	\overline{CE}_{0R}	V _{SS}	\overline{ADS}_R	A _{5R}	A _{1R}	V _{SS}	V _{DDQL}	I/O _{0R}	V _{DDQR}	R
	NC	I/O _{17L}	V _{DDQL}	V _{SS}	NC	A _{14R}	A _{10R}	\overline{UB}_R	CE _{1R}	V _{SS}	R \overline{W}_R	A _{6R}	A _{2R}	V _{SS}	NC	V _{SS}	NC	T
	V _{SS}	NC	V _{DD}	NC	A _{15R}	A _{11R}	A _{7R}	\overline{LB}_R	V _{DD}	\overline{OE}_R	\overline{CNTRST}_R	A _{3R}	A _{0R}	V _{DD}	OPT _R	NC	I/O _{0L}	U

4832 tbl 02

NOTES:

1. All V_{DD} pins must be connected to 3.3V power supply.
2. All V_{DDQ} pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to V_{IH} (3.3V), and 2.5V if OPT pin for that port is set to V_{IL} (0V).
3. All V_{SS} pins must be connected to ground supply.
4. Package body is approximately 15mm x 15mm x 1.4mm with 0.8mm ball pitch.
5. This package code is used to reference the package diagram.
6. This text does not indicate orientation of the actual part-marking.

Pin Configuration^(1,2,3,4) (con't.)

70V3389BC
BC-256⁽⁵⁾

256-Pin BGA
Top View⁽⁶⁾

12/12/01

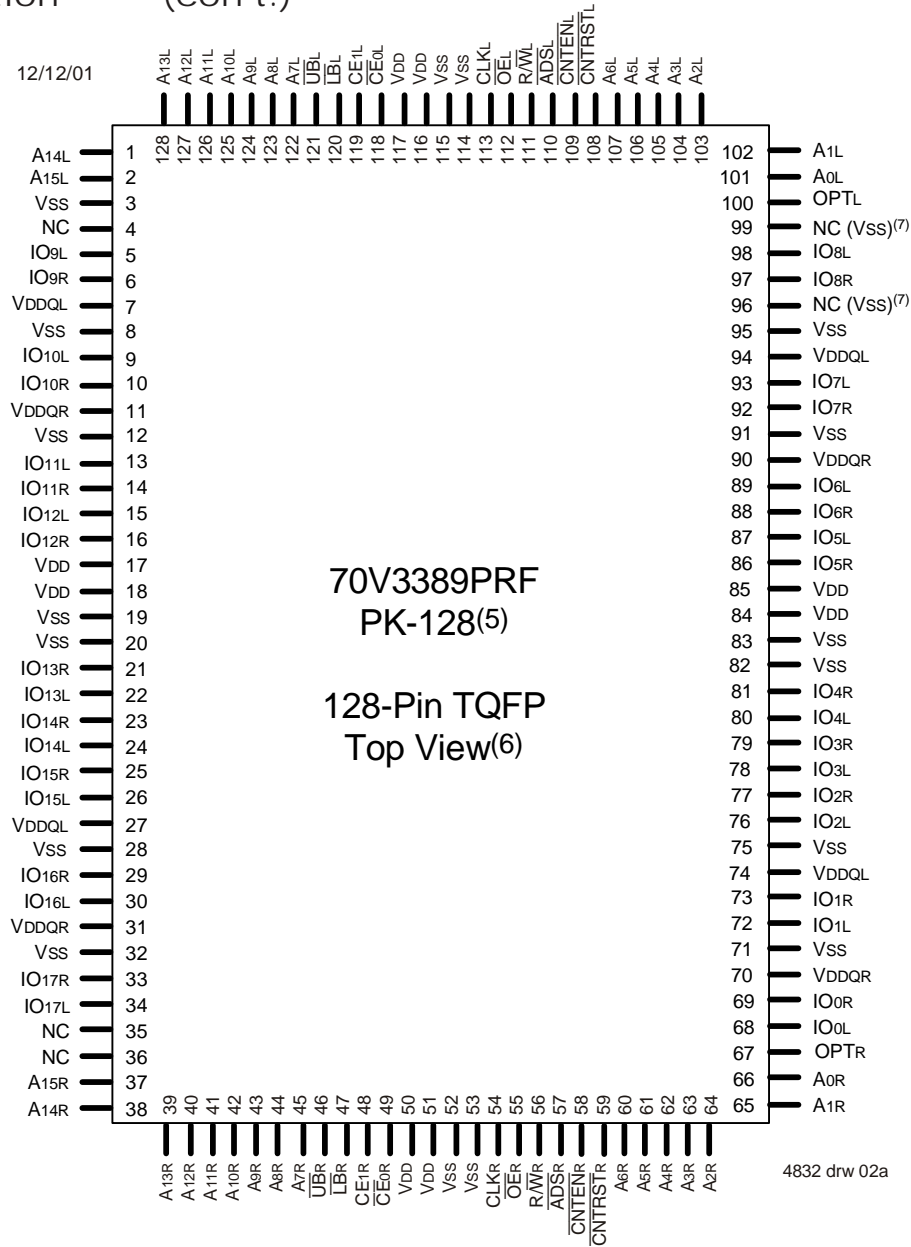
A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16
NC	NC	NC	NC	A14L	A11L	A8L	NC	CE1L	$\overline{OE}L$	CNTENL	A5L	A2L	A0L	NC	NC
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13	B14	B15	B16
NC	NC	NC	NC	A15L	A12L	A9L	$\overline{UB}L$	$\overline{CE}0L$	R/WL	$\overline{CNTR}STL$	A4L	A1L	VDD	NC	NC
C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	C11	C12	C13	C14	C15	C16
NC	I/O9L	VSS	NC	A13L	A10L	A7L	NC	$\overline{LB}L$	CLKL	ADSL	A6L	A3L	OPTL	NC	I/O8L
D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16
NC	I/O9R	NC	VDD	VDDQL	VDDQL	VDDQR	VDDQR	VDDQL	VDDQL	VDDQR	VDDQR	VDD	NC	NC	I/O8R
E1	E2	E3	E4	E5	E6	E7	E8	E9	E10	E11	E12	E13	E14	E15	E16
I/O10R	I/O10L	NC	VDDQL	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VDD	VDD	VDDQR	NC	I/O7L
I/O7R															
F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15	F16
I/O11L	NC	I/O11R	VDDQL	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD	VDDQR	I/O6R	NC
I/O6L															
G1	G2	G3	G4	G5	G6	G7	G8	G9	G10	G11	G12	G13	G14	G15	G16
NC	NC	I/O12L	VDDQR	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDQL	I/O5L	NC
I/O5R															
H1	H2	H3	H4	H5	H6	H7	H8	H9	H10	H11	H12	H13	H14	H15	H16
NC	I/O12R	NC	VDDQR	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDQL	NC	NC
I/O5R															
J1	J2	J3	J4	J5	J6	J7	J8	J9	J10	J11	J12	J13	J14	J15	J16
I/O13L	I/O14R	I/O13R	VDDQL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDQR	I/O4R	I/O3R
I/O4L															
K1	K2	K3	K4	K5	K6	K7	K8	K9	K10	K11	K12	K13	K14	K15	K16
NC	NC	I/O14L	VDDQL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDQR	NC	NC
I/O3L															
L1	L2	L3	L4	L5	L6	L7	L8	L9	L10	L11	L12	L13	L14	L15	L16
I/O15L	NC	I/O15R	VDDQR	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD	VDDQL	I/O2L	NC
I/O2R															
M1	M2	M3	M4	M5	M6	M7	M8	M9	M10	M11	M12	M13	M14	M15	M16
I/O16R	I/O16L	NC	VDDQR	VDD	VDD	VSS	VSS	VSS	VSS	VDD	VDD	VDDQL	I/O1R	I/O1L	NC
I/O1L															
N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11	N12	N13	N14	N15	N16
NC	I/O17R	NC	VDD	VDDQR	VDDQR	VDDQL	VDDQL	VDDQR	VDDQR	VDDQL	VDDQL	VDD	NC	I/O0R	NC
I/O0L															
P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12	P13	P14	P15	P16
NC	I/O17L	NC	NC	A13R	A10R	A7R	NC	$\overline{LB}R$	CLKR	ADSR	A6R	A3R	NC	NC	I/O0L
I/O0L															
R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	R15	R16
NC	NC	NC	NC	A15R	A12R	A9R	$\overline{UB}R$	$\overline{CE}0R$	R/WR	$\overline{CNTR}STR$	A4R	A1R	OPTR	NC	NC
NC															
T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	T16
NC	NC	NC	NC	A14R	A11R	A8R	NC	CE1R	$\overline{OE}R$	CNTENR	A5R	A2R	A0R	NC	NC

4832 drw 02c

NOTES:

1. All VDD pins must be connected to 3.3V power supply.
2. All VDDQ pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to VIH (3.3V), and 2.5V if OPT pin for that port is set to VIL (0V).
3. All VSS pins must be connected to ground supply.
4. Package body is approximately 17mm x 17mm x 1.4mm, with 1.0mm ball-pitch.
5. This package code is used to reference the package diagram.
6. This text does not indicate orientation of the actual part-marking.

Pin Configuration^(1,2,3,4) (con't.)



NOTES:

1. All VDD pins must be connected to 3.3V power supply.
2. All VDDQ pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to VIH (3.3V), and 2.5V if OPT pin for that port is set to VIL (0V).
3. All VSS pins must be connected to ground supply.
4. Package body is approximately 14mm x 20mm x 1.4mm.
5. This package code is used to reference the package diagram.
6. This text does not indicate orientation of the actual part-marking.
7. In the 70V3379 (32K x 18) and 70V3389 (64K x 18), pins 96 and 99 are NC. The upgrade devices 70V3399 (128K x 18) and 70V3319 (256K x 18) assign these pins as VSS. Customers who plan to take advantage of the upgrade path should treat these pins as VSS on the 70V3379 and 70V3389. If no upgrade is needed, the pins can be treated as NC.

Pin Names

Left Port	Right Port	Names
\overline{CE}_{0L} , CE _{1L}	\overline{CE}_{0R} , CE _{1R}	Chip Enables
R/ \overline{WL}	R/ \overline{WR}	Read/Write Enable
\overline{OE}_L	\overline{OE}_R	Output Enable
A _{0L} - A _{15L}	A _{0R} - A _{15R}	Address
I/O _{0L} - I/O _{17L}	I/O _{0R} - I/O _{17R}	Data Input/Output
CLK _L	CLK _R	Clock
\overline{ADS}_L	\overline{ADS}_R	Address Strobe Enable
\overline{CNTEN}_L	\overline{CNTEN}_R	Counter Enable
\overline{CNTRST}_L	\overline{CNTRST}_R	Counter Reset
UB _L - LB _L	UB _R - LB _R	Byte Enables (9-bit bytes)
V _{DD0L}	V _{DD0R}	Power (I/O Bus) (3.3V or 2.5V) ⁽¹⁾
OPT _L	OPT _R	Option for selecting V _{DD0X} ^(1,2)
V _{DD}		Power (3.3V) ⁽¹⁾
V _{SS}		Ground (0V)

4832 tbl 01

NOTES:

- V_{DD}, OPT_X, and V_{DD0X} must be set to appropriate operating levels prior to applying inputs on the I/Os and controls for that port.
- OPT_X selects the operating voltage levels for the I/Os and controls on that port. If OPT_X is set to VIH (3.3V), then that port's I/Os and controls will operate at 3.3V levels and V_{DD0X} must be supplied at 3.3V. If OPT_X is set to VIL (0V), then that port's I/Os and controls will operate at 2.5V levels and V_{DD0X} must be supplied at 2.5V. The OPT pins are independent of one another—both ports can operate at 3.3V levels, both can operate at 2.5V levels, or either can operate at 3.3V with the other at 2.5V.

Truth Table I—Read/Write and Enable Control^(1,2,3)

\overline{OE}	CLK	\overline{CE}_0	CE ₁	\overline{UB}	\overline{LB}	R/ \overline{W}	Upper Byte I/O ₉₋₁₈	Lower Byte I/O ₀₋₈	MODE
X	↑	L	H	H	H	X	High-Z	High-Z	All Bytes Deselected
X	↑	L	H	H	L	L	High-Z	D _{IN}	Write to Lower Byte Only
X	↑	L	H	L	H	L	D _{IN}	High-Z	Write to Upper Byte Only
X	↑	L	H	L	L	L	D _{IN}	D _{IN}	Write to Both Bytes
L	↑	L	H	H	L	H	High-Z	D _{OUT}	Read Lower Byte Only
L	↑	L	H	L	H	H	D _{OUT}	High-Z	Read Upper Byte Only
L	↑	L	H	L	L	H	D _{OUT}	D _{OUT}	Read Both Bytes
H	↑	L	H	L	L	X	High-Z	High-Z	Outputs Disabled

NOTES:

- "H" = VIH, "L" = VIL, "X" = Don't Care.
- \overline{ADS} , \overline{CNTEN} , \overline{CNTRST} = X.
- \overline{OE} is an asynchronous input signal.

4832 tbl 02

Truth Table II—Address Counter Control^(1,2)

Address	Previous Address	Addr Used	CLK	$\overline{\text{ADS}}$	$\overline{\text{CNTEN}}$	$\overline{\text{CNRST}}$	I/O ⁽³⁾	MODE
X	X	0	↑	X	X	L ⁽⁴⁾	D _{IO} (0)	Counter Reset to Address 0
An	X	An	↑	L ⁽⁴⁾	X	H	D _{IO} (n)	External Address Used
An	Ap	Ap	↑	H	H	H	D _{IO} (p)	External Address Blocked—Counter disabled (Ap reused)
X	Ap	Ap + 1	↑	H	L ⁽⁵⁾	H	D _{IO} (p+1)	Counter Enabled—Internal Address generation

4832 tbl 03

NOTES:

- "H" = V_{IH}, "L" = V_{IL}, "X" = Don't Care.
- Read and write operations are controlled by the appropriate setting of $\overline{\text{R}\overline{\text{W}}}$, $\overline{\text{CE}}_0$, CE₁, $\overline{\text{B}}\overline{\text{E}}_n$ and $\overline{\text{OE}}$.
- Outputs are in Pipelined mode: the data out will be delayed by one cycle.
- $\overline{\text{ADS}}$ and $\overline{\text{CNRST}}$ are independent of all other memory control signals including $\overline{\text{CE}}_0$, CE₁ and $\overline{\text{B}}\overline{\text{E}}_n$
- The address counter advances if $\overline{\text{CNTEN}} = \text{V}_{\text{IL}}$ on the rising edge of CLK, regardless of all other memory control signals including $\overline{\text{CE}}_0$, CE₁, $\overline{\text{B}}\overline{\text{E}}_n$.

Recommended Operating Temperature and Supply Voltage⁽¹⁾

Grade	Ambient Temperature	GND	V _{DD}
Commercial	0°C to +70°C	0V	3.3V ± 150mV
Industrial	-40°C to +85°C	0V	3.3V ± 150mV

4832 tbl 04

NOTES:

- Industrial temperature: for specific speeds, packages and powers contact your sales office.

Recommended DC Operating Conditions with V_{DDQ} at 2.5V

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{DD}	Core Supply Voltage	3.15	3.3	3.45	V
V _{DDQ}	I/O Supply Voltage ⁽³⁾	2.375	2.5	2.625	V
V _{SS}	Ground	0	0	0	V
V _{IH}	Input High Voltage ⁽³⁾ (Address & Control Inputs)	1.7	—	V _{DDQ} + 125mV ⁽²⁾	V
V _{IH}	Input High Voltage - I/O ⁽³⁾	1.7	—	V _{DDQ} + 125mV ⁽²⁾	V
V _{IL}	Input Low Voltage	-0.3 ⁽¹⁾	—	0.7	V

4832 tbl 05a

NOTES:

- V_{IL} ≥ -1.5V for pulse width less than 10 ns.
- V_{TERM} must not exceed V_{DDQ} + 125mV.
- To select operation at 2.5V levels on the I/Os and controls of a given port, the OPT pin for that port must be set to V_{IL} (0V), and V_{DDQX} for that port must be supplied as indicated above.

Absolute Maximum Ratings⁽¹⁾

Symbol	Rating	Commercial & Industrial	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
T _{BIAS}	Temperature Under Bias	-55 to +125	°C
T _{STG}	Storage Temperature	-65 to +150	°C
I _{OUT}	DC Output Current	50	mA

4832 tbl 06

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{TERM} must not exceed V_{DD} + 150mV for more than 25% of the cycle time or 4ns maximum, and is limited to ≤ 20mA for the period of V_{TERM} ≥ V_{DD} + 150mV.

Recommended DC Operating Conditions with V_{DDQ} at 3.3V

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{DD}	Core Supply Voltage	3.15	3.3	3.45	V
V _{DDQ}	I/O Supply Voltage ⁽³⁾	3.15	3.3	3.45	V
V _{SS}	Ground	0	0	0	V
V _{IH}	Input High Voltage (Address & Control Inputs) ⁽³⁾	2.0	—	V _{DDQ} + 150mV ⁽²⁾	V
V _{IH}	Input High Voltage - I/O ⁽³⁾	2.0	—	V _{DDQ} + 150mV ⁽²⁾	V
V _{IL}	Input Low Voltage	-0.3 ⁽¹⁾	—	0.8	V

4832 tbl 05b

NOTES:

- V_{IL} ≥ -1.5V for pulse width less than 10 ns.
- V_{TERM} must not exceed V_{DDQ} + 150mV.
- To select operation at 3.3V levels on the I/Os and controls of a given port, the OPT pin for that port must be set to V_{IH} (3.3V), and V_{DDQX} for that port must be supplied as indicated above.

Capacitance⁽¹⁾

($T_A = +25^\circ\text{C}$, $F = 1.0\text{MHz}$) TQFP ONLY

Symbol	Parameter	Conditions ⁽²⁾	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 3\text{dV}$	8	pF
$C_{OUT}^{(3)}$	Output Capacitance	$V_{OUT} = 3\text{dV}$	10.5	pF

4832 tbl 07

NOTES:

- These parameters are determined by device characterization, but are not production tested.
- 3dV references the interpolated capacitance when the input and output switch from 0V to 3V or from 3V to 0V.
- C_{OUT} also references C_{IO} .

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range ($V_{DD} = 3.3\text{V} \pm 150\text{mV}$)

Symbol	Parameter	Test Conditions	70V3389S		Unit
			Min.	Max.	
$ I_{LI} $	Input Leakage Current ⁽¹⁾	$V_{DDQ} = \text{Max.}, V_{IN} = 0\text{V to } V_{DDQ}$	—	10	μA
$ I_{LO} $	Output Leakage Current	$\overline{CE}_0 = V_{IH}$ or $CE_1 = V_{IL}, V_{OUT} = 0\text{V to } V_{DDQ}$	—	10	μA
$V_{OL} (3.3\text{V})$	Output Low Voltage ⁽²⁾	$I_{OL} = +4\text{mA}, V_{DDQ} = \text{Min.}$	—	0.4	V
$V_{OH} (3.3\text{V})$	Output High Voltage ⁽²⁾	$I_{OH} = -4\text{mA}, V_{DDQ} = \text{Min.}$	2.4	—	V
$V_{OL} (2.5\text{V})$	Output Low Voltage ⁽²⁾	$I_{OL} = +2\text{mA}, V_{DDQ} = \text{Min.}$	—	0.4	V
$V_{OH} (2.5\text{V})$	Output High Voltage ⁽²⁾	$I_{OH} = -2\text{mA}, V_{DDQ} = \text{Min.}$	2.0	—	V

4832 tbl 08

NOTES:

- At $V_{DD} \leq -2.0\text{V}$ input leakages are undefined.
- V_{DDQ} is selectable (3.3V/2.5V) via OPT pins. Refer to p.4 for details.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range⁽³⁾ ($V_{DD} = 3.3V \pm 150mV$)

Symbol	Parameter	Test Condition	Version	70V3389S4 Com'l Only		70V3389S5 Com'l & Ind		70V3389S6 Com'l Only		Unit
				Typ. ⁽⁴⁾	Max.	Typ. ⁽⁴⁾	Max.	Typ. ⁽⁴⁾	Max.	
IDD	Dynamic Operating Current (Both Ports Active)	\overline{CE}_L and $\overline{CE}_R = V_{IL}$, Outputs Disabled, $f = f_{MAX}^{(1)}$	COM'L S	375	460	285	360	245	310	mA
			IND S	—	—	285	415	245	360	
ISB1	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L = \overline{CE}_R = V_{IH}$ $f = f_{MAX}^{(1)}$	COM'L S	145	190	105	145	95	125	mA
			IND S	—	—	105	175	95	150	
ISB2	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}^*A^* = V_{IL}$ and $\overline{CE}^*B^* = V_{IH}^{(5)}$ Active Port Outputs Disabled, $f = f_{MAX}^{(1)}$	COM'L S	265	325	190	260	175	225	mA
			IND S	—	—	190	300	175	260	
ISB3	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports \overline{CE}_L and $\overline{CE}_R \geq V_{DDQ} - 0.2V$, $V_{IN} \geq V_{DDQ} - 0.2V$ or $V_{IN} \leq 0.2V$, $f = 0^{(2)}$	COM'L S	6	15	6	15	6	15	mA
			IND S	—	—	6	30	6	30	
ISB4	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}^*A^* \leq 0.2V$ and $\overline{CE}^*B^* \geq V_{DDQ} - 0.2V^{(5)}$ $V_{IN} \geq V_{DDQ} - 0.2V$ or $V_{IN} \leq 0.2V$, Active Port, Outputs Disabled, $f = f_{MAX}^{(1)}$	COM'L S	265	325	180	260	170	225	mA
			IND S	—	—	180	300	170	260	

4832 tbl 09

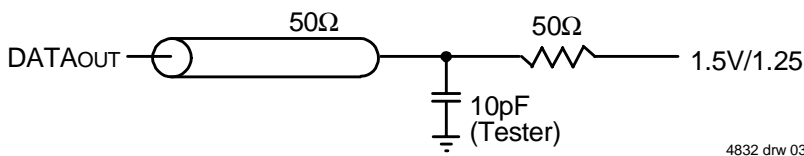
NOTES:

- At $f = f_{MAX}$, address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of $1/t_{cyc}$, using "AC TEST CONDITIONS" at input levels of GND to 3V.
- $f = 0$ means no address, clock, or control lines change. Applies only to input at CMOS level standby.
- Port "A" may be either left or right port. Port "B" is the opposite from port "A".
- $V_{DD} = 3.3V$, $T_A = 25^\circ C$ for Typ, and are not production tested. $I_{DD} \text{ dc}(f=0) = 120\text{mA}$ (Typ).
- $\overline{CE}_X = V_{IL}$ means $\overline{CE}_{0X} = V_{IL}$ and $CE_{1X} = V_{IH}$
 $\overline{CE}_X = V_{IH}$ means $\overline{CE}_{0X} = V_{IH}$ or $CE_{1X} = V_{IL}$
 $\overline{CE}_X \leq 0.2V$ means $\overline{CE}_{0X} \leq 0.2V$ and $CE_{1X} \geq V_{DDQ} - 0.2V$
 $\overline{CE}_X \geq V_{DDQ} - 0.2V$ means $\overline{CE}_{0X} \geq V_{DDQ} - 0.2V$ or $CE_{1X} \leq 0.2V$
 "X" represents "L" for left port or "R" for right port.

AC Test Conditions

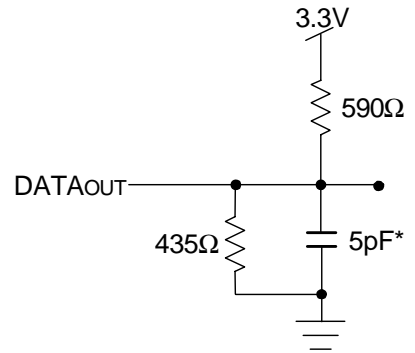
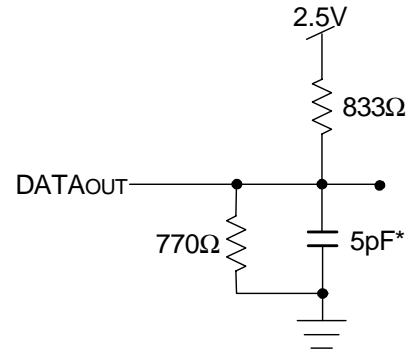
Input Pulse Levels (Address & Controls)	GND to 3.0V/GND to 2.35V
Input Pulse Levels (I/Os)	GND to 3.0V/GND to 2.35V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V/1.25V
Output Reference Levels	1.5V/1.25V
Output Load	Figures 1, 2, and 3

4832 tbl 10



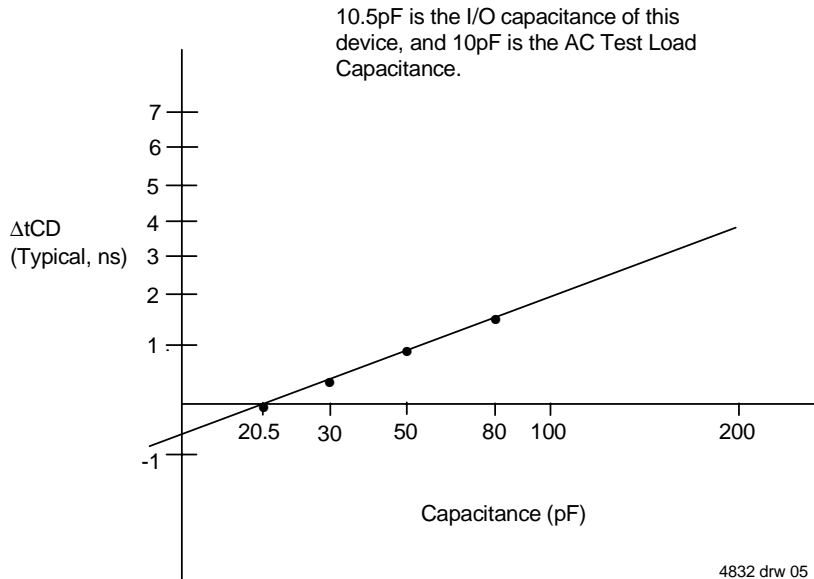
4832 drw 03

Figure 1. AC Output Test load.



4832 drw 04

Figure 2. Output Test Load
(For t_{CKLZ}, t_{CKHZ}, t_{OLZ}, and t_{OHZ}).
*Including scope and jig.



4832 drw 05

Figure 3. Typical Output Derating (Lumped Capacitive Load).

AC Electrical Characteristics Over the Operating Temperature Range (Read and Write Cycle Timing)^(1,2)

(V_{DD} = 3.3V ± 150mV, T_A = 0°C to +70°C)

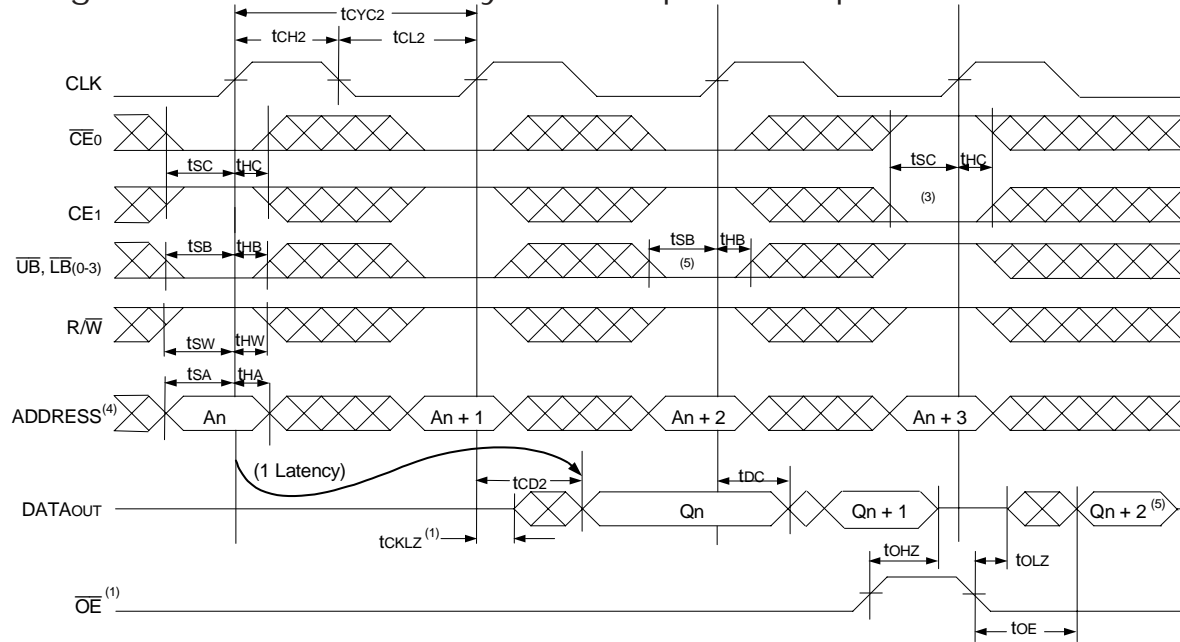
Symbol	Parameter	70V3389S4 Com'I Only		70V3389S5 Com'I & Ind		70V3389S6 Com'I Only		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{CYC2}	Clock Cycle Time (Pipelined)	7.5	—	10	—	12	—	ns
t _{CH2}	Clock High Time (Pipelined)	3	—	4	—	5	—	ns
t _{CL2}	Clock Low Time (Pipelined)	3	—	4	—	5	—	ns
t _R	Clock Rise Time	—	3	—	3	—	3	ns
t _F	Clock Fall Time	—	3	—	3	—	3	ns
t _{SA}	Address Setup Time	1.8	—	2.0	—	2.0	—	ns
t _{HA}	Address Hold Time	0.7	—	0.7	—	1.0	—	ns
t _{SC}	Chip Enable Setup Time	1.8	—	2.0	—	2.0	—	ns
t _{HC}	Chip Enable Hold Time	0.7	—	0.7	—	1.0	—	ns
t _{SB}	Byte Enable Setup Time	1.8	—	2.0	—	2.0	—	ns
t _{HB}	Byte Enable Hold Time	0.7	—	0.7	—	1.0	—	ns
t _{SW}	R/W Setup Time	1.8	—	2.0	—	2.0	—	ns
t _{HW}	R/W Hold Time	0.7	—	0.7	—	1.0	—	ns
t _{SD}	Input Data Setup Time	1.8	—	2.0	—	2.0	—	ns
t _{HD}	Input Data Hold Time	0.7	—	0.7	—	1.0	—	ns
t _{SAD}	\overline{ADS} Setup Time	1.8	—	2.0	—	2.0	—	ns
t _{HAD}	\overline{ADS} Hold Time	0.7	—	0.7	—	1.0	—	ns
t _{SCN}	\overline{CNTEN} Setup Time	1.8	—	2.0	—	2.0	—	ns
t _{HCN}	\overline{CNTEN} Hold Time	0.7	—	0.7	—	1.0	—	ns
t _{SRST}	\overline{CNTRST} Setup Time	1.8	—	2.0	—	2.0	—	ns
t _{HRST}	\overline{CNTRST} Hold Time	0.7	—	0.7	—	1.0	—	ns
t _{OE⁽¹⁾}	Output Enable to Data Valid	—	4	—	5	—	6	ns
t _{OLZ}	Output Enable to Output Low-Z	0	—	0	—	0	—	ns
t _{OHZ}	Output Enable to Output High-Z	1	4	1	4.5	1	5	ns
t _{CD2}	Clock to Data Valid (Pipelined)	—	4.2	—	5	—	6	ns
t _{DC}	Data Output Hold After Clock High	1	—	1	—	1	—	ns
t _{CKHZ}	Clock High to Output High-Z	1	3	1	4.5	1.5	6	ns
t _{CKLZ}	Clock High to Output Low-Z	1	—	1	—	1	—	ns
Port-to-Port Delay								
t _{CO}	Clock-to-Clock Offset	6	—	8	—	10	—	ns

4830 tbl 11

NOTES:

1. All input signals are synchronous with respect to the clock except for the asynchronous Output Enable (\overline{OE}).
2. These values are valid for either level of V_{DDO} (3.3V/2.5V). See page 4 for details on selecting the desired I/O voltage levels for each port.

Timing Waveform of Read Cycle for Pipelined Operation⁽²⁾

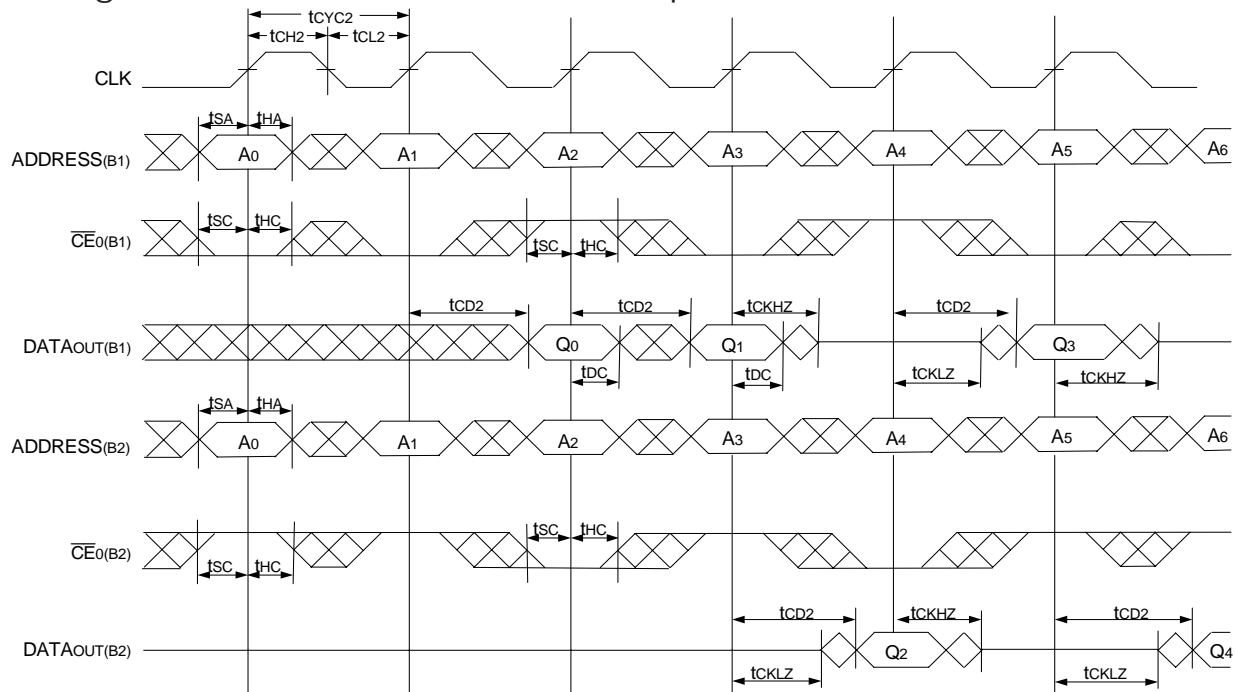


NOTES:

1. \overline{OE} is asynchronously controlled; all other inputs are synchronous to the rising clock edge.
2. $\overline{ADS} = V_{IL}$, \overline{CNTEN} and $\overline{CNTRST} = V_{IH}$.
3. The output is disabled (High-Impedance state) by $\overline{CE}_0 = V_{IH}$, $CE_1 = V_{IL}$, \overline{UB} , $\overline{LB} = V_{IH}$ following the next rising edge of the clock. Refer to Truth Table 1.
4. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. If \overline{UB} or \overline{LB} was HIGH, then the appropriate Byte of DATAout for $Q_n + 2$ would be disabled (High-Impedance state).

4832 drw 06

Timing Waveform of a Multi-Device Pipelined Read^(1,2)

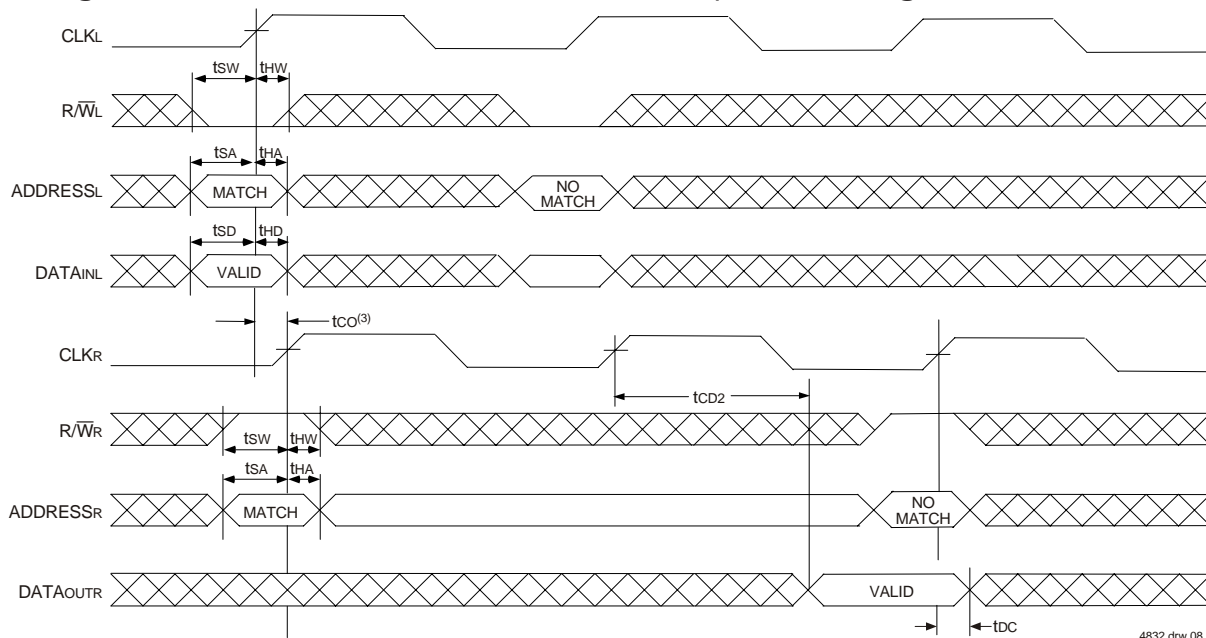


NOTES:

1. B1 Represents Device #1; B2 Represents Device #2. Each Device consists of one IDT70V3389 for this waveform, and are setup for depth expansion in this example. $ADDRESS_{(B1)} = ADDRESS_{(B2)}$ in this situation.
2. \overline{UB} , \overline{LB} , \overline{OE} , and $\overline{ADS} = V_{IL}$; $CE_1(B1)$, $CE_1(B2)$, R/\overline{W} , \overline{CNTEN} , and $\overline{CNTRST} = V_{IH}$.

4832 drw 07

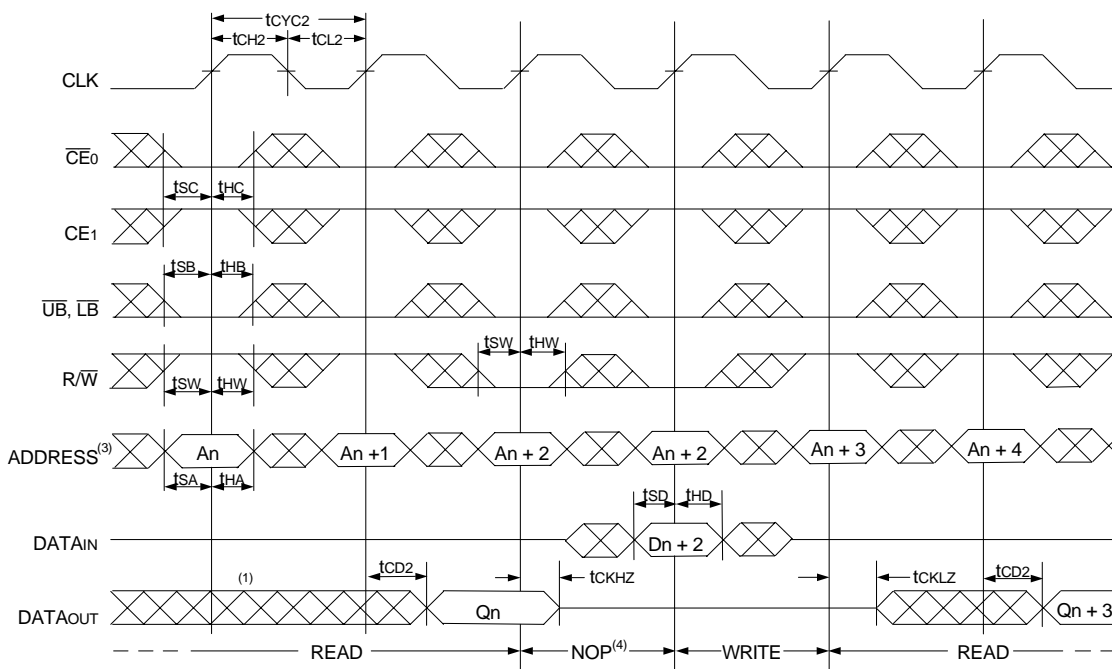
Timing Waveform of Left Port Write to Pipelined Right Port Read^(1,2)



NOTES:

1. $\overline{CE_0}$, \overline{UB} , \overline{LB} , and $\overline{ADS} = V_{IL}$; CE_1 , \overline{CNTEN} , and $\overline{CNTRST} = V_{IH}$.
2. $\overline{OE} = V_{IL}$ for the Right Port, which is being read from. $\overline{OE} = V_{IH}$ for the Left Port, which is being written to.
3. If $t_{CO} \leq$ minimum specified, then data from right port read is not valid until following right port clock cycle (ie, time from write to valid read on opposite port will be $t_{CO} + 2 t_{CYC2} + t_{CD2}$). If $t_{CO} >$ minimum, then data from right port read is available on first right port clock cycle (ie, time from write to valid read on opposite port will be $t_{CO} + t_{CYC} + t_{CD2}$).

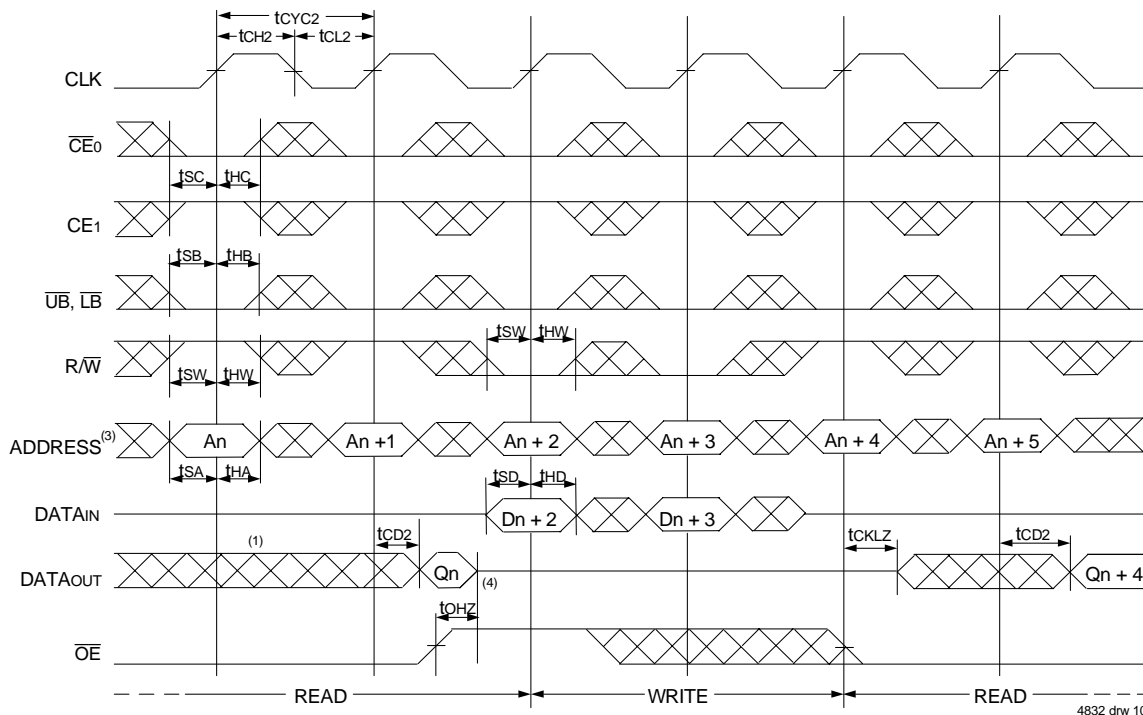
Timing Waveform of Pipelined Read-to-Write-to-Read ($\overline{OE} = V_{IL}$)⁽²⁾



NOTES:

1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2. $\overline{CE_0}$, \overline{UB} , \overline{LB} , and $\overline{ADS} = V_{IL}$; CE_1 , \overline{CNTEN} , and $\overline{CNTRST} = V_{IH}$. "NOP" is "No Operation".
3. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

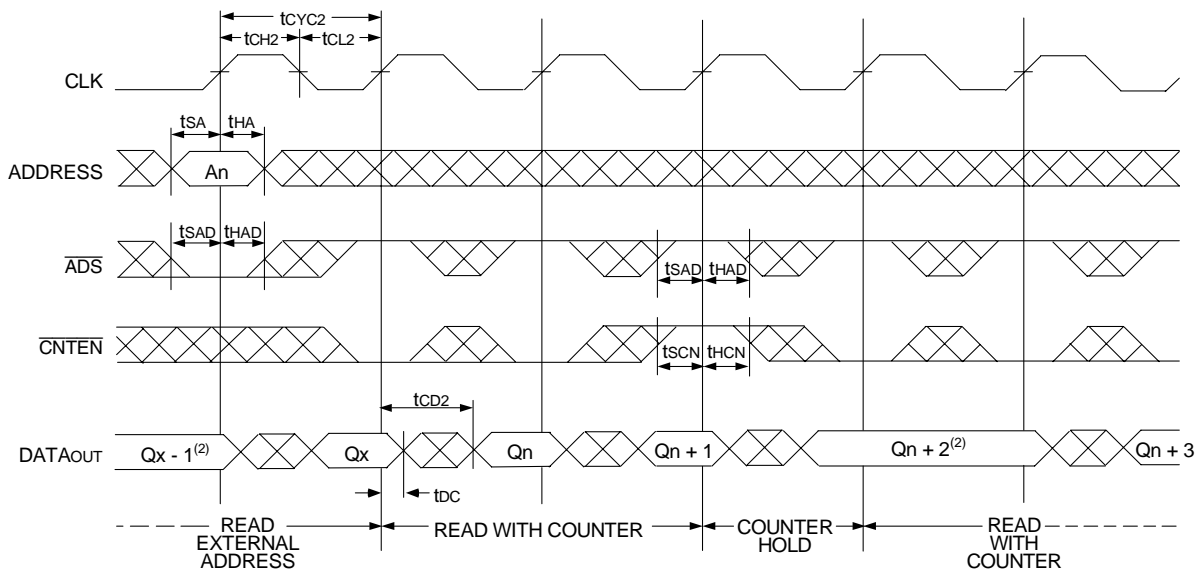
Timing Waveform of Pipelined Read-to-Write-to-Read (\overline{OE} Controlled)⁽²⁾



NOTES:

1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2. $\overline{CE0}$, \overline{UB} , \overline{LB} , and $\overline{ADS} = V_{IL}$; $\overline{CE1}$, \overline{CNTEN} , and $\overline{CNTRST} = V_{IH}$.
3. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. This timing does not meet requirements for fastest speed grade. This waveform indicates how logically it could be done if timing so allows.

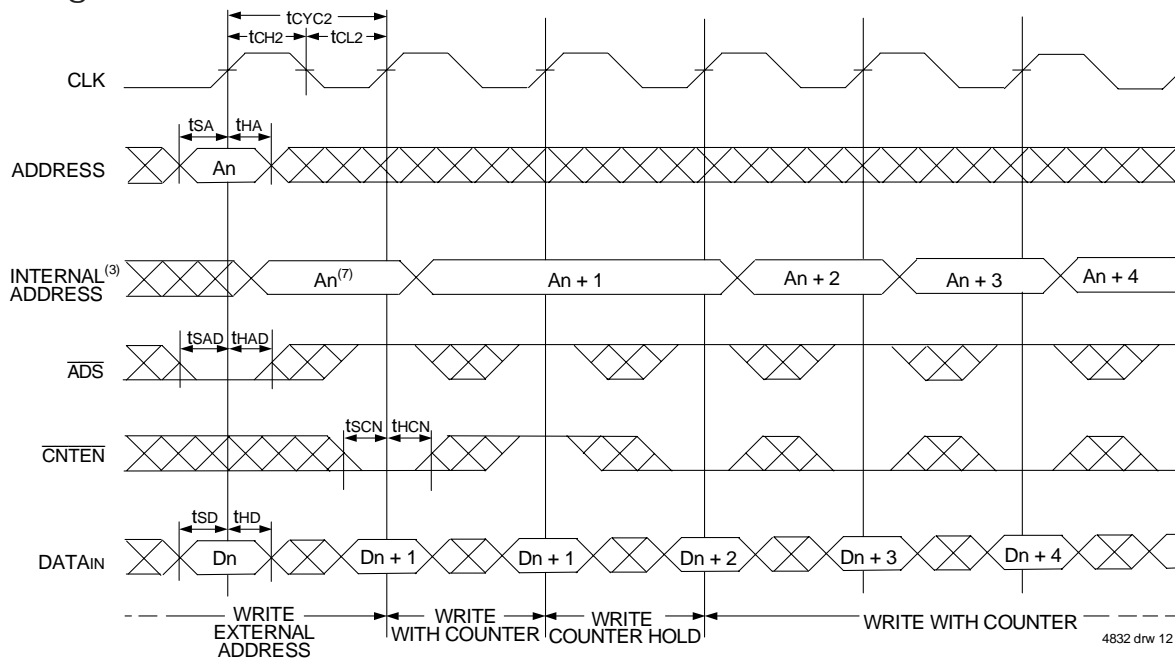
Timing Waveform of Pipelined Read with Address Counter Advance⁽¹⁾



NOTES:

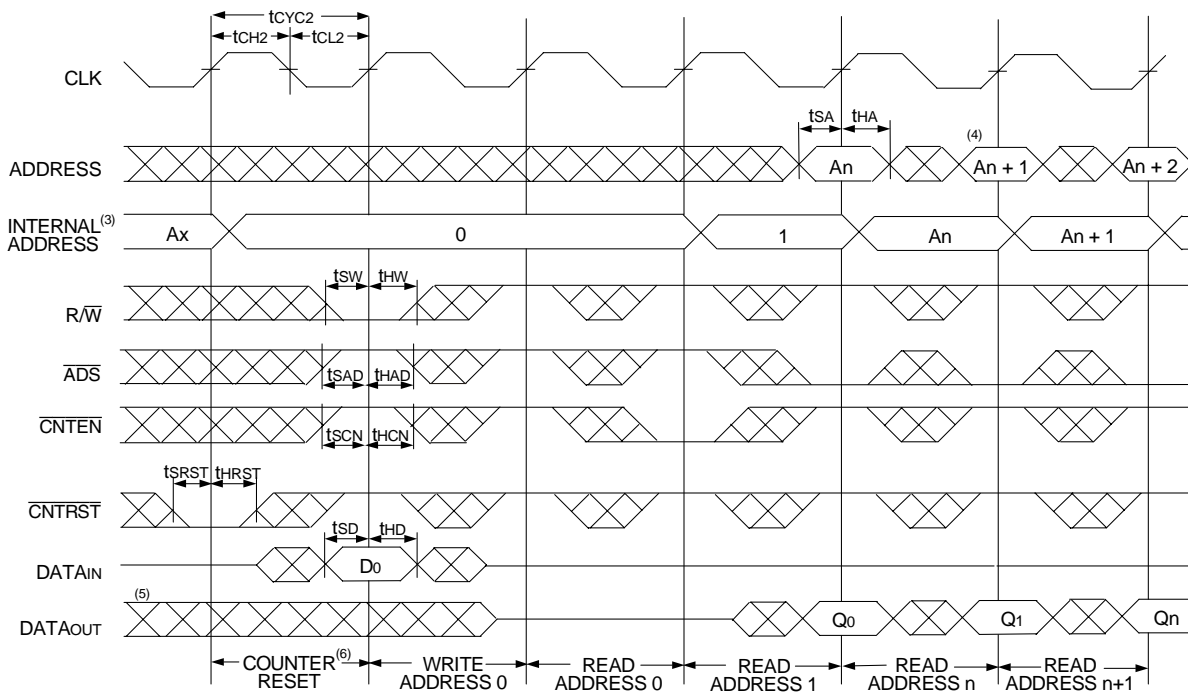
1. $\overline{CE0}$, \overline{OE} , \overline{UB} , $\overline{LB} = V_{IL}$; $\overline{CE1}$, $\overline{R/W}$, and $\overline{CNTRST} = V_{IH}$.
2. If there is no address change via $\overline{ADS} = V_{IL}$ (loading a new address) or $\overline{CNTEN} = V_{IL}$ (advancing the address), i.e. $\overline{ADS} = V_{IH}$ and $\overline{CNTEN} = V_{IH}$, then the data output remains constant for subsequent clocks.

Timing Waveform of Write with Address Counter Advance⁽¹⁾



4832 drw 12

Timing Waveform of Counter Reset⁽²⁾



4832 drw 13

NOTES:

1. \overline{CE}_0 , \overline{UB} , \overline{LB} , and $R/\overline{W} = V_{IL}$; CE_1 and $\overline{CNTRST} = V_{IH}$.
2. \overline{CE}_0 , \overline{UB} , $\overline{LB} = V_{IL}$; $CE_1 = V_{IH}$.
3. The "Internal Address" is equal to the "External Address" when $\overline{ADS} = V_{IL}$ and equals the counter output when $\overline{ADS} = V_{IH}$.
4. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
6. No dead cycle exists during counter reset. A READ or WRITE cycle may be coincidental with the counter reset cycle: Addr 0 will be accessed. Extra cycles are shown here simply for clarification.
7. $\overline{CNTEN} = V_{IL}$ advances Internal Address from 'An' to 'An +1'. The transition shown indicates the time required for the counter to advance. The 'An +1' Address is written to during this cycle.

Functional Description

The IDT70V3389 provides a true synchronous Dual-Port Static RAM interface. Registered inputs provide minimal set-up and hold times on address, data, and all critical control inputs. All internal registers are clocked on the rising edge of the clock signal, however, the self-timed internal write pulse is independent of the LOW to HIGH transition of the clock signal.

An asynchronous output enable is provided to ease asynchronous bus interfacing. Counter enable inputs are also provided to stall the operation of the address counters for fast interleaved memory applications.

A HIGH on $\overline{CE_0}$ or a LOW on CE_1 for one clock cycle will power down the internal circuitry to reduce static power consumption. Multiple chip enables allow easier banking of multiple IDT70V3389s for depth expansion configurations. Two cycles are required with $\overline{CE_0}$ LOW and CE_1 HIGH to re-activate the outputs.

Depth and Width Expansion

The IDT70V3389 features dual chip enables (refer to Truth Table I) in order to facilitate rapid and simple depth expansion with no requirements for external logic. Figure 4 illustrates how to control the various chip enables in order to expand two devices in depth.

The IDT70V3389 can also be used in applications requiring expanded width, as indicated in Figure 4. Through combining the control signals, the devices can be grouped as necessary to accommodate applications needing 36-bits or wider.

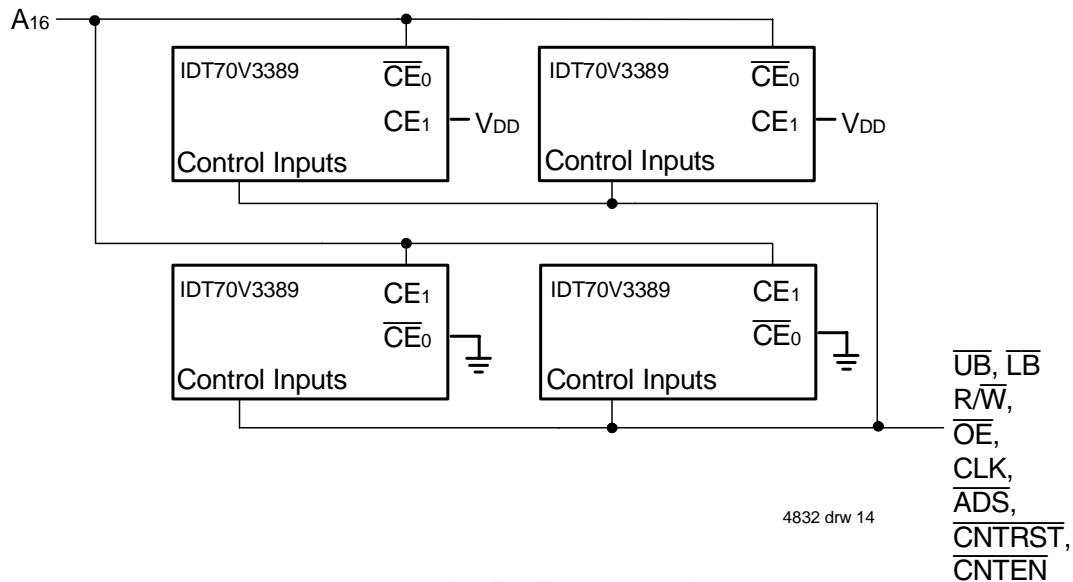
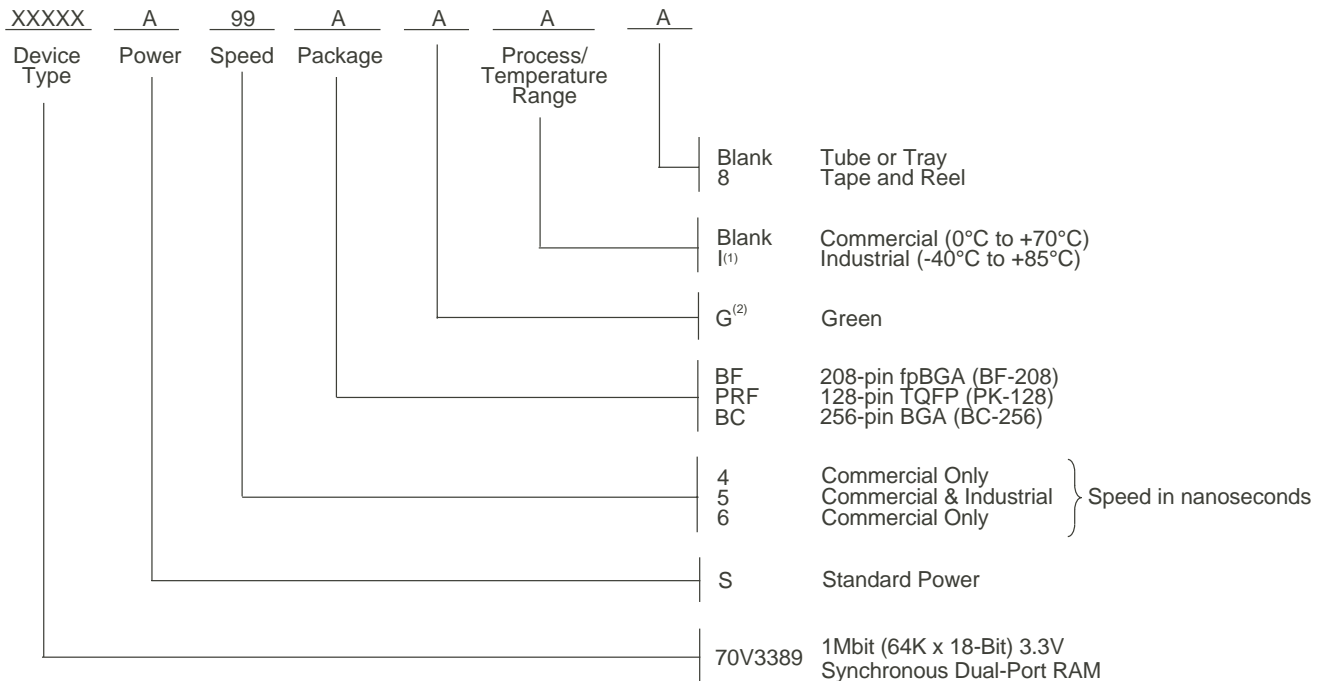


Figure 4. Depth and Width Expansion with IDT70V3389

Ordering Information



4832 drw 15a

NOTES:

- Contact your local sales office for Industrial temp range in other speeds, packages and powers.
- Green parts available. For specific speeds, packages and powers contact your local sales office.
LEAD FINISH (SnPb) parts are in EOL process. Product Discontinuation Notice - PDN# SP-17-02

Datasheet Document History

01/18/99:		Initial Public Release
03/15/99:	Page 9	Additional notes
04/28/99:		Added fpBGA package
06/08/99:	Page 2	Changed package body height from 1.5mm to 1.4mm
06/15/99:	Page 5	Deleted note 6 for Table II
07/14/99:	Page 2	Corrected pin T3 to VDDQL
08/04/99:	Page 6	Improved power numbers
10/01/99:		Upgraded speed to 133MHz, added 2.5V I/O capability
11/12/99:		Replaced IDT logo
02/28/00:		Added new BGA package, added full 2.5V interface capability
05/01/00:	Page 2	Added ball pitch
	Page 3	Renamed pins
	Page 6	Made corrections to Truth Table
	Page 9	Changed Ω numbers in figure 2
01/10/01:	Page 4	Added information to pin and pin notes
	Page 6	Increased storage temperature parameter Clarified TA Parameter
	Page 8	DC Electrical parameters—changed wording from "open" to "disabled" Removed note 7 on DC Characteristics table Removed Preliminary status
04/10/01:		Added Industrial Temperature Ranges and removed related notes

Datasheet Document History (cont'd)

- 02/12/01: Page 2, Added date revision to pin configurations
3 & 4
Page 6 Removed industrial temp footnote from table 04
Page 8 Removed industrial temp for 6ns from DC & AC Electrical Characteristic
& 10
Page 16 Removed industrial temp from 6ns in ordering information
Added industrial temp footnote
Page 1 Replaced TM logo with ® logo
& 17
- 01/05/06: Page 1 Added green availability to features
Page 16 Added green indicator to ordering information
- 02/08/06: Page 5 Changed footnote 2 for Truth Table I from $\overline{\text{ADS}}, \overline{\text{CNTEN}}, \overline{\text{CNTRST}} = V_{\text{IH}}$ to $\overline{\text{ADS}}, \overline{\text{CNTEN}}, \overline{\text{CNTRST}} = X$
- 07/25/08: Page 8 Corrected a typo in the DC Chars table
- 01/19/09: Page 16 Removed "IDT" from orderable part number
- 10/03/14: Page 16 Added Tape & Reel to Ordering Information
- 02/15/18: Product Discontinuation Notice - PDN# SP-17-02
Last time buy expires June 15, 2018



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