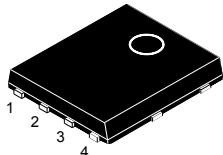
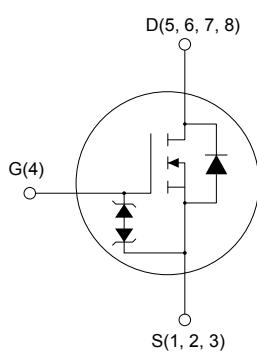


## N-channel 600 V, 255 mΩ typ., 9 A, MDmesh M6 Power MOSFET in a PowerFLAT 5x6 HV package

### Features


**PowerFLAT 5x6 HV**


AM15540v7

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STL18N60M6	600 V	308 mΩ	9 A

- Reduced switching losses
- Lower R<sub>DS(on)</sub> per area vs previous generation
- Low gate input resistance
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications
- LLC converters
- Boost PFC converters

### Description

The new MDmesh M6 technology incorporates the most recent advancements to the well-known and consolidated MDmesh family of SJ MOSFETs. STMicroelectronics builds on the previous generation of MDmesh devices through its new M6 technology, which combines excellent R<sub>DS(on)</sub> per area improvement with one of the most effective switching behaviors available, as well as a user-friendly experience for maximum end-application efficiency.



#### Product status link

[STL18N60M6](#)

#### Product summary

<b>Order code</b>	STL18N60M6
<b>Marking</b>	18N60M6
<b>Package</b>	PowerFLAT 5x6 HV
<b>Packing</b>	Tape and reel

## 1 Electrical ratings

**Table 1.** Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	$\pm 25$	V
$I_D$	Drain current (continuous) at $T_{case} = 25^\circ\text{C}$	9	A
	Drain current (continuous) at $T_{case} = 100^\circ\text{C}$	5.6	
$I_{DM}^{(1)}$	Drain current (pulsed)	36	A
$P_{TOT}$	Total power dissipation at $T_{case} = 25^\circ\text{C}$	57	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
	MOSFET $dv/dt$ ruggedness	100	
$T_{stg}$	Storage temperature range	-55 to 150	$^\circ\text{C}$
$T_j$	Operating junction temperature range		

1. Pulse width is limited by safe operating area.
2.  $I_{SD} \leq 9 \text{ A}$ ,  $di/dt \leq 400 \text{ A}/\mu\text{s}$ ,  $V_{DS(\text{peak})} < V_{(BR)DSS}$ ,  $V_{DD} = 400 \text{ V}$
3.  $V_{DS} \leq 480 \text{ V}$

**Table 2.** Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	2.2	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	50	$^\circ\text{C}/\text{W}$

1. When mounted on 1 inch<sup>2</sup> FR-4, 2 Oz copper board.

**Table 3.** Avalanche characteristics

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or non-repetitive (pulse width limited by $T_{Jmax}$ )	2.7	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50 \text{ V}$ )	210	mJ

## 2 Electrical characteristics

( $T_{case} = 25^\circ\text{C}$  unless otherwise specified).

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0 \text{ V}, I_D = 1 \text{ mA}$	600			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0 \text{ V}, V_{DS} = 600 \text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0 \text{ V}, V_{DS} = 600 \text{ V}, T_{case} = 125^\circ\text{C}$ <sup>(1)</sup>			100	
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 25 \text{ V}$			$\pm 5$	$\mu\text{A}$
$V_{GS(\text{th})}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	3.25	4	4.75	V
$R_{DS(on)}$	Static drain-source on-resistance	$I_D = 6.5 \text{ A}, V_{GS} = 10 \text{ V}$		255	308	$\text{m}\Omega$

1. Defined by design, not subject to production test.

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100 \text{ V}, f = 1 \text{ MHz}, V_{GS} = 0 \text{ V}$	-	650	-	$\text{pF}$
$C_{oss}$	Output capacitance		-	45	-	
$C_{rss}$	Reverse transfer capacitance		-	2	-	
$C_{oss \text{ eq.}}$ <sup>(1)</sup>	Equivalent output capacitance	$V_{DS} = 0 \text{ to } 480 \text{ V}, V_{GS} = 0 \text{ V}$	-	123	-	pF
$R_G$	Intrinsic gate resistance	$f = 1 \text{ MHz}, I_D = 0 \text{ A}$	-	4.6	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 480 \text{ V}, I_D = 9 \text{ A}, V_{GS} = 0 \text{ to } 10 \text{ V}$ (see Figure 14. Test circuit for gate charge behavior)	-	16.8	-	$\text{nC}$
$Q_{gs}$	Gate-source charge		-	4.5	-	
$Q_{gd}$	Gate-drain charge		-	8.4	-	

1.  $C_{oss \text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300 \text{ V}, I_D = 6.5 \text{ A}, R_G = 4.7 \Omega, V_{GS} = 10 \text{ V}$ (see Figure 13. Test circuit for resistive load switching times and Figure 17. Unclamped inductive waveform)	-	16	-	ns
$t_r$	Rise time		-	7	-	
$t_{d(off)}$	Turn-off delay time		-	28	-	
$t_f$	Fall time		-	9	-	

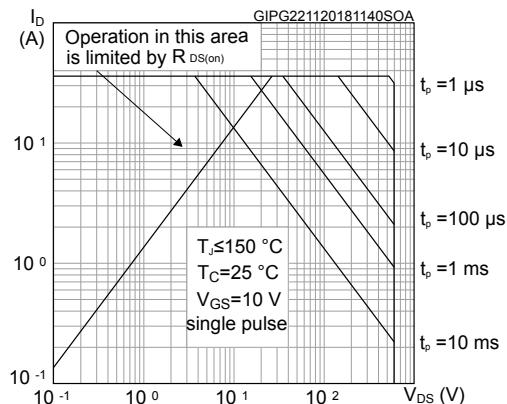
**Table 7. Source-drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		9	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		36	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 9 \text{ A}, V_{GS} = 0 \text{ V}$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 13 \text{ A}, dI/dt = 100 \text{ A}/\mu\text{s}, V_{DD} = 60 \text{ V}$	-	208		ns
$Q_{rr}$	Reverse recovery charge	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	1.9		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	18		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 13 \text{ A}, dI/dt = 100 \text{ A}/\mu\text{s}, V_{DD} = 60 \text{ V}, T_j = 150^\circ\text{C}$	-	290		ns
$Q_{rr}$	Reverse recovery charge	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	2.9		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	20		A

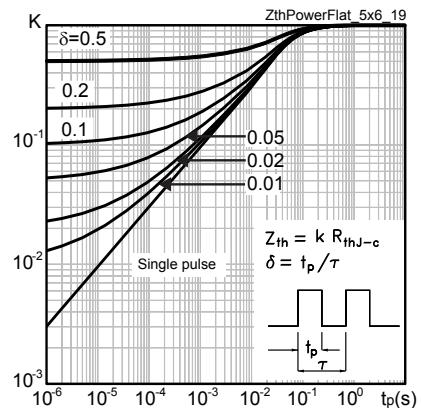
1. Pulse width is limited by safe operating area.
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

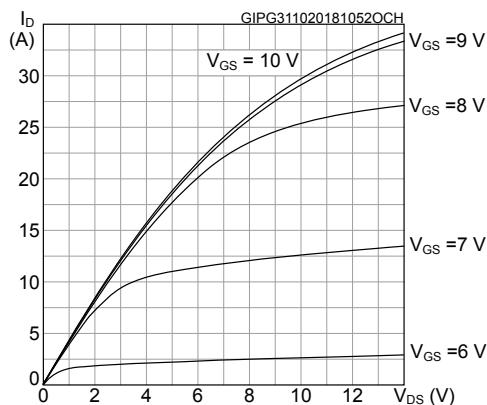
**Figure 1. Safe operating area**



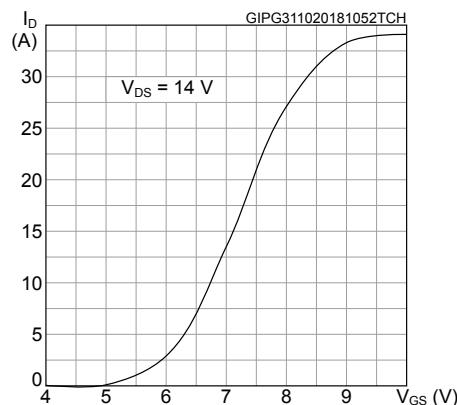
**Figure 2. Thermal impedance**



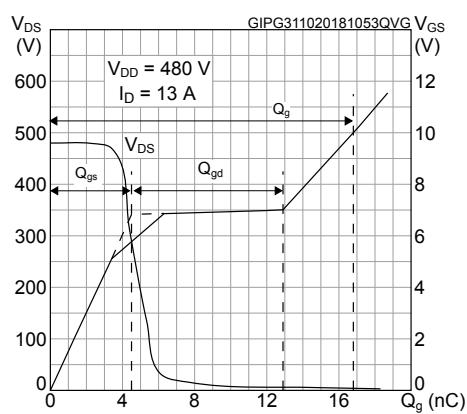
**Figure 3. Output characteristics**



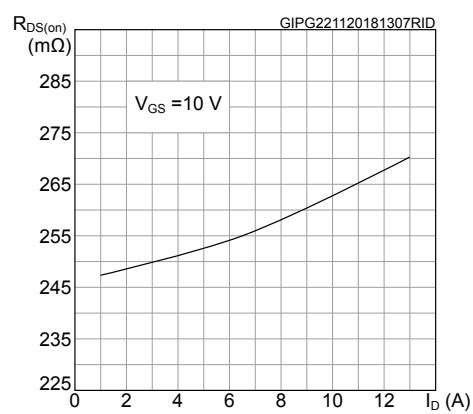
**Figure 4. Transfer characteristics**

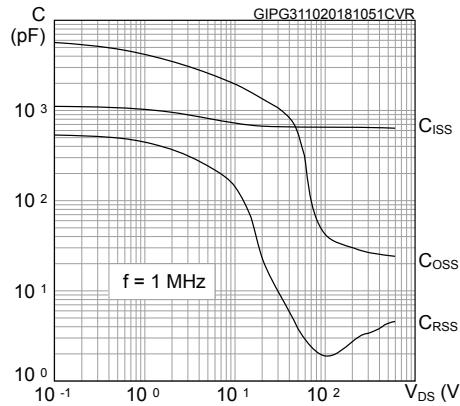
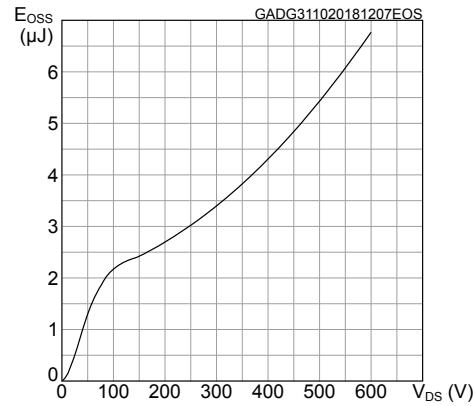
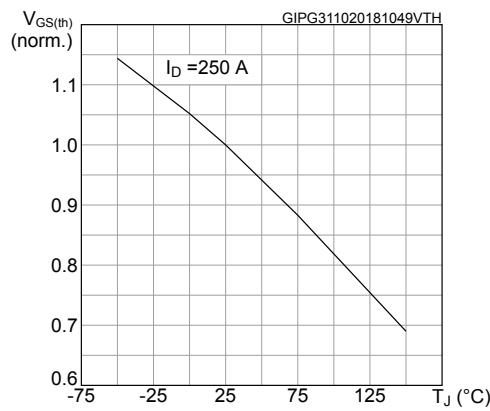
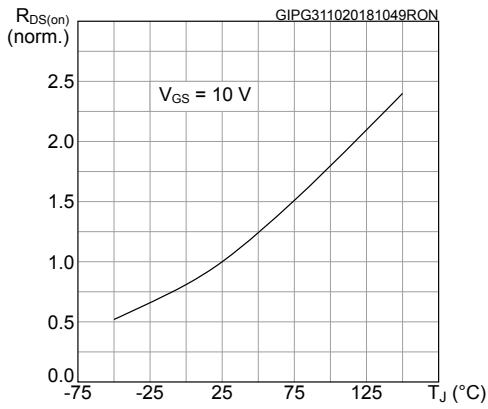
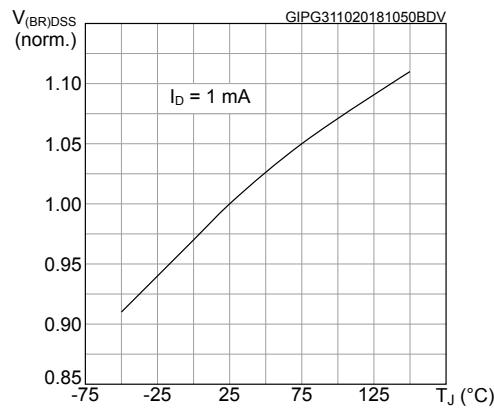
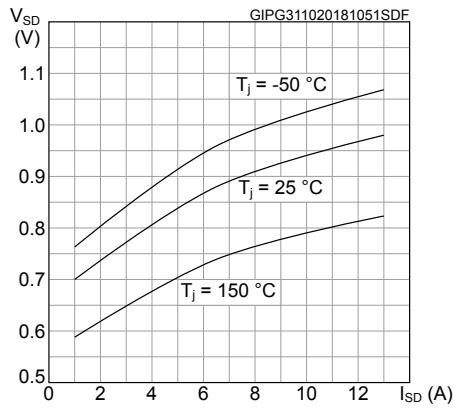


**Figure 5. Gate charge vs gate-source voltage**



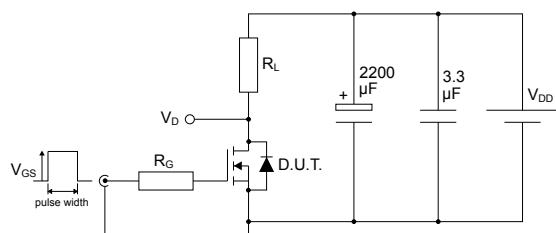
**Figure 6. Static drain-source on-resistance**



**Figure 7. Capacitance variations**

**Figure 8. Output capacitance stored energy**

**Figure 9. Normalized gate threshold voltage vs temperature**

**Figure 10. Normalized on-resistance vs temperature**

**Figure 11. Normalized V\_(BR)DSS vs temperature**

**Figure 12. Source-drain diode forward characteristics**


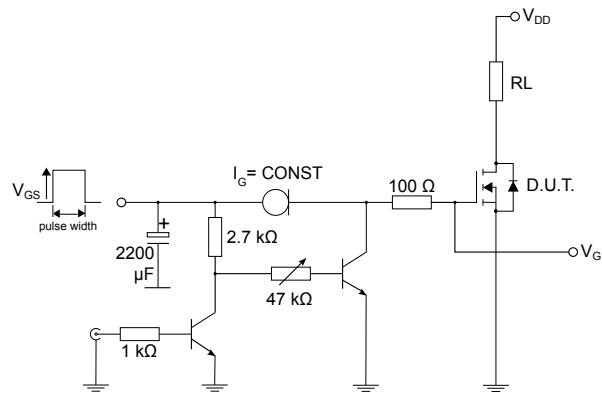
### 3 Test circuits

**Figure 13.** Test circuit for resistive load switching times



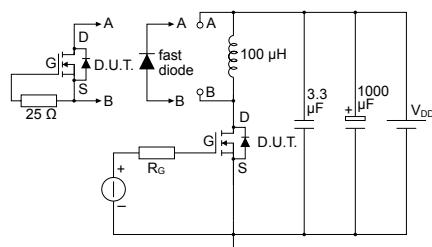
AM01468v1

**Figure 14.** Test circuit for gate charge behavior



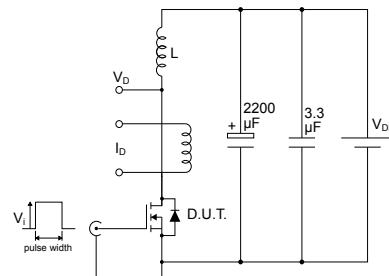
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**Figure 15.** Test circuit for inductive load switching and diode recovery times



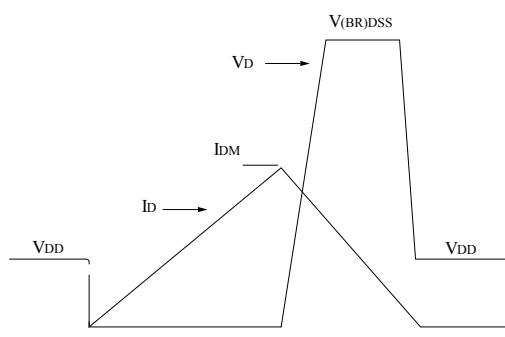
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**Figure 16.** Unclamped inductive load test circuit



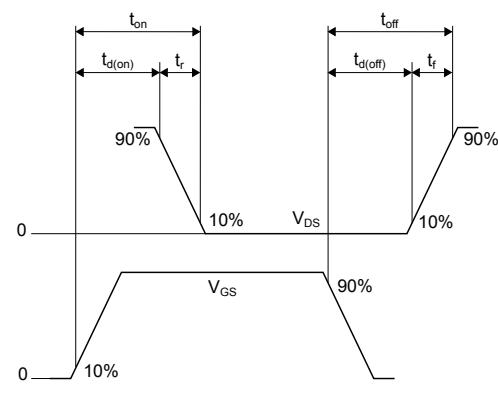
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**Figure 17.** Unclamped inductive waveform



AM01472v1

**Figure 18.** Switching time waveform



AM01473v1

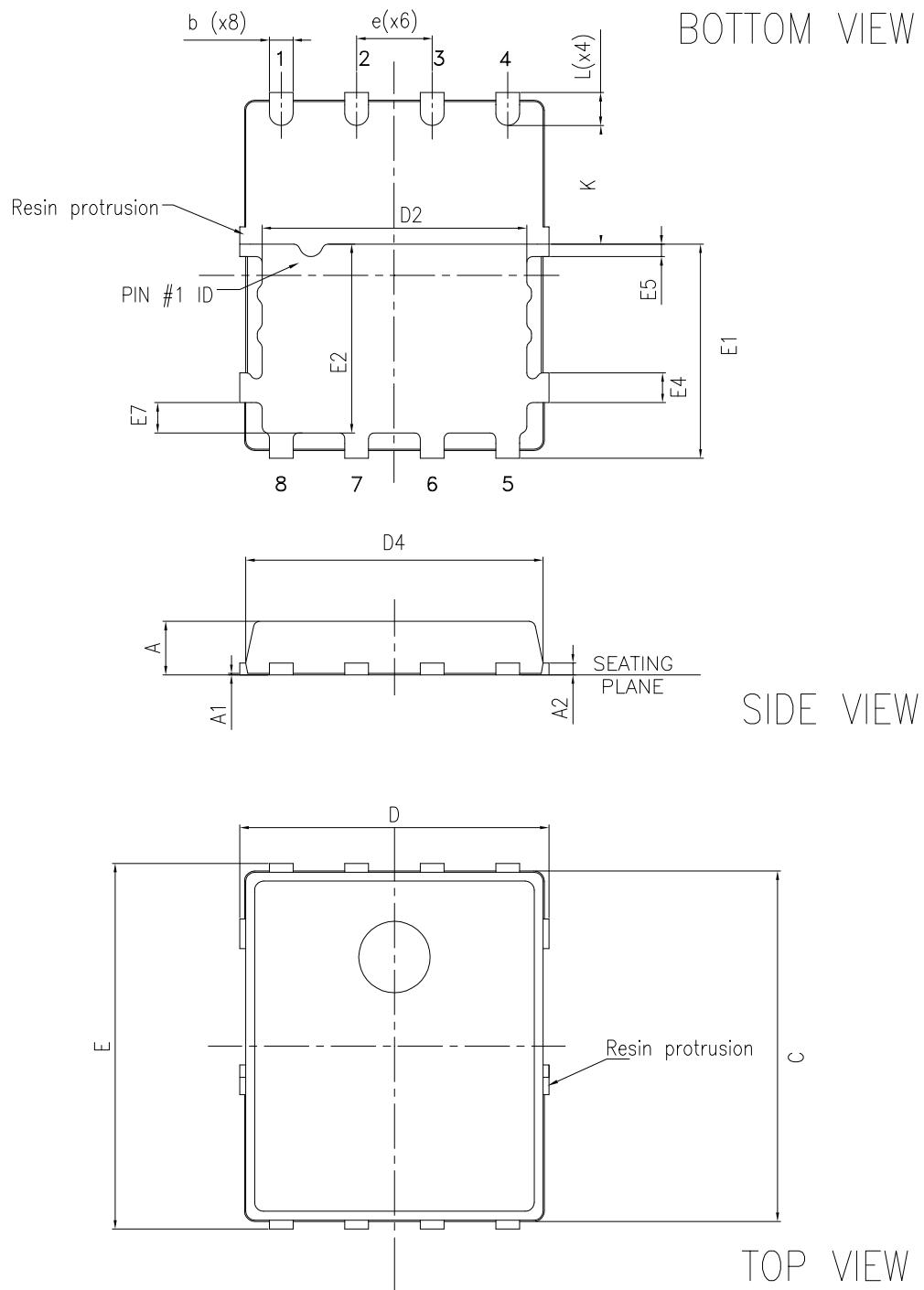
## 4 Package information

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In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

## 4.1 PowerFLAT 5x6 HV package information

Figure 19. PowerFLAT 5x6 HV package outline

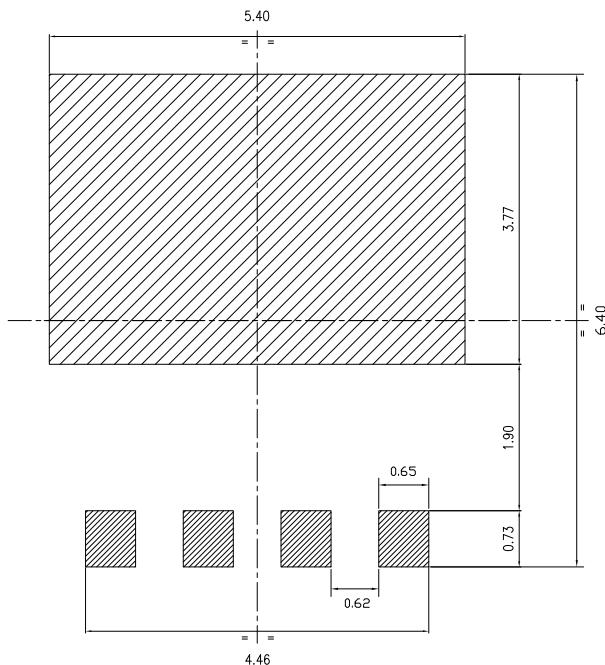


8368143\_Rev\_4

Table 8. PowerFLAT 5x6 HV mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.60	5.80	6.00
D	5.10	5.20	5.30
D2	4.30	4.40	4.50
D4	4.60	4.80	5.00
E	6.05	6.15	6.25
E1	3.50	3.60	3.70
E2	3.10	3.20	3.30
E4	0.40	0.50	0.60
E5	0.10	0.20	0.30
E7	0.40	0.50	0.60
e		1.27	
L	0.50	0.55	0.60
K	1.90	2.00	2.10

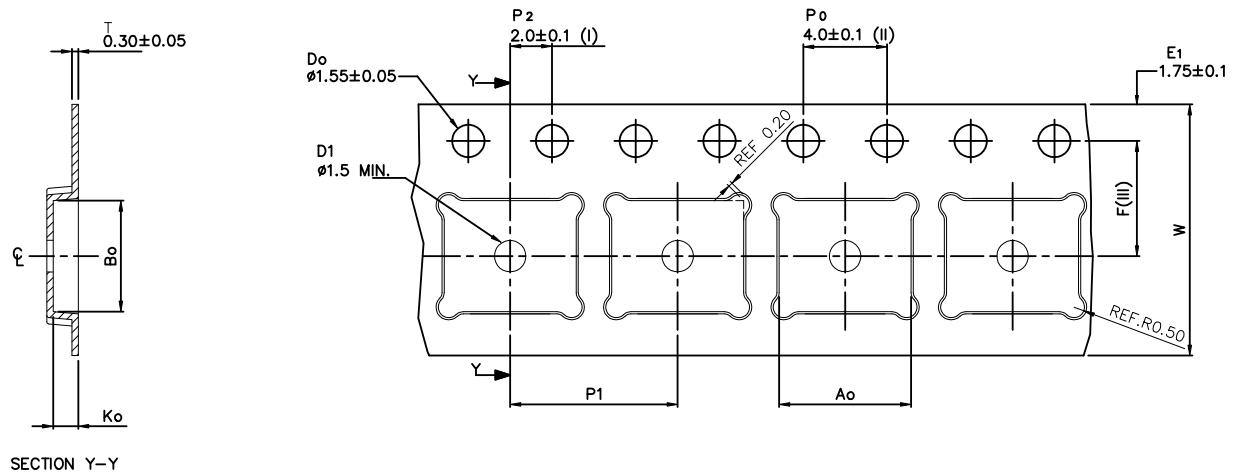
Figure 20. PowerFLAT™ 5x6 HV recommended footprint (dimensions are in mm)



8368143\_Rev\_4\_footprint

## 4.2 PowerFLAT 5x6 HV packing information

**Figure 21.** PowerFLAT 5x6 tape (dimensions are in mm)



$A_0$	$6.30 \pm 0.1$
$B_0$	$5.30 \pm 0.1$
$K_o$	$1.20 \pm 0.1$
$F$	$5.50 \pm 0.1$
$P_1$	$8.00 \pm 0.1$
$W$	$12.00 \pm 0.3$

(I) Measured from centreline of sprocket hole to centreline of pocket.

Base and bulk quantity 3000 pcs  
All dimensions are in millimeters

(II) Cumulative tolerance of 10 sprocket holes is  $\pm 0.20$ .

(III) Measured from centreline of sprocket hole to centreline of pocket

8234350\_Tape\_rev\_C

**Figure 22.** PowerFLAT 5x6 package orientation in carrier tape

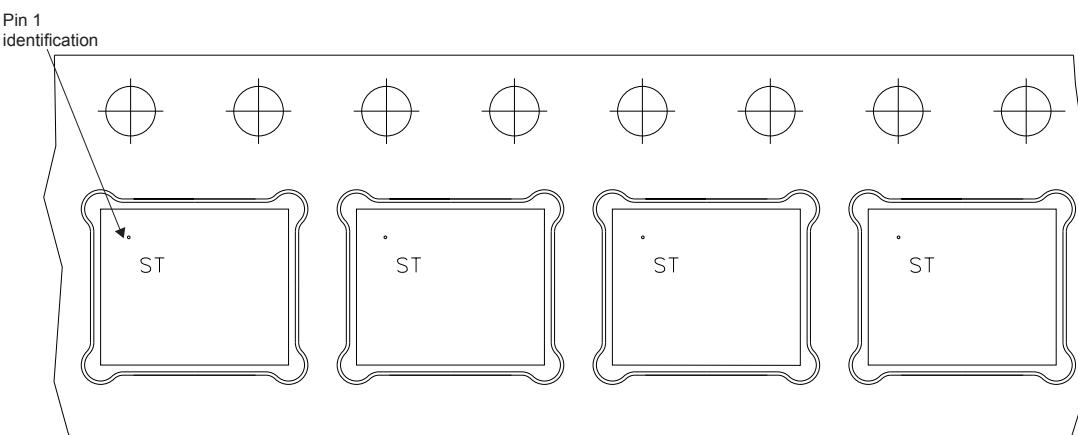
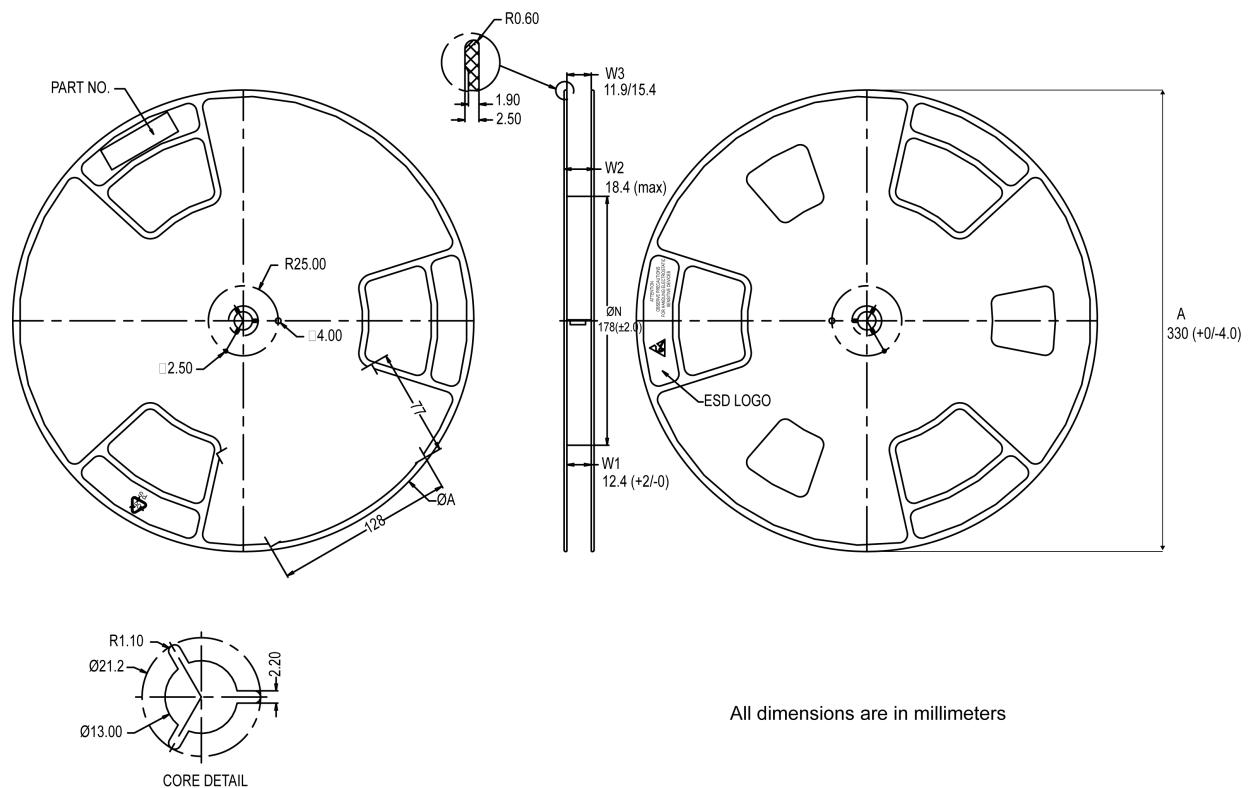


Figure 23. PowerFLAT 5x6 reel



8234350\_Reel\_rev\_C

## Revision history

**Table 9. Document revision history**

Date	Version	Changes
23-Nov-2018	1	First release.
18-Apr-2019	2	Changed package from PowerFLAT 8x8 HV to PowerFLAT 5x6 HV. Updated title in cover page, <i>Section 3 Test circuits</i> and <i>Section 4 Package information</i> . Minor text changes.
19-Apr-2019	3	Updated product status link table in cover page. Updated <a href="#">Figure 2. Thermal impedance</a> .

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Электрон  
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