

Low Voltage Video Amplifier with Y/C MIX and Filter

■ GENERAL DESCRIPTION

NJM2567 is a low voltage operating video amplifier included LPF,BPF In Y and C system.

Output with 75ohm driver optimize the TV monitor system.

The NJM2567 includes power saving circuit, suitable for portable video Application, camcorder and others.

■ PACKAGE OUTLINE

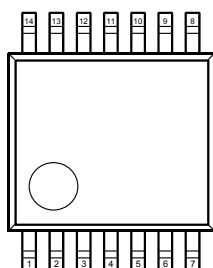


NJM2567V

■ FEATURES

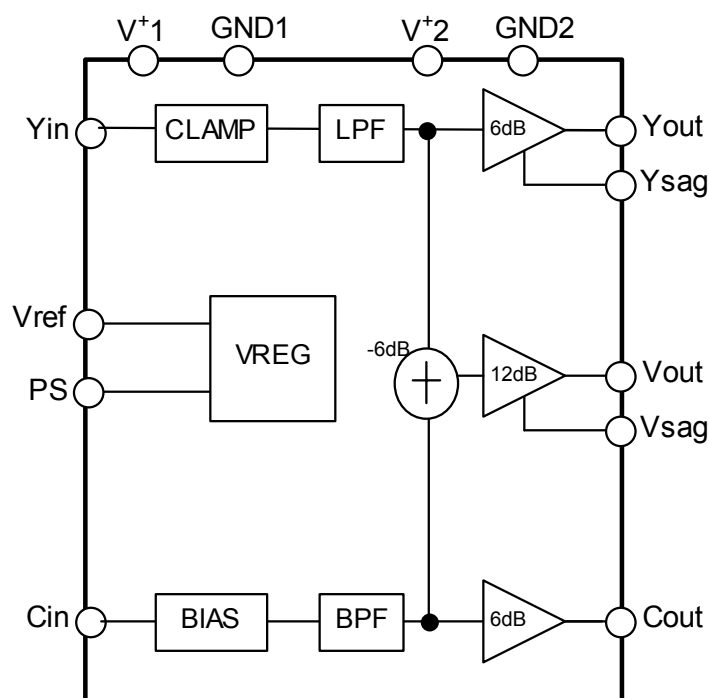
- Operating Voltage 2.8 to 5.5V
- Internal 6dB Amp. and 75ohm Driver
- Internal LPF(Y),BPF(C)
- Bipolar technology
- Package Outline SSOP14

■ PIN CONFIGURATION



- | | |
|---------------|----------|
| 1. V+1 | 8. Cout |
| 2. NC | 9. GND2 |
| 3. Yin | 10. Vsag |
| 4. Vref | 11. Vout |
| 5. Cin | 12. V+2 |
| 6. GND1 | 13. Ysag |
| 7. Power Save | 14. Yout |

■ BLOCK DIAGRAM



NJM2567

■ ABSOLUTE MAXIMUM RATINGS(Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V ⁺	7.0	V
Power Dissipation	P _D	300	mW
Operating Temperature Range	T _{opr}	-40 to +85	°C
Storage Temperature Range	T _{stg}	-40 to +125	°C

■ RECOMMENDED OPEARATING CONDITION(Ta=25°C)

PARAMETER	SYMBOL	RATINGS	MIN.	TYP.	MAX.	UNIT
Operating Voltage 1	Vopr1	V ⁺ 1	2.8	-	5.5	V
Operating Voltage 2	Vopr2	V ⁺ 2	2.8	-	5.5	V

■ ELECTRICAL CHARACTERISTICS ($V^+1 = V^+2 = 3V$, Powersave=3V, $R_L = 150\Omega$, $T_a = 25^\circ C$ at non-designation)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Circuit 1	I_{CC1}	$V^+1 = 5.0V$, No signal	-	12.0	16.0	mA
Operating Circuit 2	I_{CC2}	$V^+2 = 5.0V$, No signal	-	10.0	15.0	mA
Operating Circuit 1 at Power Save	I_{save1}	$V^+1 = 5.0V$, Power Save Mode	-	40	80	μA
Operating Circuit 2 at Power Save	I_{save2}	$V^+2 = 5.0V$, Power Save Mode	-	0	5	μA
Voltage Gain (Y Signal)	G_{vy}	$Y_{in} = 100kHz$, 1.0Vpp Input Sin Signal	6.1	6.5	6.9	dB
Voltage Gain (C Signal)	G_{vc}	$Y_{in} = 4.43MHz$, 0.3Vpp Input Sin Signal	6.1	6.5	6.9	dB
Voltage Gain (V Signal)	G_{vv}	$Y_{in} = 100kHz$, 1.0Vpp Input Sin Signal	6.1	6.5	6.9	dB
Frequency Characteristics	G_{fy1}	$Y_{in} = 6MHz/100kHz$, 1.0Vpp Input Sin Signal	-0.5	0	+0.5	dB
	G_{fy2}	$Y_{in} = 20MHz/100kHz$, 1.0Vpp Input Sin Signal	-	-25	-	
	G_{fc1}	$C_{in} = \pm 1MHz/4.43MHz$, 0.3Vpp Input Sin Signal	-0.5	0	+0.5	
	G_{fc2}	$C_{in} = 20MHz/4.43MHz$, 0.3Vpp Input Sin Signal	-	-25	-	
Group Delay Characteristic (Y Signal)	T_{dY}	$Y_{in} = 4.43MHz$, Sin Signal	-	60	-	ns
Group Delay Characteristic (C Signal)	T_{dC}	$C_{in} = 4.43MHz$, Sin Signal	-	60	-	ns
Maximum Output Voltage Swing (Y Signal)	V_{oym}	$Y_{in} = 100kHz$, Sin Signal, THD=1%, $R_L = 75\Omega$	1.1	1.2	-	Vp-p
Maximum Output Voltage Swing (C Signal)	V_{ocm}	$C_{in} = 4.43MHz$, Sin Signal, THD=1%, $R_L = 75\Omega$	0.7	1.1	-	Vp-p
Maximum Output Voltage Swing (V Signal)	V_{ovm}	$Y_{in} = 100kHz$, Sin Signal, THD=1%, $R_L = 75\Omega$	1.1	1.2	-	Vp-p
Differential Gain(Y Signal)	DG_Y	$Y_{in} = 1.0Vpp$, 10Step video signal, measure the Y_{out} .	-	0.3	-	%
Differential Phase(Y Signal)	DP_Y	$Y_{in} = 1.0Vpp$, 10Step video signal, measure the Y_{out} .	-	0.3	-	deg
Differential Gain(V Signal)	DG_V	$Y_{in} = 1.0Vpp$, $C_{in} = 0.3Vpp$, 10Step video signal, measure the V_{out} .	-	0.3	-	%
Differential Phase(V Signal)	DP_V	$Y_{in} = 1.0Vpp$, $C_{in} = 0.3Vpp$, 10Step video signal, measure the V_{out} .	-	0.3	-	deg
SW Change Voltage High Level for Power Save	V_{CH}	Active	1.4	-	V^+	V
SW Change Voltage Low Level for Power Save	V_{CL}	Non-active	0	-	0.6	V

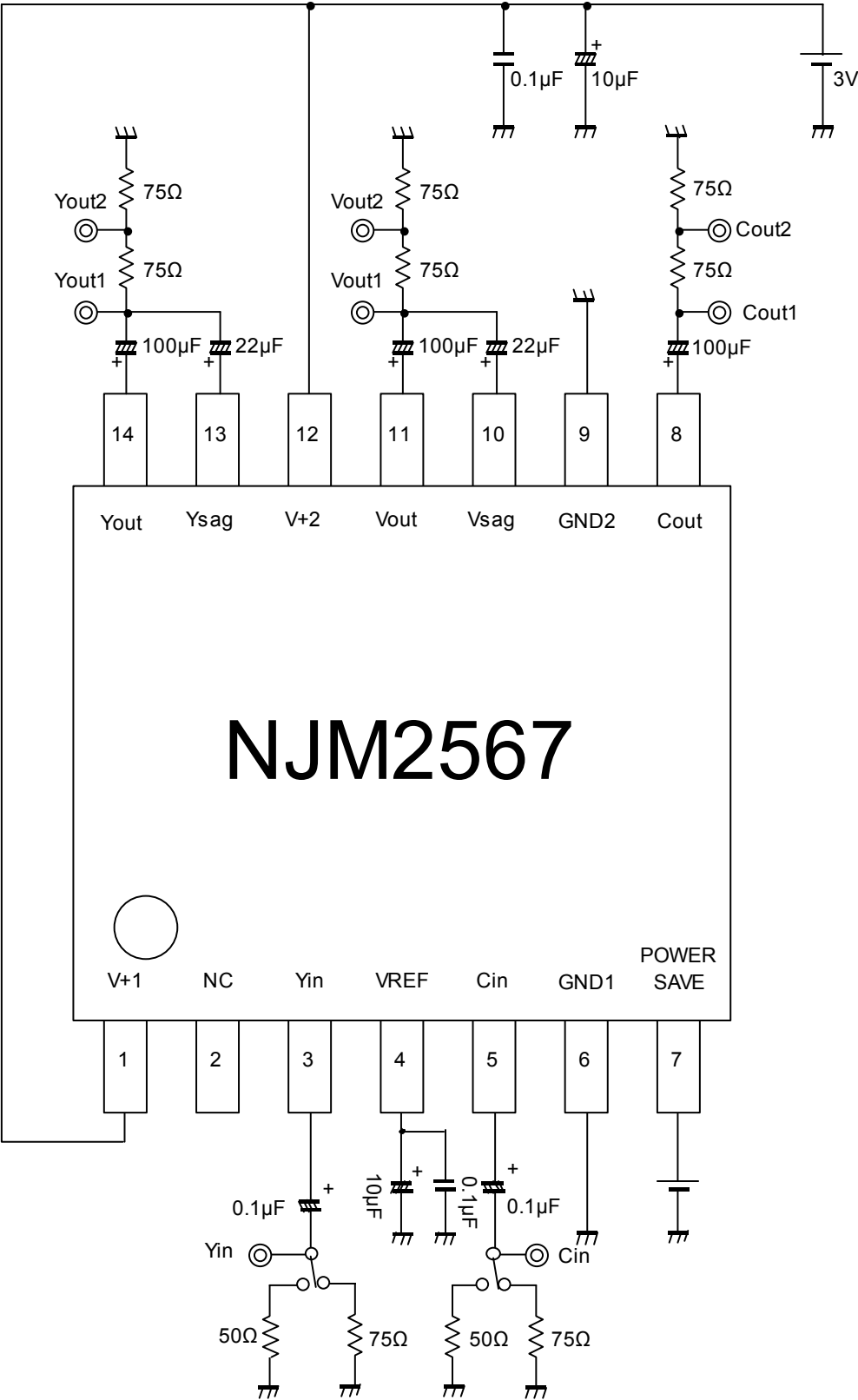
■ ELECTRICAL CHARACTERISTICS (V⁺1= V⁺2=3V, Powersave=3V, R_L=150Ω, Ta=25°C at non-designation)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Crosstalk 1(Yin to Cout)	CTyc	Yin to Cout=20log(Cout/Yout) Yin=4.43MHz, 1.0Vpp Sin Signal, Cin=AC GND	-	-50	-	dB
Crosstalk 2(Cin to Yout)	CTcy	Cin to Yout=20log(Yout/Cout) Cin=4.43MHz, 0.3Vpp Sin Signal, Yin=AC GND	-	-50	-	dB
S/N1(Y Signal)	SNy	Yin=100% White Video Signal, R _L =75Ω at Yout Bandwidth 100kHz to 6MHz	-	60	-	dB
S/N2(C Signal)	SNc1	Cin=100% Red Field Video Signal, R _L =75Ω at Cout, AM Noise Bandwidth 100kHz to 500kHz	-	60	-	dB
S/N3(C Signal)	SNc2	Cin=100% Red Field Video Signal, R _L =75Ω at Cout, PM Noise Bandwidth 100kHz to 500kHz	-	60	-	dB
S/N4 (V Signal)	SNv	Yin=100% White Video Signal, R _L =75Ω at Vout Bandwidth 100kHz to 6MHz	-	60	-	dB
2nd. Distortion 1 (Y Signal)	Hy	Yin=1MHz, 1.0Vpp Input Sin Signal	-	-50	-	dB
2nd. Distortion 2 (C Signal)	Hc	Cin=4.43MHz, 0.3Vpp Input Sin Signal	-	-50	-	dB
2nd. Distortion 3 (V Signal)	Hv	Yin=1MHz, 1.0Vpp Input Sin Signal	-	-50	-	dB

■ CONTROL TERMINAL

PARAMETER	CONTROL	NOTES
Power Save	H	Power Save: OFF
	L	Power Save: ON
	OPEN	Power Save: ON

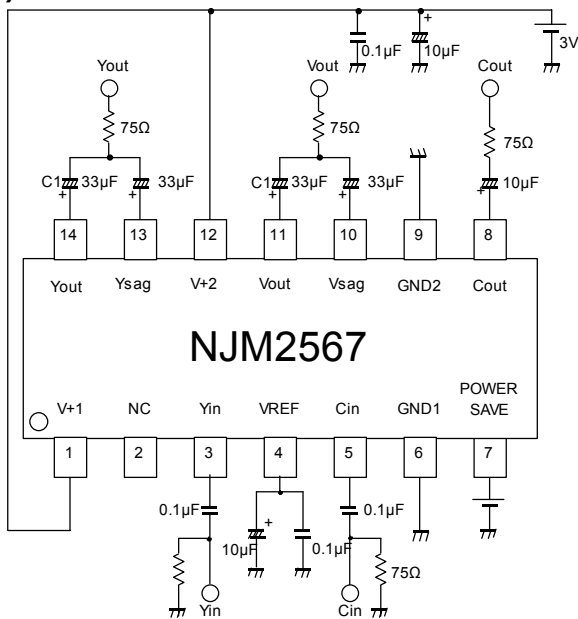
■ TEST CIRCUIT



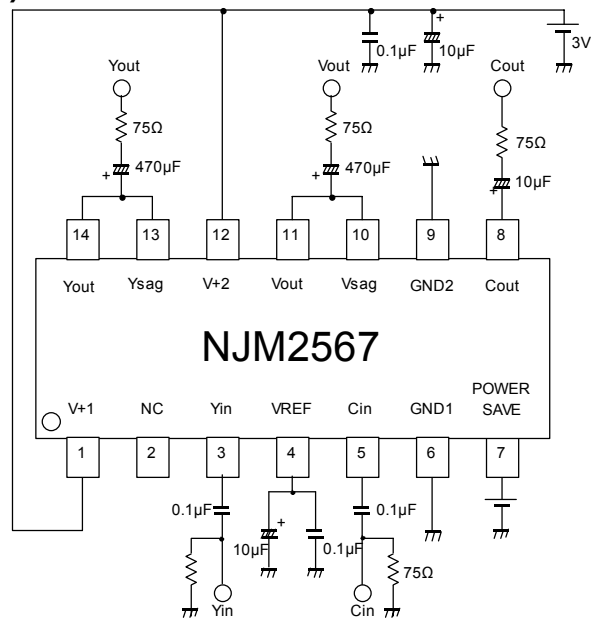
NJM2567

APPLICATION CIRCUIT

(1) Standard circuit



(2) SAG correction unused circuit



(1) Standard circuit

The SAG correction reduces output coupling capacitor values.

The capacitor of C1 (33μF) is recommended for the portable application.

However, the 33μF capacitor may deteriorate SAG, and lose synchronization by luminance fluctuation.

Adjust the C1 value, checking the waveform containing a lot of low frequency components like a bounce waveform (In case of worst condition). Change the capacitor of C1 into a large value to improve SAG.

(2) SAG correction unused circuit

Cancel the SAG correction to improve lost synchronization.

Connect the coupling capacitor after connecting the Vout pin and Vsag pin. The recommended value is 470μF or more.

■ TERMINAL DESCRIPTION

Pin No.	SYMBOL	EQUIVALENT CIRCUIT
3	Yin	
4	Vref	
5	Cin	
7	Power save	
8	Cin	
10 11 13 14	Vsag Vout Ysag Yout	

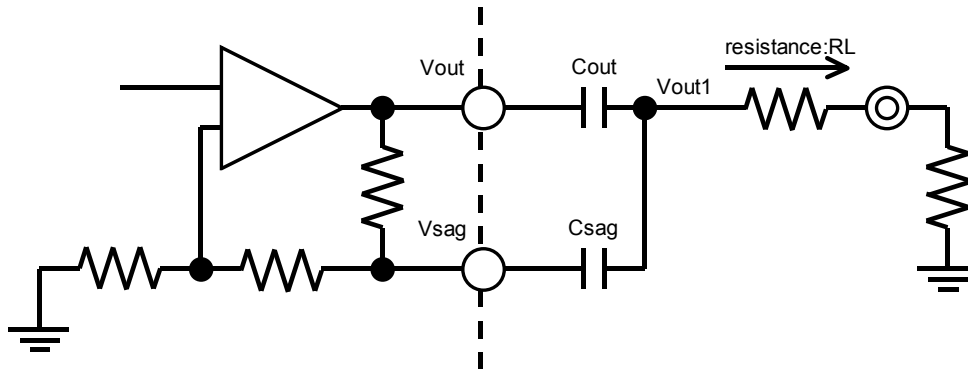
APPLICATION

◆ SAG correction circuit

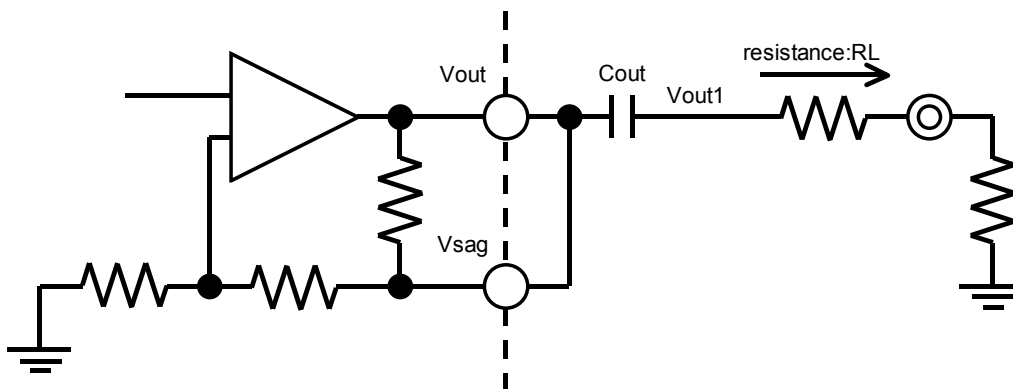
SAG correction circuit is a circuit to correct for low-frequency attenuation by high-pass filter consisting of the output coupling capacitance and load resistance. Low-frequency attenuation raises the sag in the vertical period of the video signal.

Capacitor for Vsag (C_{sag}) is connected to the negative feedback of the amplifier. This C_{sag} increase the low frequency gain to correct for the attenuation of low frequency gain.

Example SAG collection circuit

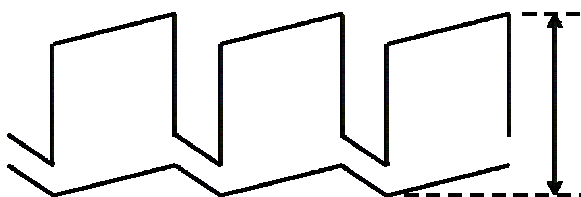


Example of not using sag compensation circuit

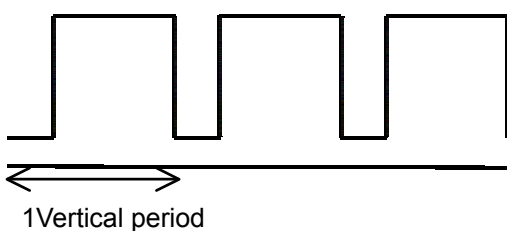


Waveform of Vout terminal and Vout1 terminal

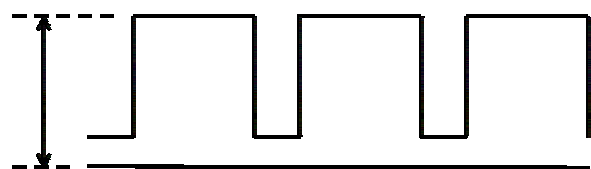
using SAG correction circuit
Waveform of Vout



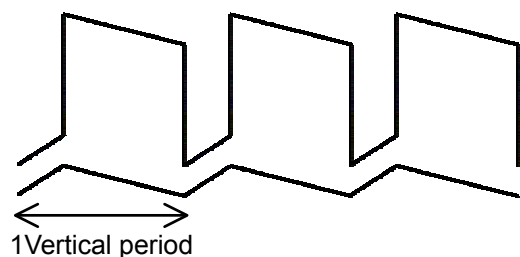
Waveform of Vout1



not using SAG correction circuit
Waveform of Vout

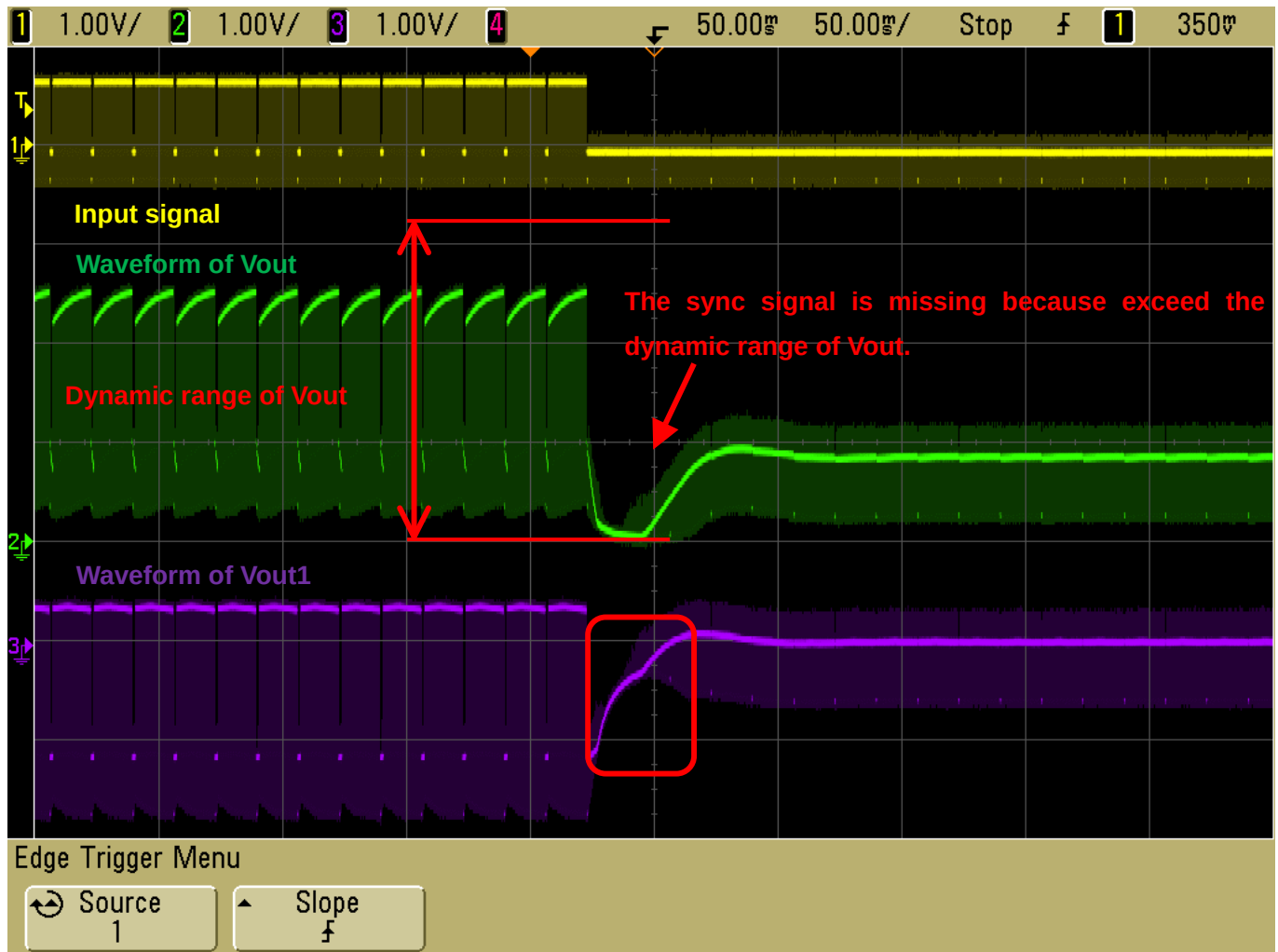


Waveform of Vout1



SAG correction circuit generates a low frequency component signal amplified to Vout terminal. Changes of the luminance signal will be low-frequency components, if you want to output a large signal luminance changes. Therefore, generate correction signal of change of a luminance signal to Vout pin. At this time, signal is over the dynamic range of Vout pin. This may cause a lack of sync signal, and waveform distortion.

Please see diagram below (green waveform), if you want to output large changes of a signal luminance, such as 100% white video signal and black signal. Thus, output signal exceed dynamic range of Vout pin and may be the signal lack.



< Countermeasure for waveform distortion >

1. Please using small value the Sag compensation capacitor (VSAG).

It can ensure the dynamic range by using small value the capacitor (VSAG). It because of low-frequency variation of Vout pin is smaller. However, the output (VOUT) must be use large capacitor for this reason sag characteristics become exacerbated.

2. Please do not use the sag correction circuit.

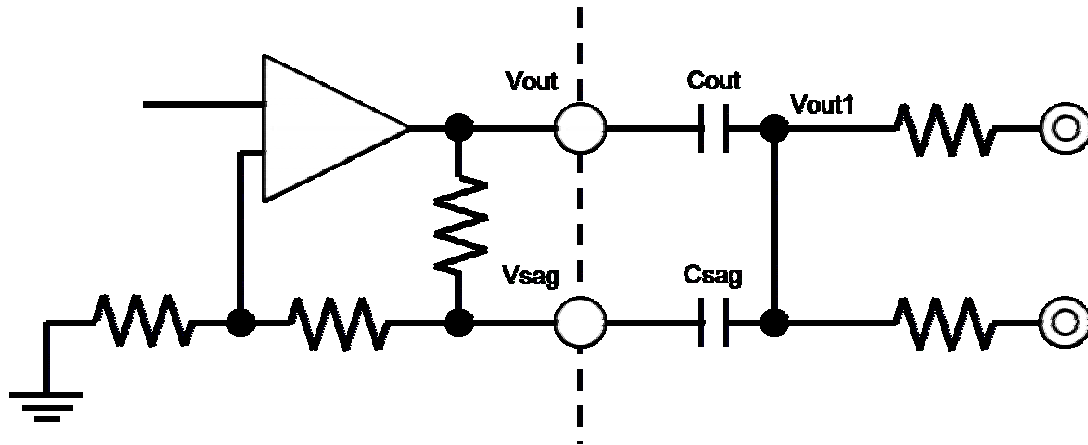
Signal can output within dynamic range for reason it does not change the DC level of the output terminal.

However, the output (VOUT) must be use large capacitor for this reason sag characteristics become exacerbated.

< Dual drive at using SAG correction circuit >

Using sag correction circuit at dual drive circuit is below. Dual drives are less load resistance. Thus, the cut-off frequency of HPF that is composed of the output capacitor and load resistance will be small. Therefore, the sag characteristics deteriorate.

Please size up to the output capacitor (Vout) for not to deteriorate the sag characteristics.



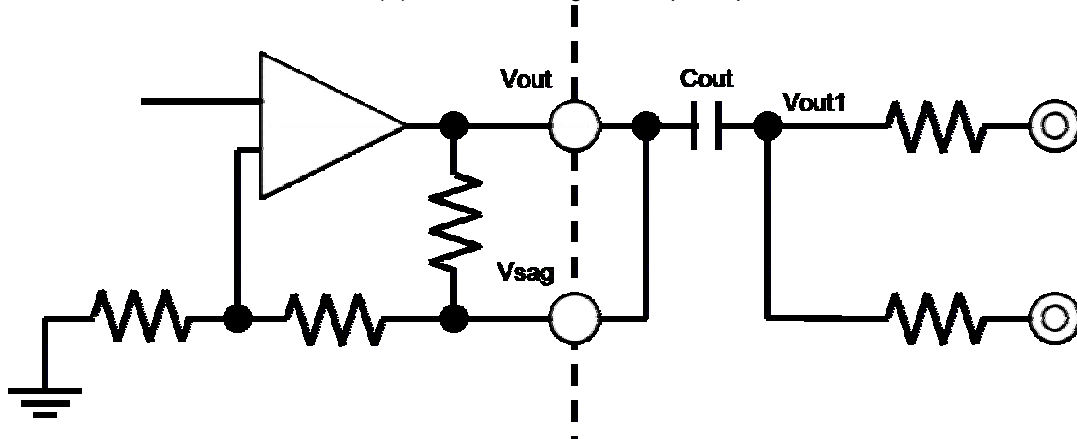
< Dual drive at not using SAG correction circuit >

We recommended two-example dual drive circuit with not use sag correction circuit. Please change the configuration to be used according to the situation. Please configure to meet the following conditions. Then you can adjust the characteristics of each configuration.

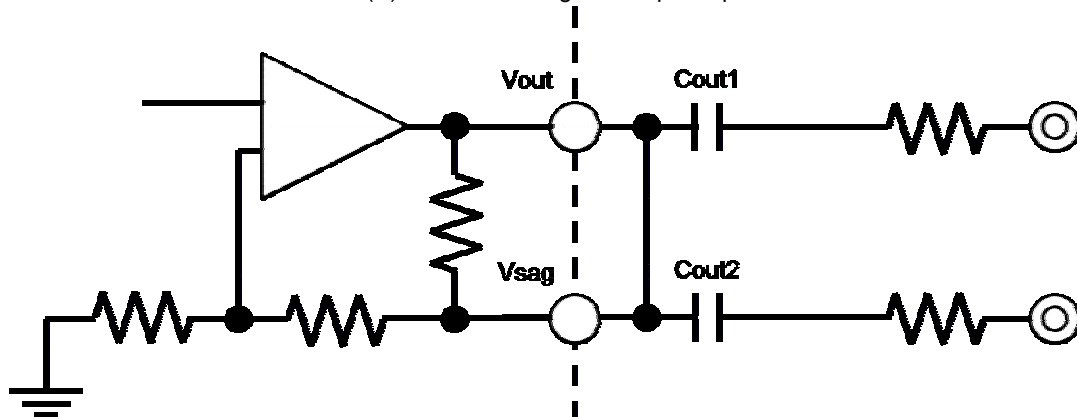
$$C_{out} = C_{out1} + C_{out2}$$

$$C_{out1} = C_{out2}$$

(A) In case of using one output capacitor



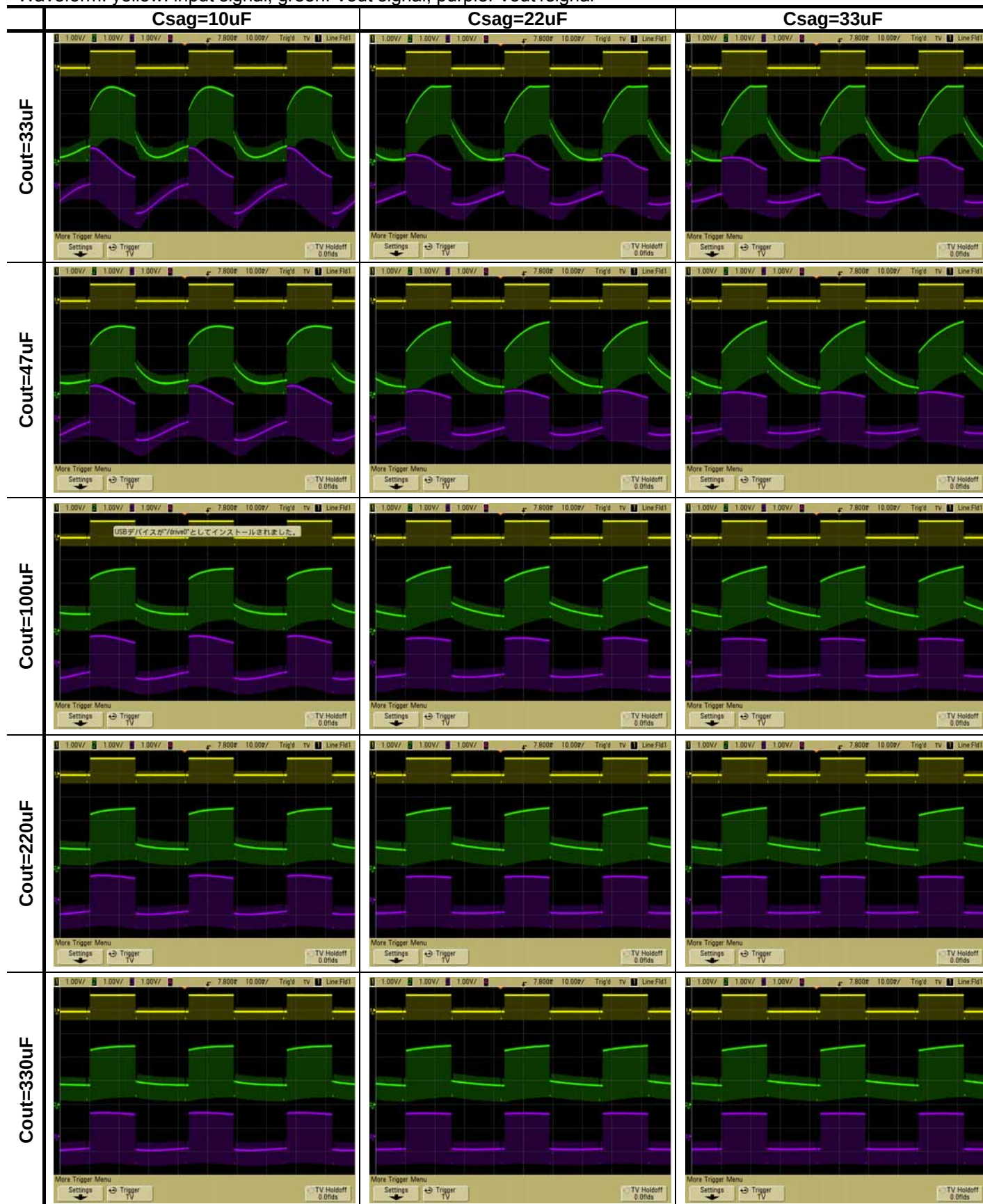
(B) In case of using two output capacitors



< Using SAG correction circuit >

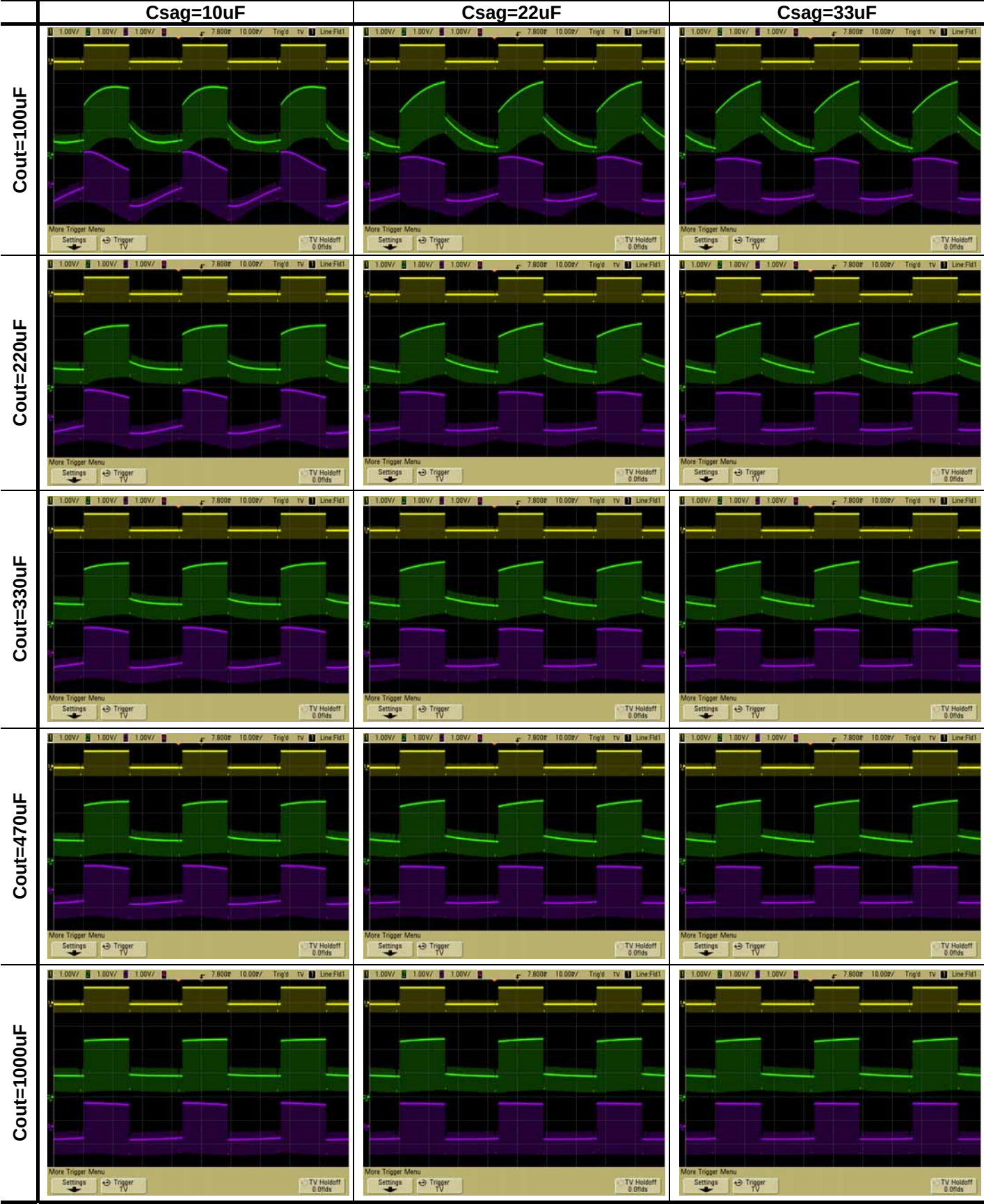
Input signal: bounce signal (IRE0%, IRE100%, 30Hz), resistance=150Ω

Waveform: yellow: input signal, green: Vout signal, purple: Vout1signal



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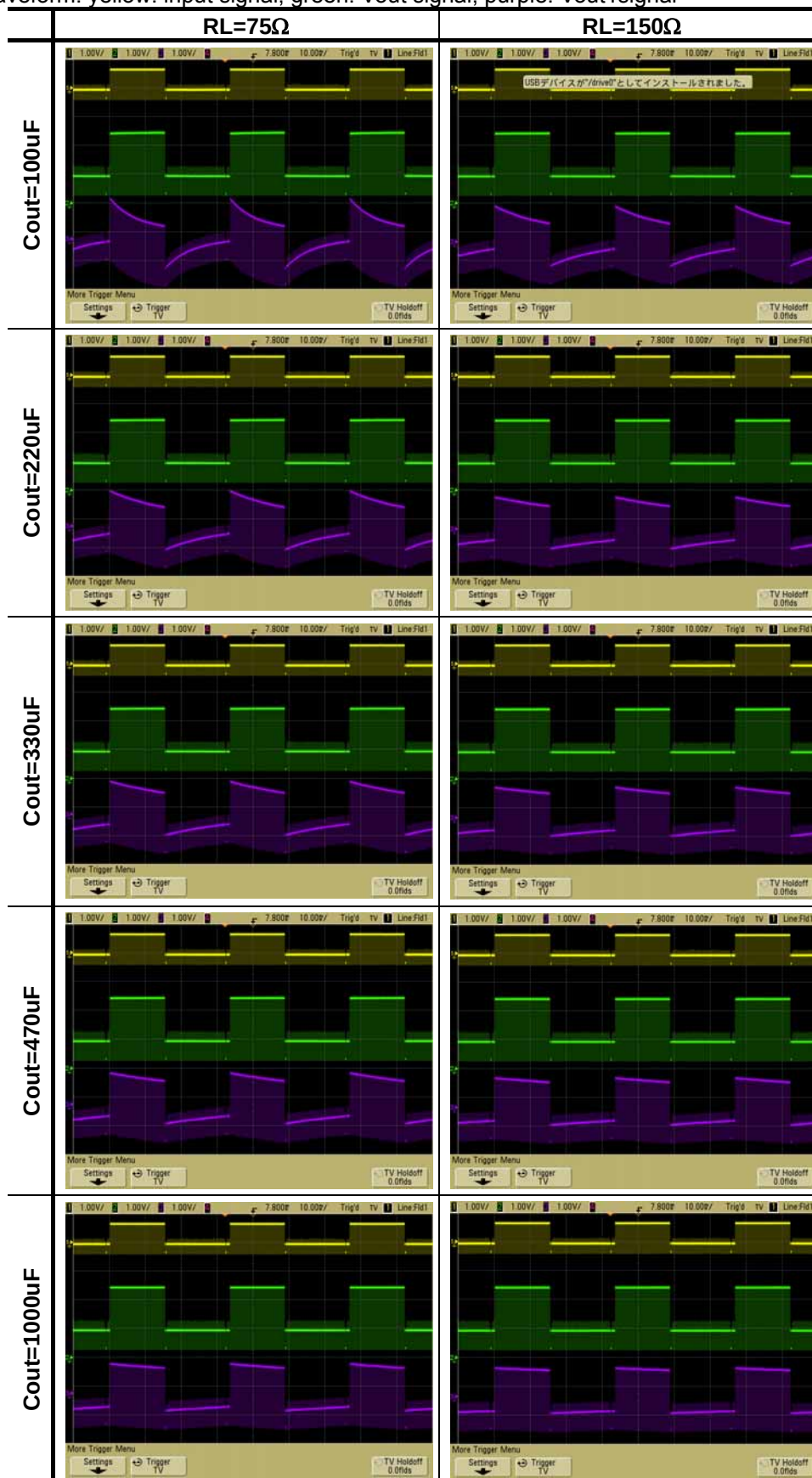
Input signal: bounce signal (IRE0%, IRE100%, 30Hz), resistance=150Ω
Waveform: yellow: input signal, green: Vout signal, purple: Vout1signal



< Not using SAG correction circuit >

Input signal: bounce signal (IRE0%, IRE100%, 30Hz), resistance=150Ω

Waveform: yellow: input signal, green: Vout signal, purple: Vout1signal

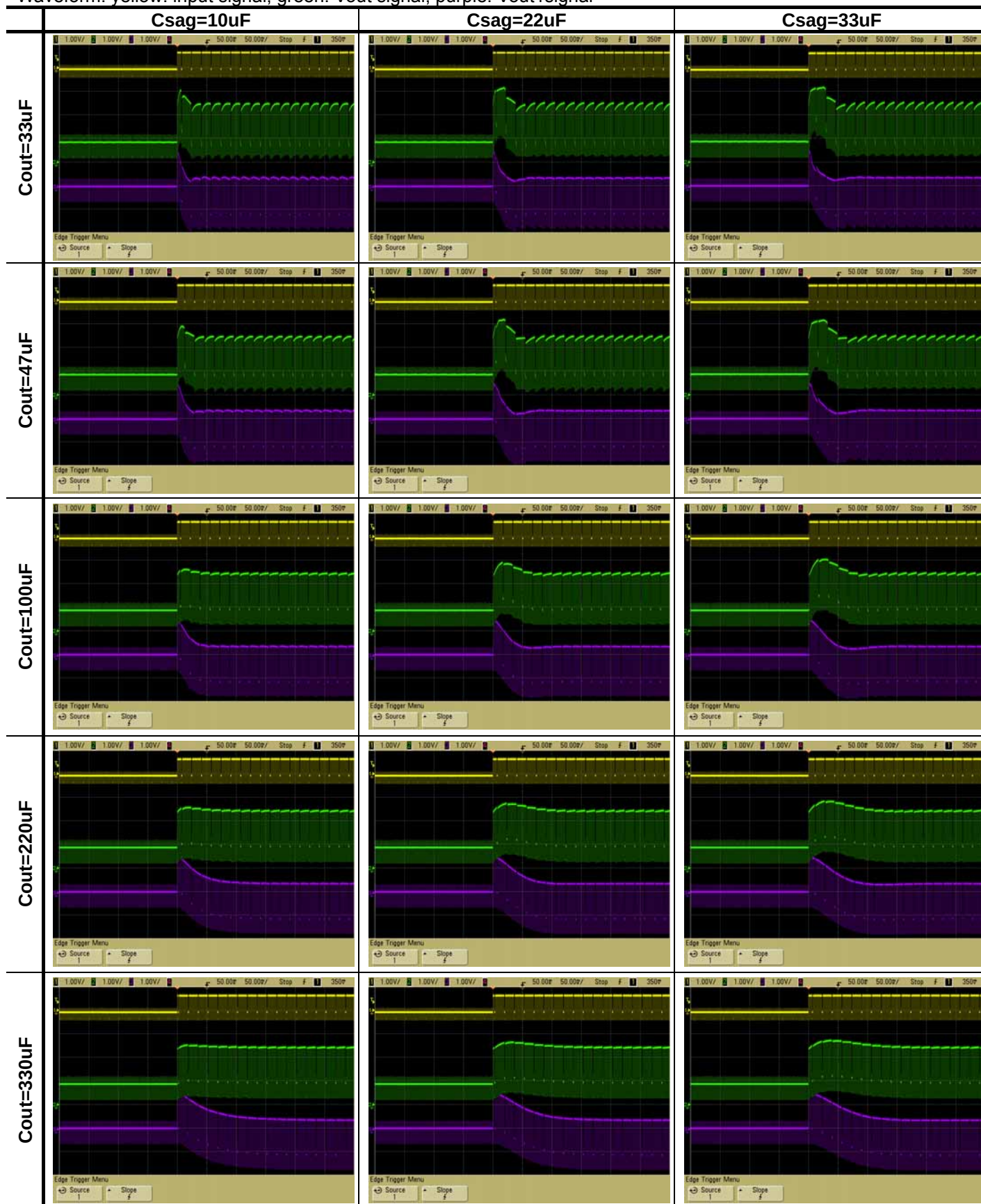


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< Using SAG correction circuit >

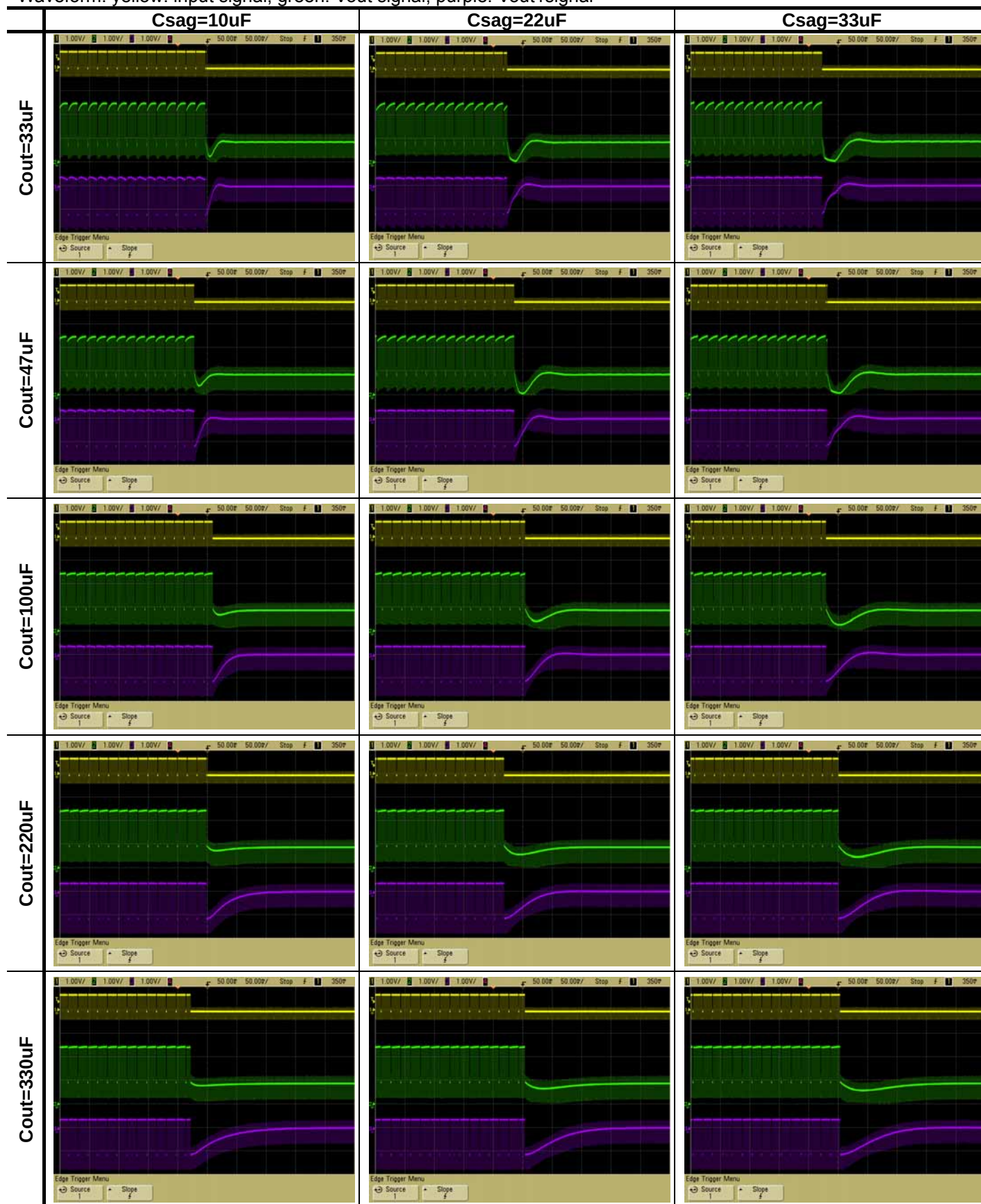
Input signal: Black to White100%, resistance150Ω

Waveform: yellow: input signal, green: Vout signal, purple: Vout1signal



Input signal: White100% to Black, resistance150Ω

Waveform: yellow: input signal, green: Vout signal, purple: Vout1signal

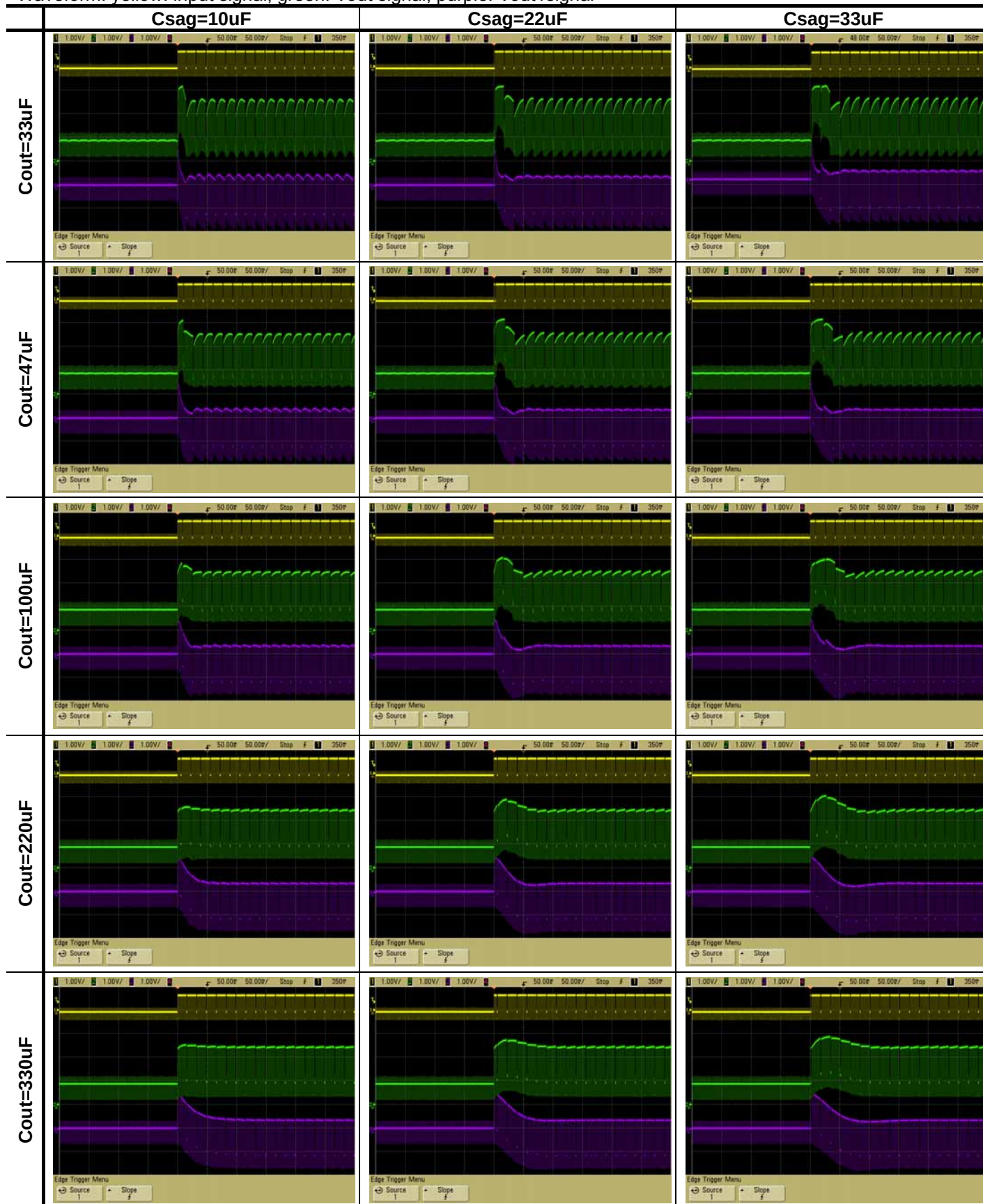


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< Using SAG correction circuit >

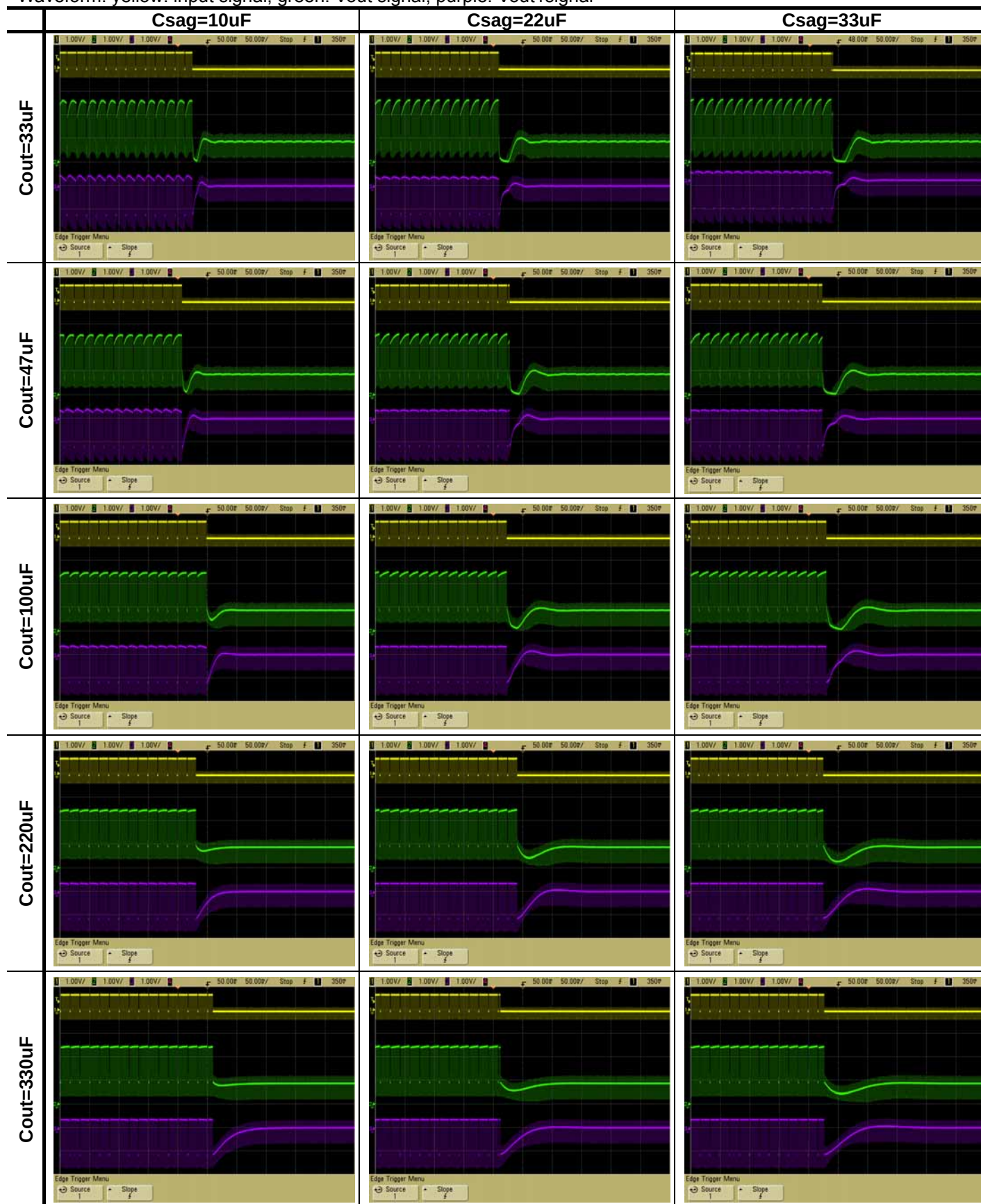
Input signal: Black to White 100%, resistance=75Ω

Waveform: yellow: input signal, green: Vout signal, purple: Vout1signal



Input signal: White100% to Black, resistance=75Ω

Waveform: yellow: input signal, green: Vout signal, purple: Vout1signal



◆Clamp circuit

1. Operation of Sync-tip-clamp

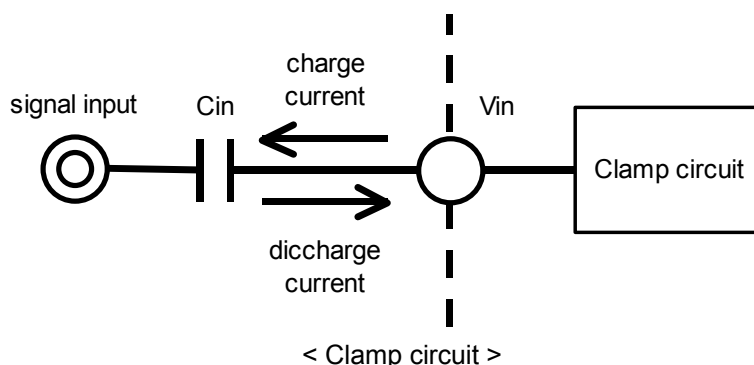
Input circuit will be explained. Sync-tip clamp circuit (below the clamp circuit) operates to keep a sync tip of the minimum potential of the video signal. Clamp circuit is a circuit of the capacitor charging and discharging of the external input C_{in} . It is charged to the capacitor to the external input C_{in} at sync tip of the video signal. Therefore, the potential of the sync tip is fixed.

And it is discharged charge by capacitor C_{in} at period other than the video signal sync tip. This is due to a small discharge current to the IC.

In this way, this clamp circuit is fixed sync tip of video signal to a constant potential from charging of C_{in} and discharging of C_{in} at every one horizontal period of the video signal.

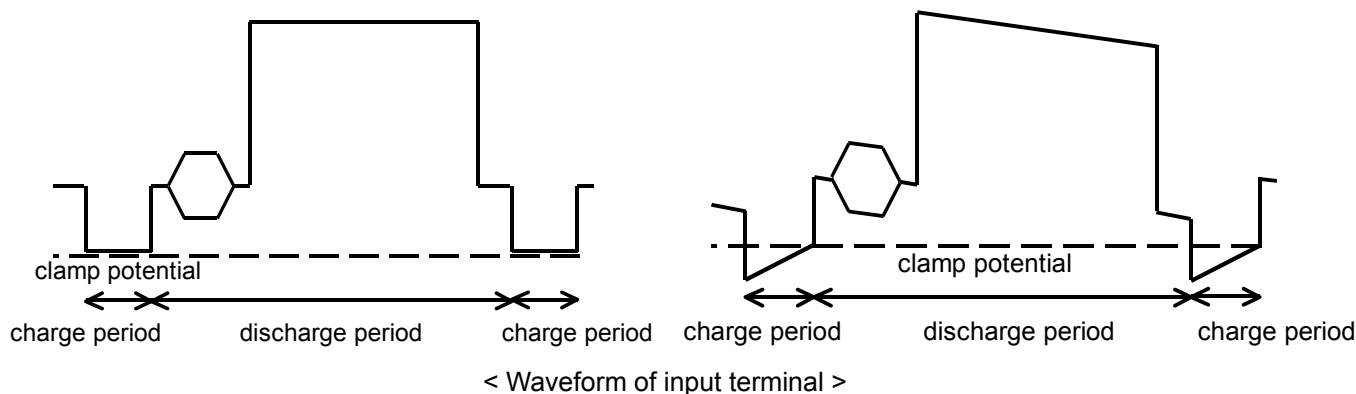
The minute current be discharged an electrical charge from the input capacitor at the period other than the sync tip of video signals. Decrease of voltage on discharge is dependent on the size of the input capacitor C_{in} .

If you decrease the value of the input capacitor, will cause distortion, called the H sag. Therefore, the input capacitor recommend on more than 0.1 μ F.



A. C_{in} is large

B. C_{in} is small (H sag experience)



2. Input impedance

The input impedance of the clamp circuit is different at the capacitor discharge period and the charge period.

The input impedance of the charging period is a few $k\Omega$. On the other hand, the input impedance of the discharge period is several $M\Omega$. Because is a small discharge-current through to the IC.

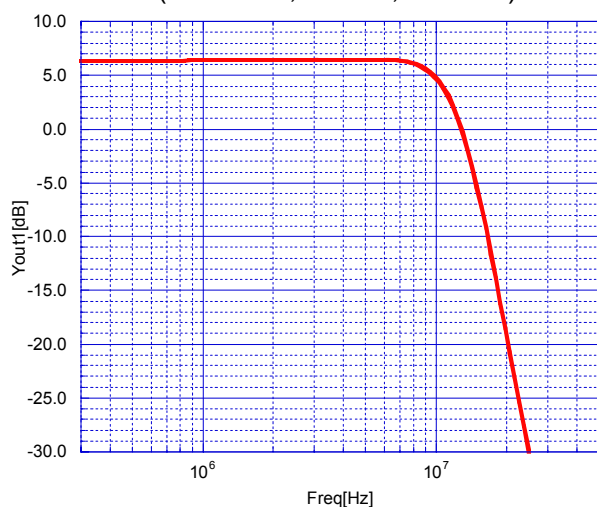
Thus the input impedance will vary depending on the operating state of the clamp circuit.

3. Impedance of signal source

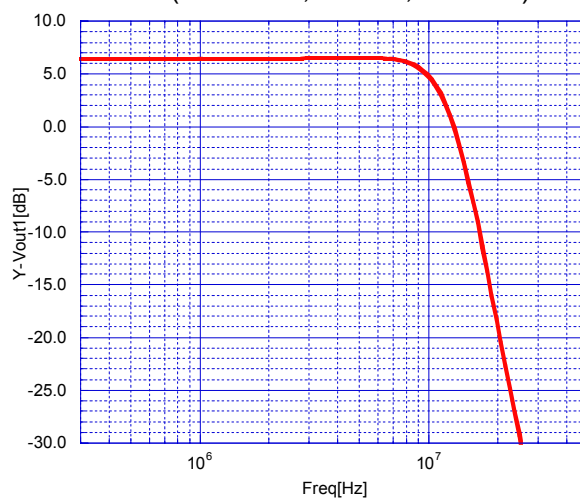
Source impedance to the input terminal, please lower than 200 Ω . A high source impedance, the signal may be distorted. If so, please to connect a buffer for impedance conversion.

TYPICAL CHARACTERISTICS

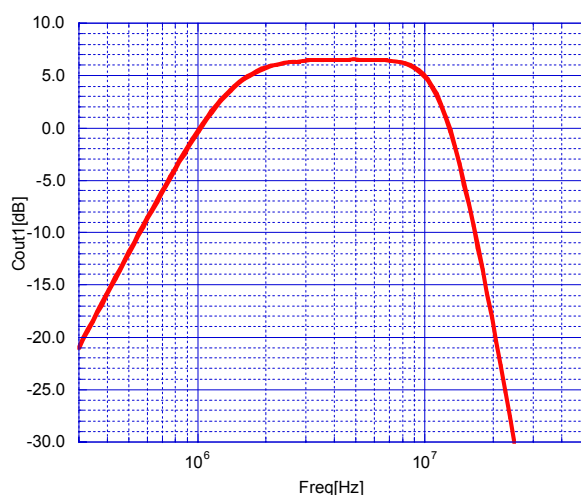
Voltage Gain vs. Frequency
($Y_{in} \rightarrow Y_{out}$, $V_{cc}=3V$, $T_a=25^\circ C$)



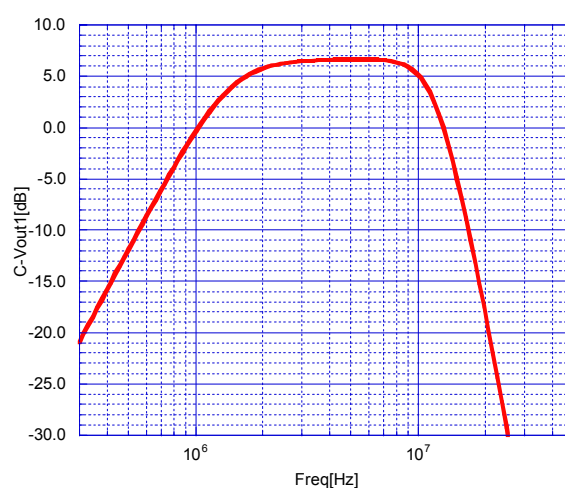
Voltage Gain vs. Frequency
($Y_{in} \rightarrow V_{out}$, $V_{cc}=3V$, $T_a=25^\circ C$)



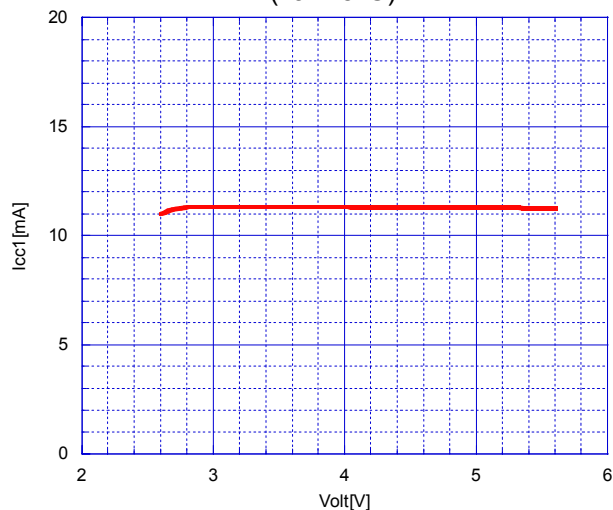
Voltage Gain vs. Frequency
($C_{in} \rightarrow C_{out}$, $V_{cc}=3V$, $T_a=25^\circ C$)



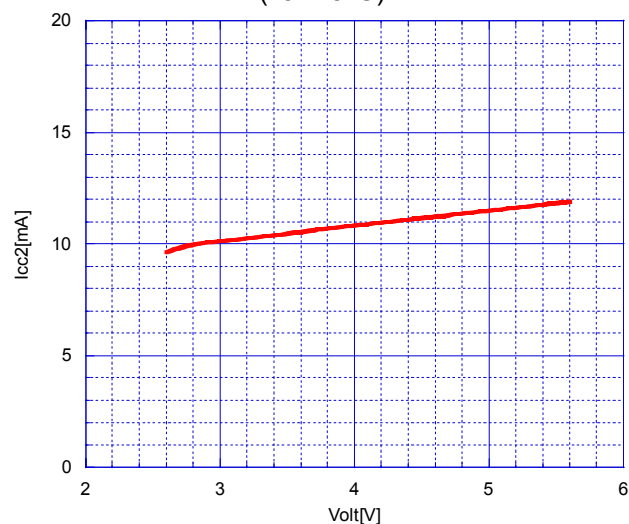
Voltage Gain vs. Frequency
($C_{in} \rightarrow V_{out}$, $V_{cc}=3V$, $T_a=25^\circ C$)



Operating Current1 vs. Operating Voltage
($T_a=25^\circ C$)

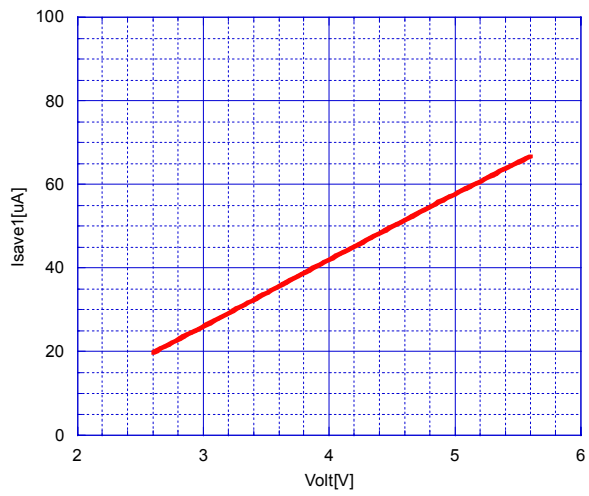


Operating Current2 vs. Operating Voltage
($T_a=25^\circ C$)

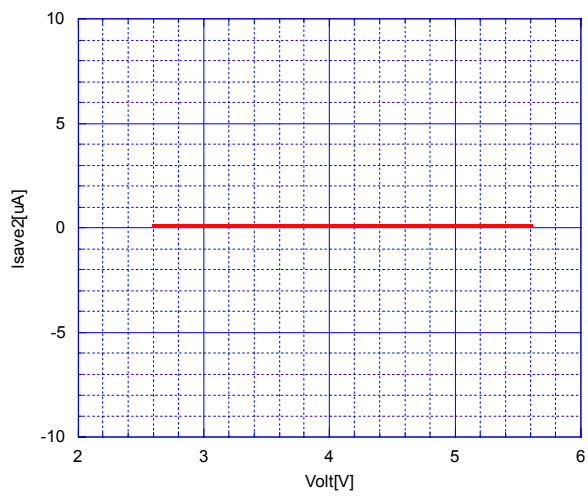


TYPYCAL CHARACTERISTICS

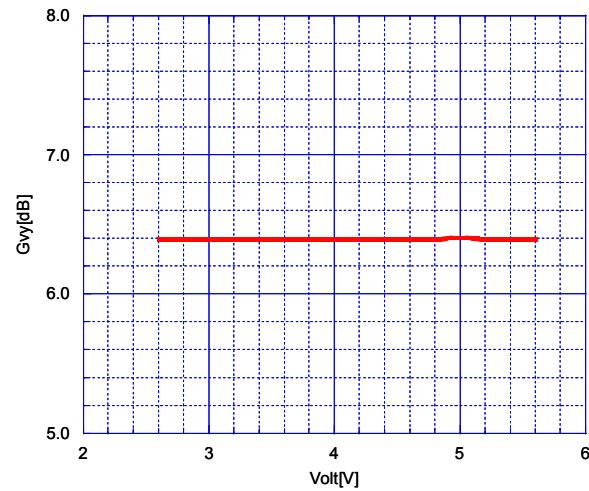
Operating Current at Power Save Mode1.
vs. Operating Voltage (Ta=25°C)



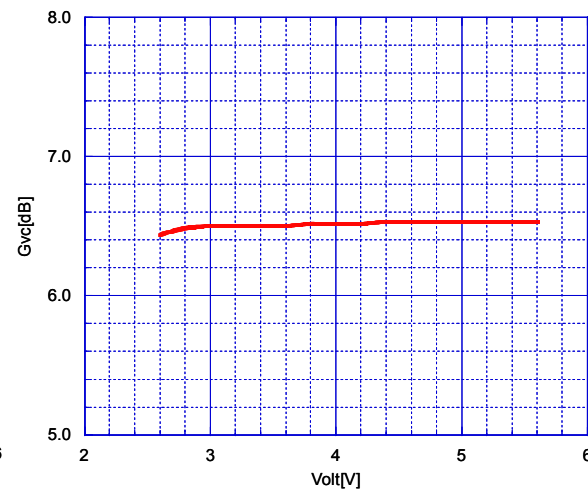
Operating Current at Power Save Mode2
vs. Operating Voltage (Ta=25°C)



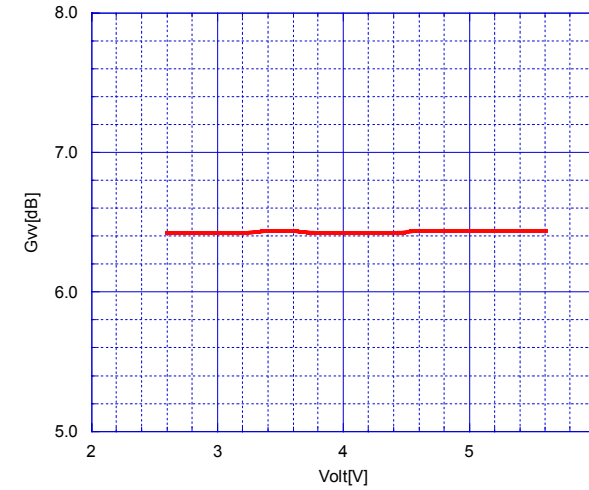
Voltage Gain(Y mode) vs. Operating Voltage
(Ta=25°C)



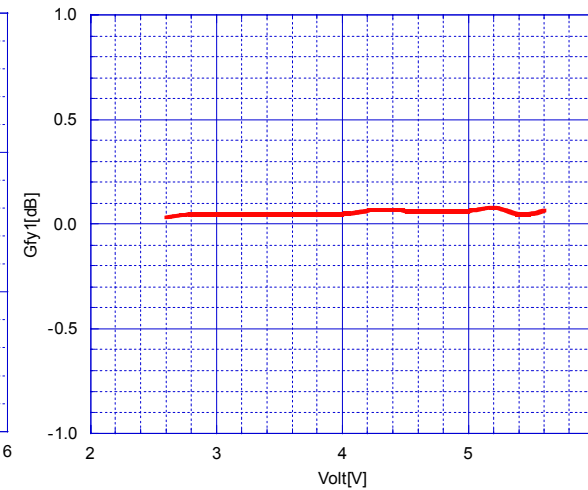
Voltage Gain(C mode) vs. Operating Voltage
(Ta=25°C)



Voltage Gain(V mode) vs. Operating Voltage
(Ta=25°C)

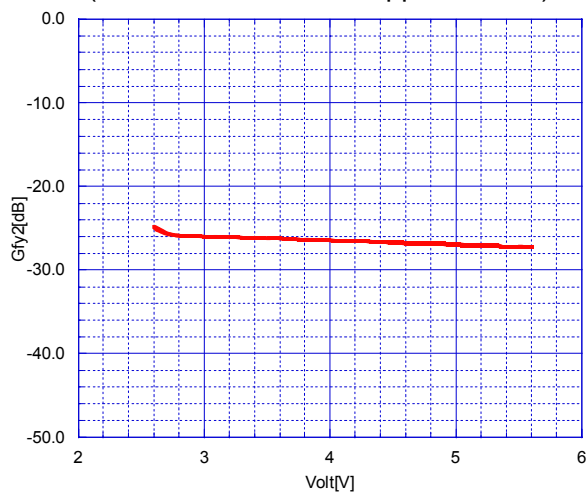


Frequency vs. Operating Voltage
(Yin=6MHz/100kHz, 1Vpp, Ta=25°C)

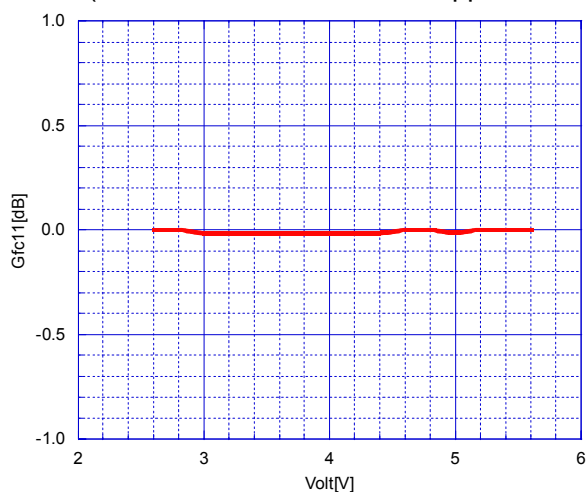


TYPICAL CHARACTERISTICS

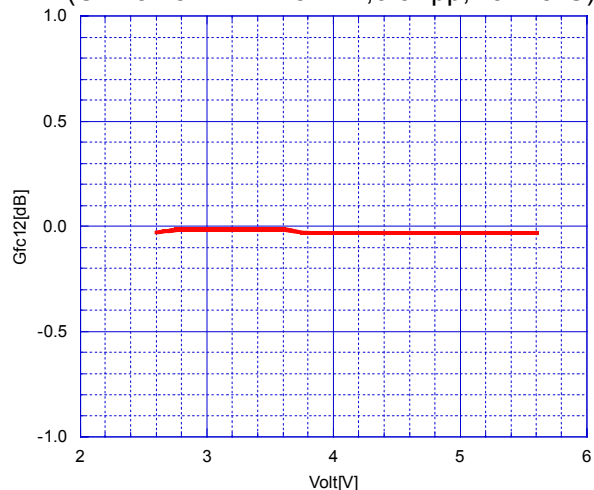
Frequency vs. Operating Voltage
(Yin=20MHz/100kHz, 1Vpp, Ta=25°C)



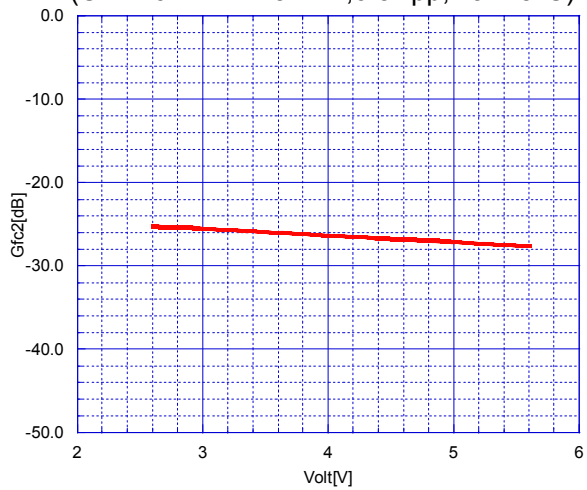
Frequency vs. Operating Voltage
(Cin=3.43MHz/4.43MHz, 0.3Vpp, Ta=25°C)



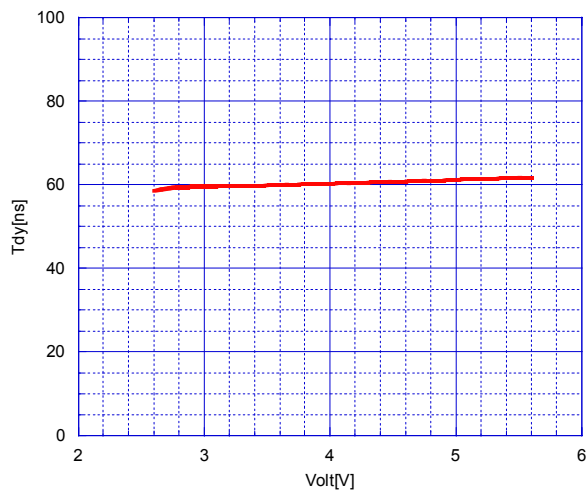
Frequency vs. Operating Voltage
(Cin=5.43MHz/4.43MHz, 0.3Vpp, Ta=25°C)



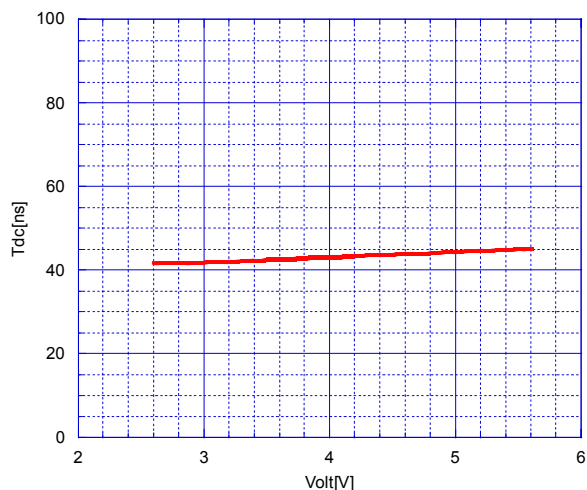
Frequency vs. Operating Voltage
(Cin=20MHz/4.43MHz, 0.3Vpp, Ta=25°C)



Group Delay(Y mode) vs. Operating Voltage
(Ta=25°C)

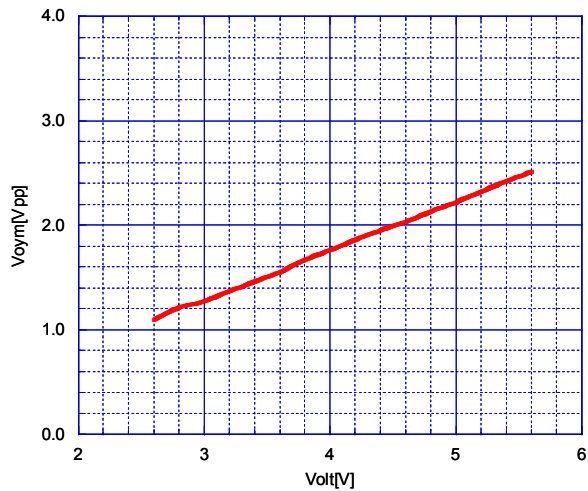


Group Delay(C mode) vs. Operating Voltage
(Ta=25°C)

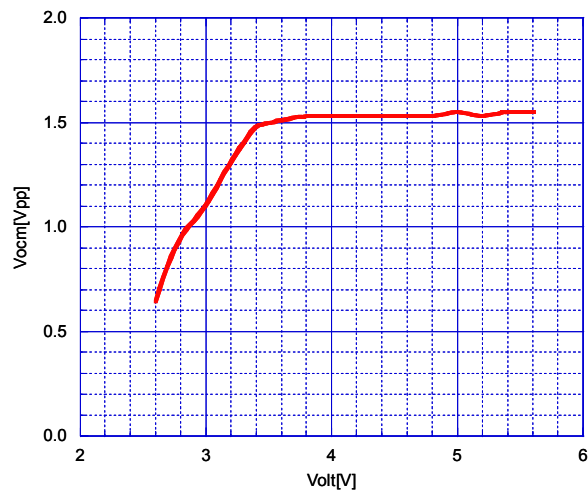


TYPICAL CHARACTERISTICS

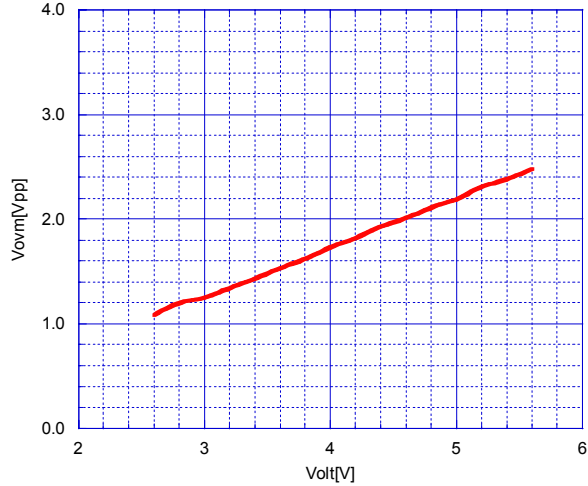
Maximum Output Voltage vs. Operating Voltage
(Yin→Yout, Ta=25°C)



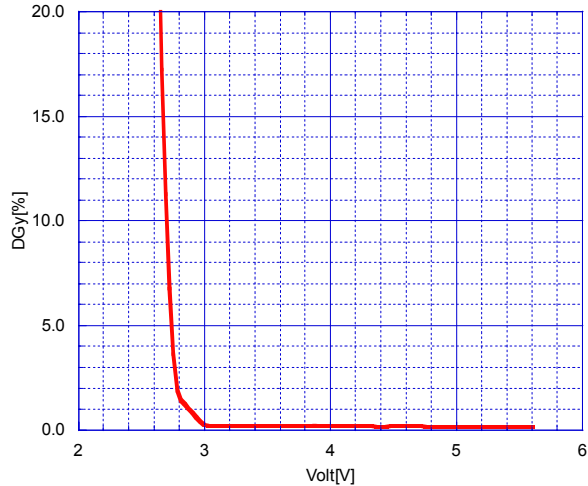
Maximum Output Voltage vs. Operating Voltage
(Cin→Cout, Ta=25°C)



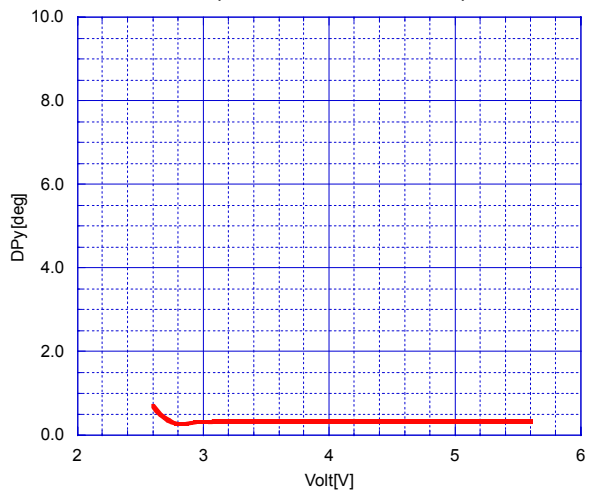
Maximum Output Voltage vs. Operating Voltage
(Yin→Vout, Ta=25°C)



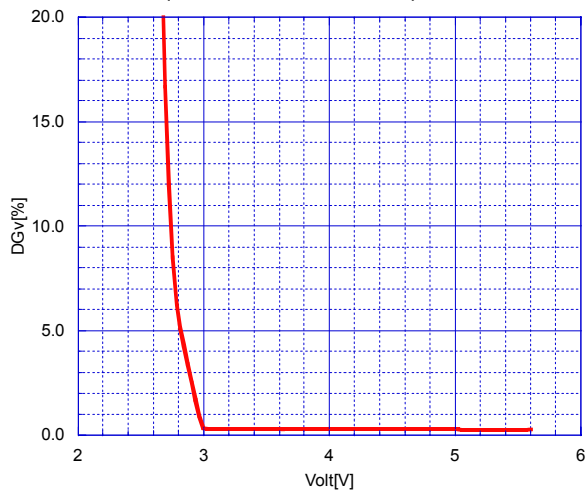
Differential Gain vs. Operating Voltage
(Yin→Yout, Ta=25°C)



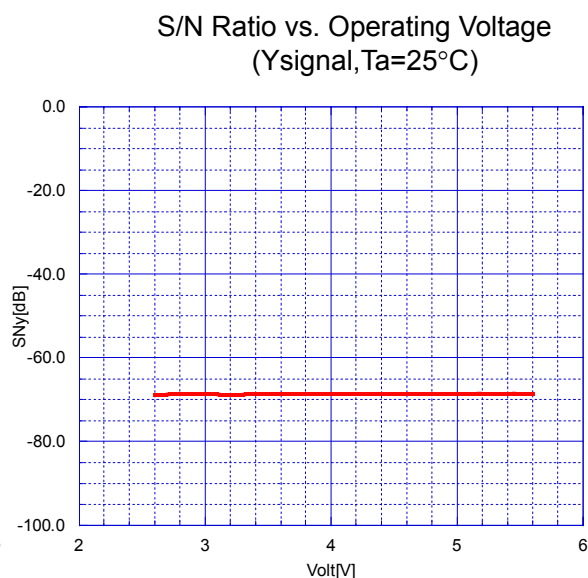
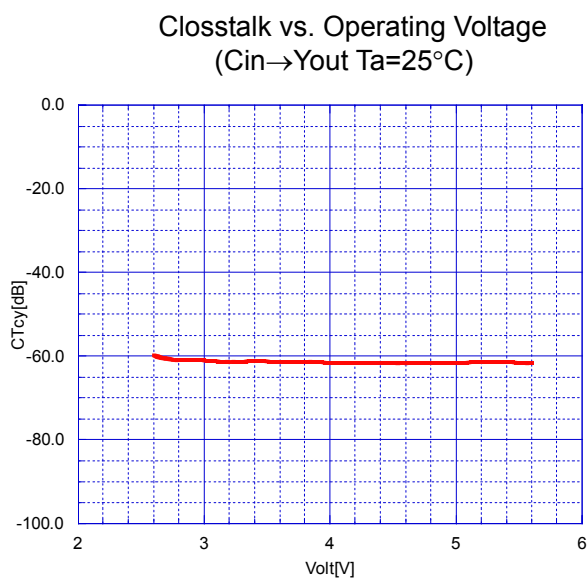
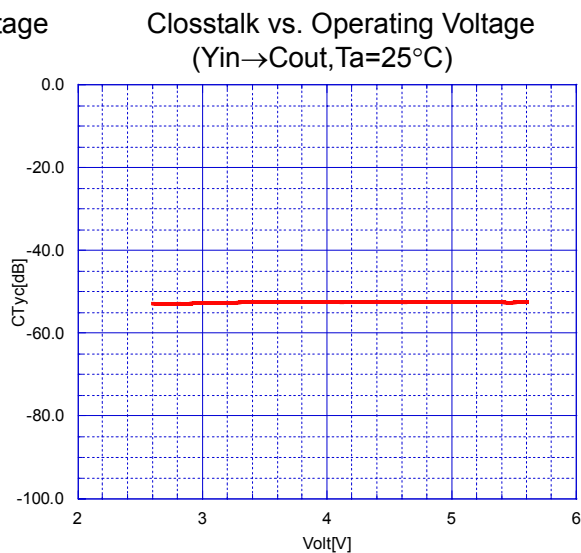
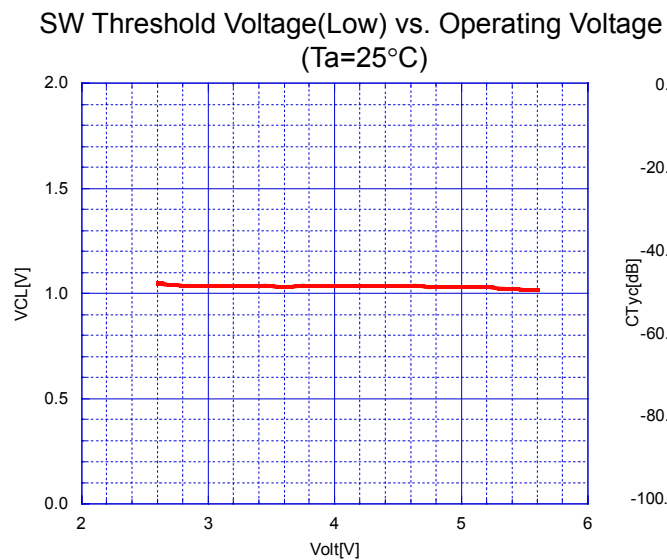
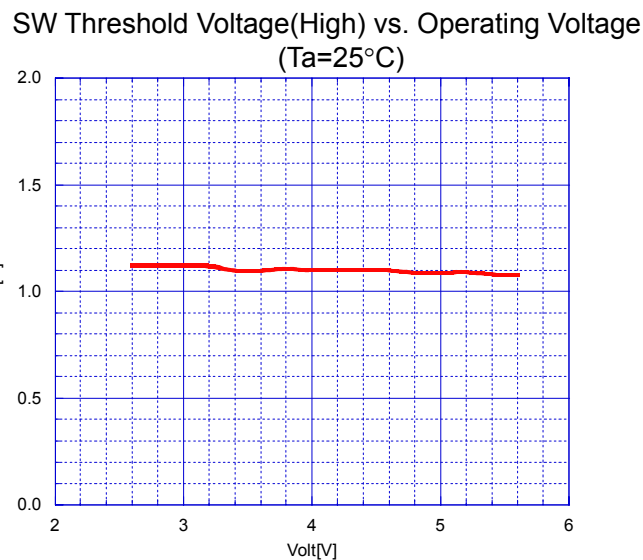
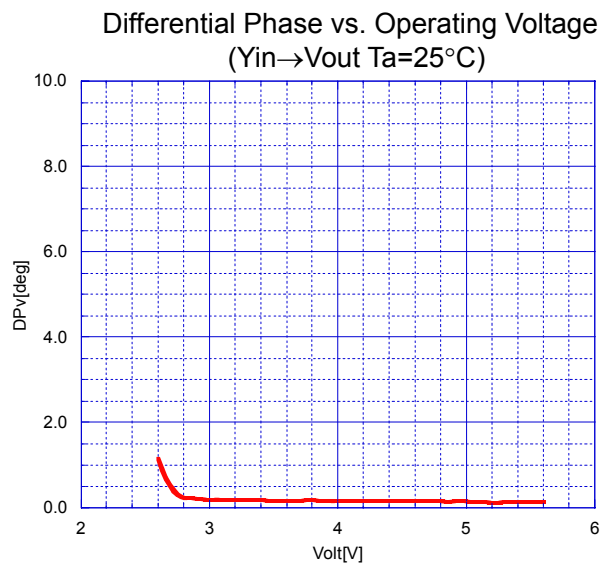
Differential Phase vs. Operating Voltage
(Yin→Yout, Ta=25°C)



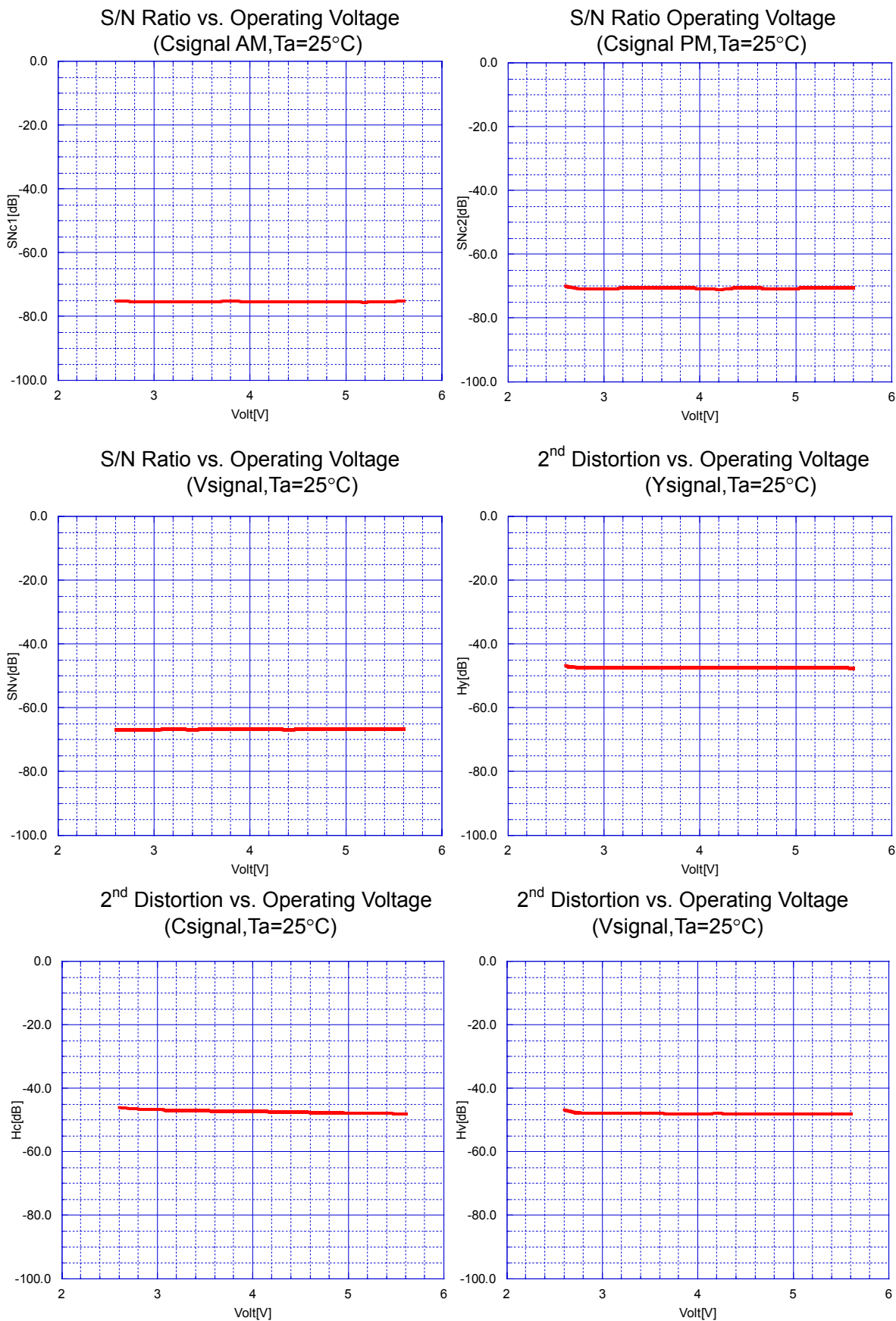
Differential Gain vs. Operating Voltage
(Yin→Vout, Ta=25°C)



TYPICAL CHARACTERISTICS

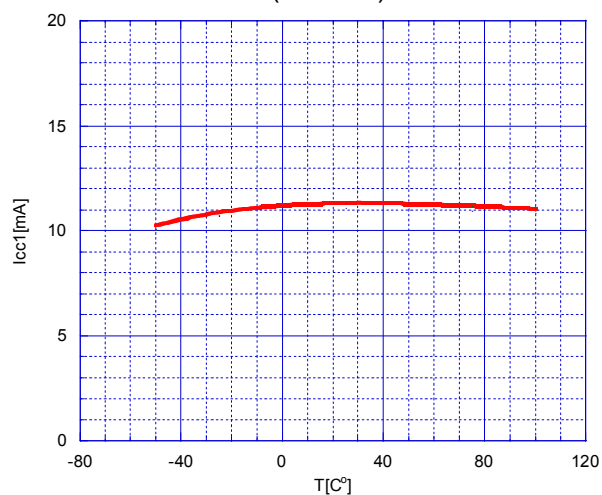


TYPICAL CHARACTERISTICS

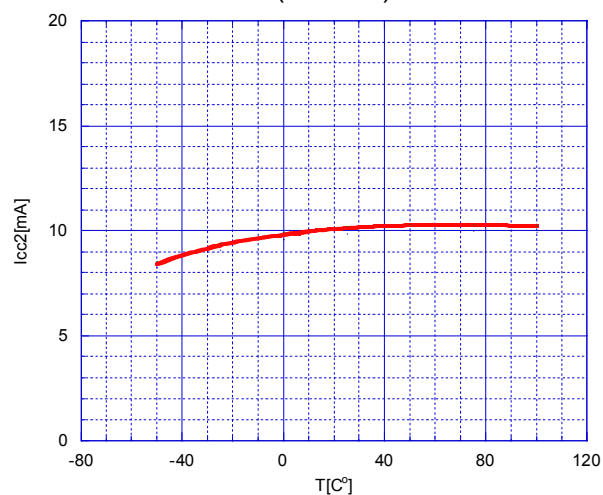


TYPICAL CHARACTERISTICS

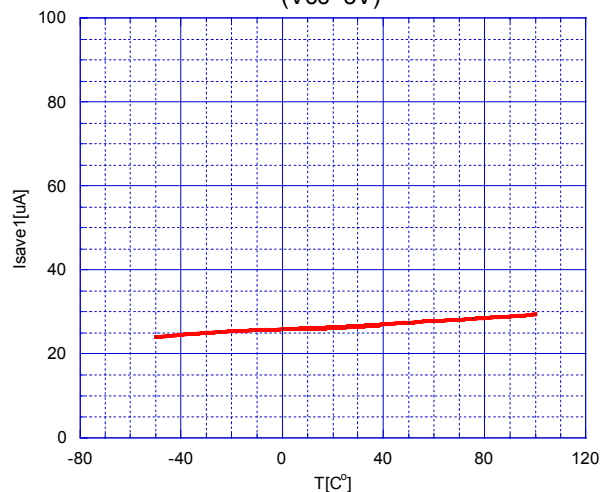
Operating Current1 vs. Temperature
(Vcc=3V)



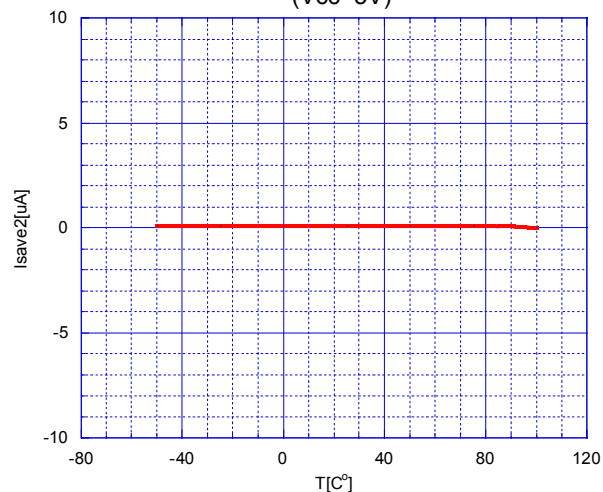
Operating Current2 vs. Temperature
(Vcc=3V)



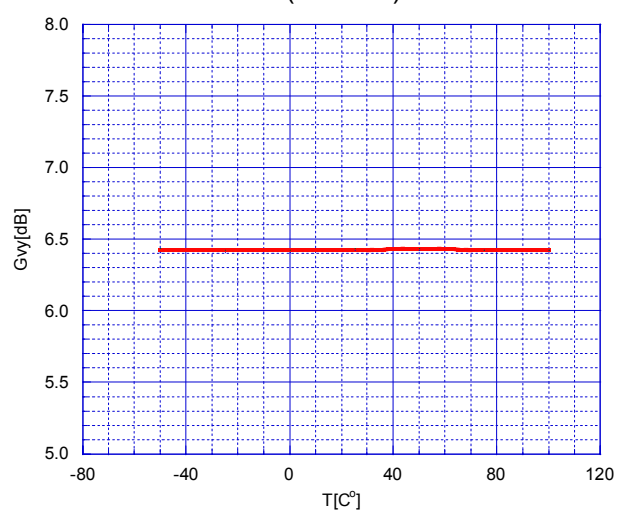
Operating Current1 at Power Save mode vs. Temperature
(Vcc=3V)



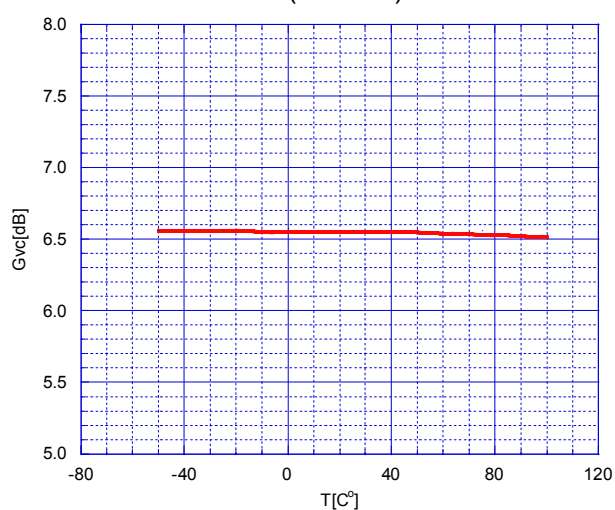
Operating Current2 at Power Save Mode vs. Temperature
(Vcc=3V)



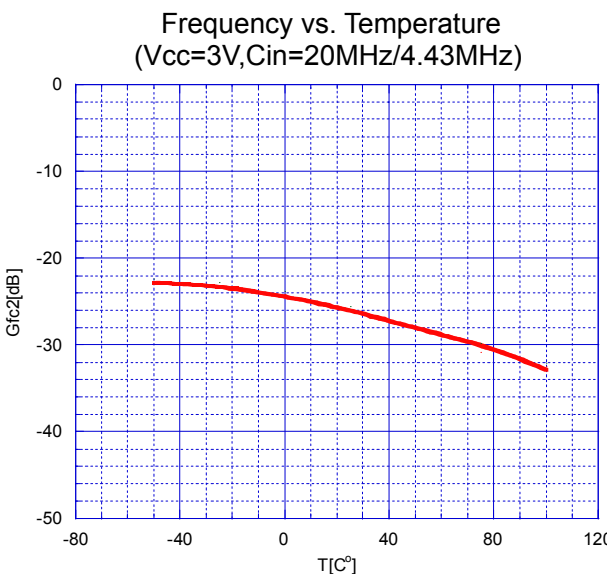
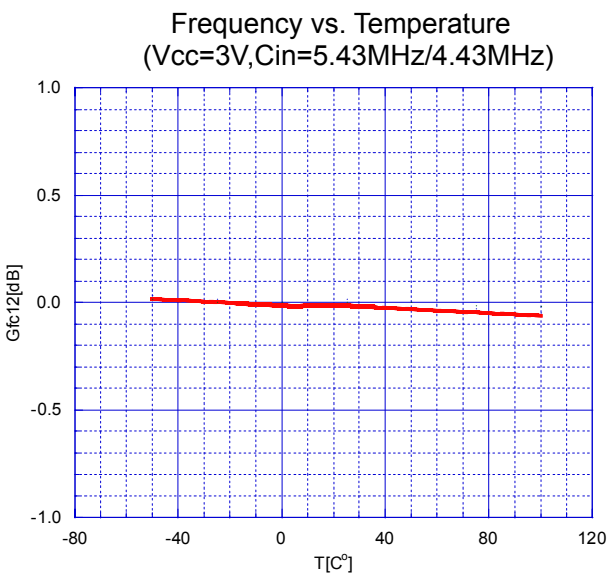
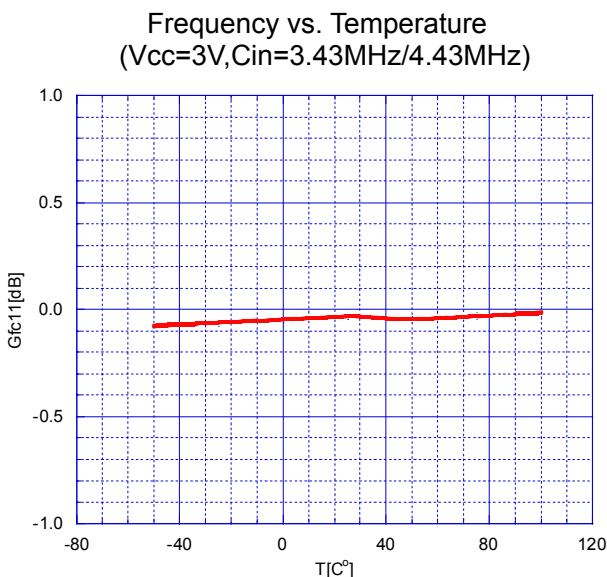
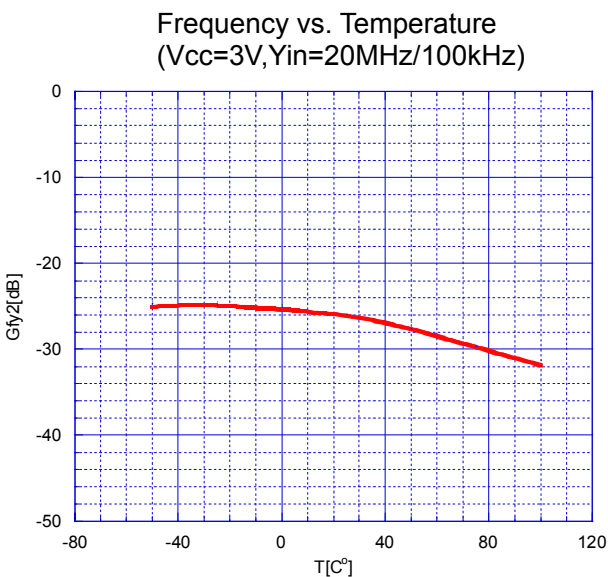
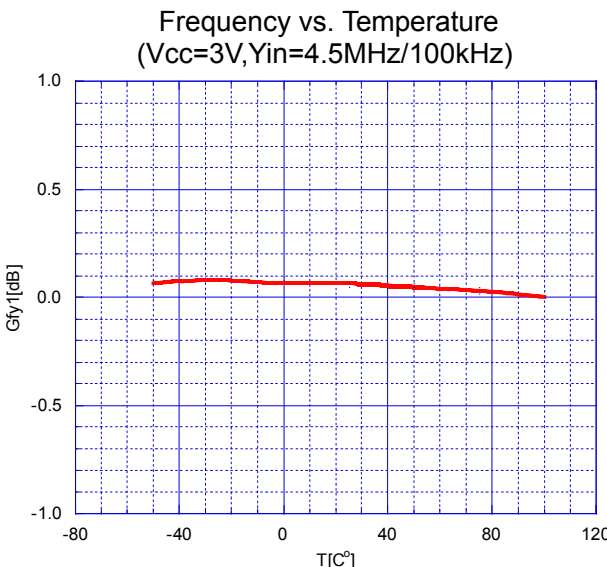
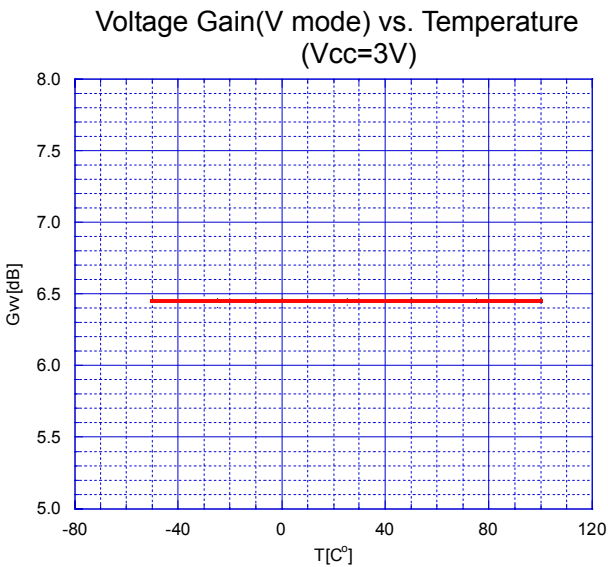
Voltage Gain(Y mode) vs. Temperature
(Vcc=3V)



Voltage Gain(C mode) vs. Temperature
(Vcc=3V)

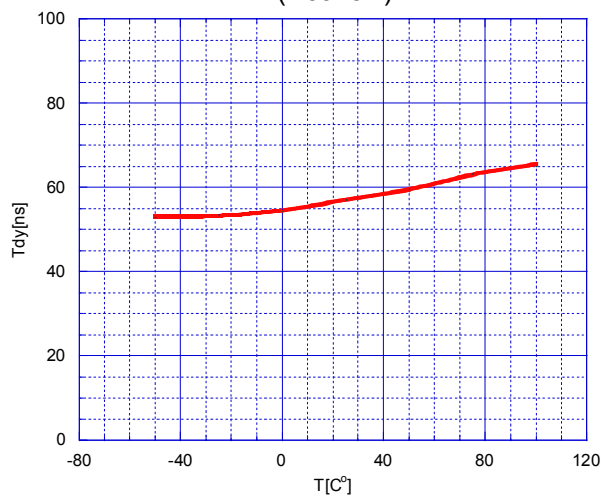


TYPICAL CHARACTERISTICS

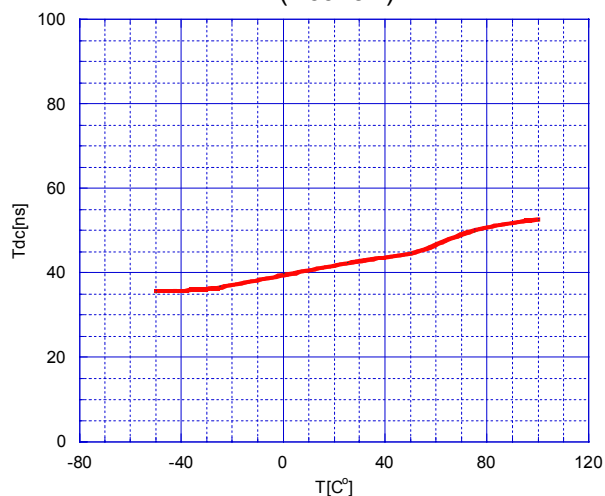


TYPICAL CHARACTERISTICS

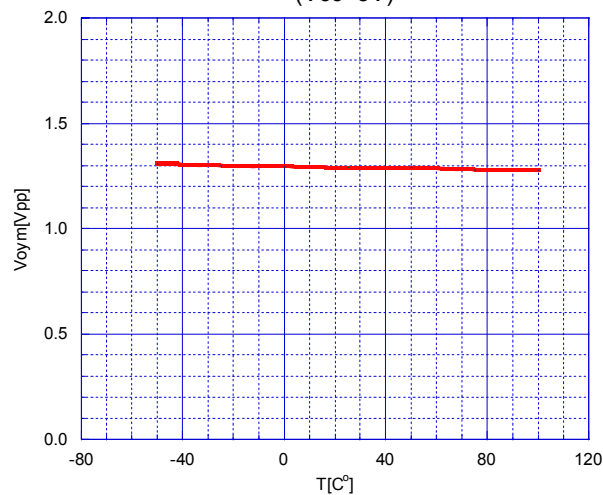
Group Delay (Y mode) vs. Temperature
(Vcc=3V)



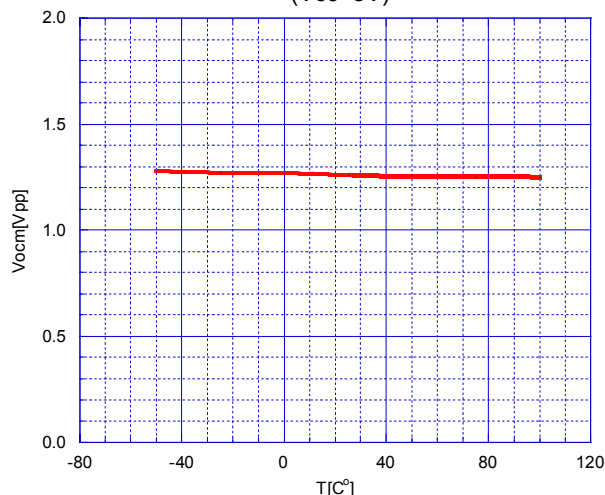
Group Delay(C mode) vs. Temperature
(Vcc=3V)



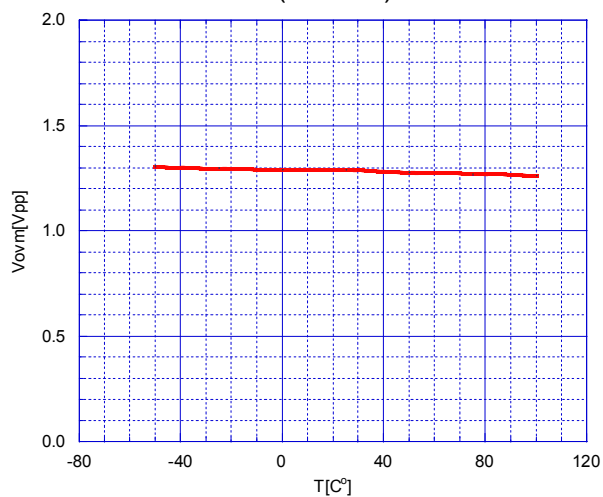
Maximum Output Voltage(Y mode) vs. Temperature
(Vcc=3V)



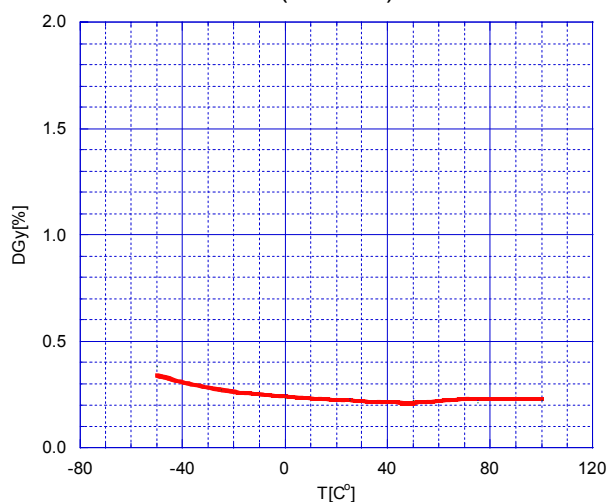
Maximum Output Voltage(Y mode) vs. Temperature
(Vcc=3V)



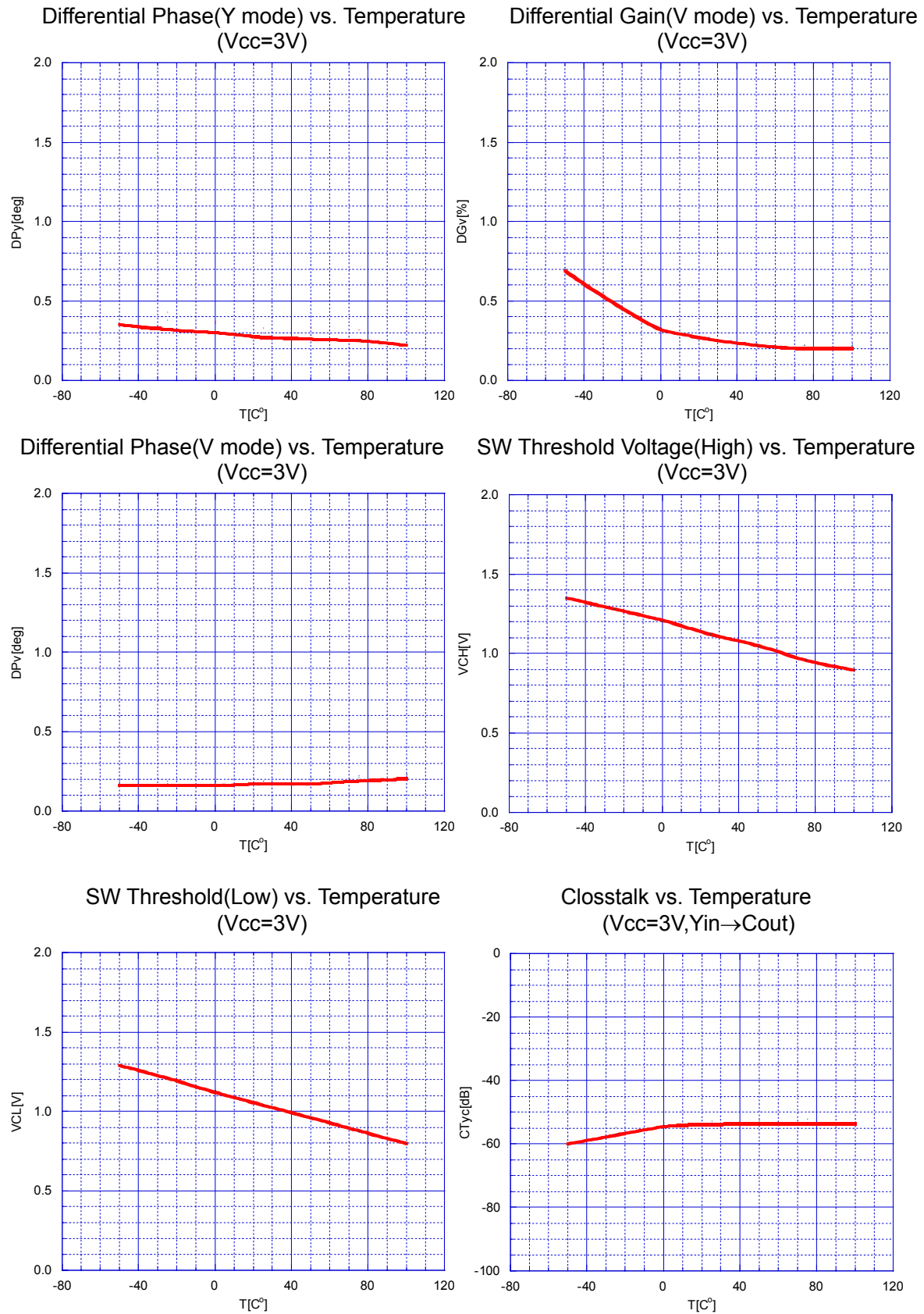
Maximum Output Voltage(V mode) vs. Temperature
(Vcc=3V)



Differential Gain(Y mode) vs. Temperature
(Vcc=3V)

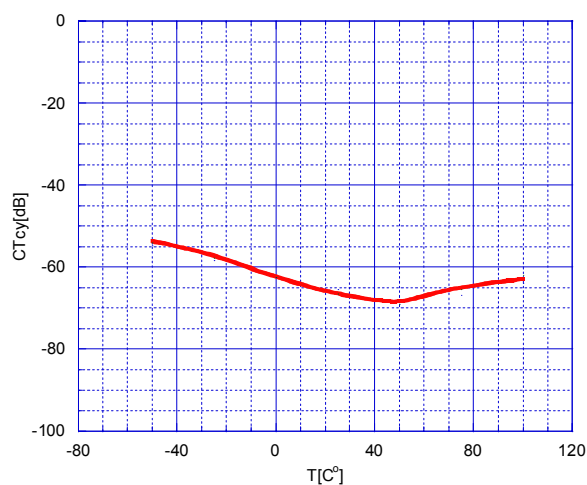


TYPICAL CHARACTERISTICS

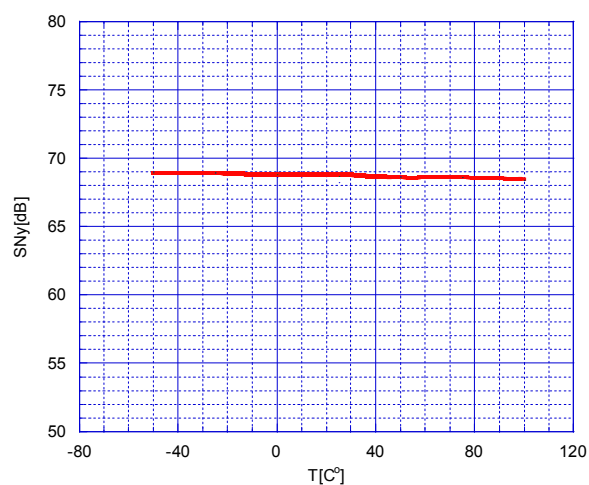


TYPICAL CHARACTERISTICS

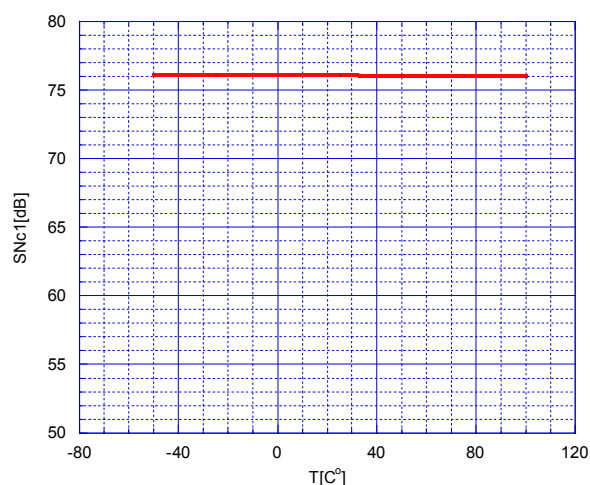
Crosstalk vs. Temperature
(Vcc=3V, Cin→Yout)



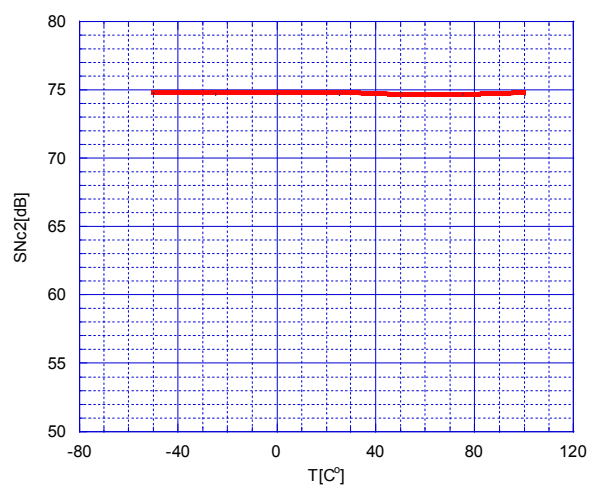
S/N Ratio vs. Temperature
(Vcc=3V, Ysignal)



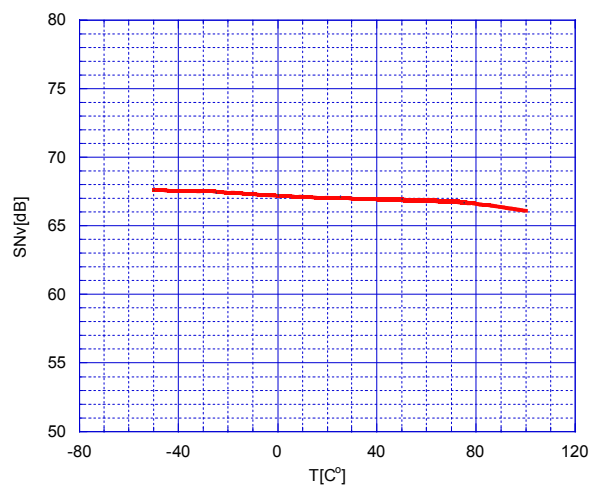
S/N Ratio vs. Temperature
(Vcc=3V, Csignal AM)



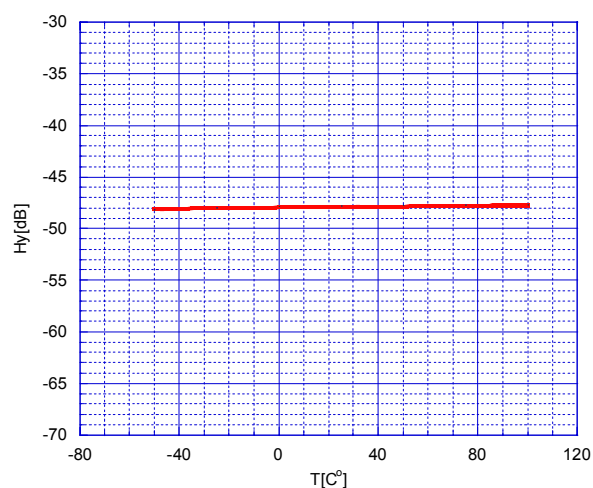
S/N Ratio vs. Temperature
(Vcc=3V, Csignal PM)



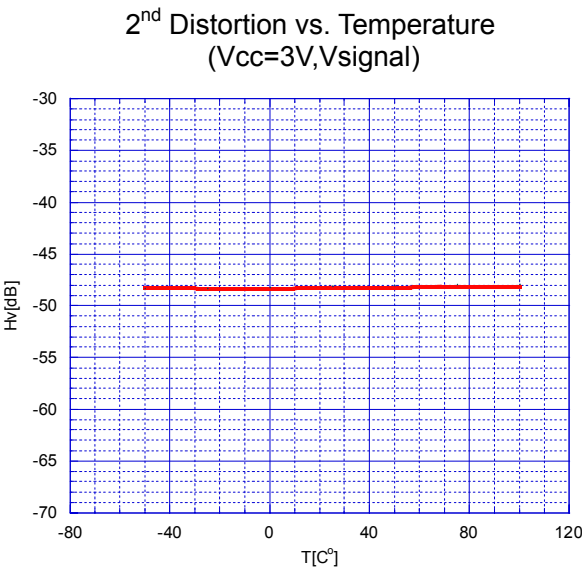
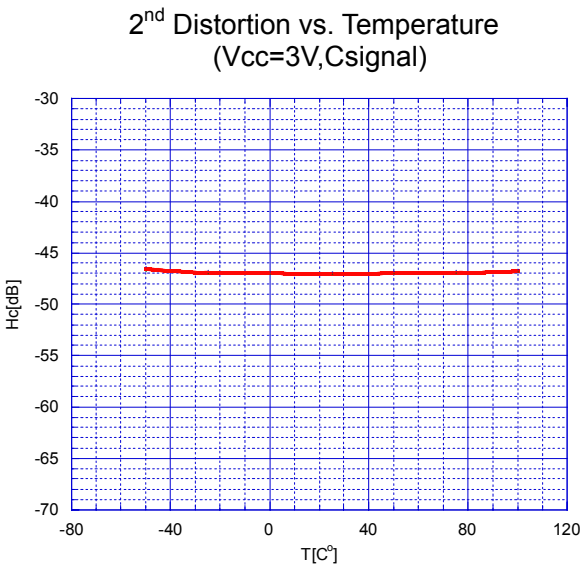
S/N Ratio vs. Temperature
(Vcc=3V, Vsignal)



2nd Distortion vs. Temperature
(Vcc=3V, Ysignal)



■TYPYCAL CHARACTERISTICS



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