

# SN5473, SN54LS73A, SN7473, SN74LS73A DUAL J-K FLIP-FLOPS WITH CLEAR

SDLS118 – DECEMBER 1983 – REVISED MARCH 1988

- Package Options Include Plastic "Small Outline" Packages, Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

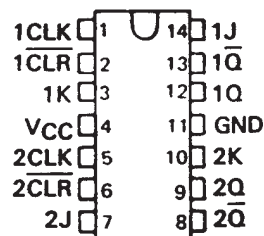
## description

The '73, and 'H73, contain two independent J-K flip-flops with individual J-K, clock, and direct clear inputs. The '73, and 'H73, are positive pulse-triggered flip-flops. J-K input is loaded into the master while the clock is high and transferred to the slave on the high-to-low transition. For these devices the J and K inputs must be stable while the clock is high.

The 'LS73A contains two independent negative-edge-triggered flip-flops. The J and K inputs must be stable one setup time prior to the high-to-low clock transition for predictable operation. When the clear is low, it overrides the clock and data inputs forcing the Q output low and the  $\bar{Q}$  output high.

The SN5473, SN54H73, and the SN54LS73A are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN7473, and the SN74LS73A are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN5473, SN54LS73A . . . J OR W PACKAGE  
SN7473 . . . N PACKAGE  
SN74LS73A . . . D OR N PACKAGE  
(TOP VIEW)



'73  
FUNCTION TABLE

| INPUTS |              |   |   | OUTPUTS |             |
|--------|--------------|---|---|---------|-------------|
| CLR    | CLK          | J | K | Q       | $\bar{Q}$   |
| L      | X            | X | X | L       | H           |
| H      | $\downarrow$ | L | L | $Q_0$   | $\bar{Q}_0$ |
| H      | $\downarrow$ | H | L | H       | L           |
| H      | $\downarrow$ | L | H | L       | H           |
| H      | $\downarrow$ | H | H | TOGGLE  | TOGGLE      |

'LS73A  
FUNCTION TABLE

| INPUTS |              |   |   | OUTPUTS |             |
|--------|--------------|---|---|---------|-------------|
| CLR    | CLK          | J | K | Q       | $\bar{Q}$   |
| L      | X            | X | X | L       | H           |
| H      | $\downarrow$ | L | L | $Q_0$   | $\bar{Q}_0$ |
| H      | $\downarrow$ | H | L | H       | L           |
| H      | $\downarrow$ | L | H | L       | H           |
| H      | $\downarrow$ | H | H | TOGGLE  | TOGGLE      |
| H      | H            | X | X | $Q_0$   | $\bar{Q}_0$ |

FOR CHIP CARRIER INFORMATION,  
CONTACT THE FACTORY

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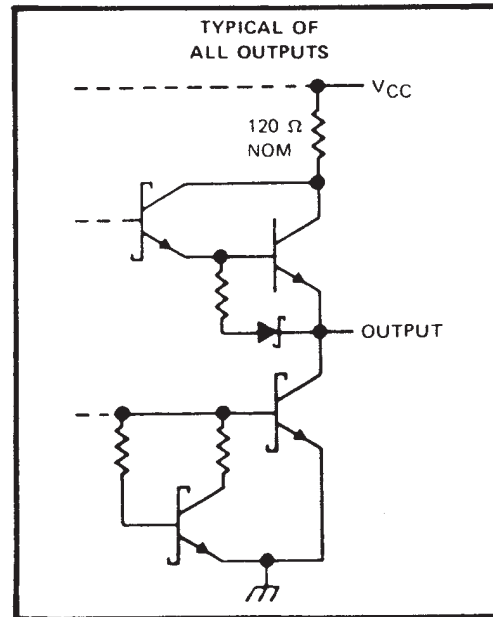
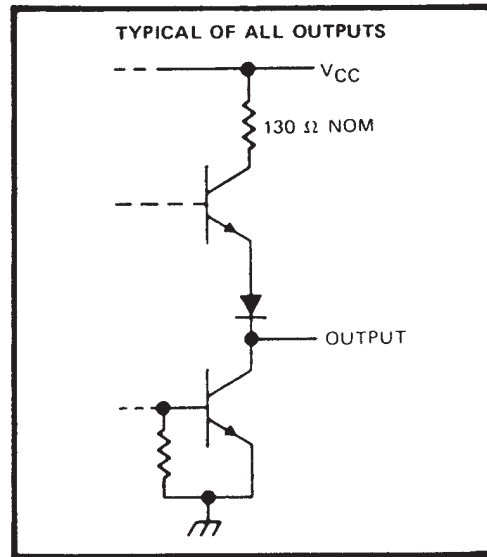
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## logic symbols†



†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

## schematics of inputs and outputs



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## logic diagrams (positive logic)



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

|   |                |
|---|----------------|
| Supply voltage, $V_{CC}$ (See Note 1) .....       | 7 V            |
| Input voltage: '73 .....                          | 5.5 V          |
| 'LS73A .....                                      | 7 V            |
| Operating free-air temperature range: SN54' ..... | -55°C to 125°C |
| SN74' .....                                       | 0°C to 70°C    |
| Storage temperature range .....                   | -65°C to 150°C |

NOTE 1: Voltage values are with respect to network ground terminal.



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# SN5473, SN54LS73A, SN7473, SN74LS73A DUAL J-K FLIP-FLOPS WITH CLEAR

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## recommended operating conditions

|          |   | SN5473               |     |      | SN7473 |     |      | UNIT |             |
|----------|---|----------------------|-----|------|--------|-----|------|------|-------------|
|          |   | MIN                  | NOM | MAX  | MIN    | NOM | MAX  |      |             |
| $V_{CC}$ | Supply voltage                              | 4.5                  | 5   | 5.5  | 4.75   | 5   | 5.25 | V    |             |
| $V_{IH}$ | High-level input voltage                    | 2                    |     |      | 2      |     |      | V    |             |
| $V_{IL}$ | Low-level input voltage                     |                      |     | 0.8  |        |     | 0.8  | V    |             |
| $I_{OH}$ | High-level output current                   |                      |     | -0.4 |        |     | -0.4 | mA   |             |
| $I_{OL}$ | Low-level output current                    |                      |     | 16   |        |     | 16   | mA   |             |
| $t_w$    | Pulse duration                              | CLK high             |     | 20   |        |     | 20   | ns   |             |
|          |   | CLK low              |     | 47   |        |     | 47   |      |             |
|          |   | $\overline{CLR}$ low |     | 25   |        |     | 25   |      |             |
| $t_{su}$ | Input setup time before CLK $\uparrow$      |                      |     | 0    |        |     | 0    | ns   |             |
| $t_h$    | Input hold time data after CLK $\downarrow$ |                      |     | 0    |        |     | 0    | ns   |             |
| $T_A$    | Operating free-air temperature              |                      |     | -55  |        | 125 | 0    | 70   | $^{\circ}C$ |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER             | TEST CONDITIONS <sup>†</sup>   | SN5473 |                  |      | SN7473 |                  |      | UNIT          |
|-----------------------|--|--------|------------------|------|--------|------------------|------|---------------|
|                       |  | MIN    | TYP <sup>‡</sup> | MAX  | MIN    | TYP <sup>‡</sup> | MAX  |               |
| $V_{IK}$              | $V_{CC} = \text{MIN}$ , $I_I = -12 \text{ mA}$   |        |                  | -1.5 |        |                  | -1.5 | V             |
| $V_{OH}$              | $V_{CC} = \text{MIN}$ , $V_{IH} = 2 \text{ V}$ , $V_{IL} = 0.8 \text{ V}$ , $I_{OH} = -0.4 \text{ mA}$ | 2.4    | 3.4              |      | 2.4    | 3.4              |      | V             |
| $V_{OL}$              | $V_{CC} = \text{MIN}$ , $V_{IH} = 2 \text{ V}$ , $V_{IL} = 0.8 \text{ V}$ , $I_{OL} = 16 \text{ mA}$   |        | 0.2              | 0.4  |        | 0.2              | 0.4  | V             |
| $I_I$                 | $V_{CC} = \text{MAX}$ , $V_I = 5.5 \text{ V}$  |        |                  | 1    |        |                  | 1    | mA            |
| $I_{IH}$              | J or K   |        |                  | 40   |        |                  | 40   | $\mu\text{A}$ |
|                       | $\overline{CLR}$ or CLK  |        |                  | 80   |        |                  | 80   |               |
| $I_{IL}$              | J or K   |        |                  | -1.6 |        |                  | -1.6 | mA            |
|                       | $\overline{CLR}$   |        |                  | -3.2 |        |                  | -3.2 |               |
|                       | CLK  |        |                  | -3.2 |        |                  | -3.2 |               |
| $I_{OS}$ <sup>§</sup> | $V_{CC} = \text{MAX}$  | -20    |                  | -57  | -18    |                  | -57  | mA            |
| $I_{CC}$ <sup>¶</sup> | $V_{CC} = \text{MAX}$ , See Note 2   |        | 10               | 20   |        | 10               | 20   | mA            |

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>‡</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}C$ .

<sup>§</sup> Not more than one output should be shorted at a time.

<sup>¶</sup> Average per flip-flop.

NOTE 2: With all outputs open,  $I_{CC}$  is measured with the Q and  $\overline{Q}$  outputs high in turn. At the time of measurement, the clock input is grounded.

## switching characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^{\circ}C$ (see note 3)

| PARAMETER <sup>#</sup> | FROM (INPUT)     | TO (OUTPUT)         | TEST CONDITIONS                            | MIN | TYP | MAX | UNIT |
|------------------------|------------------|---------------------|--|-----|-----|-----|------|
| $f_{max}$              |                  |                     |  | 15  | 20  |     | MHz  |
| $t_{PLH}$              | $\overline{CLR}$ | $\overline{Q}$      | $R_L = 400 \Omega$ , $C_L = 15 \text{ pF}$ |     | 16  | 25  | ns   |
| $t_{PHL}$              |                  | Q                   |  |     | 25  | 40  | ns   |
| $t_{PLH}$              | CLK              | Q or $\overline{Q}$ |  |     | 16  | 25  | ns   |
| $t_{PHL}$              |                  |                     |  |     | 25  | 40  | ns   |

<sup>#</sup> $f_{max}$  = maximum clock frequency;  $t_{PLH}$  = propagation delay time, low-to-high-level output;  $t_{PHL}$  = propagation delay time, high-to-low-level output.

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



# SN5473, SN54LS73A, SN7473, SN74LS73A DUAL J-K FLIP-FLOPS WITH CLEAR

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## recommended operating conditions

|   | SN54LS73A        |     |      | SN74LS73A |     |      | UNIT |    |
|---|------------------|-----|------|-----------|-----|------|------|----|
|   | MIN              | NOM | MAX  | MIN       | NOM | MAX  |      |    |
| V <sub>CC</sub> Supply voltage                | 4.5              | 5   | 5.5  | 4.75      | 5   | 5.25 | V    |    |
| V <sub>IH</sub> High-level input voltage      | 2                |     |      | 2         |     |      | V    |    |
| V <sub>IL</sub> Low-level input voltage       |                  |     | 0.7  |           |     | 0.8  | V    |    |
| I <sub>OH</sub> High-level output current     |                  |     | -0.4 |           |     | -0.4 | mA   |    |
| I <sub>OL</sub> Low-level output current      |                  |     | 4    |           |     | 8    | mA   |    |
| f <sub>clock</sub> Clock frequency            | 0                |     | 30   | 0         |     | 30   | MHz  |    |
| t <sub>w</sub> Pulse duration                 | CLK high         |     | 20   | 20        |     | ns   |      |    |
|   | CLR low          |     | 25   | 20        |     |      |      |    |
| t <sub>su</sub> Set up time-before CLK ↓      | data high or low |     | 20   | 20        |     | ns   |      |    |
|   | CLR inactive     |     | 20   | 20        |     |      |      |    |
| t <sub>h</sub> Hold time-data after CLK ↓     |                  |     | 0    | 0         |     | ns   |      |    |
| T <sub>A</sub> Operating free-air temperature |                  |     | -55  | 125       |     | 0    | 70   | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER               | TEST CONDITIONS†   | SN54LS73A                                     |      |      | SN74LS73A |      |      | UNIT |
|-------------------------|--|---|------|------|-----------|------|------|------|
|                         |  | MIN   | TYP‡ | MAX  | MIN       | TYP‡ | MAX  |      |
| V <sub>IK</sub>         | V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA   |   |      | -1.5 |           |      | -1.5 | V    |
| V <sub>OH</sub>         | V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = MAX, I <sub>OH</sub> = -0.4 mA | 2.5   | 3.4  |      | 2.7       | 3.4  |      | V    |
| V <sub>OL</sub>         | V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = 2 V, I <sub>OL</sub> = 4 mA    |   | 0.25 | 0.4  |           | 0.25 | 0.4  | V    |
|                         | V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = 2 V, I <sub>OL</sub> = 8 mA    |   |      |      |           | 0.35 | 0.5  |      |
| I <sub>I</sub>          | J or K   |   |      | 0.1  |           |      | 0.1  | mA   |
|                         | CLR  | V <sub>CC</sub> = MAX, V <sub>I</sub> = 7 V   |      | 0.3  |           |      | 0.3  |      |
|                         | CLK  |   |      | 0.4  |           |      | 0.4  |      |
| I <sub>IH</sub>         | J or K   |   |      | 20   |           |      | 20   | μA   |
|                         | CLR  | V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V |      | 60   |           |      | 60   |      |
|                         | CLK  |   |      | 80   |           |      | 80   |      |
| I <sub>IL</sub>         | J or K   | V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V |      | -0.4 |           |      | -0.4 | mA   |
|                         | CLR or CLK   |   |      | -0.8 |           |      | -0.8 |      |
| I <sub>OS</sub> §       | V <sub>CC</sub> = MAX, See Note 4  | -20   |      | -100 | -20       |      | -100 | mA   |
| I <sub>CC</sub> (Total) | V <sub>CC</sub> = MAX, See Note 2  |   | 4    | 6    |           | 4    | 6    | mA   |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: With all outputs open, I<sub>CC</sub> is measured with the Q and Q̄ outputs high in turn. At the time of measurement, the clock input is grounded.

NOTE 4: For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with V<sub>O</sub> = 2.25 V and 2.125 V for the 54 family and the 74 family, respectively, with the minimum and maximum limits reduced to one half of their stated values.

## switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see note 3)

| PARAMETER        | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS                               | MIN | TYP | MAX | UNIT |
|------------------|--------------|-------------|---|-----|-----|-----|------|
| f <sub>max</sub> |              |             |   | 30  | 45  |     | MHz  |
| t <sub>PLH</sub> | CLR or CLK   | Q or Q̄     | R <sub>L</sub> = 2 kΩ, C <sub>L</sub> = 15 pF |     | 15  | 20  | ns   |
| t <sub>PHL</sub> |              |             |   |     | 15  | 20  | ns   |

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup>    | Lead/<br>Ball Finish | MSL Peak Temp <sup>(3)</sup> | Samples<br>(Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|----------------------------|----------------------|------------------------------|-----------------------------|
| 5962-9675101QCA  | ACTIVE                | CDIP         | J               | 14   | 1           | TBD                        | Call TI              | Call TI                      |                             |
| 5962-9675101QDA  | ACTIVE                | CFP          | W               | 14   | 1           | TBD                        | Call TI              | Call TI                      |                             |
| 5962-9675101QDA  | ACTIVE                | CFP          | W               | 14   | 1           | TBD                        | Call TI              | Call TI                      |                             |
| 5962-9675101VCA  | ACTIVE                | CDIP         | J               | 14   | 25          | TBD                        | A42                  | N / A for Pkg Type           |                             |
| 5962-9675101VCA  | ACTIVE                | CDIP         | J               | 14   | 25          | TBD                        | A42                  | N / A for Pkg Type           |                             |
| 5962-9675101VDA  | ACTIVE                | CFP          | W               | 14   | 25          | TBD                        | A42                  | N / A for Pkg Type           |                             |
| 5962-9675101VDA  | ACTIVE                | CFP          | W               | 14   | 25          | TBD                        | A42                  | N / A for Pkg Type           |                             |
| SN54LS73AJ       | ACTIVE                | CDIP         | J               | 14   | 1           | TBD                        | A42                  | N / A for Pkg Type           |                             |
| SN54LS73AJ       | ACTIVE                | CDIP         | J               | 14   | 1           | TBD                        | A42                  | N / A for Pkg Type           |                             |
| SN7473N          | OBSOLETE              | PDIP         | N               | 14   |             | TBD                        | Call TI              | Call TI                      |                             |
| SN7473N          | OBSOLETE              | PDIP         | N               | 14   |             | TBD                        | Call TI              | Call TI                      |                             |
| SN7473N3         | OBSOLETE              | PDIP         | N               | 14   |             | TBD                        | Call TI              | Call TI                      |                             |
| SN7473N3         | OBSOLETE              | PDIP         | N               | 14   |             | TBD                        | Call TI              | Call TI                      |                             |
| SN74LS73AD       | ACTIVE                | SOIC         | D               | 14   | 50          | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| SN74LS73AD       | ACTIVE                | SOIC         | D               | 14   | 50          | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| SN74LS73ADE4     | ACTIVE                | SOIC         | D               | 14   | 50          | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| SN74LS73ADE4     | ACTIVE                | SOIC         | D               | 14   | 50          | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| SN74LS73ADG4     | ACTIVE                | SOIC         | D               | 14   | 50          | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| SN74LS73ADG4     | ACTIVE                | SOIC         | D               | 14   | 50          | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| SN74LS73ADR      | ACTIVE                | SOIC         | D               | 14   | 2500        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| SN74LS73ADR      | ACTIVE                | SOIC         | D               | 14   | 2500        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| SN74LS73ADRE4    | ACTIVE                | SOIC         | D               | 14   | 2500        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/<br>Ball Finish | MSL Peak Temp <sup>(3)</sup> | Samples<br>(Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|----------------------|------------------------------|-----------------------------|
| SN74LS73ADRE4    | ACTIVE                | SOIC         | D               | 14   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| SN74LS73ADRG4    | ACTIVE                | SOIC         | D               | 14   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| SN74LS73ADRG4    | ACTIVE                | SOIC         | D               | 14   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| SN74LS73AN       | ACTIVE                | PDIP         | N               | 14   | 25          | Pb-Free (RoHS)          | CU NIPDAU            | N / A for Pkg Type           |                             |
| SN74LS73AN       | ACTIVE                | PDIP         | N               | 14   | 25          | Pb-Free (RoHS)          | CU NIPDAU            | N / A for Pkg Type           |                             |
| SN74LS73ANE4     | ACTIVE                | PDIP         | N               | 14   | 25          | Pb-Free (RoHS)          | CU NIPDAU            | N / A for Pkg Type           |                             |
| SN74LS73ANE4     | ACTIVE                | PDIP         | N               | 14   | 25          | Pb-Free (RoHS)          | CU NIPDAU            | N / A for Pkg Type           |                             |
| SNJ54LS73AFD     | OBSOLETE              | LCCC         | FK              | 20   |             | TBD                     | POST-PLATE           | N / A for Pkg Type           |                             |
| SNJ54LS73AFD     | OBSOLETE              | LCCC         | FK              | 20   |             | TBD                     | POST-PLATE           | N / A for Pkg Type           |                             |
| SNJ54LS73AJ      | ACTIVE                | CDIP         | J               | 14   | 1           | TBD                     | A42                  | N / A for Pkg Type           |                             |
| SNJ54LS73AJ      | ACTIVE                | CDIP         | J               | 14   | 1           | TBD                     | A42                  | N / A for Pkg Type           |                             |
| SNJ54LS73AW      | ACTIVE                | CFP          | W               | 14   | 1           | TBD                     | A42                  | N / A for Pkg Type           |                             |
| SNJ54LS73AW      | ACTIVE                | CFP          | W               | 14   | 1           | TBD                     | A42                  | N / A for Pkg Type           |                             |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**OTHER QUALIFIED VERSIONS OF SN54LS73A, SN54LS73A-SP, SN74LS73A :**

- Catalog: [SN74LS73A](#), [SN54LS73A](#)
  
- Military: [SN54LS73A](#)
  
- Space: [SN54LS73A-SP](#)

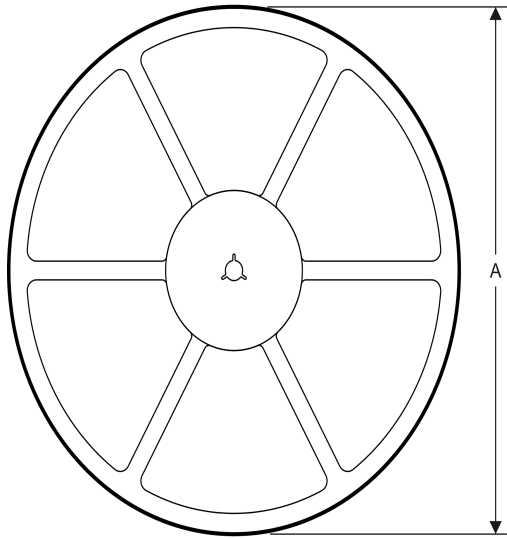
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
  
- Military - QML certified for Military and Defense Applications
  
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application



**TAPE AND REEL INFORMATION**

**REEL DIMENSIONS**



**TAPE DIMENSIONS**



|    |   |
|----|---|
| A0 | Dimension designed to accommodate the component width     |
| B0 | Dimension designed to accommodate the component length    |
| K0 | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape                         |
| P1 | Pitch between successive cavity centers                   |

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LS73ADR | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |

TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LS73ADR | SOIC         | D               | 14   | 2500 | 367.0       | 367.0      | 38.0        |

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14                     | 16                     | 18                     | 20                     |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A             | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX         | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN         | —                      | —                      | —                      | —                      |
| C MAX         | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN         | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF TERMINALS ** | A                |                  | B                |                  |
|---------------------|------------------|------------------|------------------|------------------|
|                     | MIN              | MAX              | MIN              | MAX              |
| 20                  | 0.342<br>(8,69)  | 0.358<br>(9,09)  | 0.307<br>(7,80)  | 0.358<br>(9,09)  |
| 28                  | 0.442<br>(11,23) | 0.458<br>(11,63) | 0.406<br>(10,31) | 0.458<br>(11,63) |
| 44                  | 0.640<br>(16,26) | 0.660<br>(16,76) | 0.495<br>(12,58) | 0.560<br>(14,22) |
| 52                  | 0.740<br>(18,78) | 0.761<br>(19,32) | 0.495<br>(12,58) | 0.560<br>(14,22) |
| 68                  | 0.938<br>(23,83) | 0.962<br>(24,43) | 0.850<br>(21,6)  | 0.858<br>(21,8)  |
| 84                  | 1.141<br>(28,99) | 1.165<br>(29,59) | 1.047<br>(26,6)  | 1.063<br>(27,0)  |



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211283-3/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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**Телефон:** +7 812 627 14 35

**Электронная почта:** [sales@st-electron.ru](mailto:sales@st-electron.ru)

**Адрес:** 198099, Санкт-Петербург,  
Промышленная ул, дом № 19, литера Н,  
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