

# Intelligent Power Module and Gate Drive Interface Hermetically Sealed Optocouplers

## Technical Data

**HCPL-5300**  
**HCPL-5301**  
**HCPL-530K**  
**5962-96852**

### Features

- Performance Specified Over Full Military Temperature Range: -55°C to +125°C
- Fast Maximum Propagation Delays  
 $t_{PHL} = 450$  ns,  
 $t_{PLH} = 650$  ns
- Minimized Pulse Width Distortion (PWD = 450 ns)
- High Common Mode Rejection (CMR): 10 kV/ $\mu$ s at  $V_{CM} = 1000$  V
- CTR > 30% at  $I_F = 10$  mA
- 1500 Vdc Withstand Test Voltage
- Manufactured and Tested on a MIL-PRF-38534 Certified Line
- Hermetically Sealed Packages
- Dual Marked with Device Part Number and DSCC Drawing Number
- QML-38534, Class H and K
- HCPL-4506 Function Compatibility

### Applications

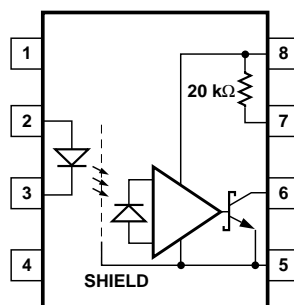
- Military and Space
- High Reliability Systems
- Harsh Industrial Environments
- Transportation, Medical, and Life Critical Systems
- IPM Isolation
- Isolated IGBT/MOSFET Gate Drive
- AC and Brushless DC Motor Drives
- Industrial Inverters

### Description

The HCPL-530X devices consist of a GaAsP LED optically coupled to an integrated high gain photo detector in a hermetically sealed package. The products are

capable of operation and storage over the full military temperature range and can be purchased as either standard product or with full MIL-PRF-38534 Class Level H or K testing or from the DSCC Drawing 5962-96852. All devices are manufactured and tested on a MIL-PRF-38534 certified line and are included in the DSCC Qualified Manufacturers List QML-38534 for Hybrid Micro-circuits. Minimized propagation delay difference between devices make these optocouplers excellent solutions for improving inverter efficiency through reduced switching dead time. An on chip 20 k $\Omega$  output pull-up resistor can be enabled by shorting output pins 6 and 7, thus eliminating the need for an external pull-up resistor in common IPM applications. Specifications and performance plots are given for typical IPM applications.

### Schematic Diagram



### Truth Table

LED	$V_O$
ON	L
OFF	H

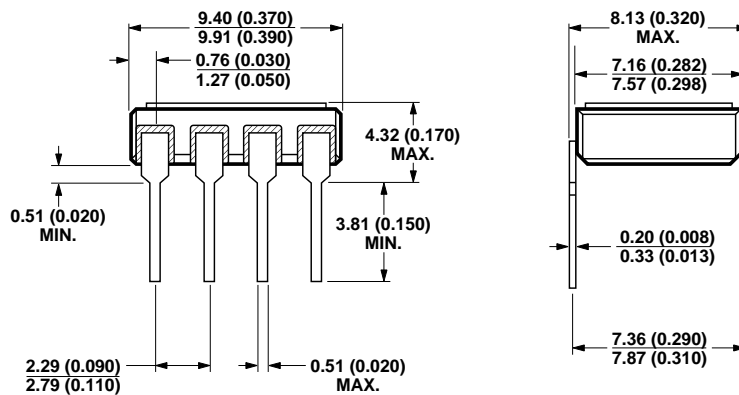
The connection of a 0.1  $\mu$ F bypass capacitor between pins 5 and 8 is recommended.

**CAUTION:** It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

## Selection Guide-Package Styles and Lead Configuration Options

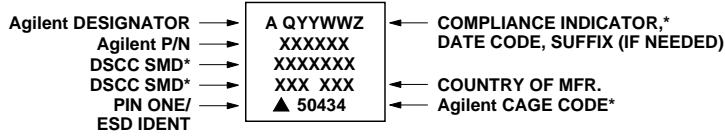
<b>Agilent Part # and Options</b>	
Commercial	HCPL-5300
MIL-PRF-38534, Class H	HCPL-5301
MIL-PRF-38534, Class K	HCPL-530K
Standard Lead Finish	Gold Plate
Solder Dipped	Option #200
Butt Cut/Gold Plate	Option #100
Gull Wing/Soldered	Option #300
<b>Class H SMD Part #</b>	
Prescript for all below	5962-
Either Gold or Solder	9685201HPX
Gold Plate	9685201HPC
Solder Dipped	9685201HPA
Butt Cut/Gold Plate	9685201HYC
Butt Cut/Soldered	9685201HYA
Gull Wing/Soldered	9685201HXA
<b>Class K SMD Part #</b>	
Prescript for all below	5962-
Either Gold or Solder	9685201KPX
Gold Plate	9685201KPC
Solder Dipped	9685201KPA
Butt Cut/Gold Plate	9685201KYC
Butt Cut/Soldered	9685201KYA
Gull Wing/Soldered	9685201KXA

## Outline Drawing



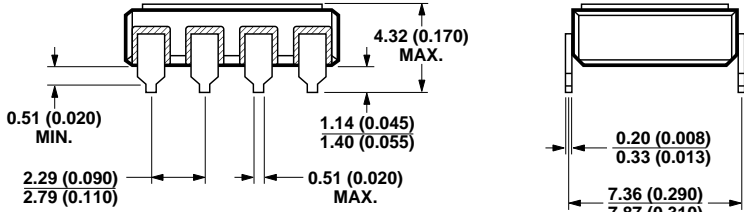
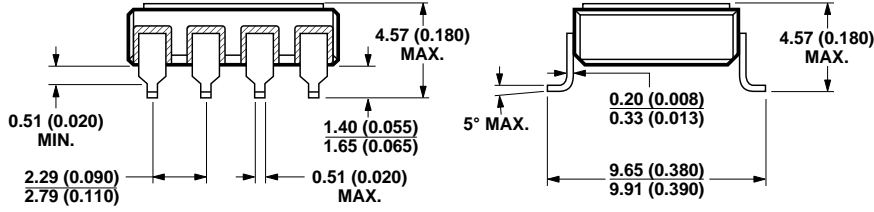
NOTE: DIMENSIONS IN MILLIMETERS (INCHES).

## Device Marking



\* QUALIFIED PARTS ONLY

## Hermetic Optocoupler Options

Option	Description
100	<p>Surface mountable hermetic optocoupler with leads trimmed for butt joint assembly. This option is available on commercial and hi-rel product in 8 pin DIP (see drawings below for details).</p>  <p>NOTE: DIMENSIONS IN MILLIMETERS (INCHES).</p>
200	<p>Lead finish is solder dipped rather than gold plated. This option is available on commercial and hi-rel product in 8 pin DIP. DSCC Drawing part numbers contain provisions for lead finish.</p>
300	<p>Surface mountable hermetic optocoupler with leads cut and bent for gull wing assembly. This option is available on commercial and hi-rel product in 8 pin DIP (see drawings below for details). This option has solder dipped leads.</p>  <p>NOTE: DIMENSIONS IN MILLIMETERS (INCHES).</p>

## Absolute Maximum Ratings

Storage Temperature ( $T_S$ ) .....	-65 to 150°C
Operating Temperature ( $T_A$ ) .....	-55 to 125°C
Junction Temperature ( $T_J$ ) .....	175°C
Average Input Current ( $I_{F(AVG)}$ ) .....	25 mA
Peak Input Current (50% duty cycle, $\leq 1$ ms pulse width) ( $I_{F(PEAK)}$ ) .....	50 mA
Peak Transient Input Current ( $< 1 \mu s$ pulse width, 300 pps) ( $I_{F(TRAN)}$ ) .....	1.0 A
Reverse Input Voltage (Pin 3-2) ( $V_R$ ) .....	5 V
Average Output Current (Pin 6) ( $I_{O(AVG)}$ ) .....	15 mA
Resistor Voltage (Pin 7) ( $V_7$ ) .....	-0.5 V to $V_{CC}$
Output Voltage (Pin 6-5) ( $V_O$ ) .....	-0.5 to 30 V
Supply Voltage (Pin 8-5) ( $V_{CC}$ ) .....	-0.5 to 30 V
Output Power Dissipation ( $P_O$ ) .....	100 mW
Total Power Dissipation ( $P_T$ ) .....	145 mW
Lead Solder Temperature (soldering, 10 seconds) .....	260°C

## ESD Classification

(MIL-STD-883,  
Method 3015).....( $\Delta$ ), Class 1

## Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage	$V_{CC}$	4.5	30	Volts
Output Voltage	$V_O$	0	30	Volts
Input Current (ON)	$I_{F(ON)}$	10	20	mA
Input Voltage (OFF)	$V_{F(OFF)}$	-5	0.8	V

## Electrical Specifications

Over recommended operating conditions ( $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $V_{CC} = +4.5\text{ V}$  to  $30\text{ V}$ ,  $I_{F(\text{ON})} = 10\text{ mA}$  to  $20\text{ mA}$ ,  $V_{F(\text{OFF})} = -5\text{ V}$  to  $0.8\text{ V}$ ) unless otherwise specified.

Parameter	Symbol	Group A Sub-groups <sup>[12]</sup>	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR	1, 2, 3	30	90		%	$I_F = 10\text{ mA}$ , $V_O = 0.6\text{ V}$		1
Low Level Output Current	$I_{OL}$	1, 2, 3	3.0	9.0		mA	$I_F = 10\text{ mA}$ , $V_O = 0.6\text{ V}$	1, 2	
Low Level Output Voltage	$V_{OL}$	1, 2, 3		0.3	0.6	V	$I_O = 2.4\text{ mA}$		
Input Threshold Current	$I_{TH}$	1, 2, 3		1.5	5.0	mA	$V_O = 0.8\text{ V}$ , $I_O = 0.75\text{ mA}$	1	7
High Level Output Current	$I_{OH}$	1, 2, 3		5	75	$\mu\text{A}$	$V_F = 0.8\text{ V}$	3	
High Level Supply Current	$I_{CCH}$	1, 2, 3		0.6	1.5	mA	$V_F = 0.8\text{ V}$ , $V_O = \text{Open}$		7
Low Level Supply Current	$I_{CCL}$	1, 2, 3		0.6	1.5	mA	$I_F = 10\text{ mA}$ , $V_O = \text{Open}$		7
Input Forward Voltage	$V_F$	1, 2, 3	1.0	1.5	1.8	V	$I_F = 10\text{ mA}$	4	
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			-1.6		mV/ $^\circ\text{C}$	$I_F = 10\text{ mA}$		
Input Reverse Breakdown Voltage	$BV_R$	1, 2, 3	5			V	$I_R = 100\ \mu\text{A}$		
Input Capacitance	$C_{IN}$			90		pF	$f = 1\text{ MHz}$ , $V_F = 0\text{ V}$		
Input-Output Insulation Leakage Current	$I_{I-O}$	1			1.0	$\mu\text{A}$	$RH = 45\%$ , $t = 5\text{ sec}$ , $V_{I-O} = 1500\text{ Vdc}$ , $T_A = 25^\circ\text{C}$		2
Resistance (Input-Output)	$R_{I-O}$			$10^{12}$		$\Omega$	$V_{I-O} = 500\text{ Vdc}$		2
Capacitance (Input-Output)	$C_{I-O}$			2.4		pF	$f = 1\text{ MHz}$		2
Internal Pull-up Resistor	$R_L$	1	14	20	28	k $\Omega$	$T_A = 25^\circ\text{C}$		4, 5, 6
Internal Pull-up Resistor Temperature Coefficient	$\frac{\Delta R_L}{\Delta T_A}$			0.014		k $\Omega$ / $^\circ\text{C}$			

\*All typical values at  $25^\circ\text{C}$ ,  $V_{CC} = 15\text{ V}$ .

### Switching Specifications ( $R_L = 20 \text{ k}\Omega$ External)

Over recommended operating conditions:

( $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $V_{CC} = +4.5 \text{ V}$  to  $30 \text{ V}$ ,  $I_{F(ON)} = 10 \text{ mA}$  to  $20 \text{ mA}$ ,  $V_{F(OFF)} = -5 \text{ V}$  to  $0.8 \text{ V}$ ) unless otherwise specified.

Parameter	Symbol	Group A Subgrps. <sup>[12]</sup>	Min.	Typ.*	Max.	Units	Test Conditions		Fig.	Note
Propagation Delay Time to Low Output Level	$t_{PHL}$	9, 10, 11	30	180	450	ns	$C_L = 100 \text{ pF}$	$I_{F(on)} = 10 \text{ mA}$ , $V_{F(off)} = 0.8 \text{ V}$ , $V_{CC} = 15.0 \text{ V}$ , $V_{THLH} = 2.0 \text{ V}$ , $V_{THHL} = 1.5 \text{ V}$	5, 7, 9-12	3, 4, 5, 6, 7
				100		ns	$C_L = 10 \text{ pF}$			
Propagation Delay Time to High Output Level	$t_{PLH}$	9, 10, 11	250	350	650	ns	$C_L = 100 \text{ pF}$			
				130		ns	$C_L = 10 \text{ pF}$			
Pulse Width Distortion	PWD	9, 10, 11		150	450	ns	$C_L = 100 \text{ pF}$			11
Propagation Delay Difference Between Any Two Parts	$t_{PLH} - t_{PHL}$	9, 10, 11	-170	140	500	ns				8
Output High Level Common Mode Immunity Transient	$ CM_H $	9	10	17		kV/ $\mu\text{s}$	$I_F = 0 \text{ mA}$ , $V_O > 3.0 \text{ V}$	$V_{CC} = 15.0 \text{ V}$ , $C_L = 100 \text{ pF}$ , $V_{CM} = 1000 V_{P-P}$ , $T_A = 25^\circ\text{C}$	6, 17, 18, 21	9, 13
Output Low Level Common Mode Immunity Transient	$ CM_L $	9	10	17		kV/ $\mu\text{s}$	$I_F = 10 \text{ mA}$ , $V_O < 1.0 \text{ V}$			10, 13

\*All typical values at  $25^\circ\text{C}$ ,  $V_{CC} = 15 \text{ V}$ .

## Switching Specifications ( $R_L$ = Internal Pull-up)

Over recommended operating conditions:

( $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $V_{CC} = +4.5\text{ V}$  to  $30\text{ V}$ ,  $I_{F(\text{ON})} = 10\text{ mA}$  to  $20\text{ mA}$ ,  $V_{F(\text{OFF})} = -5\text{ V}$  to  $0.8\text{ V}$ ) unless otherwise specified.

Parameter	Symbol	Group A Subgrps. <sup>[12]</sup>	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note		
Propagation Delay Time to Low Output Level	$t_{\text{PHL}}$	9, 10, 11	20	185	500	ns	$I_{F(\text{on})} = 10\text{ mA}$ , $V_{F(\text{off})} = 0.8\text{ V}$ , $V_{CC} = 15.0\text{ V}$ , $C_L = 100\text{ pF}$ , $V_{\text{THLH}} = 2.0\text{ V}$ $V_{\text{THHL}} = 1.5\text{ V}$	5, 8,	3, 4, 5, 6, 7		
Propagation Delay Time to High Output Level	$t_{\text{PLH}}$	9, 10, 11	220	415	750	ns					
Pulse Width Distortion	PWD	9, 10, 11		150	600	ns					11
Propagation Delay Difference Between Any Two Parts	$t_{\text{PLH}} - t_{\text{PHL}}$	9, 10, 11	-225	150	650	ns					8
Output High Level Common Mode Transient Immunity	$ CM_H $			10		kV/ $\mu\text{s}$	$I_F = 0\text{ mA}$ , $V_O > 3.0\text{ V}$ $V_{CC} = 15.0\text{ V}$ , $C_L = 100\text{ pF}$ , $V_{CM} = 1000$ $T_A = 25^\circ\text{C}$	6, 21	9		
Output Low Level Common Mode Transient Immunity	$ CM_L $			10		kV/ $\mu\text{s}$			$I_F = 16\text{ mA}$ $V_O < 1.0\text{ V}$	10	
Power Supply Rejection	PSR			1.0		$V_{P-P}$	Square Wave, $t_{\text{RISE}}, t_{\text{FALL}} > 5\text{ ns}$ , no bypass capacitors.		7		

\*All typical values at  $25^\circ\text{C}$ ,  $V_{CC} = 15\text{ V}$ .

### Notes:

- CURRENT TRANSFER RATIO in percent is defined as the ratio of output collector current ( $I_O$ ) to the forward LED input current ( $I_F$ ) times 100.
- Device considered a two-terminal device: Pins 1, 2, 3 and 4 shorted together and Pins 5, 6, 7 and 8 shorted together.
- Pulse:  $f = 20\text{ kHz}$ , Duty Cycle = 10%
- The internal  $20\text{ k}\Omega$  resistor can be used by shorting pins 6 and 7 together.
- Due to the tolerance of the internal resistor, and since propagation delay is dependent on the load resistor value, performance can be improved by using an external  $20\text{ k}\Omega$  1% load resistor. For more information on how propagation delay varies with load resistance, see Figure 8.
- The  $R_L = 20\text{ k}\Omega$ ,  $C_L = 100\text{ pF}$  represents a typical IPM (Intelligent Power Module) load.
- Use of a  $0.1\text{ }\mu\text{F}$  bypass capacitor connected between pins 5 and 8 can improve performance by filtering power supply line noise.
- The difference in  $t_{\text{PLH}}$  and  $t_{\text{PHL}}$  between any two parts under the same test condition. (See IPM Dead Time and Propagation Delay Specifications section.)
- Common mode transient immunity in a Logic High level is the maximum tolerable  $dV_{CM}/dt$  of the common mode pulse,  $V_{CM}$ , to assure that the output will remain in a Logic High state (i.e.,  $V_O > 3.0\text{ V}$ ).
- Common mode transient immunity in a Logic Low level is the maximum tolerable  $dV_{CM}/dt$  of the common mode pulse,  $V_{CM}$ , to assure that the output will remain in a Logic Low state (i.e.,  $V_O < 1.0\text{ V}$ ).
- Pulse Width Distortion (PWD) is defined as the difference between  $t_{\text{PLH}}$  and  $t_{\text{PHL}}$  for any given device.
- Standard parts receive 100% testing at  $25^\circ\text{C}$  (Subgroups 1 and 9). Hi-Rel and SMD parts receive 100% testing at  $25^\circ\text{C}$ ,  $+125^\circ\text{C}$ , and  $-55^\circ\text{C}$  (Subgroups 1 and 9, 2 and 10, 3 and 11 respectively).
- Parameters are tested as part of device initial characterization and after design and process changes. Parameters are guaranteed to limits specified for all lots not specifically tested.

## LED Drive Circuit Considerations For Ultra High CMR Performance

Without a detector shield, the dominant cause of optocoupler CMR failure is capacitive coupling from the input side of the optocoupler, through the package, to the detector IC as shown in Figure 14. The HCPL-530X improves CMR performance by using a detector IC with an optically transparent Faraday shield, which diverts the capacitively coupled current away from the sensitive IC circuitry. However, this shield does not eliminate the capacitive coupling between the LED and the optocoupler output pins and output ground as shown in Figure 15. This capacitive coupling causes perturbations in the LED current during common mode transients and becomes the major source of CMR failures for a shielded optocoupler. The main design objective of a high CMR LED drive circuit becomes keeping the LED in the proper state (on or off) during common mode transients. For example, the recommended application circuit (Figure 13), can achieve 10 kV/ $\mu$ s CMR while minimizing component complexity. Note that a CMOS gate is recommended in Figure 13 to keep the LED off when the gate is in the high state.

Another cause of CMR failure for a shielded optocoupler is direct coupling to the optocoupler output pins through  $C_{LEDO1}$  and  $C_{LEDO2}$  in Figure 15. Many factors influence the effect and magnitude of the direct coupling including: the use of an internal or external output pull-up resistor, the position of the LED current setting resistor, the connection of the unused input

package pins, and the value of the capacitor at the optocoupler output (CL).

Techniques to keep the LED in the proper state and minimize the effect of the direct coupling are discussed in the next two sections.

### CMR With The LED On (CMR<sub>L</sub>)

A high CMR LED drive circuit must keep the LED on during common mode transients. This is achieved by overdriving the LED current beyond the input threshold so that it is not pulled below the threshold during a transient. The recommended minimum LED current of 10 mA provides adequate margin over the maximum  $I_{TH}$  of 5.0 mA (see Figure 1) to achieve 10 kV/ $\mu$ s CMR. Capacitive coupling is higher when the internal load resistor is used (due to  $C_{LEDO2}$ ) and an  $I_F = 16$ mA is required to obtain 10 kV/ $\mu$ s CMR.

The placement of the LED current setting resistor affects the ability of the drive circuit to keep the LED on during transients and interacts with the direct coupling to the optocoupler output. For example, the LED resistor in Figure 16 is connected to the anode. Figure 17 shows the AC equivalent circuit for Figure 16 during common mode transients. During a  $+dV_{CM}/dt$  in Figure 17, the current available at the LED anode ( $I_{TOTAL}$ ) is limited by the series resistor. The LED current ( $I_F$ ) is reduced from its DC value by an amount equal to the current that flows through  $C_{LEDP}$  and  $C_{LEDO1}$ . The situation is made worse because the current through  $C_{LEDO1}$  has the effect of trying to pull the output high

(toward a CMR failure) at the same time the LED current is being reduced. For this reason, the recommended LED drive circuit (Figure 13) places the current setting resistor in series with the LED cathode. Figure 18 is the AC equivalent circuit for Figure 13 during common mode transients. In this case, the LED current is not reduced during a  $+dV_{CM}/dt$  transient because the current flowing through the package capacitance is supplied by the power supply. During a  $-dV_{CM}/dt$  transient, however, the LED current is reduced by the amount of current flowing through  $C_{LEDN}$ . But better CMR performance is achieved since the current flowing in  $C_{LEDO1}$  during a negative transient acts to keep the output low.

Coupling to the LED and output pins is also affected by the connection of pins 1 and 4. If CMR is limited by perturbations in the LED on current, as it is for the recommended drive circuit (Figure 13), pins 1 and 4 should be connected to the input circuit common. However, if CMR performance is limited by direct coupling to the output when the LED is off, pins 1 and 4 should be left unconnected.

### CMR With The LED Off (CMR<sub>H</sub>)

A high CMR LED drive circuit must keep the LED off ( $V_F \leq V_{F(OFF)}$ ) during common mode transients. For example, during a  $+dV_{CM}/dt$  transient in Figure 18, the current flowing through  $C_{LEDN}$  is supplied by the parallel combination of the LED and series resistor. As long as the voltage developed across the resistor is less than  $V_{F(OFF)}$  the LED will remain off and no



common mode failure will occur. Even if the LED momentarily turns on, the 100 pF capacitor from pins 6-5 will keep the output from dipping below the threshold. The recommended LED drive circuit (Figure 13) provides about 10 V of margin between the lowest optocoupler output voltage and a 3 V IPM threshold during a 10 kV/ $\mu$ s transient with  $V_{CM} = 1000$  V. Additional margin can be obtained by adding a diode in parallel with the resistor, as shown by the dashed line connection in Figure 18, to clamp the voltage across the LED below  $V_{F(OFF)}$ .

Since the open collector drive circuit, shown in Figure 19, cannot keep the LED off during a  $+dV_{CM}/dt$  transient, it is not desirable for applications requiring ultra high  $CMR_H$  performance. Figure 20 is the AC equivalent circuit for Figure 16 during common mode transients. Essentially all the current flowing through  $C_{LEDN}$  during a  $+dV_{CM}/dt$  transient must be supplied by the LED.  $CMR_H$  failures can occur at  $dv/dt$  rates where the current through the LED and  $C_{LEDN}$  exceeds the input threshold. Figure 21 is an alternative drive circuit which does achieve ultra high  $CMR$  performance by shunting the LED in the off state.

### IPM Dead Time and Propagation Delay Specifications

These devices include a Propagation Delay Difference specification intended to help designers minimize “dead time” in their power inverter designs. Dead time is the time period during which both the high and low side power transistors (Q1 and Q2 in Figure 22) are off. Any overlap in Q1 and Q2 conduction will result in large currents flowing through the power devices between the high and low voltage motor rails.

To minimize dead time the designer must consider the propagation delay characteristics of the optocoupler as well as the characteristics of the IPM IGBT gate drive circuit. Considering only the delay characteristics of the optocoupler (the characteristics of the IPM IGBT gate drive circuit can be analyzed in the same way) it is important to know the minimum and maximum turn-on ( $t_{PHL}$ ) and turn-off ( $t_{PLH}$ ) propagation delay specifications, preferably over the desired operating temperature range.

The limiting case of zero dead time occurs when the input to Q1 turns off at the same time that the input to Q2 turns on. This case determines the minimum delay between LED1 turn-off and LED2

turn-on, which is related to the worst case optocoupler propagation delay waveforms, as shown in Figure 23. A minimum dead time of zero is achieved in Figure 23 when the signal to turn on LED2 is delayed by ( $t_{PLH\ max} - t_{PHL\ min}$ ) from the LED1 turn off. This delay is the maximum value for the propagation delay difference specification which is specified at 500 ns for the HCPL-530X over an operating temperature range of  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$ .

Delaying the LED signal by the maximum propagation delay difference ensures that the minimum dead time is zero, but it does not tell a designer what the maximum dead time will be. The maximum dead time occurs in the highly unlikely case where one optocoupler with the fastest  $t_{PLH}$  and another with the slowest  $t_{PHL}$  are in the same inverter leg. The maximum dead time in this case becomes the sum of the spread in the  $t_{PLH}$  and  $t_{PHL}$  propagation delays as shown in Figure 24. The maximum dead time is also equivalent to the difference between the maximum and minimum propagation delay difference specifications. The maximum dead time (due to the optocouplers) for the HCPL-530X is 670 ns (= 500 ns - (-170 ns)) over an operating temperature range of  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$ .

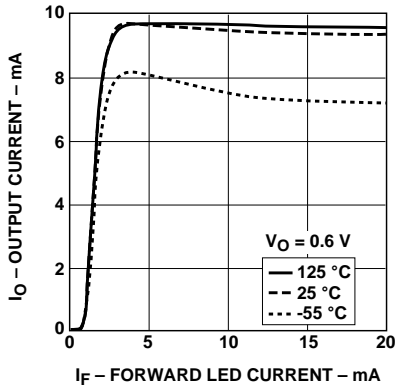


Figure 1. Typical Transfer Characteristics.

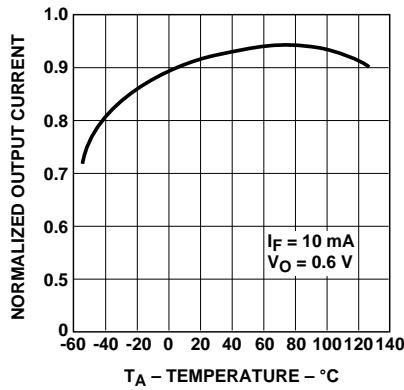


Figure 2. Normalized Output Current vs. Temperature.

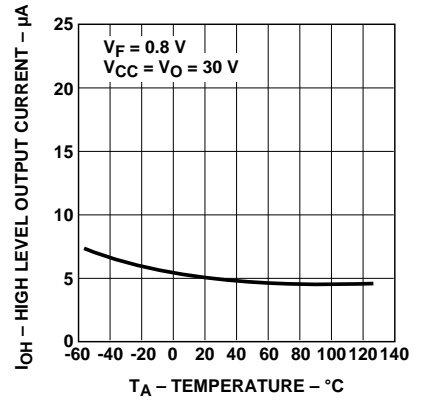


Figure 3. High Level Output Current vs. Temperature.

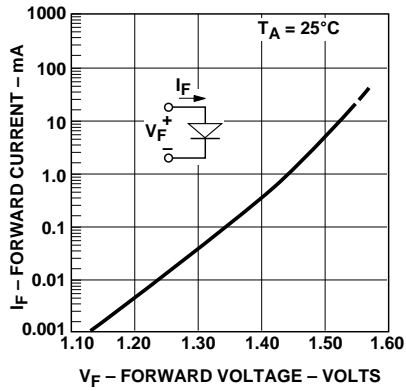


Figure 4. Input Current vs. Forward Voltage.

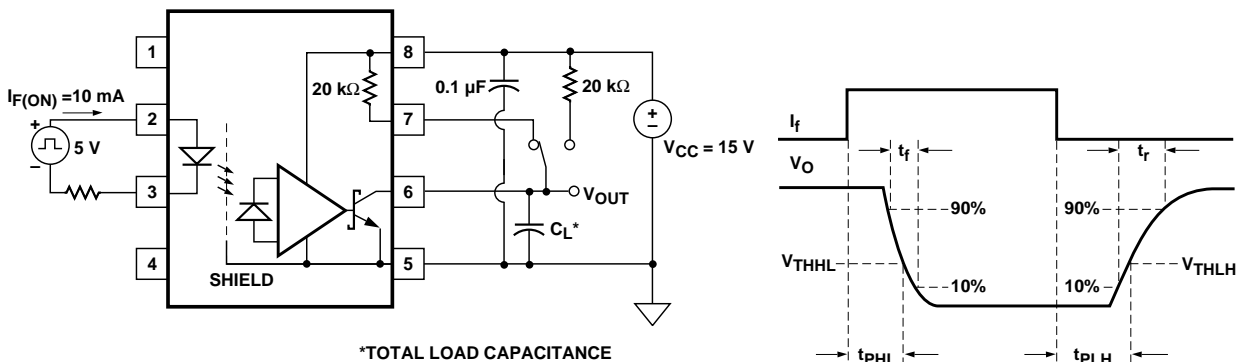


Figure 5. Propagation Delay Test Circuit.

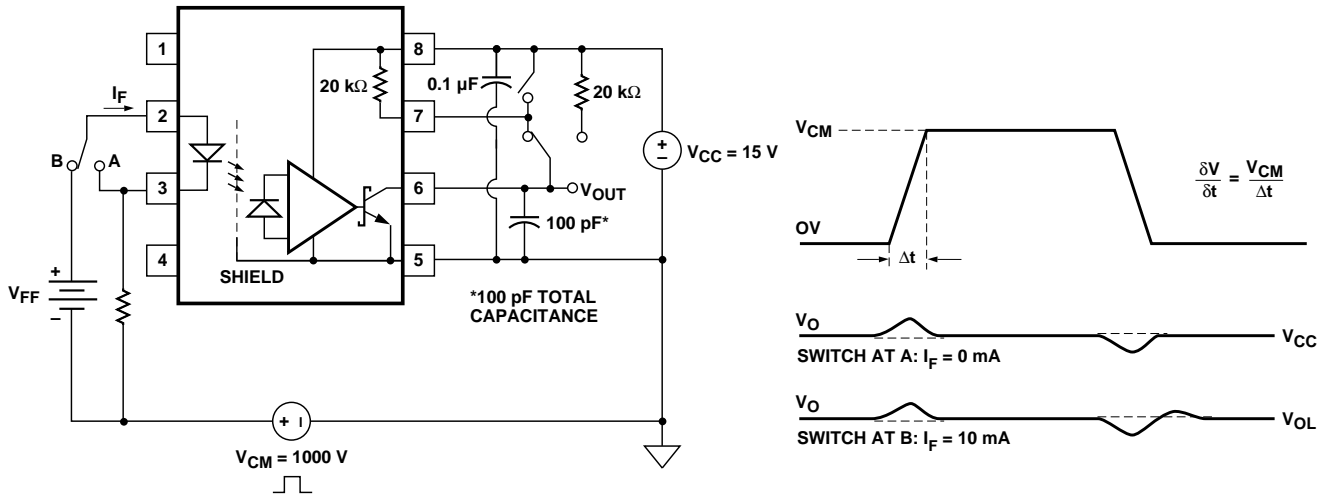


Figure 6. CMR Test Circuit. Typical CMR Waveform.

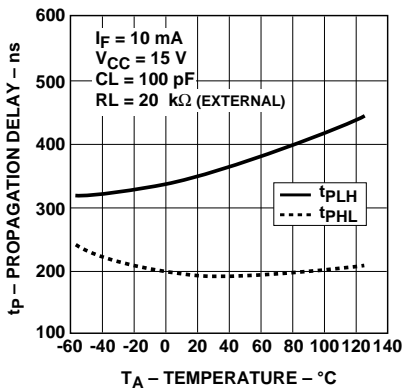


Figure 7. Propagation Delay with External 20 kΩ RL vs. Temperature.

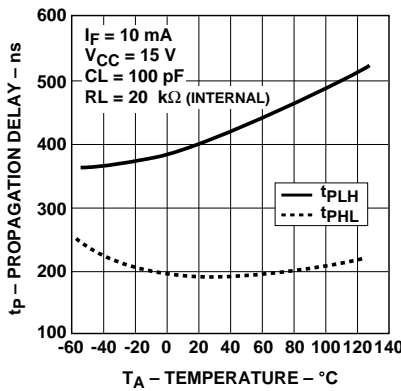


Figure 8. Propagation Delay with Internal 20 kΩ RL vs. Temperature.

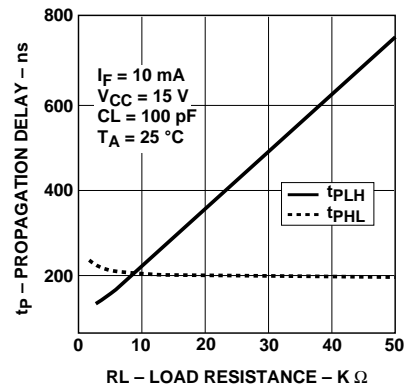


Figure 9. Propagation Delay vs. Load Resistance.

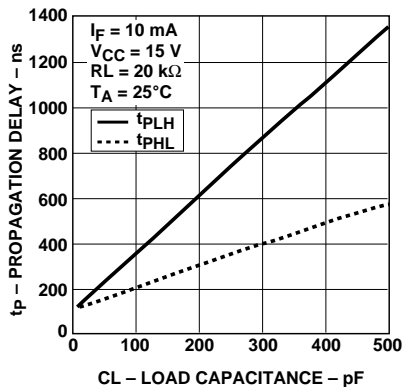


Figure 10. Propagation Delay vs. Load Capacitance.

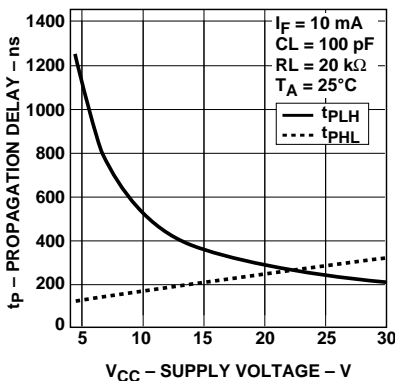


Figure 11. Propagation Delay vs. Supply Voltage.

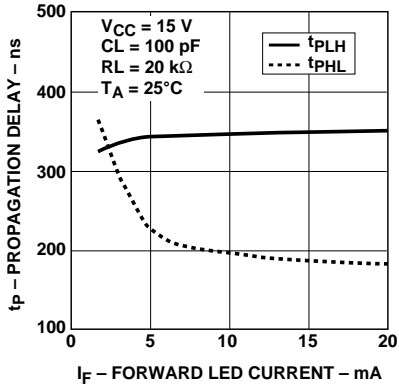


Figure 12. Propagation Delay vs. Input Current.

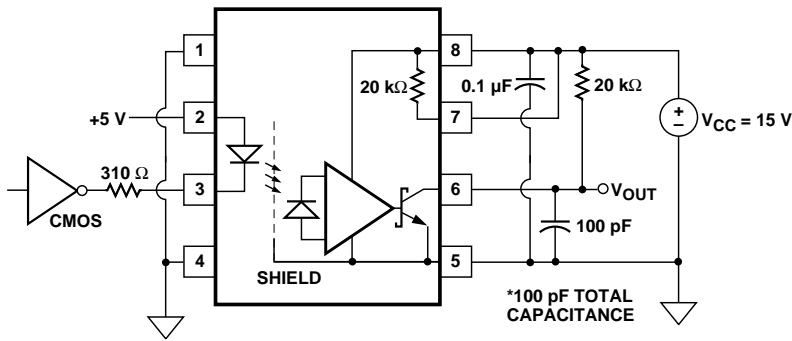


Figure 13. Recommended LED Drive Circuit.

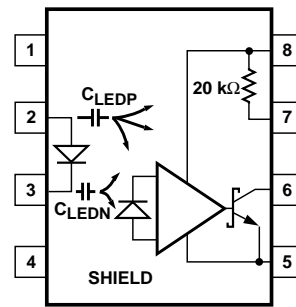


Figure 14. Optocoupler Input to Output Capacitance Model for Unshielded Optocouplers.

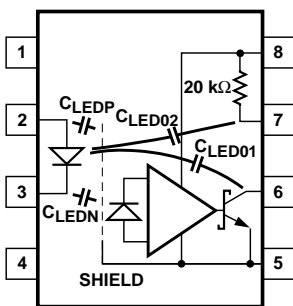


Figure 15. Optocoupler Input to Output Capacitance Model for Shielded Optocouplers.

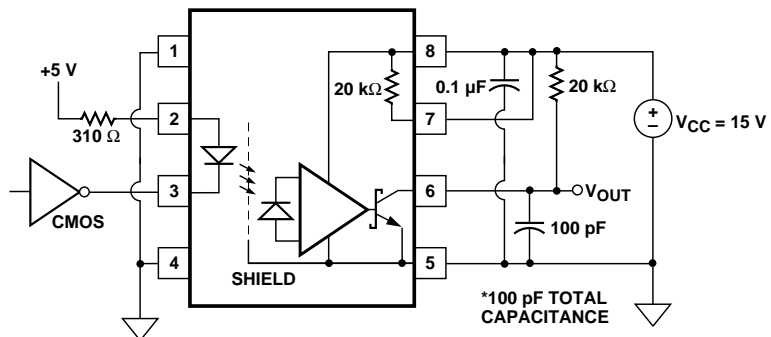


Figure 16. LED Drive Circuit with Resistor Connected to LED Anode (Not Recommended).

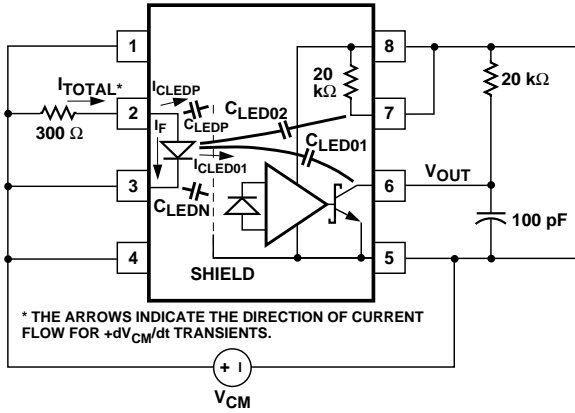


Figure 17. AC Equivalent Circuit for Figure 16 During Common Mode Transients.

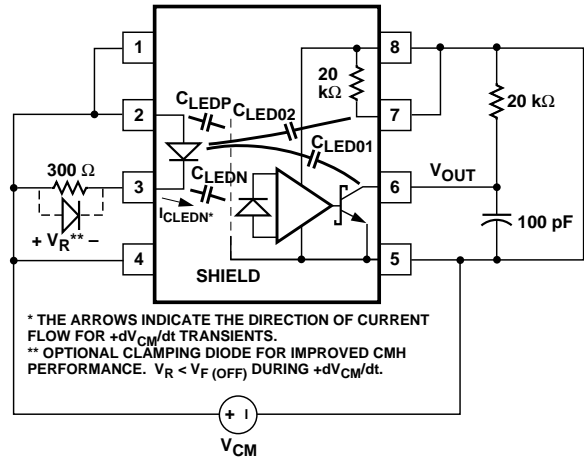


Figure 18. AC Equivalent Circuit for Figure 13 During Common Mode Transients.

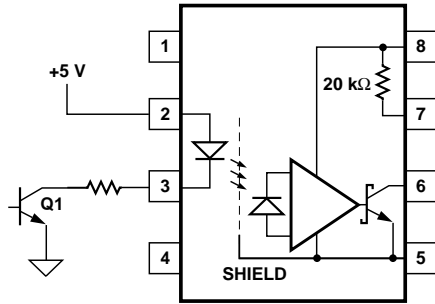


Figure 19. Not Recommended Open Collector LED Drive Circuit.

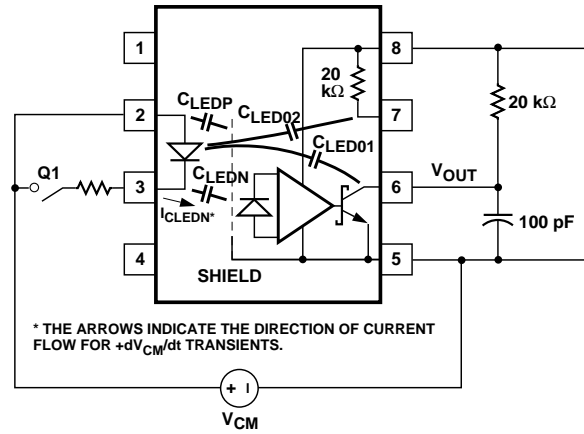


Figure 20. AC Equivalent Circuit for Figure 19 During Common Mode Transients.

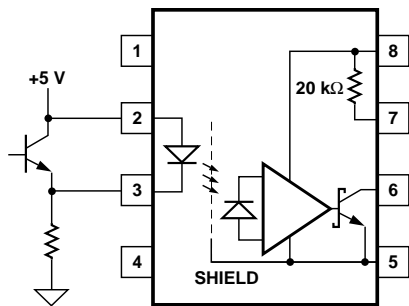


Figure 21. Recommended LED Drive Circuit for Ultra High CMR.

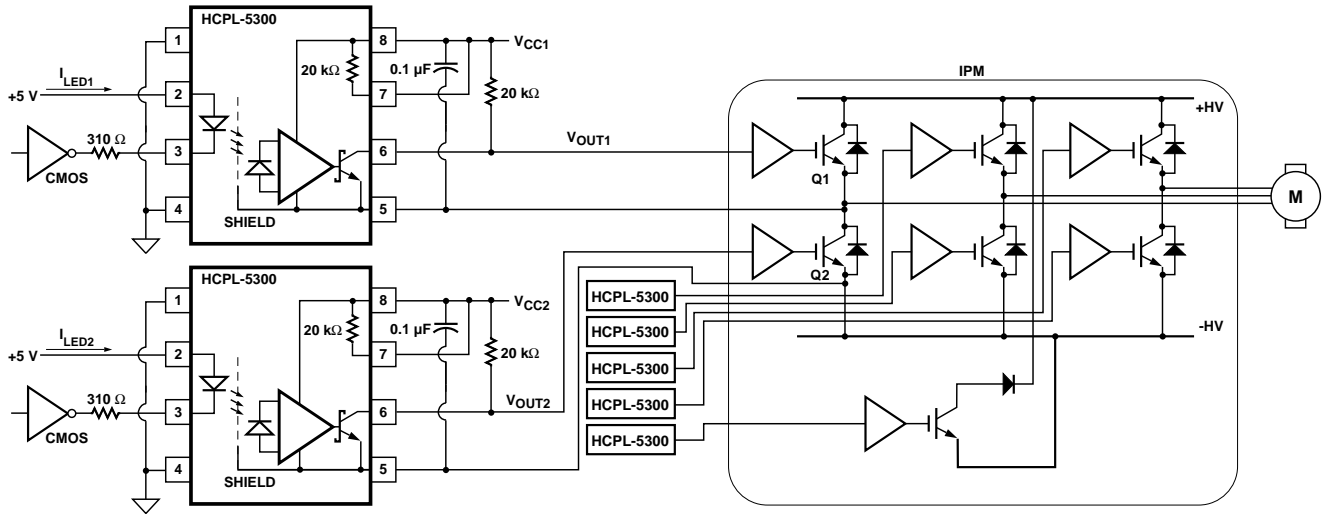
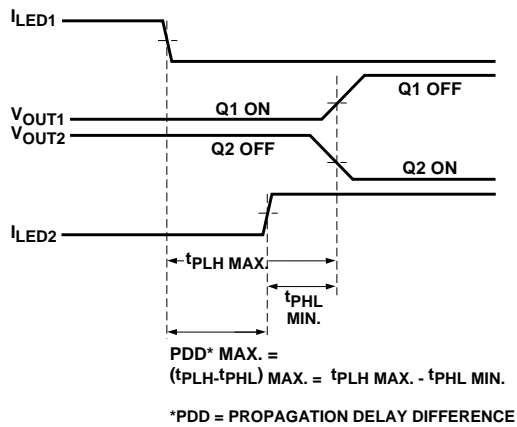


Figure 22. Typical Application Circuit.



NOTE: THE PROPAGATION DELAYS USED TO CALCULATE PDD ARE TAKEN AT EQUAL TEMPERATURES.

Figure 23. Minimum LED Skew for Zero Dead Time.

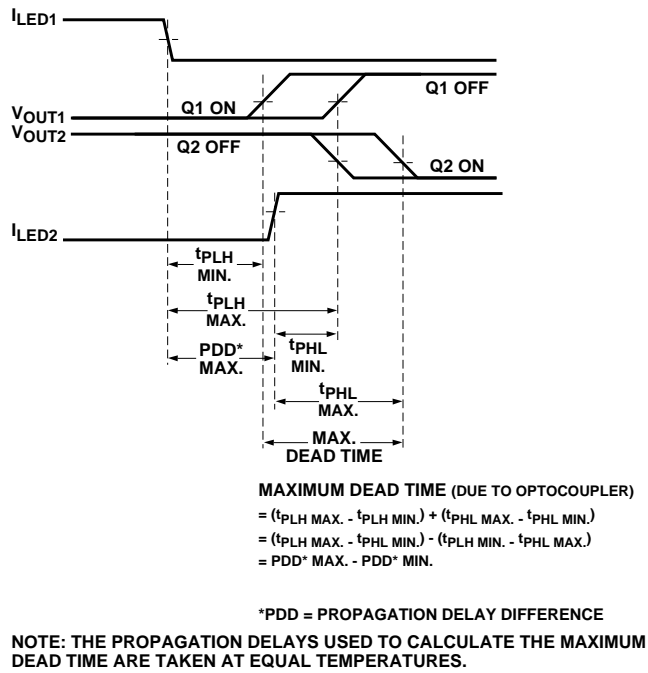


Figure 24. Waveforms for Dead Time Calculations.

### MIL-PRF-38534 Class H, Class K, and DSCC SMD Test Program

Agilent Technologies' Hi-Rel Optocouplers are in compliance with MIL-PRF-38534 Classes H and K. Class H and Class K devices are also in compliance with DSCC drawing 5962-96852.

Testing consists of 100% screening and quality conformance inspection to MIL-PRF-38534.







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