

CMOS Micropower Phase-Locked Loop

■ CD4046B CMOS Micropower Phase-Locked Loop (PLL) consists of a low-power, linear voltage-controlled oscillator (VCO) and two different phase comparators having a common signal-input amplifier and a common comparator input. A 5.2-V zener diode is provided for supply regulation if necessary.

The CD4046B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (NSR suffix), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

VCO Section

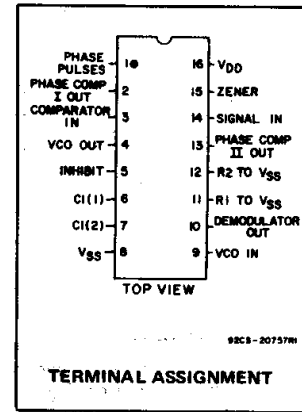
The VCO requires one external capacitor C1 and one or two external resistors (R1 or R1 and R2). Resistor R1 and capacitor C1 determine the frequency range of the VCO and resistor R2 enables the VCO to have a frequency offset if required. The high input impedance ($10^{12}\Omega$) of the VCO simplifies the design of low-pass filters by permitting the designer a wide choice of resistor-to-capacitor ratios. In order not to load the low-pass filter, a source-follower output of the VCO input voltage is provided at terminal 10 (DEMODULATED OUTPUT). If this terminal is used, a load resistor (R_S) of 10 k Ω or more should be connected from this terminal to VSS. If unused this terminal should be left open. The VCO can be connected either directly or through frequency dividers to the comparator input of the phase comparators. A full CMOS logic swing is available at the output of the VCO and allows direct coupling to CMOS frequency dividers such as the RCA-CD4024, CD4018, CD4020, CD4022, CD4029, and CD4059. One or more CD4018 (Presettable Divide-by-N Counter) or CD4029 (Presettable Up/Down Counter), or CD4059A (Programmable Divide-by-N Counter), together with the CD4046B (Phase-Locked Loop) can be used to build a micropower low-frequency synthesizer. A logic 0 on the INHIBIT input "enables" the VCO and the source follower, while a logic 1 "turns off" both to minimize stand-by power consumption.

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})	-0.5V to +20V
Voltages referenced to V_{SS} Terminal)	
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5V to $V_{DD} + 0.5V$
DC INPUT CURRENT, ANY ONE INPUT	$\pm 10\mu A$
POWER DISSIPATION PER PACKAGE (P_D):	
For $T_A = -55^\circ C$ to $+100^\circ C$	500mW
For $T_A = +100^\circ C$ to $+125^\circ C$	Derate Linearly at 12mW/ $^\circ C$ to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR $T_A =$ FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100mW
OPERATING-TEMPERATURE RANGE (T_A)	$-55^\circ C$ to $+125^\circ C$
STORAGE TEMPERATURE RANGE (T_{stg})	$-65^\circ C$ to $+150^\circ C$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 \pm 1/32 inch (1.59 \pm 0.79mm) from case for 10s max	+265 $^\circ C$

Features:

- Very low power consumption: 70 μW (typ.) at VCO $f_o = 10$ kHz, $V_{DD} = 5$ V
- Operating frequency range up to 1.4 MHz (typ.) at $V_{DD} = 10$ V, $R1 = 5$ k Ω
- Low frequency drift: 0.04%/ $^\circ C$ (typ.) at $V_{DD} = 10$ V
- Choice of two phase comparators: Exclusive-OR network (I) Edge-controlled memory network with phase-pulse output for lock indication (II)
- High VCO linearity: <1% (typ.) at $V_{DD} = 10$ V
- VCO inhibit control for ON-OFF keying and ultra-low standby power consumption
- Source-follower output of VCO control input (Demod. output)
- Zener diode to assist supply regulation
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"



Applications:

- FM demodulator and modulator
- Frequency synthesis and multiplication
- Frequency discriminator
- Data synchronization
- Voltage-to-frequency conversion
- Tone decoding
- FSK - Modems
- Signal conditioning
- (See ICAN-6101) "RCA COS/MOS Phase-Locked Loop - A Versatile Building Block for Micropower Digital and Analog Applications"

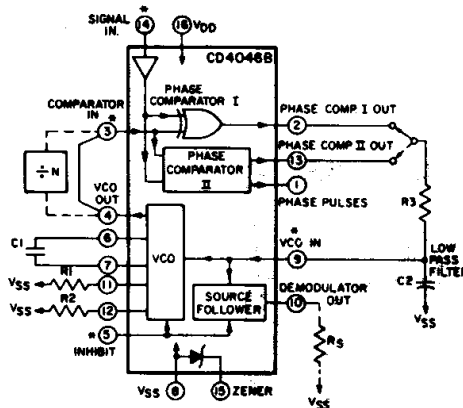
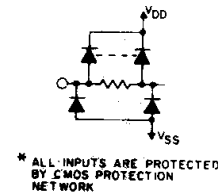


Fig.1 - CMOS phase-locked loop block diagram.



* ALL INPUTS ARE PROTECTED BY CMOS PROTECTION NETWORK

92C9-29172

Phase Comparators

The phase-comparator signal input (terminal 14) can be direct-coupled provided the signal swing is within CMOS logic levels [logic "0" $\leq 30\%$ ($V_{DD}-V_{SS}$), logic "1" $\geq 70\%$ ($V_{DD}-V_{SS}$)]. For smaller swings the signal must be capacitively coupled to the self-biasing amplifier at the signal input.

Phase comparator I is an exclusive-OR network; it operates analogously to an overdriven balanced mixer. To maximize the lock range, the signal- and comparator-input frequencies must have a 50% duty cycle. With no signal or noise on the signal input, this phase comparator has an average output voltage equal to $V_{DD}/2$. The low-pass filter connected to the output of phase comparator

CD4046B Types

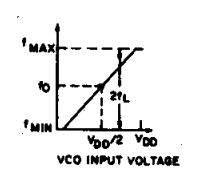
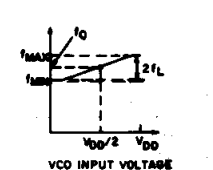
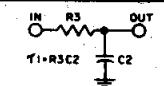
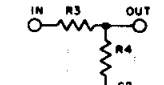
RECOMMENDED OPERATING CONDITIONS at T_A = Full Package-Temperature Range
 For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range VCO Section: As Fixed Oscillator Phased-Lock-Loop Operation	3	18	V
	5	18	
Supply-Voltage Range Phase Comparator Section: Comparators VCO Operation	3	18	
	5	18	

DESIGN INFORMATION

This information is a guide for approximating the values of external components for the CD4046B in a Phase-Locked-Loop system.

The selected external components must be within the following ranges:
 $5\text{ k}\Omega \leq R_1, R_2, R_S \leq 1\text{ M}\Omega$
 $C_1 \geq 100\text{ pF}$ at $V_{DD} \geq 5\text{ V}$;
 $C_1 \geq 50\text{ pF}$ at $V_{DD} \geq 10\text{ V}$

Characteristics	Phase Comparator Used	Design Information
VCO Frequency	1	VCO WITHOUT OFFSET $R_2 = \infty$ 
	2	VCO WITH OFFSET 
For No. Signal Input	1	Same as for No. 1
	2	VCO will adjust to lowest operating frequency, f_{min}
Frequency Lock Range, $2f_L$	1	$2f_L = \text{full VCO frequency range}$ $2f_L = f_{max} - f_{min}$
	2	Same as for No. 1
Frequency Capture Range, $2f_C$	1	 $2f_C \approx \frac{1}{\pi} \sqrt{\frac{2\pi f_L}{\tau_1}}$
	2	For $2f_C$, see Ref. (2)
Loop Filter Component Selection	1	 $f_C = f_L$
	2	$f_C = f_L$
Phase Angle Between Signal and Comparator	1	90° at center frequency (f_0) approximating 0° and 180° at ends of lock range ($2f_L$)
	2	Always 0° in lock
Locks On Harmonic of Center Frequency	1	Yes
	2	No
Signal Input Noise Rejection	1	High
	2	Low

For further information, see

- (1) F. Gardner, "Phase-Lock Techniques" John Wiley and Sons, New York, 1966
- (2) G. S. Moschytz, "Miniaturized RC Filters Using Phase-Locked Loop", BSTJ, May, 1965.

I supplies the averaged voltage to the VCO input, and causes the VCO to oscillate at the center frequency (f_0).

The frequency range of input signals on which the PLL will lock if it was initially out of lock is defined as the frequency capture range ($2f_C$).

The frequency range of input signals on which the loop will stay locked if it was initially in lock is defined as the frequency lock range ($2f_L$). The capture range is \leq the lock range.

With phase comparator I the range of frequencies over which the PLL can acquire lock (capture range) is dependent on the low-pass-filter characteristics, and can be made as large as the lock range. Phase-comparator I enables a PLL system to remain in lock in spite of high amounts of noise in the input signal.

One characteristic of this type of phase comparator is that it may lock onto input frequencies that are close to harmonics of the VCO center-frequency. A second characteristic is that the phase angle between the signal and the comparator input varies between 0° and 180° , and is 90° at the center frequency. Fig. 2 shows the typical, triangular, phase-to-output response characteristic of phase-comparator I. Typical waveforms for a CMOS phase-locked-loop employing phase comparator I in locked condition of f_0 is shown in Fig. 3.

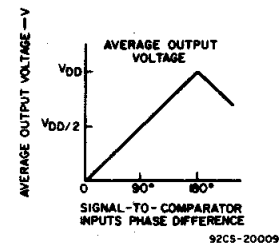


Fig. 2 - Phase-comparator I characteristics at low-pass filter output.

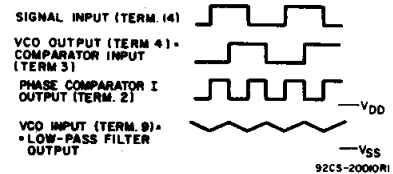


Fig. 3 - Typical waveforms for CMOS phase-locked loop employing phase comparator in locked condition of f_0 .

Phase-comparator II is an edge-controlled digital memory network. It consists of four flip-flop stages, control gating, and a three-state output circuit comprising p- and n-type drivers having a common output node. When the p-MOS or n-MOS drivers are ON they pull the output up to V_{DD} or down to V_{SS} , respectively. This type of phase-comparator acts only on the positive edges of the signal and comparator inputs. The duty cycles of the signal and comparator inputs are not important since positive transitions

COMMERCIAL CMOS HIGH VOLTAGE ICs

CD4046B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V _O (V)	V _{IN} (V)	V _{DD} (V)	-55	-40	+85	+125	+25			
								Min.	Typ.	Max.	
VCO Section											
Output Low (Sink) Current I _{OL} Min.	0.4	0.5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA
	0.5	0.10	10	1.6	1.5	1.1	0.9	1.3	2.6	—	
	1.5	0.15	15	4.2	4	2.8	2.4	3.4	6.8	—	
Output High (Source) Current, I _{OH} Min.	4.6	0.5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	—	mA
	2.5	0.5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	—	
	9.5	0.10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	—	
	13.5	0.15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	—	
Output Voltage: Low-Level, V _{OL} Max.	Term. 4 driving CMOS	0.5	5	0.05			—	0	0.05	V	
		0.10	10	0.05			—	0	0.05		
		0.15	15	0.05			—	0	0.05		
Output Voltage: High-Level, V _{OH} Min.	e.g. Term. 3	0.5	5	4.95			4.95	5	—	V	
		0.10	10	9.95			9.95	10	—		
		0.15	15	14.95			14.95	15	—		
Input Current I _{IN} Max.	—	0.18	18	±0.1	±0.1	±1	±1	—	±10 ⁻⁵	±0.1	μA
Phase Comparator Section											
Total Device Current, I _{DD} Max. Term. 14 open, Term. 5 = V _{DD}	—	0.5	5	0.2			—	0.1	0.2	mA	
	—	0.10	10	1			—	0.5	1		
	—	0.15	15	1.5			—	0.75	1.5		
	—	0.20	20	4			—	2	4		
Term. 14 = V _{SS} or V _{DD} , Term. 5 = V _{DD}	—	0.5	5	20			—	10	20	μA	
	—	0.10	10	40			—	20	40		
	—	0.15	15	80			—	40	80		
	—	0.20	20	160			—	80	160		
Output Low (Sink) Current I _{OL} Min.	0.4	0.5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA
	0.5	0.10	10	1.6	1.5	1.1	0.9	1.3	2.6	—	
	1.5	0.15	15	4.2	4	2.8	2.4	3.4	6.8	—	
Output High (Source) Current I _{OH} Min.	4.6	0.5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	—	mA
	2.5	0.5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	—	
	9.5	0.10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	—	
	13.5	0.15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	—	
DC-Coupled Signal Input and Comparator Input Voltage Sensitivity	0.5,4.5	—	5	1.5			—	—	1.5	V	
	1.9	—	10	3			—	—	3		
	1.5,13.5	—	15	4			—	—	4		
	0.5,4.5	—	5	3.5			3.5	—	—		
	1.9	—	10	7			7	—	—		
	1.5,13.5	—	15	11			11	—	—		

control the PLL system utilizing this type of comparator. If the signal-input frequency is higher than the comparator-input frequency, the p-type output driver is maintained ON most of the time, and both the n and p drivers OFF (3 state) the remainder

of the time. If the signal-input frequency is lower than the comparator-input frequency, the n-type output driver is maintained ON most of the time, and both the n and p drivers OFF (3 state) the remainder of the time. If the signal- and comparator-

input frequencies are the same, but the signal input lags the comparator input in phase, the n-type output driver is maintained ON for a time corresponding to the phase difference. If the signal- and comparator-input frequencies are the same, but

CD4046B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V _O (V)	V _{IN} (V)	V _{DD} (V)	-55	-40	+85	+125	+25			
								Min.	Typ.	Max.	
Phase Comparator Section (cont'd)											
Input Current I _{IN} Max. (except Term.14)	-	0.18	18	±0.1	±0.1	±1	±1	-	±10 ⁻⁵	±0.1	μA
3-State Leakage Current, I _{OUT} Max.	0.18	0.18	18	±0.1	±0.1	±0.2	±0.2	-	±10 ⁻⁵	±0.1	μA

*Limit determined by minimum feasible leakage current measurement for automatic testing.

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	TEST CONDITIONS	V _{DD} (V)	LIMITS			UNITS	
			Min.	Typ.	Max.		
VCO Section							
Operating Power Dissipation, P _D	f _o = 10 kHz R ₂ = ∞ VCO _{IN} = $\frac{V_{DD}}{2}$	R ₁ = 1 MΩ	5	-	70	140	μW
			10	-	800	1600	
			15	-	3000	6000	
Maximum Operating Frequency f _{max}	C ₁ = 50 pF R ₂ = ∞ VCO _{IN} = V _{DD}	R ₁ = 10 kΩ	5	0.3	0.6	-	MHz
			10	0.6	1.2	-	
			15	0.8	1.6	-	
	C ₁ = 50 pF R ₂ = ∞ VCO _{IN} = V _{DD}	R ₁ = 5 kΩ	5	0.5	0.8	-	
			10	1	1.4	-	
			15	1.4	2.4	-	
Center Frequency (f _o) and Frequency Range (f _{max} - f _{min})	Programmable with external components R1, R2, and C1 See Design Information						
Linearity	VCO _{IN} = 2.5 V ± 0.3V, R ₁ = 10 kΩ		5	-	1.7	-	%
	= 5 V ± 1 V, = 100 kΩ		10	-	0.5	-	
	= 5 V ± 2.5 V, = 400 kΩ		10	-	4	-	
	= 7.5 V ± 1.5 V, = 100 kΩ		15	-	0.5	-	
	= 7.5 V ± 5 V, = 1 MΩ		15	-	7	-	
Temperature-Frequency Stability: No Frequency Offset f _{MIN} = 0			5	-	±0.12	-	%°C
			10	-	±0.04	-	
			15	-	±0.015	-	
Frequency Offset f _{MIN} ≠ 0			5	-	±0.09	-	
			10	-	±0.07	-	
			15	-	±0.03	-	
Output Duty Cycle			5,10,15	-	50	-	%
Output Transition Times, t _{THL} , t _{TLH}			5	-	100	200	ns
			10	-	50	100	
			15	-	40	80	

the comparator input lags the signal in phase, the p-type output driver is maintained ON for a time corresponding to the phase difference. Subsequently, the capacitor voltage of the low-pass filter connected to this phase comparator is adjusted until the signal and comparator inputs are equal in both phase and frequency. At this stable point both p- and n-type output drivers remain OFF and thus the phase comparator output becomes an open circuit and holds the voltage on the capacitor of the low-pass filter constant. Moreover the signal at the "phase pulses" output is a high level which can be used for indicating a locked condition. Thus, for phase comparator II, no phase difference exists between signal and comparator input over the full VCO frequency range. Moreover, the power dissipation due to the low-pass filter is reduced when this type of phase comparator is used because both the p- and n-type output drivers are OFF for most of the signal input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range, independent of the low-pass filter. With no signal present at the signal input, the VCO is adjusted to its lowest frequency for phase comparator II. Fig. 10 shows typical waveforms for a CMOS PLL employing phase comparator II in a locked condition.

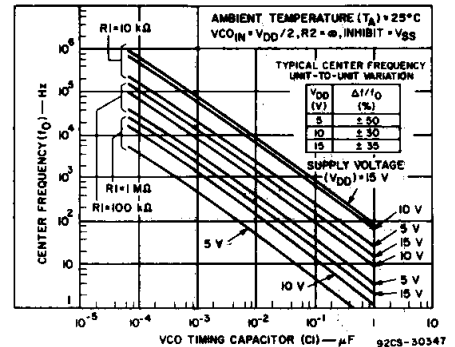


Fig. 4 - Typical center frequency as a function of C1 and R1 at V_{DD} = 5 V, 10 V, and 15 V.

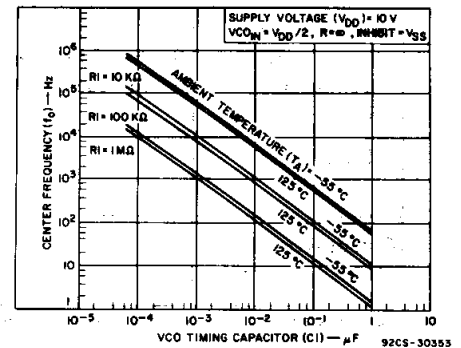


Fig. 5 - Center frequency as a function of C1 and R1 for ambient temperatures of -55°C to 125°C.

3
COMMERCIAL CMOS
HIGH VOLTAGE ICs

CD4046B Types

ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$

CHARACTERISTIC	TEST CONDITIONS	V_{DD} (V)	LIMITS			UNITS
			ALL TYPES			
			Min.	Typ.	Max.	
VCO Section (cont'd)						
Source-Follower Output (Demodulated Output): Offset Voltage $ V_{COIN} - V_{DEM} $	$R_S > 10\text{ k}\Omega$	5 10 15	—	1.8	2.5	V
Linearity	$R_S = 100\text{ k}\Omega$ $= 300\text{ k}\Omega$ $= 500\text{ k}\Omega$	$V_{COIN} = 2.5 \pm 0.3\text{ V}$ $= 5 \pm 2.5\text{ V}$ $= 7.5 \pm 5\text{ V}$	5 10 15	—	0.3 0.7 0.9	— — —
Zener Diode Voltage (V_Z)	$I_Z = 50\text{ }\mu\text{A}$		4.45	5.5	6.15	V
Zener Dynamic Resistance, R_Z	$I_Z = 1\text{ mA}$		—	40	—	Ω
Phase Comparator Section						
Term. 14 (SIGNAL IN) Input Resistance R_{14}		5 10 15	1 0.2 0.1	2 0.4 0.2	— — —	$M\Omega$
AC Coupled Signal Input Voltage Sensitivity* (peak-to-peak)	$f_{IN} = 100\text{ kHz}$, sine wave	5 10 15	— — —	180 330 900	360 660 1800	mV
Propagation Delay Times, Terms. 14 to 1: High to Low Level, t_{PHL}		5 10 15	— — —	225 100 65	450 200 130	ns
Low to High Level, t_{PLH}		5 10 15	— — —	350 150 100	700 300 200	ns
3-State Propagation Delay Times, Terms. 3 to 13: High Level to High Impedance, t_{PHZ}		5 10 15	— — —	225 100 95	450 200 190	ns
Terms. 14 to 13: Low Level to High Impedance, t_{PLZ}		5 10 15	— — —	285 130 95	570 260 190	ns
Input Rise or Fall Times, t_r , t_f Comparator Input, Term. 3	See Fig. 5 for Phase Comp. II output loading	5 10 15	— — —	— — —	50 1 0.3	μs
Signal Input, Term. 14		5 10 15	— — —	— — —	500 20 2.5	μs
Output Transition Times, t_{THL} , t_{TLH}		5 10 15	— — —	100 50 40	200 100 80	ns

* For sine wave, the frequency must be greater than 10 kHz for Phase Comparator II.

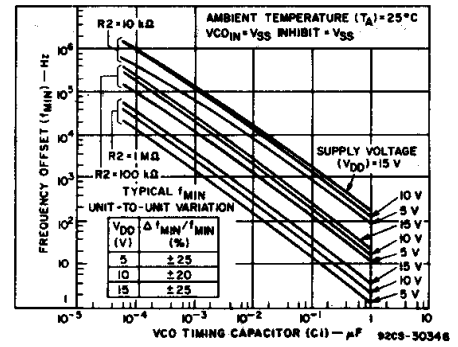


Fig. 6 - Typical frequency offset as a function of C_1 and R_2 for $V_{DD} = 5\text{ V}$, 10 V , and 15 V .

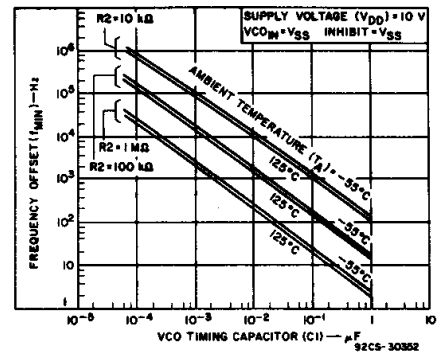


Fig. 7 - Frequency offset as a function of C_1 and R_2 for ambient temperatures of -55°C to 125°C .

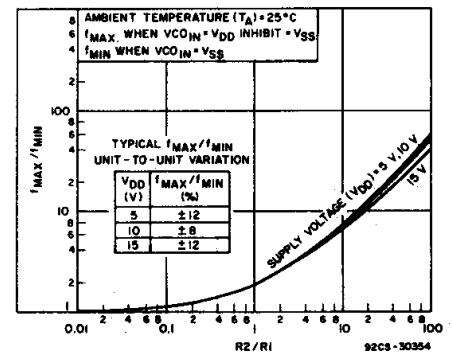


Fig. 8 - Typical f_{MAX}/f_{MIN} as a function of R_2/R_1 .

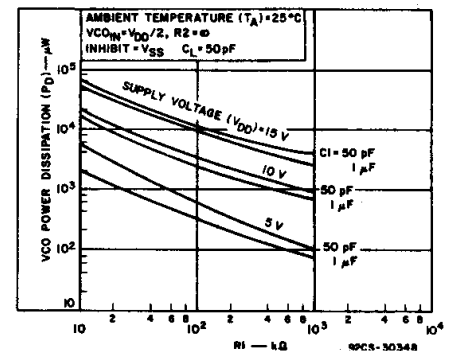


Fig. 9 - Typical VCO power dissipation at center frequency as a function of R_1 .

CD4046B Types

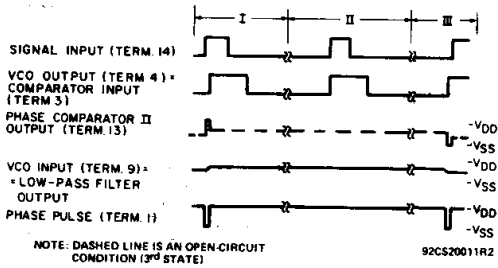


Fig. 10 - Typical waveforms for COS/MOS phase-locked loop employing phase comparator II in locked condition.

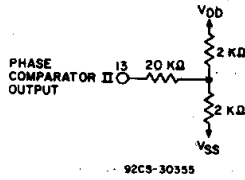


Fig. 11 - Phase comparator II output loading circuit.

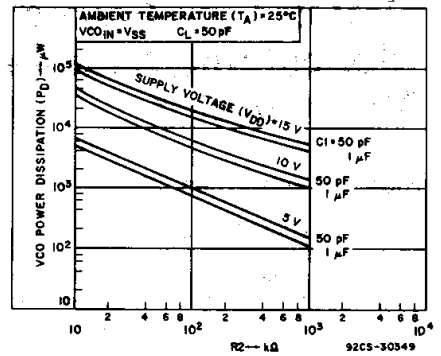


Fig. 12 - Typical VCO power dissipation at f_{MIN} as a function of R_2 .

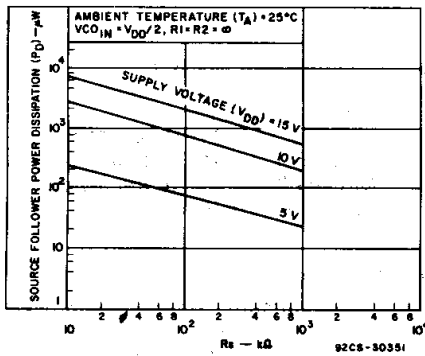


Fig. 13 - Typical source follower power dissipation as a function of R_s .

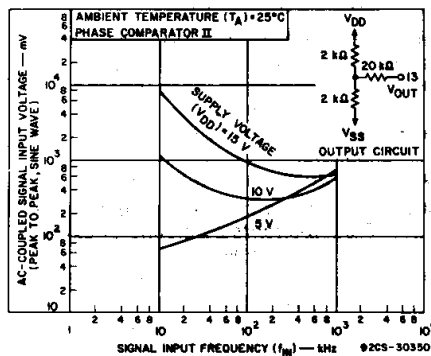


Fig. 14 - AC-coupled signal input voltage as a function of signal input frequency.

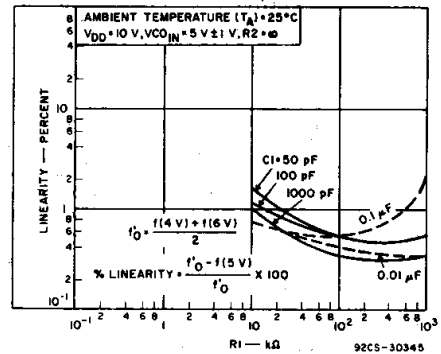


Fig. 15 - Typical VCO linearity as a function of R_1 and C_1 at $V_{DD} = 10$ V.

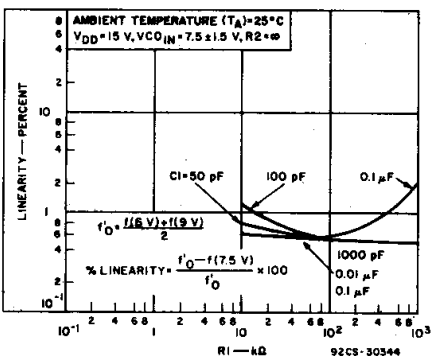
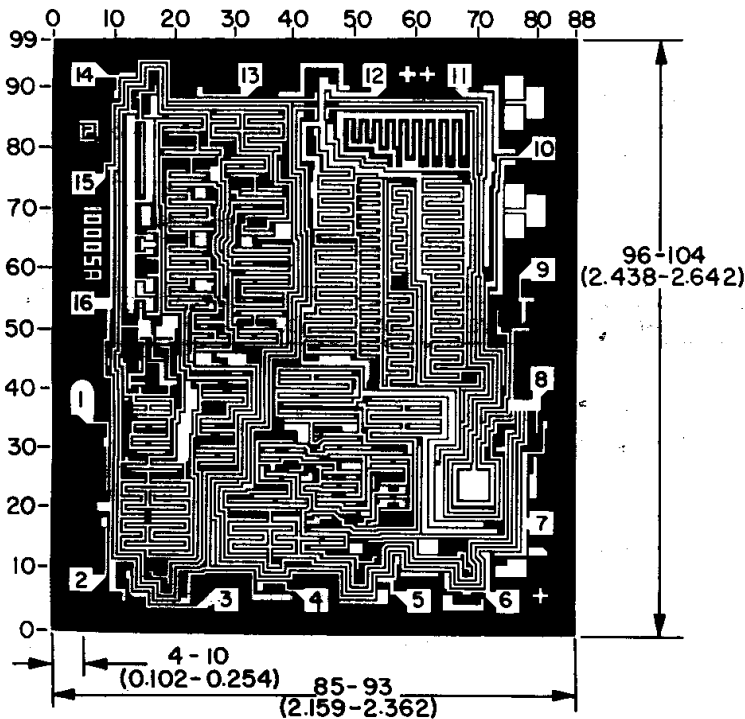


Fig. 16 - Typical VCO linearity as a function of R_1 and C_1 at $V_{DD} = 15$ V.



92CM-36467

Dimensions and pad layout for CD4046BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

3
COMMERCIAL CMOS
HIGH VOLTAGE ICs

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9466401MEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9466401ME A CD4046BF3A	Samples
CD4046BE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD4046BE	Samples
CD4046BEE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD4046BE	Samples
CD4046BF	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD4046BF	Samples
CD4046BF3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9466401ME A CD4046BF3A	Samples
CD4046BNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4046B	Samples
CD4046BNSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4046B	Samples
CD4046BNSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4046B	Samples
CD4046BPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM046B	Samples
CD4046BPWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM046B	Samples
CD4046BPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM046B	Samples
CD4046BPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM046B	Samples
CD4046BPWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM046B	Samples
CD4046BPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM046B	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD4046B, CD4046B-MIL :

● Catalog: [CD4046B](#)

● Military: [CD4046B-MIL](#)

NOTE: Qualified Version Definitions:

● Catalog - TI's standard catalog product

● Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4046BNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD4046BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4046BNSR	SO	NS	16	2000	367.0	367.0	38.0
CD4046BPWR	TSSOP	PW	16	2000	367.0	367.0	35.0

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE

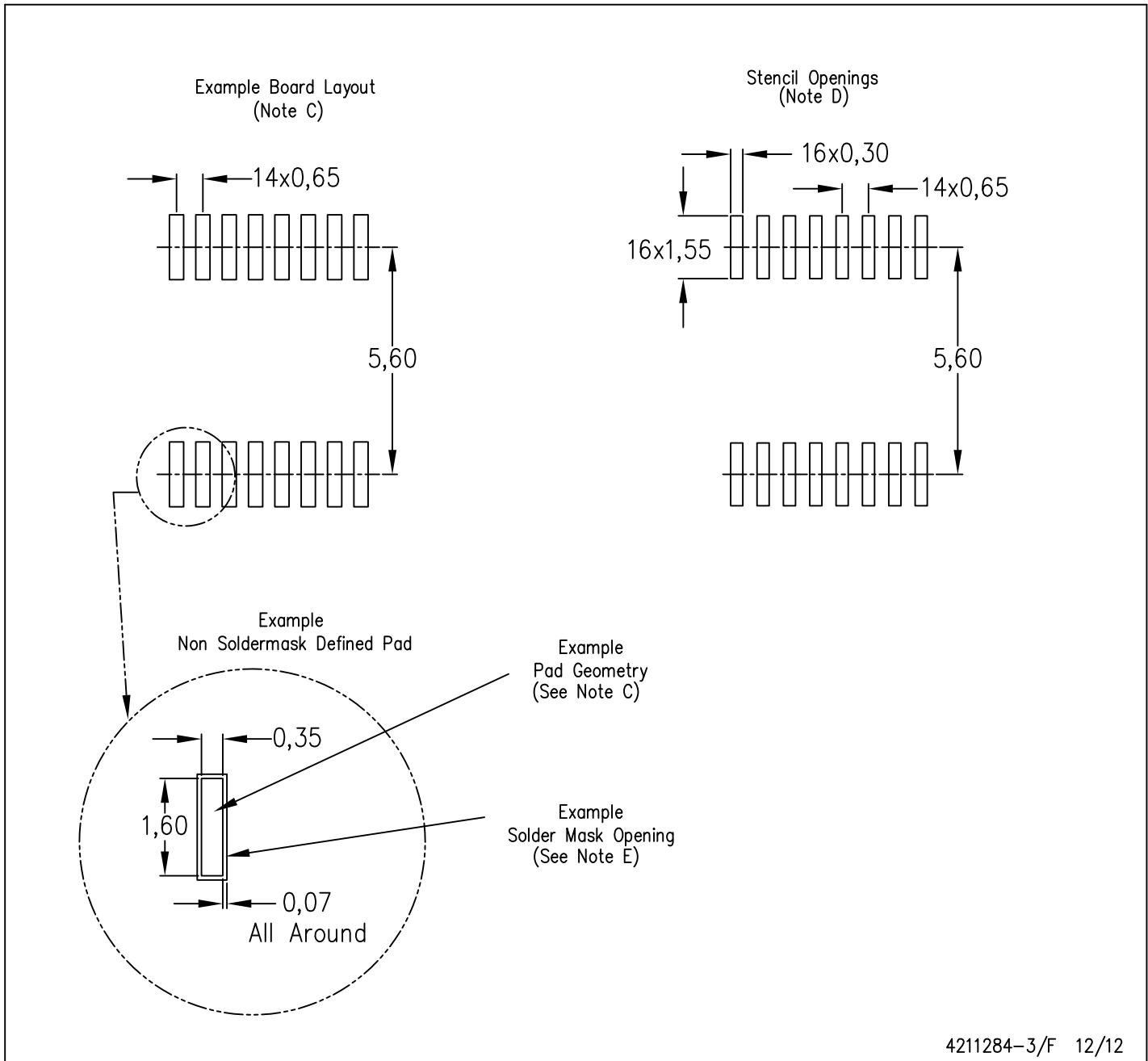


4040064-4/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com



Стандарт Электрон Связь

Мы молодая и активно развивающаяся компания в области поставок электронных компонентов. Мы поставляем электронные компоненты отечественного и импортного производства напрямую от производителей и с крупнейших складов мира.

Благодаря сотрудничеству с мировыми поставщиками мы осуществляем комплексные и плановые поставки широчайшего спектра электронных компонентов.

Собственная эффективная логистика и склад в обеспечивает надежную поставку продукции в точно указанные сроки по всей России.

Мы осуществляем техническую поддержку нашим клиентам и предпродажную проверку качества продукции. На все поставляемые продукты мы предоставляем гарантию .

Осуществляем поставки продукции под контролем ВП МО РФ на предприятия военно-промышленного комплекса России , а также работаем в рамках 275 ФЗ с открытием отдельных счетов в уполномоченном банке. Система менеджмента качества компании соответствует требованиям ГОСТ ISO 9001.

Минимальные сроки поставки, гибкие цены, неограниченный ассортимент и индивидуальный подход к клиентам являются основой для выстраивания долгосрочного и эффективного сотрудничества с предприятиями радиоэлектронной промышленности, предприятиями ВПК и научно-исследовательскими институтами России.

С нами вы становитесь еще успешнее!

Наши контакты:

Телефон: +7 812 627 14 35

Электронная почта: sales@st-electron.ru

Адрес: 198099, Санкт-Петербург,
Промышленная ул, дом № 19, литера Н,
помещение 100-Н Офис 331