DATASHEET

TEN CHANNEL HD AUDIO CODEC

92HD68F

Low Power Optimized for ECR15b and EuP

Description

The 92HD68F is a low power optimized, high fidelity, 10-channel audio codec compatible with Intel's High Definition (HD) Audio Interface.

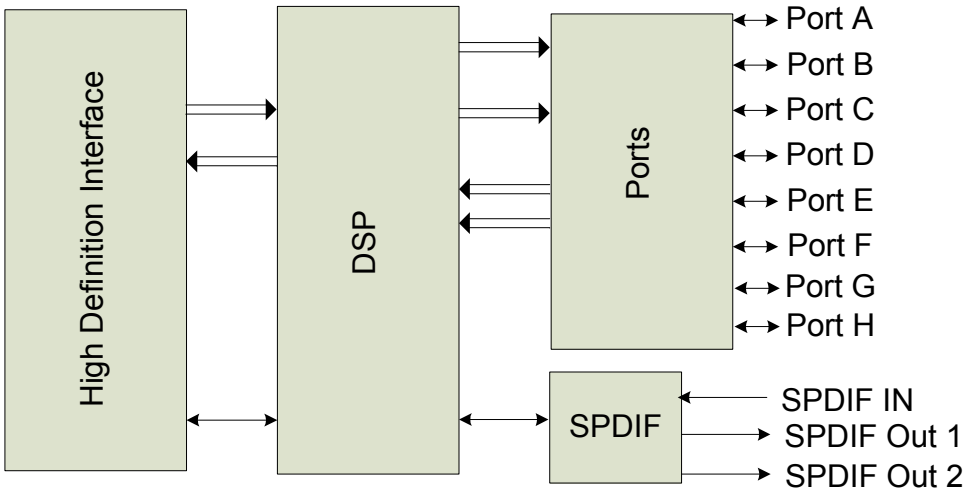
The 92HD68F provides full rate lossless audio playback from Blu-ray or other protected content with stereo 24-bit resolution and sample rates up to 192kHz.

The 92HD68F provides high quality, HD Audio capability to notebook and desktop PC applications.

Features

- **10 Channels (5 stereo DACs and 2 stereo ADCs) with 24-bit resolution**
  - Supports full-duplex 7.1 audio and simultaneous VoIP
- **Supports full rate lossless audio playback from blu-ray or other protected audio content**
- **ECR 15b and EuP low power support**
- **Microsoft WLP premium logo compliant, per Logo Point**
- **8 analog ports with port presence detect + CD In**
- **3 integrated headphone amps**
- **4 adjustable VREF Out pins for microphone bias**
- **Dual SPDIF for WLP compliant support of simultaneous HDMI and SPDIF output**
- **SPDIF Input**
- **Digital microphone input (mono or stereo or quad)**
- **High performance analog mixer**
- **Support for 1.5V and 3.3V HDA signaling**
- **Digital and Analog PC Beep to all outputs**
- **48-pin QFP and 40-pad QFN RoHS packages**

Block Diagram



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Software Support

- Intuitive TSI HD Sound graphical user interface that allows configurability and preference settings
- 12 band fully parametric equalizer
  - Constant, system-level effects tuned to optimize a particular platform can be combined with user-mode “presets” tailored for specific acoustical environments and applications
  - System-level effects automatically disabled when external audio connections made
- Dynamics Processing
  - Enables improved voice articulation
  - Compressor/limiter allows higher average volume level without resonances or damage to speakers.
- TSI Vista APO wrapper
  - Enables multiple APOs to be used with the TSI Driver
- Microphone Beam Forming, Acoustic Echo Cancellation, and Noise Suppression
- Dynamic Stream Switching
  - Improved multi-streaming user experience with less support calls
- Broad 3rd party branded software including Creative, Dolby, DTS, and SRS
- Smart Configuration Suite (SCS) improves time to market and software quality
  - Online pin and feature configuration tool generates BIOS verb table for Windows and Linux.
  - Downloadable WHQL compliant, self configurable driver for XP, Vista and Win7 based on verb table and test files generated.
  - BIOS verb tables can be tested with the self configurable driver prior to flashing into BIOS.

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1. DESCRIPTION

1.1. Overview

The 92HD68F is a high fidelity, 10-channel audio codec compatible with the Intel High Definition (HD) Audio Interface. The 92HD68F provides full rate lossless audio playback from Blu-ray or other protected content with stereo 24-bit resolution and sample rates up to 192kHz. The 92HD68F codec provides high quality, HD Audio capability notebooks and desktops.

The 92HD68F is designed to meet or exceed premium logo requirements for Microsoft's Windows Logo Program (WLP) per Logo Point.

The 92HD68F provides stereo 24-bit, full duplex resolution supporting sample rates up to 192kHz by the DAC and ADC. 92HD68F SPDIF outputs support sample rates of 192kHz, 176.4kHz, 96kHz, 88.2kHz, 48kHz, and 44.1kHz.

The 92HD68F supports a wide range of notebook and desktop 10-channel configurations. The 2 independent SPDIF output interfaces provides connectivity to Consumer Electronic equipment like Dolby Digital decoders, powered speakers, mini disk drives or to a home entertainment system. Simultaneous HDMI and SPDIF output is possible.

MIC inputs can be programmed with 0/10/20/30dB boost. For more advanced configurations, the 92HD68F has up to 7 General Purpose I/O (GPIO).

The port presence detect capabilities allow the codecs to detect when audio devices are connected to the codec. The fully parametric IDT SoftEQ can be initiated upon headphone jack insertion and removal for protection of notebook speakers.

The 92HD68F operates with a 3.3V digital supply and a 5V analog supply. It can also work with 1.5V and 3.3V HDA signaling.

The 92HD68F is available in a 48-pin QFP or 40-pad QFN Environmental (ROHS) package.

1.2. Orderable Part Numbers

92HD68F1X5NDGXyyX	5V Analog, 40QFN, 1.5V HDA Signaling
92HD68F2X5NDGXyyX	5V Analog, 40QFN, 3.3V HDA Signaling
92HD68F3X5PRGXyyX	5V Analog, 48QFP, switchable 1.5V or 3.3V HDA Signaling

yy = silicon stepping/revision, contact sales for current data.
Add an "8" to the end for tape and reel delivery.

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1.3. Block Diagram

Figure 1. 92HD68F Block Diagram

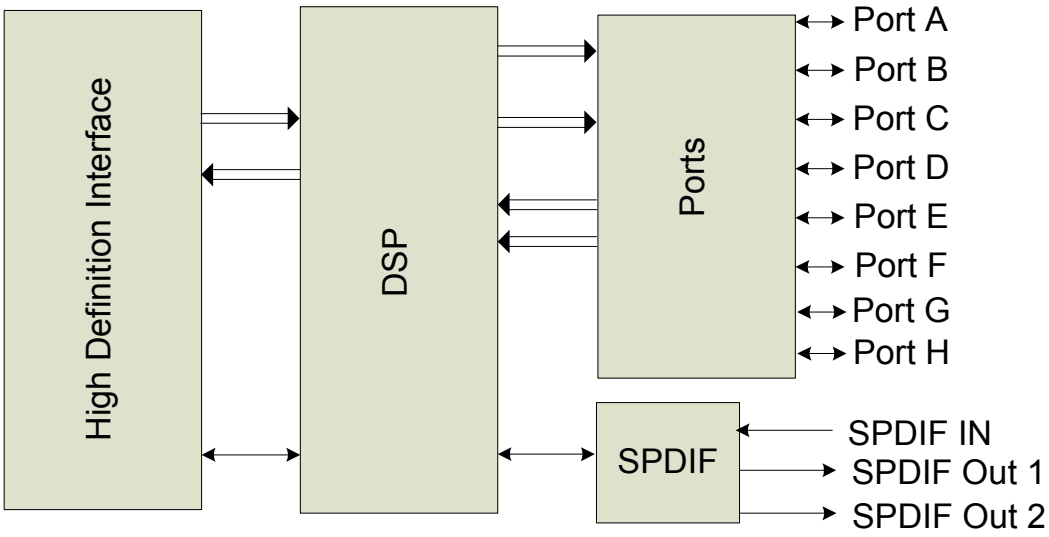
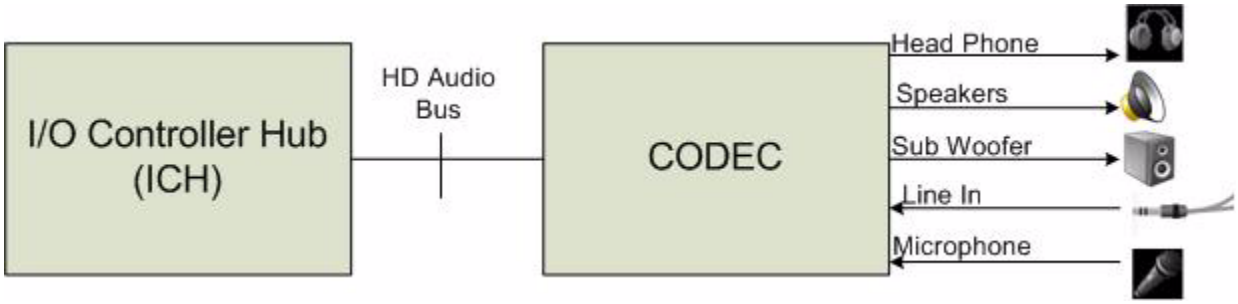


Figure 2. System Diagram



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2. DETAILED DESCRIPTION

2.1. Port Functionality

Multi-function (Input / output) ports allow for the highest possible flexibility. 8 bi-directional ports, 3 are headphone capable, support a wide variety of consumer desktop and mobile system use models.

Pins	Port	Input	Output	Headphone	Mic Bias (Vref pin)	Input boost amp
39/41	A	Yes	Yes	Yes	Yes	Yes
21/22	B	Yes	Yes	Yes	Yes	Yes
23/24	C	Yes	Yes		Yes	Yes
35/36	D	Yes	Yes	Yes		Yes
14/15	E	Yes	Yes		Yes	Yes
16/17	F	Yes	Yes			Yes
43/44	G	Yes	Yes			Yes
45/46	H	Yes	Yes			Yes
48	SPDIF_OUT0		Yes			
40	SPDIF_OUT1		Yes			
47	SPDIF_IN/OUT1	Yes	Yes			
4 (CLK=2)	DMIC0	Yes				Yes
30 (CLK=2)	DMIC1	Yes				Yes

Table 1. 48QFP Port Characteristics

Pins	Port	Input	Output	Headphone	Mic Bias (Vref pin)	Input boost amp
33/34	A	Yes	Yes	Yes	Yes	Yes
18/19	B	Yes	Yes	Yes	Yes	Yes
20/21	C	Yes	Yes			Yes
29/30	D	Yes	Yes	Yes		Yes
11/12	E	Yes	Yes		Yes	Yes
13/14	F	Yes	Yes			Yes
36/37	G	Yes	Yes			Yes
38/39	H	Yes	Yes			Yes
1	SPDIF_OUT0		Yes			
40	SPDIF_OUT1		Yes			

Table 2. 40QFN Port Characteristics

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2.1.1. Port Characteristics

Universal (Bi-directional) jacks are supported on ports A, B, C, D, E, F, G and H for all family members. Ports A, B, and D are designed to drive 32 ohm (nominal) headphones or a 10K (nominal) load. Line Level outputs are intended to drive an external 10K load (nominal) and an on board shunt resistor of 20-47K (nominal). However, applications may support load impedances of 2.8K ohms and above when implementing ports capable of operating as microphone inputs or line outputs. Input ports are 75K (nominal) at the pin.

DAC full scale outputs and intended full scale input levels are greater than 1V rms at 5V (+5%/-10%) to meet WLP requirements. Line output ports and Headphone output ports on the 92HD68F codec may be configured for +3dBV full scale output levels by using a vendor specific verb.

Output ports are always on to prevent pops/clicks associated with charging and discharging output coupling capacitors. This maintains proper bias on output coupling caps even in power state D3 as long as AVDD is available. Unused ports should be left unconnected. When updating existing designs, ensure that there are no conflicts between the output ports on the codec and existing circuitry.

AFG Power State	Input Enable	Output Enable	Port Behavior
D0-D1	1	1	Not allowed. Port is active as Input.
	1	0	Active - Port enabled as input
	0	1	Active - Port enabled as output
	0	0	Inactive -port is powered on (low output impedance) but drives silence only.
D2	1	1	Not allowed. Port is active as Input.
	1	0	Inactive - Port enabled as input but powered down
	0	1	Active - Port enabled as output
	0	0	Inactive -port is powered on (low output impedance) but drives silence only.
D3	1	1	Not allowed. Port is active as Input.
	1	0	Inactive (lower power) - Port keeps output coupling caps charged.
	0	1	Low power state. If enabled, Beep will output from the port
	0	0	Inactive (lower power) - Port keeps output coupling caps charged.
D3cold	-	-	Inactive (lower power) - Port keeps output coupling caps charged.
D4	-	-	Inactive (lower power) - Port keeps output coupling caps charged.
D5	-	-	Off - Charge on coupling caps will not be maintained.

Table 3. Analog Output Port Behavior

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2.1.2. Vref_Out

Ports A, B, C (48-pin package only), & E support Vref_Out pins for biasing electret cartridge microphones. Settings of 80% AVDD, 50% AVDD, GND, and Hi-Z are supported. Attempting to program a pin widget control with a reserved or unsupported value will cause the associated Vref_Out pin to assume a Hi-Z state and the pin widget control Vref_En field will return a value of '000' (Hi-Z) when read.

2.1.3. Jack Detect

Plugs inserted to a jack are detected using SENSE inputs as described in the tables below. Per ECR15-B, the detection circuit operates when the CODEC is in D0 - D3 and can also operate if both the CODEC and Controller are in D3 (no bus clock.) Jack detection requires that all supplies (analog and digital) are active and stable. When AVDD is not present, the value reported in the pin widget is invalid.

When the HD Audio bus is in a low power state (reset asserted and clock stopped) the CODEC will generate a Power State Change Request when a change in port connectivity is sensed and then generate an unsolicited response after the HD Audio link has been brought out of a low power state and the device has been enumerated. Per ECR015-B, this will take less than 10mS.

The following table summarizes the proper resistor tolerances for different analog supply voltages.

AVdd Nominal Voltage (+/- 5%)	Resistor Tolerance Pull-Up	Resistor Tolerance SENSE_A/B/C
4.75 or 5VV	1%	1%

Resistor	SENSE_A	SENSE_B	SENSE_C
39.2K	PORT A	PORT E	SPDIFOUT0
20.0K	PORT B	PORT F	SPDIFOUT1(pin40)
10.0K	PORT C	PORT G	DMIC0
5.11K	PORT D	Port H	DMIC1
2.49K	Pull-up to AVDD	Pull-up to AVDD	Pull-up to AVDD

Table 4. 48pin Jack Detect

Resistor	SENSE_A	SENSE_B
39.2K	PORT A	PORT E
20.0K	PORT B	PORT F
10.0K	PORT C	PORT G
5.11K	PORT D	PORT H
2.49K	Pull-up to AVDD	Pull-up to AVDD

Table 5. 40pin Jack Detect

See reference design for more information on Jack Detect implementation.

2.1.4. SPDIF Output

Both SPDIF Outputs can operate at 44.1kHz, 48kHz, 88.2kHz, 96kHz and 192KHz as defined in the Intel High Definition Audio Specification with resolutions up to 24 bits. This insures compatibility with

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all consumer audio gear and allows for convenient integration into home theater systems and media center PCs.

The two SPDIF output converters can not be aligned in phase with the DACs. Even when attached to the same stream, the two SPDIF output converters may be misaligned with respect to their frame boundaries.

Per the HDA015-B ECR, the SPDIF outputs support the ability to provide clocking information even when no stream is selected for the converter, or when in a low power state. Also, as stated in the ECR, the SPDIF output ports support port presence detect.

SPDIF Outputs are outlined in tables below.

AFG Power State	RESET#	Output Enable	Keep Alive Enable	Converter Dig Enable	Stream ID	Pin Behavior
D0-D3	Asserted (Low)	-	-	-	-	Hi-Z[1] immediately after power on, otherwise the previous state is retained.
D0	De-Asserted (High)	Disabled	-	-	-	Hi-Z
		Enabled	Disabled	Disabled	-	Active - Pin drives 0
				Enabled	0	Active - Pin drives SPDIF-format, but data is zeroes
					1-15	Active - Pin drives SPDIFOut0 data
			Enabled	Disabled	-	Active - Pin drives SPDIF-format, but data is zeroes
				Enabled	0	Active - Pin drives SPDIF-format, but data is zeroes
					1-15	Active - Pin drives SPDIFOut0 data
D1-D2		Disabled	-	-	-	Hi-Z
		Enabled	Disabled	Disabled	-	Active - Pin drives 0
				Enabled	-	Active - Pin drives 0
			Enabled	Disabled	-	Active - Pin drives SPDIF-format, but data is zeroes
				Enabled	-	Active - Pin drives SPDIF-format, but data is zeroes
D3		Disabled	-	-	-	Hi-Z
		Enabled	Disabled	Disabled	-	Hi-Z
				Enabled	-	Hi-Z
			Enabled	Disabled	-	Active - Pin drives SPDIF-format, but data is zeroes
				Enabled	-	Active - Pin drives SPDIF-format, but data is zeroes
D3cold	-	-	-	-	-	Hi-Z
D4	-	-	-	-	-	Hi-Z
D5	-	-	-	-	-	Hi-Z

Table 6. SPDIF OUT 0 Behavior

1.Internal Pull-Down always enabled

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AFG Power State	RESET#	GPIO0 Enable	Input Enable	Output Enable	Keep Alive En	Converter Dig En	Strm ID	Pin Mode	Pin Behavior
D0-D4	Asserted (Low)	-	-	-	-	-	-		EAPD (internal pull-up enabled) immediately after power on, otherwise the previous state is retained.
D0-D4	De-Asserted (High)	0	0	0	-	-	-	EAPD	Pin functions as EAPD
D0-D4	De-Asserted (High)	1	-	-	-	-	-	GPIO	Active - Pin reflects GPIO0 configuration (internal pull-down enabled)
D0-D4	De-Asserted (High)	0	1	0	-	-	-	SPDIF IN	Pin functions as SPDIF input (internal bias enabled)
D0	De-Asserted (High)	0	0	1	0	0	-	SPDIF OUT	Active - Pin drives 0
						1	0		Active - Pin drives SPDIF-format, but data is zeroes
							1-15		Active - Pin drives SPDIFOut1 data
					1	0	-		Active - Pin drives SPDIF-format, but data is zeroes
						1	0		Active - Pin drives SPDIF-format, but data is zeroes
							1-15		Active - Pin drives SPDIFOut1 data
D1-D2	De-Asserted (High)	0	0	1	0	0	-		Active - Pin drives 0
					0	1	-		Active - Pin drives 0
					1	0	-		Active - Pin drives SPDIF-format, but data is zeroes
					1	1	-		Active - Pin drives SPDIF-format, but data is zeroes
D3	De-Asserted (High)	0	0	1	0	0	-		Hi-Z
					0	1	-		Hi-Z
					1	0	-		Active - Pin drives SPDIF-format, but data is zeroes
					1	1	-		Active - Pin drives SPDIF-format, but data is zeroes
D3cold	De-Asserted (High)	0	0	1	-	-	-		Hi-Z
D4	De-Asserted (High)	0	0	1	-	-	-		Hi-Z
D5	-	-	-	-	-	-	-		Hi-Z

Table 7. SPDIF OUT 1 Behavior

2.2. SPDIF Input

SPDIF IN can operate at 44.1 KHz, 48 KHz, or 96 KHz, and implements internal Jack Sensing (Port presence Detect).

A sophisticated digital PLL allows automatic rate detection and accurate data recovery. The ability to directly accept consumer SPDIF voltage levels eliminates the need for costly external receiver ICs.

Status flags from the input stream are updated only after the entire valid block has been received (or at least when all bits of a particular status flag have been received) to ensure that software does not read an invalid mixture of old and new data.

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In general, the SPDIF input block does not alter the data received. However, it is sometimes necessary to alter the data when the converter widget settings do not match the stream format. The following table outlines a few cases and the expected behavior.

Port presence detect for SPDIF_IN operates differently from other ports. Once the PLL has locked and valid framing (no errors) has been detected, then the port presence detect bit is set. In D3, and D3 without a clock, it is not possible to check for proper framing. Monitoring of activity (rising and falling edges) is sufficient to verify a change in connectivity in D3. If no clock is present, then the internal oscillator is used until a clock is restored. When the HD Audio bus is in a low power state (reset asserted and clock stopped) the CODEC will generate a Power State Change Request when a change in SPDIF_IN port connectivity is sensed and then generate an unsolicited response after the HD Audio link has been brought out of a low power state and the device has been enumerated. Per ECR015-B, this will take less than 10mS.

Conflict	Behavior	Resolution
Converter widget rate does not equal the stream rate	Although the SPDIF input block is designed to handle inputs slightly above or below the programmed rate, samples may be lost if the input rate is much higher than the rate programmed into the converter widget.	Program the converter widget with the same rate as indicated by the input stream.
Converter widget programmed for a word length less than the word length provided by the input stream	If the input stream indicates non PCM data, the data will be truncated to the requested word length. If LPCM data is indicated in the input stream, the CODEC will round the received data to the requested length.[1]	Program the converter widget with the word length indicated in the input stream.
Converter widget programmed with a word length greater than the word length provided by the input stream.	Regardless of content, 24 bits per channel of data will be transferred from the SPDIF input stream to the HD Audio bus interface. Truncation or rounding to the requested word length will be handled as described as above. Any non-zero data in the incoming stream will cause problems.	Program the converter widget with the word length indicated in the input stream. Although not recommended, application or driver software may program the converter widget with a word length of 24 bits, truncate the input to the word length indicated by the input stream, then right extend the data using 0s to the desired word length.

Table 8. SPDIF Behavior

1.Rounding may be disabled by setting the disable bit (AFG vendor specific verb -see widget list) or setting the SPDIF_IN converter widget Frmt StrmType field to 1 (non-PCM)

2.3. Analog Mixer

The mixer supports independent gain (-34.5 to +12dB in 1.5dB steps) on each input as well as independent mutes on each input. The following inputs are available: The output of the mixer may be sent to the ADC where the ADC record gain can adjust the volume. If the output of the mixer is sent to an analog port, then a separate volume control is provided to adjust the output volume. This mixer output volume control supports a gain range of -46.5dB to 0dB in 1.5dB steps. (Selecting -46.5dB will automatically mute the output.)

- inMux0
- inMux1
- inMux2
- inMux3
- CD In

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2.4. Input Multiplexers

The codec implements 4 port input multiplexers. These multiplexers allow a preselection of one of four possible inputs:

Inport0_Mux	Inport1_Mux	Inport2_Mux	Inport3_mux
Port A	Port A	Port B	DAC 0
Port B	Port E	Port C	DAC 1
Port D	Port G	Port G	DAC 2
Port F	Port H	Port H	DAC 3

Table 9. Input Multiplexers

2.5. ADC Multiplexers

The codec implements 2 ADC input multiplexers. These multiplexers incorporate the ADC record gain function (0 to +22.5dB gain in 1.5dB steps) as an output amp and allow a preselection of one of these possible inputs:

- Port A
- Port B
- Port C
- Port D
- Port E
- Port F
- Port G
- Port H
- CD In
- Mixer Output
- DMIC 0 (only available in 48 pin package)
- DMIC1 (only available in 48 pin package)

2.6. Power Management

The HD Audio specification defines power states, power state widgets, and power state verbs. Power management is implemented at several levels. The Audio Function Group (AFG) , all converter widgets, and all pin complexes support the power state verb F05/705. Converter widgets are active in D0 and inactive in D1-D3.

The following table describes what functionality is active in each power state.

Function	D0	D1[1]	D2	D3	D3cold	Vendor Specific D4[2]	Vendor SpecificD5[2]
SPDIF Outputs	On	On	On (idle)	On (idle)[6]	Off	Off	Off
SPDIF Input	On	Off	Off	Off	Off	Off	Off
Digital Microphone inputs	On	Off	Off	Off	Off	Off	Off
DAC	On	Off	Off	Off	Off	Off	Off
D2S	On	Off	Off	Off	Off	Off	Off
ADC	On	Off	Off	Off	Off	Off	Off

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Function	D0	D1[1]	D2	D3	D3cold	Vendor Specific D4[2]	Vendor SpecificD5[2]
ADC Volume Control	On	Off	Off	Off	Off	Off	Off
Ref ADC	On	Off	Off	Off	Off	Off	Off
Analog Clocks	On	Off	Off	Off	Off	Off	Off
GPIO pins	On	On	On	On[6]	On	On	Off
VrefOut Pins	On	On	Off	Off	Off	Off	Off
Input Boost	On	On	Off	Off	Off	Off	Off
Analog mixer	On	On	Off	Off	Off	Off	Off
Mixer Volumes	On	On	Off	Off	Off	Off	Off
Analog PC_Beep	On	On	On	On	Off	Off	Off
Digital PC_Beep	On	On	On	On[6]	Off	Off	Off
Lo/HP Amps	On	On	On	Low Drive[3]	Low Drive[3]	Low Drive[3]	Off
VAG amp	On	On	On	Low Drive[4]	Low Drive	Low Drive	Off
Port Sense	On	On	On	On[5]	Off	Off	Off
Reference Bias generator	On	On	On	On	On	On	Off
Reference Bandgap core	On	On	On	On	On	On	Off
HD Audio-Link	On	On	On	On[6]	Limited[7]	Off	Off
PLL	On	On	On	Off[8]	Off[9]	Off	Off

1.No DAC or ADC streams are active. Analog mixing and loop thru are supported.
2.D4 and D5 power states are entered only when D3cold is requested. D4 and D5 may be viewed as D3cold behavioral options.
3.VAG is kept active when ports are disabled or in D3/D3cold/D4. PC_Beep is supported in D3 but may be attenuated and distorted depending on load impedance.
4.VAG is always ramped up and down gradually, except in the case of a sudden power removal. VAG is active in D2/D3 but in a low power state.
5. Both AVDD and DVDD must be available for Port Sense to operate.
6.Not active if BITCLK is not running (Controller in D3), but can signal power state change request (PME)
7.Only double function group reset verbs and link reset supported per ECR15b
8.PLL remains on if SPDIF_Out Keep Alive is enabled. PLL disabled only after DAC fading is complete and SDM has settled.
9.PLL disabled only after DAC fading is complete and SDM has settled.

The D3-default state is available for HD Audio compliance. The programmable values, exposed via vendor-specific settings, are under TSI Device Driver control for further power reduction. The analog mixer, line and headphone amps, port presence detect, and internal references may be disabled using vendor specific verbs. Use of these vendor specific verbs will cause pops.

The default power state for the Audio Function Group after reset is D3.

2.7. AFG D0

The AFG D0 state is the active state for the device. All functions are active if their power state (if they support power management at their node level) has been set to D0.

2.8. AFG D1

D1 is a lower power mode where all converter widgets are disabled. Analog mixer and port functions are active. The part will resume from theD1 to theD0 state within 1 mS.

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2.9. AFG D2

The D2 state further reduces power by disabling the mixer and port functions. The port amplifiers and internal references remain active to keep port coupling caps charged and the system ready for a quick resume to either the D1 or D0 state. The part will resume from the D2 state to the D0 state within 2mS.

2.10. AFG D3

The D3-default state is available for HD Audio compliance. All converters are shut down. Port amplifiers and references are active but in a low power state to prevent pops. Resume times may be longer than those from D2, but still less than 10mS to meet Intel low power goals. The default power state for the Audio Function Group after power is applied is D3.

The traditional use for D3 was as a transitional state before power was removed (D3 cold) before the system entered into standby, hibernate, or shut-down. To conserve power, Intel now promotes using D3 whenever there are no active streams or other activity that requires the part to consume full power. The system remains in S0 during this time. When a stream request or user activity requires the CODEC to become active, the driver will immediately transition the CODEC from D3 to D0. To enable this use model, the CODEC must resume within 10mS and not pop. Intel HDA ECR-15b / Low Power White paper power goals are < 30mW when analog PC_Beep is not enabled, and < 60mW when analog PC_Beep is enabled.

While in AFG D3, the HD Audio controller may be in a D0 state (HD Audio bus active) or in a D3 state (HD Audio bus held in reset with no Bit_Clk, SData_Out, or Sync activity.) The expected behavior is as follows (see the ECR15b section for more information):

Function	HDA Bus active	HDA Bus stopped
Port Presence Detect state change	Unsolicited Response	Wake Event followed by an unsolicited response
GPIO state change	Unsolicited Response	Wake Event followed by an unsolicited response

2.10.1. AFG D3cold

The D3cold power state is the lowest power state available that does not use vendor specific verbs. While in D3cold, the CODEC will still respond to bus requests to revert to a higher power state (double AFG reset, link reset). However, audio processing, port presence detect, and other functions are disabled. Per the HD Audio bus ECR 015b, the D3cold state is intended to be used just prior to removing power to the CODEC. Typically, power will be removed within 200mS. However, the codec may exit from the D3cold state by generating 2, back-to-back, AFG reset events. Resume time from D3cold is less than 200mS.

2.11. Vendor Specific Function Group Power States D4/D5

The codec introduces vendor specific power states. A vendor defined verb is added to the Audio Function Group that combines multiple vendor specific power control bits into logical power states for use by the audio driver. The 2 states defined offer lower power than the 5 existing states defined in the HD Audio specification and ECR15b. The Vendor Specific D4 state provides lower digital power consumption relative to D3cold by disabling HD Audio link responses. Vendor specific D5 further reduces power consumption on the digital supply by turning off GPIO drivers, and reduces analog power consumption by turning off all analog circuitry except for reset circuits.

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States D4/D5 are not entered until D3cold has been requested so are actually D3cold options rather than true, independent, power states. Software can pre-program the D4 or D5 state as a re-definition of how the part will behave when the D3cold power state is requested or software may enter D3cold, then set the D4 or D5 before performing the power state get command. The preferred method is to request D3cold, then select D4 or D5 as desired.This will reduce the severity of pops encountered when entering D4 or D5.

Both power states require a link reset or removal of DVDD to exit.

The CODEC may pop when using these verbs and transition times to an active state (D1 or D0 for example) may take several seconds.

2.12. Low-voltage HDA Signaling

The codec is compatible with either 1.5V or 3.3V HDA bus signaling; in the 48QFP package the voltage selection is done dynamically based on the input voltage of DVDD_IO. For the 40-QFN package, seperate orderable part numbers to use 1.5V or 3.3V HDA bus signaling.

DVDD_IO is currently not a logic configuration pin, but rather provides the digital power supply to be used for the HDA bus signals.

When in 1.5V mode, the codec can correctly decode BITCLK, SYNC, RESET# and SDO as they operate at 1.5V; additionally it will drive SDI and SDO at 1.5V. None of the GPIOs are affected, as they always function at their nominal voltage (DVDD or AVDD).

2.13. Multi-channel capture

The capability to assign multiple “ADC Converters” to the same stream is supported to meet the microphone array requirements of Vista and future operating systems. Single converter streams are still supported this is done by assigning unique non zero Stream IDs to each converter. All capture devices (ADCs 0 and 1) may be used to create a multi-channel input stream. There are no restrictions regarding digital microphones.

The ADC Converters can be associated with a single stream as long the sample rate and the bits per sample are the same. The assignment of converter to channel is done using the “CnvtrID” widget and is restricted to even values. The ADC converters will always put out a stereo sample and therefore require 2 channels per converter.

The stream will not be generated unless all entries for the targeted converters are set identically, and the total number of assigned converter channels matches the value in the NmbrChan field. These are listed the “Multi-Converter Stream Critical Entries.” table.

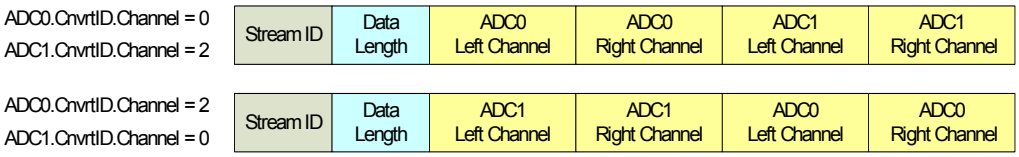
An example of a 4 Channel Steam with ADC0 supplying channels 0&1 and ADC1 supplying channels 2 & 3 is shown below. A 4 Channel stream can be created by assigning the same non-zero stream id “Strm= N” to both ADC0 and ADC1. The sample rates must be set the same and the number of channels must be set to 4 channels “NmbrChan = 0011”.

ADC1 CnvtrID	**(NID = 0x08)**	
	[3:0]	Ch = 2
ADC0 CnvtrID	**(NID = 0x07)**	
	[3:0]	Ch=0

Table 10. Example channel mapping

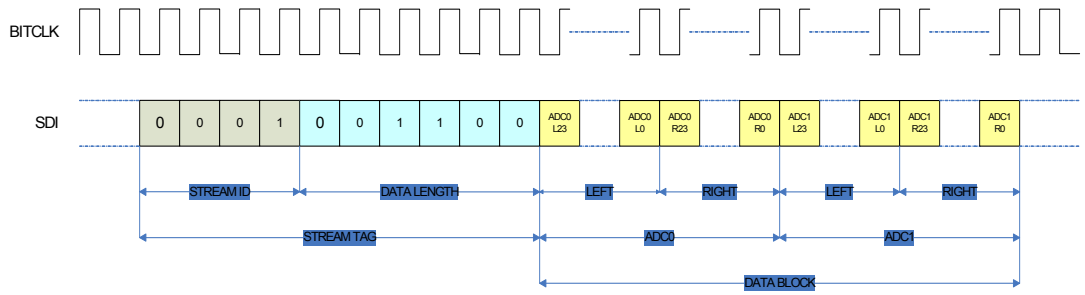
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Figure 3. Multi-channel capture



The following figure describes the bus waveform for a 24-bit, 48KHz capture stream with ID set to 1.

Figure 4. Multi-channel timing diagram



ADC[1:0] Cnvtr	Bit Number	Sub Field Name	Description
	[15]	StrmType	Stream Type (TYPE): 0: PCM 1: Non-PCM (not supported)
	[14]	FrmtSmplRate	Sample Base Rate 0= 48kHz 1=44.1KHz
	[13:11]	SmplRateMultp	Sample Base Rate Multiple 000=48kHz/44.1kHz or less 001= x2 010= x3 (not supported) 011= x4 192kHz only, 176.4 not supported 100-111= Reserved
	[10:8]	SmplRateDiv	Sample Base Rate Divisor 000= Divide by 1 001= Divide by 2 (not supported) 010= Divide by 3 (not supported) 011= Divide by 4 (not supported) 100= Divide by 5 (not supported) 101= Divide by 6 (not supported) 110= Divide by 7 (not supported) 111= Divide by 8 (not supported)

Table 11: Mult-channel

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	[6:4]	BitsPerSmpl	Bits per Sample 000= 8 bits (not supported) 001= 16 bits 010= 20 bits 011= 24 bits 100-111= Reserved
	[3:0]	NmbrChan	Number of Channels Number of channels for this stream in each “sample block” of the “packets” in each “frame” on the link. 0000=1 channel (not supported) 0001 = 2 channels … 1111= 16 channels.
	[7:4]	Strm	Software-programmable integer representing link stream ID used by the converter widget. By convention stream 0 is reserved as unused.
	[3:0]	Ch	Integer representing lowest channel used by converter. 0 and 2 are valid Entries If assigned to the same stream, one ADC must be assigned a value of 0 and the other ADC assigned a value of 2.

Table 11: Mult-channel

2.14. Digital Microphone Support

The digital microphone interface permits connection of a digital microphone(s) to the CODEC via the DMIC0 and DMIC_CLK 2-pin interface. The DMIC0 signal is an input that carries individual channels of digital microphone data to the ADC. In the event that a single microphone is used, the data is ported to both ADC channels. This mode is selected using a vendor specific verb and the left time slot is copied to the ADC left and right inputs.

The DMIC_CLK output is controllable from 4.704Mhz, 3.528Mhz, 2.352Mhz, 1.176Mhz and is synchronous to the internal master clock. The default frequency is 2.352Mhz.

The DMIC data input is reported as a stereo input pin widget that incorporates a boost amplifier. The pin widget is shown connected to the ADCs through the same multiplexors as the analog ports. Although the internal implementation is different between the analog ports and the digital microphones, the functionality is the same. In most cases, the default values for the DMIC clock rate and data sample phase will be appropriate and an audio driver will be able to configure and use the digital microphones exactly like an analog microphone.

To conserve power, the analog portion of the ADC will be turned off if the D-mic input is selected. When switching from the digital microphone to an analog input to the ADC, the analog portion of the ADC will be brought back to a full power state and allowed to stabilize before switching from the digital microphone to the analog input. This should take less than 10mS.

DMIC pin widgets support port presence detect directly using SENSE-C input on 4/5 DAC parts in a 48-pin package.

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The codec supports the following digital microphone configurations:

Digital Mics	Data Sample	ADC Conn.	Notes
0	N/A	N/A	No Digital Microphones
1	Single Edge	0, or 1	Available on either DMIC_0 or DMIC_1 When using a microphone that supports multiplexed operation (2-mics can share a common data line), configure the microphone for “Left” and select mono operation using the vendor specific verb. “Left” D-mic data is used for ADC left and right channels.
2	Double Edge on either DMIC_0 or 1	0, or 1	Available on either DMIC_0 or DMIC_1, External logic required to support sampling on a single Digital Mic pin channel on rising edge and second Digital Mic right channel on falling edge of DMIC_CLK for those digital microphones that don’t support alternative clock edge (multiplexed output) capability.
3	Double Edge on one DMIC pin and Single Edge on the second DMIC pin.	0, or 1	Requires both DMIC_0 and DMIC_1, External logic required to support sampling on a single Digital Mic pin channel on rising edge and second Digital Mic right channel on falling edge of DMIC_CLK for those digital microphones that don’t support alternative clock edge (multiplexed output) capability. Two ADC units are required to support this configuration
4	Double Edge	0, or 1	Connected to DMIC_0 and DMIC_1, External logic required to support sampling on a single Digital Mic pin channel on rising edge and second Digital Mic right channel on falling edge of DMIC_CLK for those digital microphones that don’t support alternative clock edge capability. Two ADC units are required to support this configuration

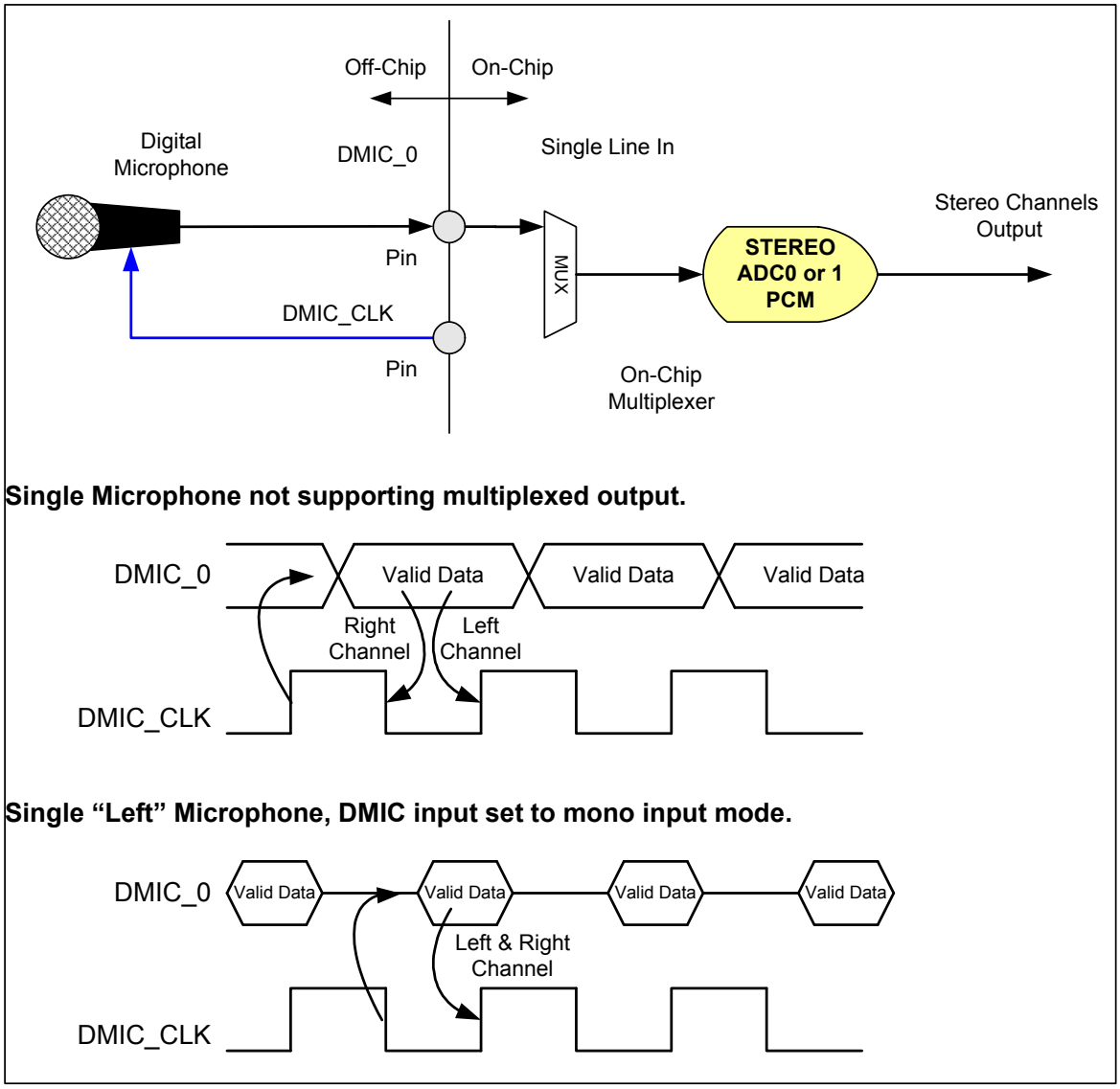
Table 12. Valid Digital Mic Configurations

Power State	DMIC Widget Enabled?	DMIC_CLK Output	DMIC_0,1	Notes
D0	Yes	Clock Capable	Input Capable	DMIC_CLK Output is Enabled when either DMIC_0 or DMIC_1 Input Widget is Enabled. Otherwise, the DMIC_CLK remains Low
D1-D3	Yes	Clock Disabled	Input Disabled	DMIC_CLK is HIGH-Z with Weak Pull-down
D0-D3	No	Clock Disabled	Input Disabled	DMIC_CLK is HIGH-Z with Weak Pull-down
D4	-	Clock Disabled	Input Disabled	DMIC_CLK is HIGH-Z with Weak Pull-down
D5	-	Clock Disabled	Input Disabled	DMIC_CLK is HIGH-Z with Weak Pull-down

Table 13. DMIC_CLK and DMIC_0,1 Operation During Power State

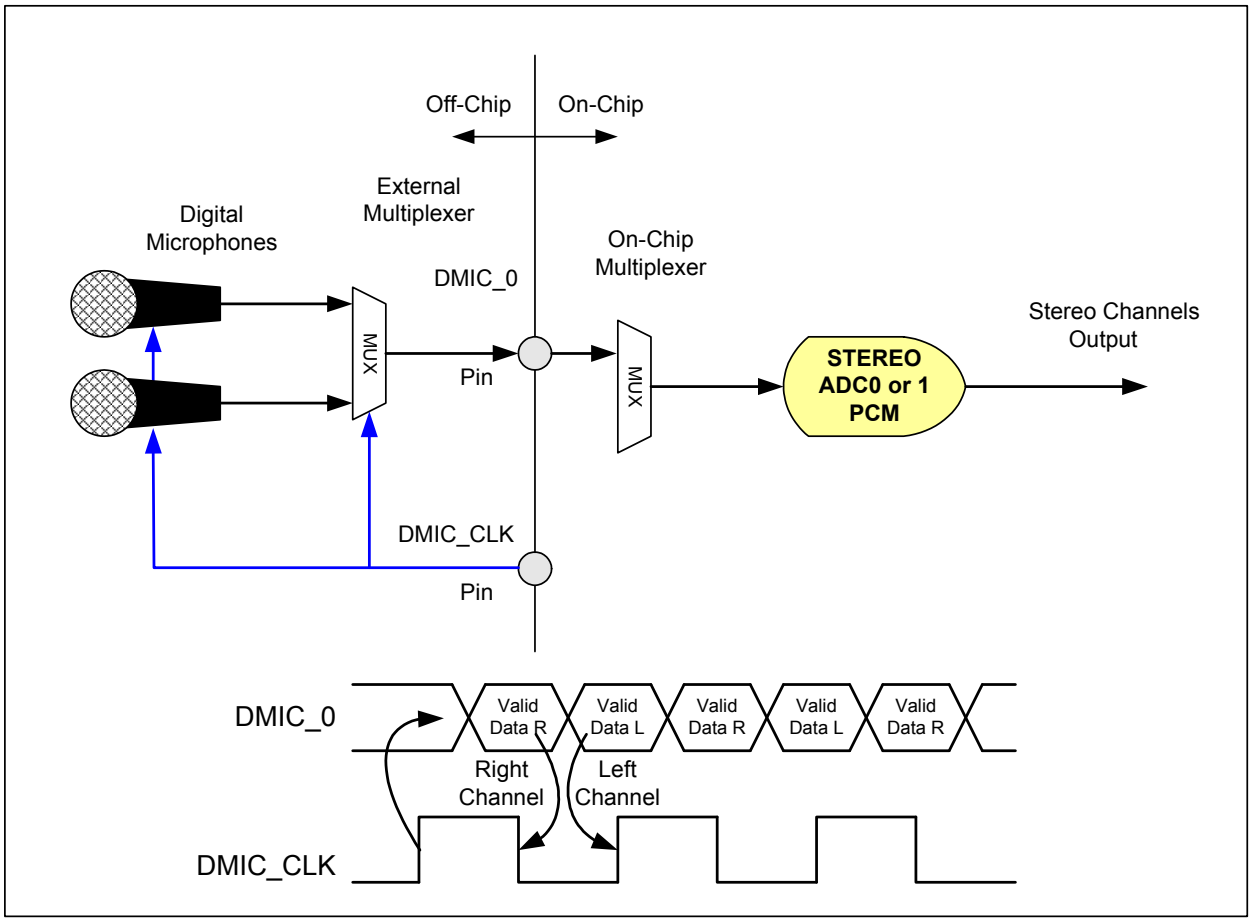
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Figure 5. Single Digital Microphone (data is ported to both left and right channels



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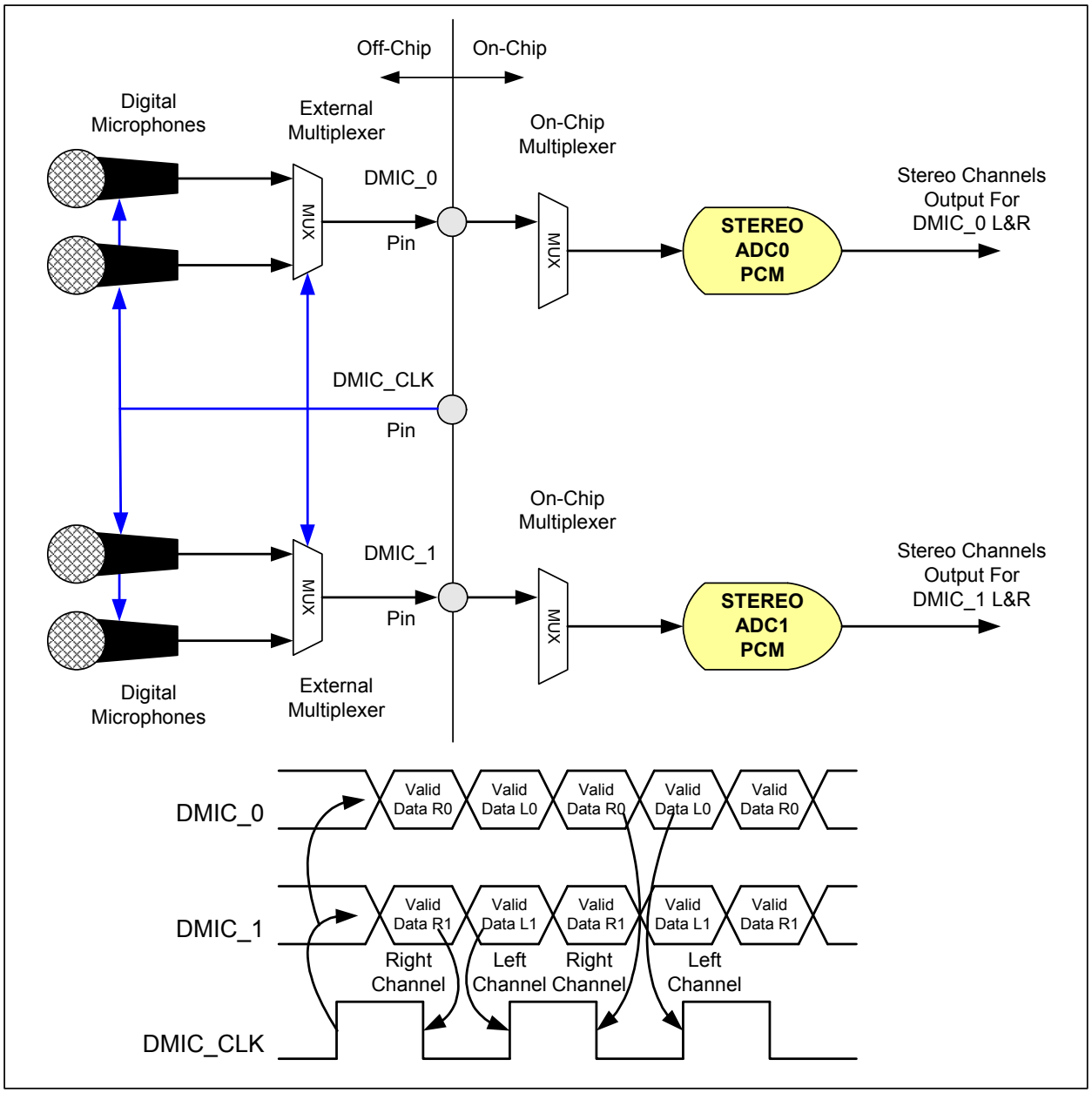
Figure 6. Stereo Digital Microphone Configuration



Note: Some Digital Microphone Implementations support data on either edge, therefore, the external mux may not be required.

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Figure 7. Quad Digital Microphone Configuration



Note: Some Digital Microphone Implementations support data on either edge, in this case the external multiplexer is not required.

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2.15. Analog PC-Beep

The codec supports automatic routing of the PC_Beep pin to several outputs when the HD-Link is in reset. Codec will route PC_Beep to ports A, B, D, and F by default when reset is applied. To prevent pops, beep is not enabled immediately when power is applied. Codec will mute outputs and wait until reference and ampliers have stabalized before enabling beep pass thru after power on reset. To prevent pops when removing power, automatic routing of PC_Beep is not supported in D3cold, D4, or D5.

Analog PC-Beep may also be supported during HD-Link Reset if analog PC_Beep is manually enabled before entering reset. Analog PC_Beep is mixed at the port and only ports enabled as outputs will pass PC_Beep.

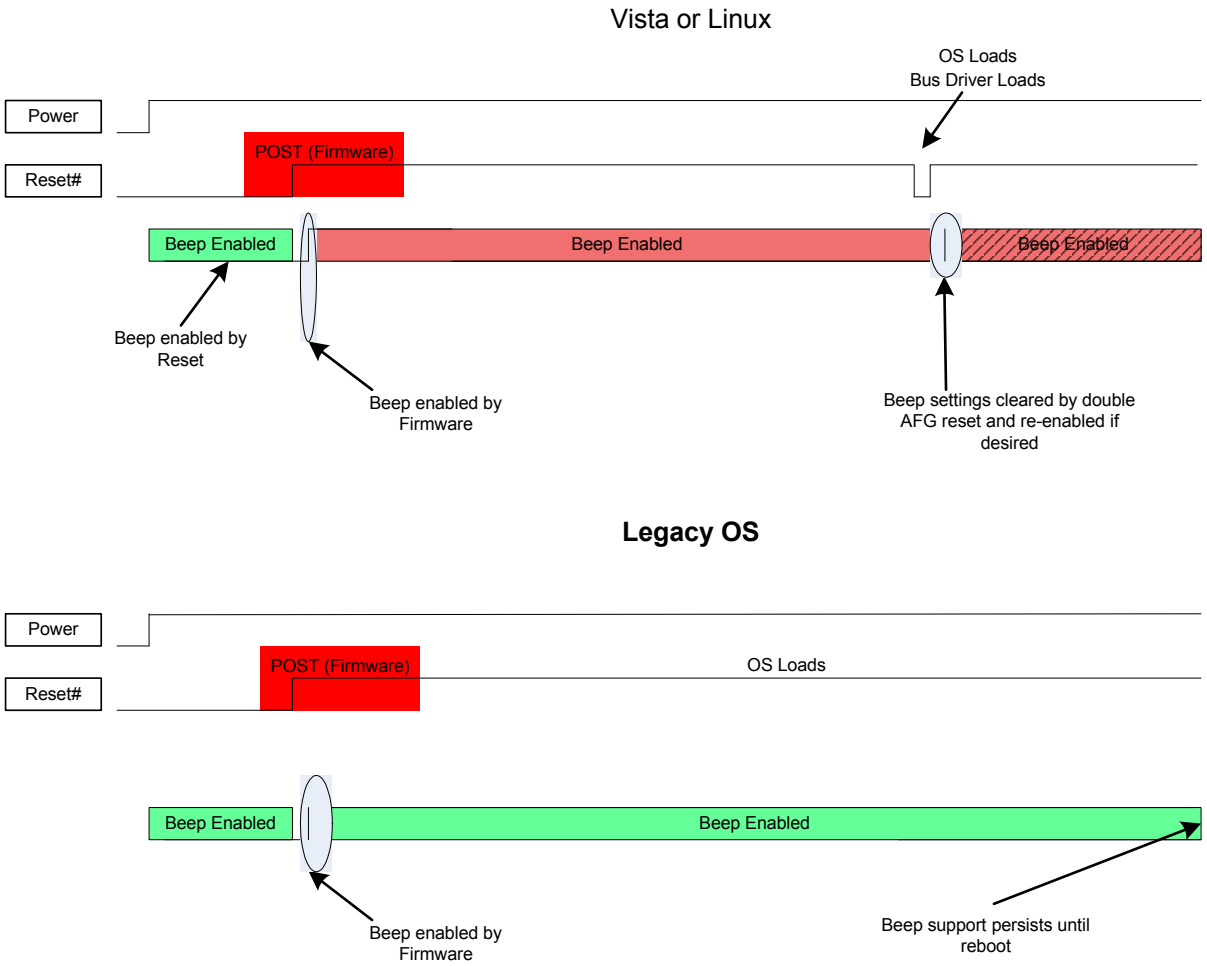
PC-Beep may be attenuated and distorted when the CODEC is in D3 depending on the load impedance seen by the output amplifier since all ports are in a low power state while in D3. Load impedances of 10K or larger can support full scale outputs but lower impedance loads will distort unless the output amplitude is reduced.

Analog PC_Beep is not supported in D3 Cold, or the vendor specific states D4/D5.

Analog PC_Beep is typically used during POST to route error beep codes to internal speakers for diagnostic purposes. When using a legacy OS such as DOS, analog PC_Beep routes “Bell” and “Alarm” tones from the south bridge to internal speakers or headphones. Keyboard controller “Keyclick” sounds are also routed to internal speakers using the analog beep function in both Windows and legacy operating systems

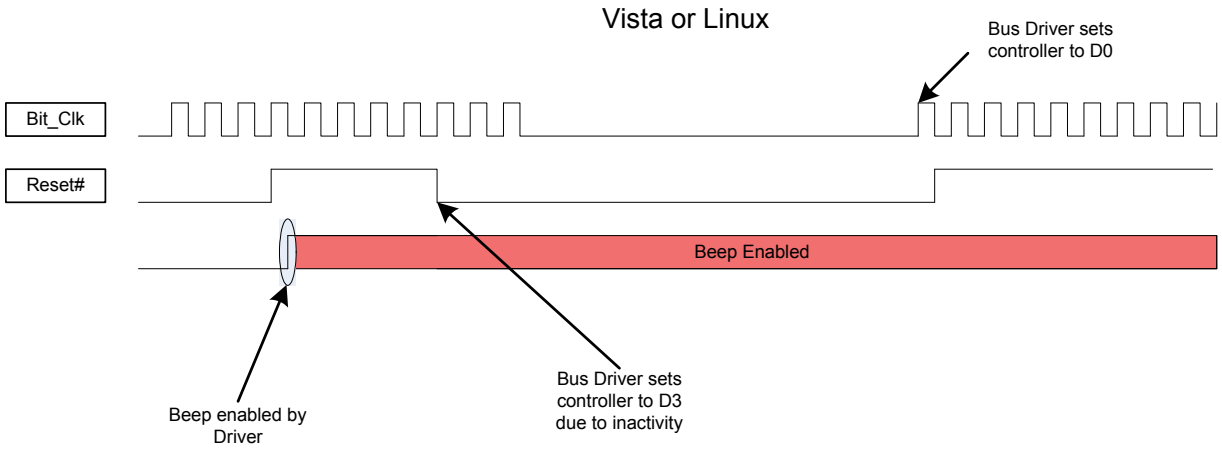
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Analog PC_Beep Behavior - Boot



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Analog PC_Beep Behavior – D3 clockless



2.16. Digital PC-Beep

This block uses an 8-bit divider value to generate the PC beep from the 48kHz HD Audio Sync pulse. The digital PC_Beep block generates the beep tone on all Pin Complexes that are currently configured as outputs. The HD Audio spec states that the beep tone frequency = (48kHz HD Audio SYNC rate) / (4*Divider), producing tones from 47 Hz to 12 kHz (logarithmic scale). Other audio sources are disabled when digital PC_Beep is active.

It should be noted that digital PC Beep is disabled if the divider = 00h.

PC-Beep may be attenuated and distorted when the CODEC is in D3 depending on the load impedance seen by the output amplifier since all ports are in a low power state while in D3. Load impedances of 10K or larger can support full scale outputs but lower impedance loads will distort unless the output amplitude is reduced. Digital PC_Beep requires a clock to operate and the CODEC will prevent the system from stopping the bus clock while in D3 by setting the Clock_Stop_OK bit to 0 to indicate that the part requires a clock.

2.17. Headphone Drivers

The codec implements headphone capable outputs on some ports. The Microsoft Windows Logo Program allows up to the equivalent of 100ohms in series. However, an output level of +3dBV at the pin is required to support 300mV at the jack with a 32ohm load and 1V with a 320 ohm load. Microsoft allows device and system manufactures to limit output voltages to address EU safety requirements. (WLP 3.09 - please refer to the latest Windows Logo Program requirements from Microsoft.) Power limiting may be implemented through the use of an external series resistance.

Although 3 Headphone amplifiers are present, only two may be used simultaneously. Headphone performance will degrade if more than one port is driving a 32 ohm load.

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2.18. EAPD

The EAPD pin (pin 47) also supports SPDIF_OUT, SPDIF_IN, and GPIO functions. The pin defaults to EAPD after power on reset and will remain in EAPD mode until either GPIO is enabled for pin 47 or the port I/O is enabled as an input to support SPDIF_IN or an output to support SPDIF_OUT. Although named External Amplifier Power Down (EAPD) by the HD Audio specification, this pin operates as an external amplifier power up signal. The EAPD value is reflected on the EAPD pin; a 1 causes the external amplifier to power up (equivalent to D0), and a 0 causes it to power down (equivalent to D3.) When the EAPD value = 1, the EAPD pin must be placed in a state appropriate to the current power state of the associated Pin Widget even though the EAPD value (in the register) may remain 1. The pin defaults to an open-drain configuration (an external pull-up is recommended.)

Per the HD Audio specification and ECR15b, multiple ports may control EAPD. The EAPD pin assumes the highest power state of all the the EAPD bits in all of the pin complexes. The default value of EAPD is 1 (powered on), but the FG power state will override and the pin will be low.

Vendor specific verbs are available to configure this pin. These verbs retain their values across link and single function group resets but are set to their default values by power on reset:

MODE1	MODE0	EAPD Pin Function	Description
0	0	Open Drain I/O	Value at pin is wired-AND of EAPD bit and external signal. (default)
0	1	CMOS Output	Value of EAPD bit in pin widget is forced at pin
1	0	CMOS Input	External signal controls internal amps. EAPD bit in pin widget ignored
1	1	CMOS Input	External signal controls internal amps. EAPD bit in pin widget ignored

Control Flag	Description
EAPD PIN MODE 1:0	Defines if EAPD pin is used as input, output, or bi-directional port (Open Drain)
HP SD	0 = Amp controlled by EAPD pin only (default) / 1 = Amp controlled by power state (pin and FG) only
HP SD MODE	0 = Amp will mute when disabled. (default) / 1 = Amp will shut down (enter a low power state) when disabled
HP SD INV	0 = AMP will power down (or mute) when EAPD pin is low (default) / 1 = Amp will power down (or mute) when EAPD pin is high.

HP SD	HP SD MODE	HP SD INV	EAPD Pin State	Headphone Amp State
0	0	0	0	Amplifier is mute (default[1])
0	0	0	1	Amplifier is active
0	0	1	0	Amplifier is active
0	0	1	1	Amplifier is mute
0	1	0	0	Amplifier is in a low power state
0	1	0	1	Amplifier is active

Table 14. Headphone Amp Enable Configuration

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HP SD	HP SD MODE	HP SD INV	EAPD Pin State	Headphone Amp State
0	1	1	0	Amplifier is active
0	1	1	1	Amplifier is in a low power state
1	0	NA	NA	Amplifier follows pin/function group power stateand will mute when disabled
1	1	NA	NA	Amplifier follows pin/function group power state and will enter a low power state when disabled

Table 14. Headphone Amp Enable Configuration

1.EAPD bit is set to one by default but the EAPD state is 0 after power-on reset because the function group is not in D0. The state after a single or double function group reset will be compliant with ECR15b.

Note: NOTE: Each Headphone port has its own configuration bits for SD, SD MODE, and SD INV.

Analog BEEP enabled	EAPD Pin value[1]	Description
0	Forced to low when in D2 or D3	Follows description in HD Audio spec. External amplifier is shut down when pin or function group power state is D2 or D3 independent of value in EAPD bit.
1	Forced low in D2 or D3 unless port is enabled as output	Power state is ignored if port is enabled as output and port EAPD=1 to allow PC_Beep support in D2 and D3

Table 15. EAPD Analog PC_Beep behavior

1.When pin is enabled as Open Drain or CMOS output.

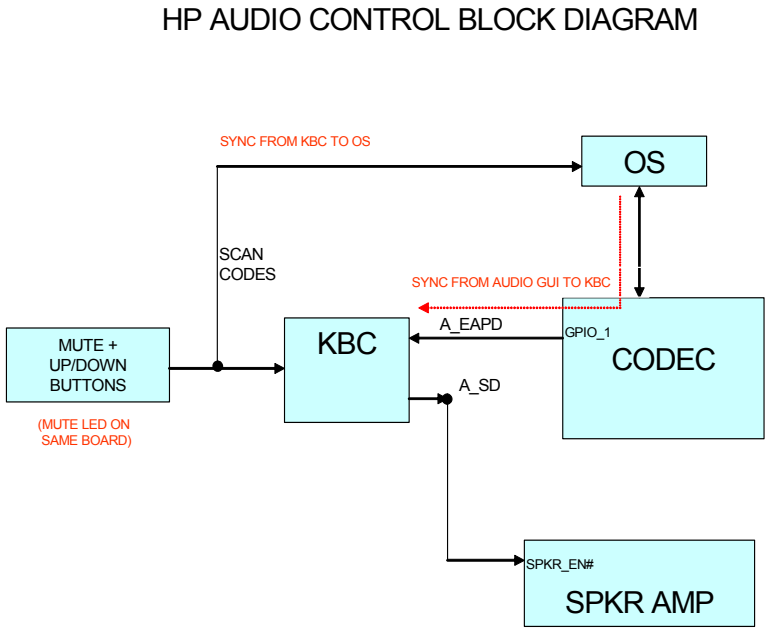
AFG Power State	RESET#	Analog PC_BEEP	Port Power State	Pin Behavior
D0-D3	Asserted (Low)	Enabled[1]	-	Active high immediately after power on, otherwise the previous state is retained across FG and link reset events
D0-D3	Asserted (Low)	Disabled	-	The previous state is retained across FG and link reset events
D0	De-Asserted (High)	-	-	Active - Pin reflects EAPD bit unless held low by external source.
D1	De-Asserted (High)	-	D0-D1	Active - Pin reflects EAPD bit unless held low by external source.
D2	De-Asserted (High)	Disabled	D0-D2	Pin forced low to disable external amp
D2	De-Asserted (High)	Enabled	D0-D2	Active - EAPD Pin high if any port EAPD bit =1 and that port also enabled as output.
D3	De-Asserted (High)	Disabled	D0-D3	Pin forced low to disable external amp
D3	De-Asserted (High)	Enabled	D0-D3	Active - EAPD Pin high if any port EAPD bit=1 and that port also enabled as output.
D3cold	De-Asserted (High)	-	-	Pin forced low to disable external amp
D4	De-Asserted (High)	-	-	Pin forced low to disable external amp
D5	De-Asserted (High)	-	-	Pin Hi-Z (off)

Table 16. EAPD Behavior

1.PC_Beep is automatically routed to ports A, B, D, and F after power-on reset while link reset is active and EAPD will be high to enable an external amplifier. This may be disabled using a vendor specific verb. If the automatic beep path is disabled, beep will still be supportedwith EAPD active in link reset if Analog Beep is manually enabled and at least one port is configured as an output before entering link reset. If the automatic Beep routing is disabled and Analog Beep has not been manually configured before entering link reset, then the EAPD pin will retain its current state.

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Figure 8. HP EAPD Example to be replaced by single pin for internal amp



2.19. GPIO

2.19.1. GPIO Pin mapping and shared functions

GPIO#	48 QFN	40 QFN	Supply	SPDIF In	SPDIF Out	EAPD	GPI/O	VrefOut	DMIC	Pull Up	Pull Down
0	47	40	DVDD	YES	YES	YES	YES			50K	50K
1	37	31	AVDD				YES	YES			
2	31	26	AVDD				YES	YES			
3	2	-	DVDD				YES		CLK		50K
4	4	-	DVDD				YES		IN		50K
5	40	-	AVDD		YES		YES				50K
6	30	-	AVDD				YES		IN		50K

Table 17. GPIO Pin mapping

2.19.2. SPDIF/GPIO Selection

2 functions are available on the SPDIFOUT1/GPIO5 pin. To determine which function is enabled, the order of precedence is followed:

1. If GPIO for that pin is enabled, it will override the SPDIF_OUT function.
2. If the GPIOs are not enabled through the AFG, then at reset, the pin is pulled low by an internal pull-down resistor.
3. If the port is enabled as an output, the SPDIF output will be used.

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2.19.3. Digital Microphone/GPIO Selection

2 functions are available on the DMIC_CLK/GPIO3, the DMIC_0/GPIO4, and the DMIC_1/GPIO6 pins. To determine which function is enabled, the order of precedence is followed:

1. If GPIOs are not enabled through the AFG, then at reset, the pins are pulled low by an internal pull-down resistor.
2. If the port is not enabled as an input or if the pin is configured as a GPIO, the digital microphone path will be mute.

2.19.4. Vref_Out/GPIO Selection

2 functions are available on the VrefOut-A/GPIO1 and VrefOut-E/GPIO2 pins. To determine which function is enabled, the order of precedence is followed:

1. If GPIO is enabled for that pin, it overrides the VrefOut function for that pin.
2. If the GPIO function is not enabled for that pin, then the VrefOut function is enabled and in its programmed state.

2.19.5. EAPD/SPDIF_IN/SPDIF_OUT/GPIO0 Selection

4 functions are available on the EAPD/SPDIF_IN/SPDIF_OUT1/GPIO0 pin. To determine which function is enabled, the order of precedence is followed:

1. Default at power-on is EAPD
2. If GPIO is enabled for that pin, it overrides the SPDIF_IN, SPDIF_OUT and EAPD functions for that pin.
3. If the GPIO function is not enabled for that pin, then the SPDIF_IN or SPDIF_OUT function may be enabled by setting the pin input or output enable to 1, respectively. (Setting input and output enable to 1 at the same time will only enable SPDIF_IN)

2.20. HD Audio ECR 15b support

Although ECR15b is not yet complete (not a DCN), the 92HD68F will implement complete support for the specification building on the support already present in previous products. ECR 15b features supported are:

- Persistence of many configuration options through bus and function group reset.
- The ability to support port presence detect in D3 even when the HD Audio bus is in a low power state (no clock.)
- Fast resume times from low power states: 1ms D1 to D0, 2ms D2 to D0, 10mS D3 to D0.
- Notification if persistent register settings have been unexpectedly reset.
- SPDIF active in D3 (required)
- The ability to notify the driver that a clock is necessary so entering D3 with the clock stopped is not permissible.

2.21. Digital Core Voltage Regulator

The digital core operates fat 1.5V. Many systems require that the CODEC use a single 3.3V digital supply, so an integrated regulator is included on die. The regulator uses pin 9, DVDD, as its voltage source. The output of the LDO is connected to pin 1 and the digital core. A 10uF capacitor must be placed on pin 1 for proper load regulation and regulator stability.

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The digital core voltage regulator is only dependent on DVDD. DVDDIO may be either 3.3 or 1.5V and may precede or follow DVDD in sequence. The CODEC digital logic and I/O (unless referenced to AVDD) will operate in the absence of AVDD. DVDD and AVDD supply sequencing for the application of power and the removal of power is neither defined nor guaranteed. It is common for desktop systems to supply AVDD from the system standby supply and the CODEC will tolerate, indefinitely, the condition where AVDD is active but DVDD and DVDDIO are inactive.

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3. CHARACTERISTICS

3.1. Electrical Specifications

3.1.1. Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 92HD68F. These ratings, which are standard values for TSI commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Pin	Maximum Rating
Analog maximum supply voltage	AVdd	6 Volts
Digital maximum supply voltage	DVdd	5.5 Volts
VREFOUT output current		5 mA
Voltage on any pin relative to ground		Vss - 0.3 V to Vdd + 0.3 V
Operating temperature		0 ^{o}C to +70 ^{o}C
Storage temperature		-55 ^{o}C to +125 ^{o}C
Soldering temperature		Soldering temperature information for all available in the package section of this datasheet.

Table 18. Electrical Specification: Maximum Ratings

3.1.2. Recommended Operating Conditions

Parameter		Min.	Typ.	Max.	Units
Power Supplies	DVDD_Core	1.4		1.98	V
	DVDD_IO (3.3V signaling)	3.135	3.3	3.465	V
	DVDD_IO (1.5V signaling)	1.418	1.5	1.583	V
Power Supply Voltage	Digital - 3.3 V	3.135	3.3	3.465	V
	Analog - 5 V	4.75	5	5.25	V
Ambient Operating Temperature		0		+70	°C
Case Temperature	T_{case} (48-QFN)			+95	°C

Table 19. Recommended Operating Conditions

ESD: The 92HD68F is an ESD (electrostatic discharge) sensitive device. The human body and test equipment can accumulate and discharge electrostatic charges up to 4000 Volts without detection. Even though the 92HD68F implements internal ESD protection circuitry, proper ESD precautions should be followed to avoid damaging the functionality or performance.

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3.2. 92HD68F Analog Performance Characteristics

(Tambient = 25 ºC, AVdd = Supply ± 5%, DVdd = 3.3V ± 5%, AVss=DVss=0V; 20Hz to 20KHz swept sinusoidal input; Sample Frequency = 48 kHz; 0 dB = 1 VRMS, 10KΩ//50pF load, Testbench Characterization BW: 20 Hz – 20 kHz, 0 dB settings on all gain stages)

Parameter	Conditions	Min	Typ	Max	Unit
Digital to Analog Converters					
Resolution			24		Bits
Dynamic Range[1]: PCM to All Analog Outputs	-60dB FS signal level, Analog Mixer disabled	94	97	-	dB
SNR[2] - DAC to All Line-Out Ports	Analog Mixer Disabled, PCM data	97	99		dB
THD+N[3] - DAC to All Line-Out Ports	Analog Mixer Disabled, 0/-1/-3dB FS Signal, PCM data	83	85		dBr
SNR[2] - DAC to All Headphone Ports	Analog Mixer Disabled, 10KΩ load, PCM data	97	99		dB
THD+N[3] - DAC to All Headphone Ports	Analog Mixer Disabled, 0/-1/-3dB FS Signal, 10KΩ load, PCM data	83	85		dBr
SNR[2] - DAC to All Headphone Ports	Analog Mixer Disabled, 32Ω load, PCM data	98	99		dB
THD+N[3] - DAC to All Headphone Ports	Analog Mixer Disabled, 0/-1/-3dB FS Signal, 32Ω load, PCM data	70	85		dBr
Any Analog Input (ADC) to DAC Crosstalk	10KHz Signal Frequency. 0dBV signal applied to ADC, DACs idle, ports enabled as output.	-65	-95	-	dB
Any Analog Input (ADC) to DAC Crosstalk	1KHz Signal Frequency see above	-65	-97	-	dB
DAC L/R crosstalk	DAC to LO or HP 20-15KHz into 10KΩ load	73	81		dB
DAC L/R crosstalk	DAC to HP 20-15KHz into 32Ω load	68	72		dB
Gain Error	Analog Mixer Disabled			0.5	dB
Interchannel Gain Mismatch	Analog Mixer Disabled		.016	0.5	dB
D/A Digital Filter Pass Band[4]		20	-	21,000	Hz
D/A Digital Filter Pass Band Ripple[5]				0.1	+/- dB
D/A Digital Filter Transition Band		21,000	-	31,000	Hz
D/A Digital Filter Stop Band		31,000	-	-	Hz
D/A Digital Filter Stop Band Rejection[6]		-100	-108	-	dB
D/A Out-of-Band Rejection[7]		-55	-50	-	dB
Group Delay (48KHz sample rate)		-	-	1	ms
Attenuation, Gain Step Size DIGITAL		-	0.75	-	dB
DAC Offset Voltage		-	0.4	20	mV
Deviation from Linear Phase		-	1	10	deg.
Analog Outputs					
Full Scale All Mono/Line-Outs	DAC PCM Data	1.00	1.08	-	Vrms
Full Scale All Mono/Line-Outs	DAC PCM Data	2.83	3.05	-	Vp-p

Table 20. 92HD68F Analog Performance Characteristics

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Parameter	Conditions	Min	Typ	Max	Unit
All Headphone Capable Outputs	32Ω load	40	47	-	mW (peak)
Amplifier output impedance	Mono/Line Outputs Headphone Outputs		150 0.1		Ohms
External load Capacitance	Mono/Line Outputs Headphone Outputs		220		pF
Analog inputs					
Full Scale Input Voltage	0dB Boost @4.75V (input voltage required for 0dB FS output)	1.05	1.31	-	Vrms
All Analog Inputs with boost	10dB Boost	0.320	0.42	-	Vrms
All Analog Inputs with boost	20dB Boost	0.105	0.136	-	Vrms
All Analog Inputs with boost	30dB Boost	0.032	0.042	-	Vrms
Boost Gain Accuracy		-2	0.6	2	dB
Input Impedance		-	75	-	KΩ
Input Capacitance		-	15	-	pF
Analog Mixer					
Dynamic Range: PCM to All Analog Outputs	-60dB FS signal level Analog Beep enabled all other mixer inputs mute	93	93		
SNR[2] - All Line-Inputs to all Line Outputs	All inputs unmuted, single line input driven by ATE.	85	85		dB
THD+N[3] - All Line-Inputs to all Line Outputs	0dB Full Scale Input on one input, all others silent.	65	83		dBr
SNR[2] - DAC to All Ports	Analog Mixer Enabled, PCM data, all others inputes mute.	85	94		dB
THD+N[3] - DAC to All Line-Out Ports	Analog Mixer Enabled, 0/-1/-3dB FS signal, PCM data, all others inputes unmute/silent	75	81		dBr
THD+N[3] - DAC to All Ports	Analog Mixer Enabled, 0dB FS Signal, PCM data, all others inputes unmute/silent	65	78		dBr
Attenuation, Gain Step Size ANALOG		-	1.5	-	dB
Analog to Digital Converter					
Resolution			24		Bits
Full Scale Input Voltage	0dB Boost (input voltage required to generate 0dBFS per AES 17)	1.05	1.31		
Dynamic Range[1], All Analog Inputs to A/D	High Pass Filer Enabled, -60dB FS, No boost	93	94		dB
Full Scale Input Voltage	20dB Boost (input voltage required to generate 0dBFS per AES 17)	0.105	0.136		
Dynamic Range[1], All Analog Inputs to A/D	20dB Boost High Pass Filter Enabled, -60dB FS	81	90		
SNR[2] - All Analog Inputs to A/D	High Pass Filter Enabled	93	94		
THD+N[3] All Analog Inputs to A/D	High Pass Filter enabled, -1/-3dB FS signal level	78	80		dB

Table 20. 92HD68F Analog Performance Characteristics

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Parameter	Conditions	Min	Typ	Max	Unit
THD+N[3] All Analog Inputs to A/D	20dB Boost, High Pass Filter enabled, -1/-3dB FS signal level	72	80		dB
Analog Frequency Response[8]		10	-	30,000	Hz
A/D Digital Filter Pass Band[4]		20	-	21,000	Hz
A/D Digital Filter Pass Band Ripple[5]				0.1	+/- dB
A/D Digital Filter Transition Band		21,000	-	31,000	Hz
A/D Digital Filter Stop Band		31,000	-	-	Hz
A/D Digital Filter Stop Band Rejection[6]		-100	-127	-	dB
Group Delay	48 KHz sample rate	-	-	1	ms
Any unselected analog Input to ADC Crosstalk	10KHz Signal Frequency	-65	-94	-	dB
Any unselected analog Input to ADC Crosstalk	1KHz Signal Frequency	-65	-94	-	dB
ADC L/R crosstalk	Any selected input to ADC 20-15Khz	-65	-84		dB
DAC to ADC crosstalk	DAC output 0dBFS. All outputs loaded. Input to ADC open. 20-15Khz	-65	-90		dB
Spurious Tone Rejection[9]		-	-102	-	dB
Attenuation, Gain Step Size (analog)		-	1.5	-	dB
Interchannel Gain Mismatch ADC		-	0.161	0.5	dB
Power Supply					
Power Supply Rejection Ratio	10kHz	-	-60	-	dB
Power Supply Rejection Ratio	1kHz	-	-70	-	dB
D0 Didd[10]	3.3V, 1.8V, 1.5V		22		mA
D0 Aidd[10]	4.75V		60		mA
D0 Didd[11]	3.3V, 1.8V, 1.5V		11.5		mA
D0 Aidd[11]	4.75V		33		mA
D1 Didd[12]	3.3V, 1.8V, 1.5V		6.35		mA
D1 Aidd[12]	4.75V		27.5		mA
D2 Didd	3.3V, 1.8V, 1.5V		6.33		mA
D2 Aidd	4.75V		15		mA
D3 (Beep enabled) Didd[13]	3.3V, 1.8V, 1.5V		1.84		mA
D3 (Beep enabled) Aidd[13]	4.75V		5.74		mA
D3 Didd[13]	3.3V, 1.8V, 1.5V		1		mA
D3 Aidd[13]	4.75V,		2.78		mA
D3cold Didd[13]	3.3V, 1.8V, 1.5V		0.4		mA
D3cold Aidd[13]	4.75V		2.78		mA
Vendor D4 Didd	3.3V, 1.8V, 1.5V		0.4		mA
Vendor D4 Aidd	4.75V		2.78		mA

Table 20. 92HD68F Analog Performance Characteristics

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Parameter	Conditions	Min	Typ	Max	Unit
Vendor D5 Didd	3.3V, 1.8V, 1.5V		0.4		mA
Vendor D5 Aidd	4.75V		0.25		mA
One Stereo ADC Didd	3.3V, 1.8V, 1.5V		3.63		mA
One Stereo ADC Aidd	4.75		4.13		mA
One Stereo DAC Didd	3.3V, 1.8V, 1.5V		2.41		mA
One Stereo DAC Aidd	4.75V		5.33		mA
Voltage Reference Outputs					
VREFOut[14]		-	0.5 X AVdd	-	V
VREFOut Drive			1.6		mA
VREFILT (VAG)			0.45 X AVdd		V
Phased Locked Loop					
PLL lock time			96	200	usec
PLL (or HD Audio Bit CLK) 24MHz clock jitter			150	500	psec
ESD / Latchup					
IEC1000-4-2		1			Level
JESD22-A114-B		2			Class
JESD22-C101		4			Class

Table 20. 92HD68F Analog Performance Characteristics

1.Dynamic Range is the ratio of the full scale signal to the noise output with a -60dBFS signal as defined in AES17 as SNR in the presence of signal and outlined in AES6id, measured “A weighted” over 20 Hz to 20 kHz bandwidth

2.Ratio of Full Scale signal to idle channel noise output is measured “A weighted” over a 20 Hz to a 20 kHz bandwidth. (AES17-1991 Idle Channel Noise or EIAJ CP-307 Signal-to-noise Ratio).

3.THD+N ratio as defined in AES17 and outlined in AES6id,non-weighted, over 20 Hz to 20 kHz bandwidth.Results at the jack are dependent on external components and will likely be 1 - 2dB worse.

4.Peak-to-Peak Ripple over Passband meets ± 0.125dB limits, 48 kHz or 44.1 kHz Sample Frequency. 1dB limit.

5.Peak-to-Peak Ripple over Passband meets ± 0.125dB limits, 48 kHz or 44.1 kHz Sample Frequency. 1dB limit.

6.Stop Band rejection determines filter requirements. Out-of-Band rejection determines audible noise.

7.The integrated Out-of-Band noise generated by the DAC process, during normal PCM audio playback, over a bandwidth 28.8 to 100 kHz, with respect to a 1 Vrms DAC output.

8.± 1dB limits for Line Output & 0 dB gain, at -20dBV

9.Spurious tone rejection is tested with ADC dither enabled and compared to ADC performance without dither.

10.All functions/converters active, pin complexes enabled, two FDX streams, line (10Kohm) loads. Add 24mA analog current per stereo 32 ohm headphone.

11.One stereo DAC and corresponding pin widgets enabled (playback mode)

12.Mixer enabled

13.Idle measurement D3 set for minimum clicks/pops (biases and min. amps. on)

14.Can be set to 0.5 or 0.8 AVdd.

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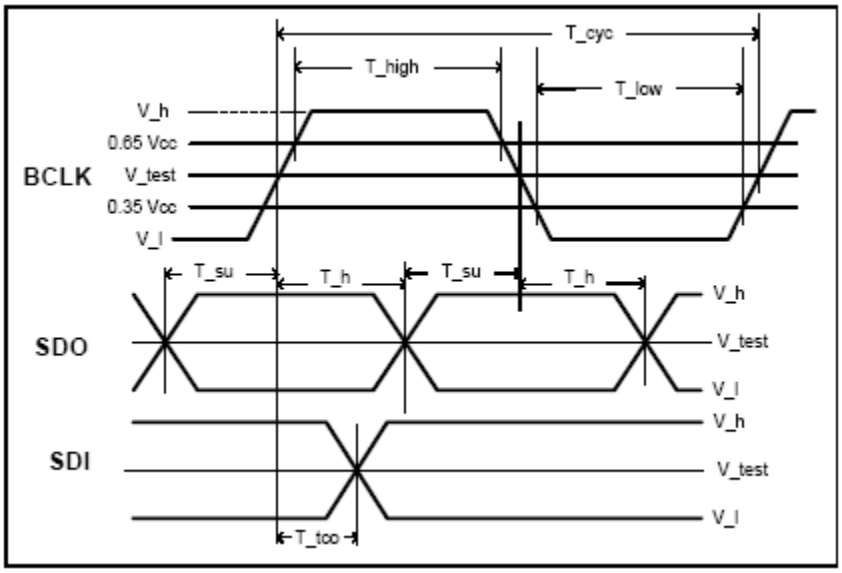
3.3. AC Timing Specs

3.3.1. HD Audio Bus Timing

Parameter	Definition	Symbol	Min	Typ	Max	Units
BCLK Frequency	Average BCLK frequency		23.9976	24.0	24.0024	Mhz
BCLK Period	Period of BCLK including jitter	Tcyc	41.163	41.67	42.171	ns
BCLK High Phase	High phase of BCLK	T_high	17.5		24.16	ns
BCLK Low Phase	Low phase of BCLK	T_low	17.5		24.16	ns
BCLK jitter	BCLK jitter			150	500	ps
SDI delay	Time after rising edge of BCLK that SDI becomes valid	T_tco	3		11	ns
SDO setup	Setup for SDO at both rising and falling edges of BCLK	T_su	5			ns
SDO hold	Hold for SDO at both rising and falling edges of BCLK	T_h	5			ns

Table 21. HD Audio Bus Timing

Figure 9. HD Audio Bus Timing



3.3.2. SPDIF Timing

Parameter	Definition	Symbol	Min	Typ	Max	Units
SPDIF_OUT Frequency	highest rate of encoded signal 64 times the sample rate		2.8224	3.072	12.288	MHz
SPDIF_OUT unit interval	1/(128 times the sample rate)	UI	177.15	162.76	40.69	ns
SPDIF_OUT jitter	SPDIF_OUT jitter				4.43	ns

Table 22. SPDIF Timing

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Parameter	Definition	Symbol	Min	Typ	Max	Units
SPDIF_OUT rise time		T_rise			15	ns
SPDIF_OUT fall time		T_fall			15	ns

Table 22. SPDIF Timing

3.3.3. Digital Microphone Timing

Parameter	Definition	Symbol	Min	Typ	Max	Units
DMIC_CLK Frequency	Average DMIC_CLK frequency		1.176	2.352	4.704	MHz
DMIC_CLK Period	Period of DMIC_CLK	Tdmic_cyc	850.34	425.17	212.59	ns
DMIC_CLK jitter	DMIC_CLK jitter				5000	ps
DMIC Data setup	Setup for the microphone data at both rising and falling edges of DMIC_CLK	Tdmic_su	5			ns
DMIC Data hold	Hold for the microphone data at both rising and falling edges of DMIC_CLK	Tdmic_h	5			ns

Table 23. Digital Mic timing

3.3.4. GPIO Characteristics

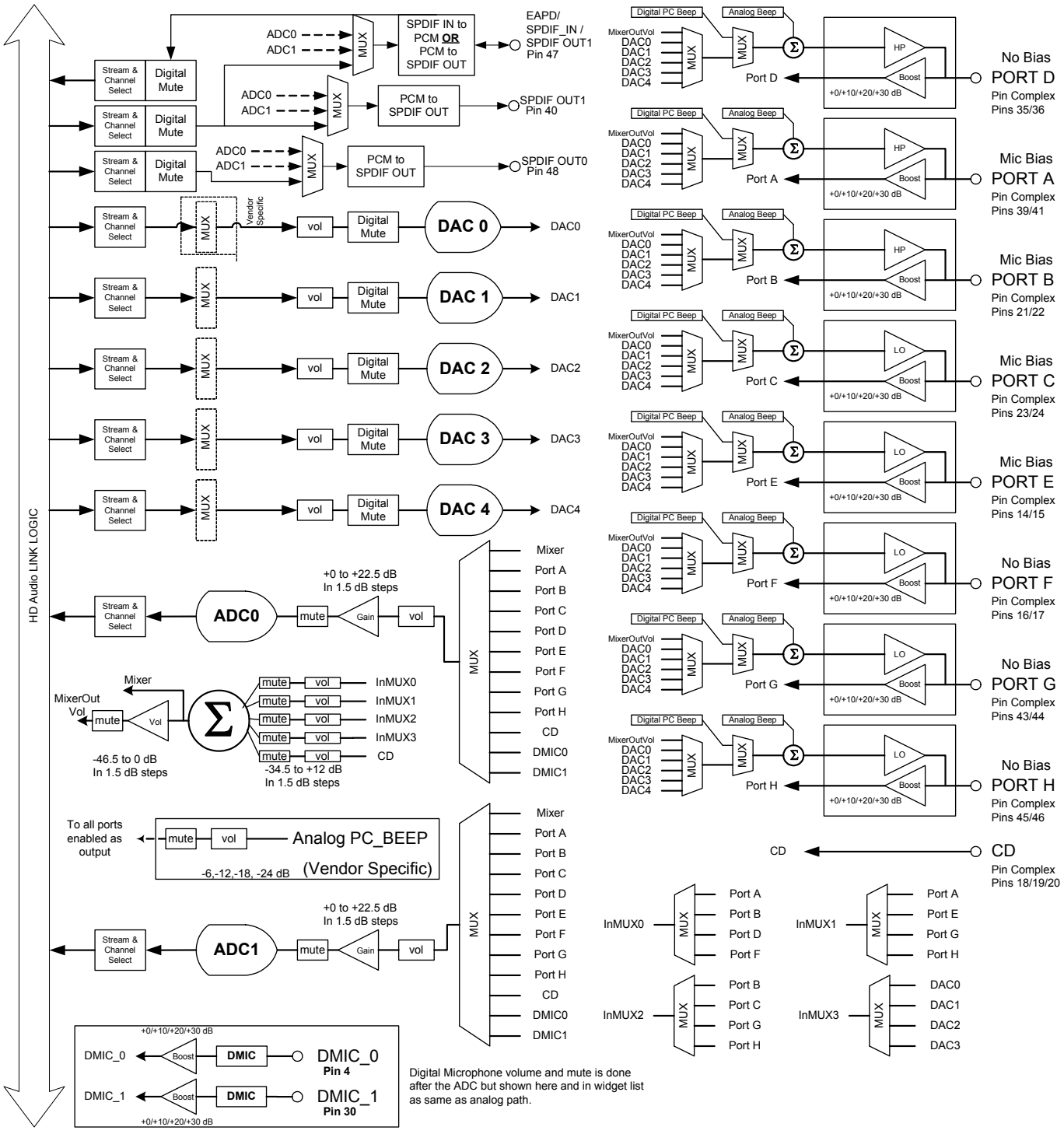
Parameter	Definition	Symbol	Min	Typ	Max	Units
Input High Voltage	input level at or above which a 1 is reliably recorded	Vih	0.6 x VDD			V
Input Low Voltage	input level at or below which a 0 is reliably recorded VDD may be DVDD or AVDD	Vil			0.35 x VDD	V
Output High Voltage	iout = 4mA VDD may be DVDD or AVDD depending on pin	Voh	0.9 x VDD			V
Output Low Voltage	iout = -4mA VDD may be DVDD or AVDD depending on pin	Vol			0.1 x VDD	V
Input rise/fall time	transition time between 10% and 90% of supply	T_rise/T_fall			10	ns
Input/Tristate High Leakage Current	Vin = VDD VDD may be DVDD or AVDD depending on pin (does not include pull-up or pull-down resistor if present)			0.5		uA
Input/Tristate Low Leakage Current	Vin = 0 VDD may be DVDD or AVDD depending on pin (does not include pull-up or pull-down resistor if present)			-50		uA

Table 24. GPIO Characteristics

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4. FUNCTIONAL BLOCK DIAGRAMS

4.1. 48QFP



Digital Microphone volume and mute is done after the ADC but shown here and in widget list as same as analog path.

Figure 10. 48QFP Functional Block Diagram

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4.2. 40QFN

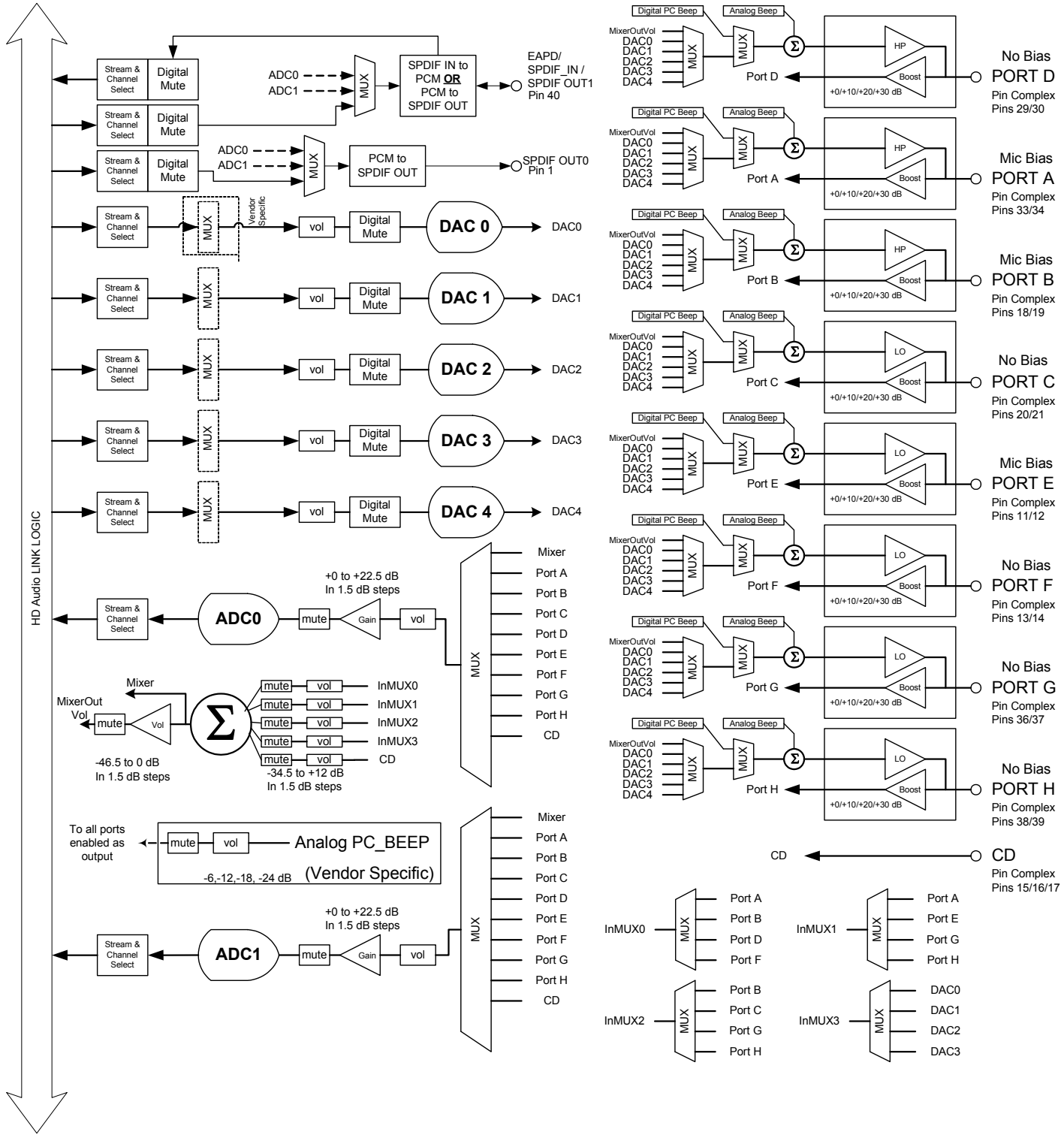


Figure 11. 40QFN Functional Block Diagram

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5. WIDGET BLOCK DIAGRAM

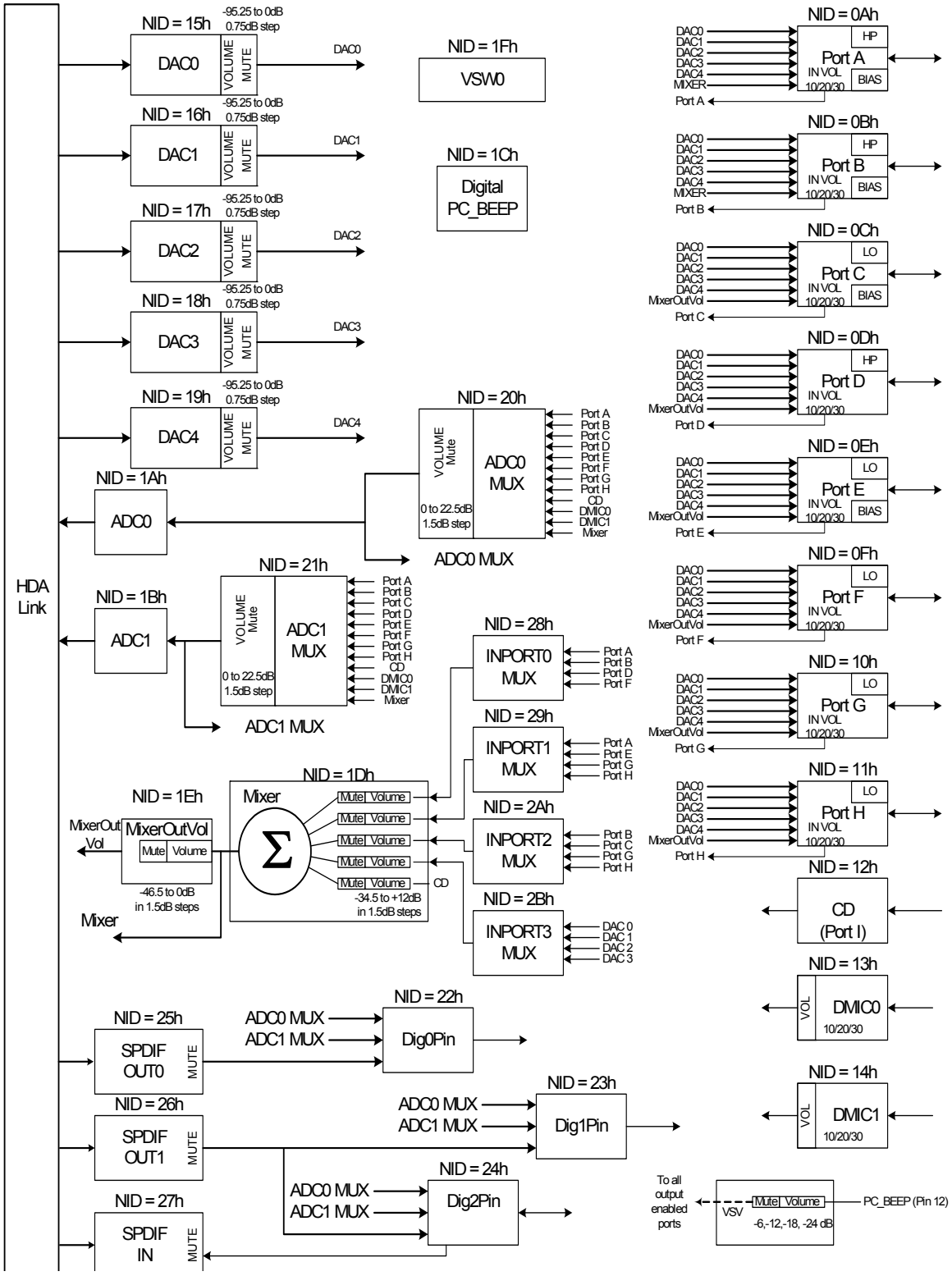


Figure 12. Widget Diagram (same for both package option)

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6. PORT CONFIGURATIONS

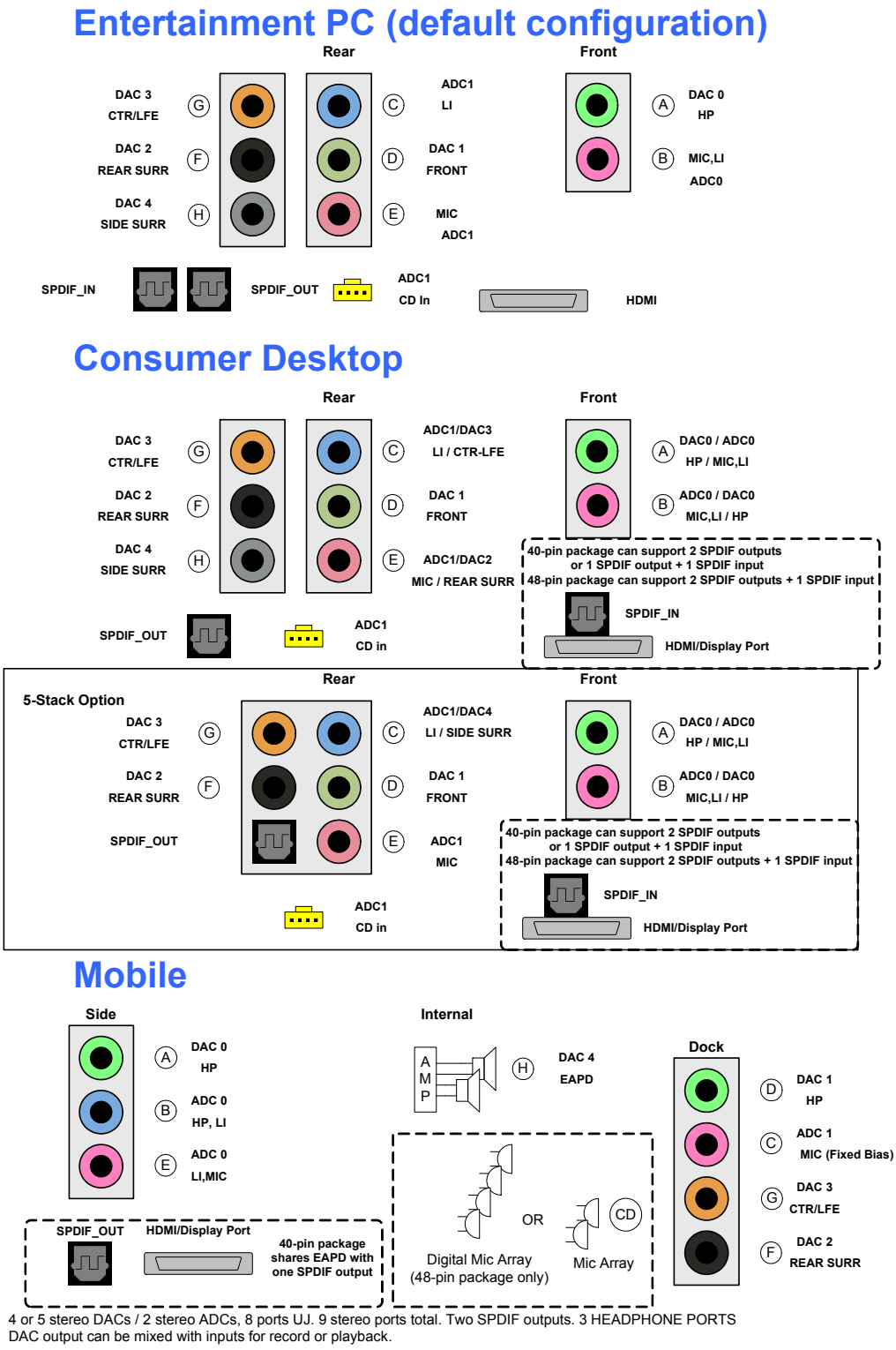


Figure 13. Port Configurations

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6.1. Pin Configuration Default Register Settings

The following table shows the Pin Widget Configuration Default settings. Consumer Desktop 5-jack implementation with 2 jacks in front and 5 or 6 jacks in rear. The front panel headphone and mic are dedicated to RTC as suggested by Microsoft. SPDIF_OUT is implemented as an SPDIF optical out jack and a second port as HDMI. SPDIF_In is implemented as an optical input. Digital Microphones are listed as part of the muxed capture device.

Pin Name	Port	Location	Device	Connection	Color	Misc	Assoc.	Seq
PortAPin	Jack 00b	Main Front 2h	HP Out 2h	1/8 inch Jack 1h	Green 4h	Jack Detect Override=0	1h	0h
PortBPin	Jack 00b	Main Front 2h	Mic In Ah	1/8 inch Jack 1h	Pink 9h	Jack Detect Override=0	2h	0h
PortCPin	Jack 00b	Main Rear 1h	Line In 8h	1/8 inch Jack 1h	Blue 3h	Jack Detect Override=0	4h	0h
PortDPin	Jack 00b	Main Rear 1h	Line Out 0h	1/8 inch Jack 1h	Green 4h	Jack Detect Override=0	3h	0h
PortEPin	Jack 00b	Main Rear 1h	Mic In Ah	1/8 inch Jack 1h	Pink 9h	Jack Detect Override=0	4h	Eh
PortFPin	Jack 00b	Main Rear 1h	Line Out 0h	1/8 inch Jack 1h	Black 1h	Jack Detect Override=0	3h	2h
PortGPin	Jack 00b	Main Rear 1h	Line Out 0h	1/8 inch Jack 1h	Orange 6h	Jack Detect Override=0	3h	1h
PortHPin	Jack 00b	Main Rear 1h	Line Out 0h	1/8 inch Jack 1h	Gray 2h	Jack Detect Override=0	3h	4h
DMIC0 (48pin)	Internal 10b	Internal 010000b	Mic In Ah	ATAPI 3h	Unknown 0h	Jack Detect Override=1	4h	2h
DMIC0 (40pin)	NA	NA	NA	NA	NA	NA	NA	NA
DMIC1 (48pin)	Internal 10b	Internal 010000b	Mic In Ah	ATAPI 3h	Unknown 0h	Jack Detect Override=1	4h	3h
DMIC1 (40pin)	NA	NA	NA	NA	NA	NA	NA	NA
Dig0Pin	Jack 00b	Main Rear 000001b	SPDIF Out 4h	optical 5h	Black 1h	Jack Detect Override=1	5h	0h
DIG1pin(48pin)	Internal 10b	Internal 011000b	Dig Other Out 5h	Other Digital 6h	Unknown 0h	Jack Detect Override=1	6h	0h
DIG1pin(40pin)	NA	NA	NA	NA	NA	NA	NA	NA
Dig2Pin	Jack 00b	Main Rear 000001b	SPDIF IN Ch	optical 5h	Gray 2h	Jack Detect Override=1	7h	0h
CDPin	Internal 10b	Int ATAPI 011001b	CD 3h	ATAPI 3h	Unknown 0h	Jack Detect Override=0	4h	1h

Table 25. Pin Configuration Default Settings

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7. WIDGET INFORMATION

Bits [39:32]	Bits [31:28]	BITS [27:20]	BITS[19:16]	BITS [15:0]
Reserved	CODEC Address	NID	Verb ID (4-bit)	Payload Data (16-bit)

Table 26. Command Format for Verb with 4-bit Identifier

Bits [39:32]	Bits [31:28]	BITS [27:20]	BITS[19:8]	BITS [7:0]
Reserved	CODEC Address	NID	Verb ID (12-bit)	Payload Data (8-bit)

Table 27. Command Format for Verb with 12-bit Identifier

There are two types of responses: Solicited and Unsolicited. Solicited responses are provided as a direct response to an issued command and will be provided in the frame immediately following the command. Unsolicited responses are provided by the CODEC independent of any command. Unsolicited responses are the result of CODEC events such as a jack insertion detection. The formats for Solicited Responses and Unsolicited Responses are shown in the tables below. The “Tag” field in bits [31:28] of the Unsolicited Response identify the event.

Bit [35]	Bit [34]	BITS [33:32]	BITS[31:0]
Valid (Valid = 1)	UnSol = 0	Reserved	Response

Table 28. Solicited Response Format

Bit [35]	Bit [34]	BITS [33:32]	BITS[31:28]	BITS [27:0]
Valid (Valid = 1)	UnSol = 1	Reserved	Tag	Response

Table 29. Unsolicited Response Format

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7.1. Widget List

ID	Widget Name	Description
00h	Root	Root Node
01h	AFG	Audio Function Group
0Ah	Port A	Port A Pin Widget
0Bh	Port B	Port B Pin Widget
0Ch	Port C	Port C Pin Widget
0Dh	Port D	Port D Pin Widget
0Eh	Port E	Port E Pin Widget
0Fh	Port F	Port F Pin Widget
10h	Port G	Port G Widget
11h	Port H	Port H Pin Widget
12h	CD	CD input
13h	DigMic0	Digital Microphone Pin Widget (48pin only, Rsvd in 40pin)
14h	DigMic1	Digital Microphone Pin Widget (48pin only, Rsvd in 40pin)
15h	DAC0	DAC
16h	DAC1	DAC
17h	DAC2	DAC
18h	DAC3	DAC
19h	DAC4	DAC
1Ah	ADC0	ADC
1Bh	ADC1	ADC
1Ch	PCBeep	Digital PC Beep Widget
1Dh	Mixer	Input Mixer (Input Ports, DACs, Analog PC_Beep)
1Eh	MixerOutVol	Volume control for analog mixer
1Fh	DAC5	DAC
20h	ADC0Mux	ADC Mux with volume and mute
21h	ADC1Mux	ADC Mux with volume and mute
22h	Dig0Pin	Digital I/O Pin
23h	Dig1Pin	Digital I/O Pin (48pin only, Rsvd in 40pin)
24h	Dig2Pin	Digital I/O Pin
25h	SPDIFOut0	Stereo Output for SPDIF_Out
26h	SPDIFOut1	Stereo Output for SPDIF_Out
27h	SPDIFIN	SPDIF Input
28h	InPort0Mux	Input port pre-select for mixer
29h	InPort1Mux	Input port pre-select for mixer
2Ah	InPort2Mux	Input port pre-select for mixer

Table 30. Widget List

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ID	Widget Name	Description
2Bh	InPort3Mux	Input port pre-select for mixer
2Ch	VSW	Vendor Specific Widget

Table 30. Widget List

7.2. Root (NID = 00h): VendorID

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0000h			

Field Name	Bits	R/W	Default	Reset
Vendor	31:16	R	111Dh	N/A
	Vendor ID.			
DeviceFix	15:8	R	see table below	N/A
	Device ID.			
DeviceProg	7:0	R	see table below	N/A
	Device ID.			

Device	Device ID	Package	HD Audio Bus Voltage
92HD89E3	76CCh	48QFP	DVDDIO selectable
92HD89E2	76CDh	40QFN	3.3V‘
92HD89E1	76CEh	40QFN	1.5V

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7.3. Root (NID = 00h): RevID

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0002h			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:24	R	00h	N/A (Hard-coded)
	Reserved.			
Major	23:20	R	1h	N/A (Hard-coded)
	Major rev number of compliant HD Audio spec.			
Minor	19:16	R	0h	N/A (Hard-coded)
	Minor rev number of compliant HD Audio spec.			
RevisionFix	15:12	R	xh	N/A (Hard-coded)
	Vendor's rev number for this device.			
RevisionProg	11:8	R	xh	N/A (Hard-coded)
	Vendor's rev number for this device.			
SteppingFix	7:4	R	xh	N/A (Hard-coded)
	Vendor stepping number within the Vendor RevID.			
SteppingProg	3:0	R	xh	N/A (Hard-coded)
	Vendor stepping number within the Vendor RevID.			

7.3.1. Root (NID = 00h): NodeInfo

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0004h			

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Field Name	Bits	R/W	Default	Reset
Rsvd2	31:24	R	00h	N/A (Hard-coded)
	Reserved.			
StartNID	23:16	R	01h	N/A (Hard-coded)
	Starting node number (NID) of first function group			
Rsvd1	15:8	R	00h	N/A (Hard-coded)
	Reserved.			
TotalNodes	7:0	R	01h	N/A (Hard-coded)
	Total number of nodes			

7.4. AFG (NID = 01h): NodeInfo

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0004h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:24	R	00h	N/A (Hard-coded)
	Reserved.			
StartNID	23:16	R	0Ah	N/A (Hard-coded)
	Starting node number for function group subordinate nodes.			
Rsvd1	15:8	R	00h	N/A (Hard-coded)
	Reserved.			
TotalNodes	7:0	R	22h	N/A (Hard-coded)
	Total number of nodes.			

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7.4.1. AFG (NID = 01h): FGType

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0005h			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:9	R	000000h	N/A (Hard-coded)
	Reserved.			
UnSol	8	R	1h	N/A (Hard-coded)
	Unsolicited response supported: 1 = yes, 0 = no.			
NodeType	7:0	R	1h	N/A (Hard-coded)
	Function group type: 00h = Reserved 01h = Audio Function Group 02h = Vendor Defined Modem Function Group 03h-7Fh = Reserved 80h-FFh = Vendor Defined Function Group			

7.4.2. AFG (NID = 01h): AFGCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0008h			

Field Name	Bits	R/W	Default	Reset
Rsvd3	31:17	R	00h	N/A (Hard-coded)
	Reserved.			
BeepGen	16	R	1h	N/A (Hard-coded)
	Beep generator present: 1 = yes, 0 = no.			

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Field Name	Bits	R/W	Default	Reset
Rsvd2	15:12	R	0h	N/A (Hard-coded)
	Reserved.			
InputDelay	11:8	R	Dh	N/A (Hard-coded)
	Typical latency in frames. Number of samples between when the sample is received as an analog signal at the pin and when the digital representation is transmitted on the HD Audio link.			
Rsvd1	7:4	R	0h	N/A (Hard-coded)
	Reserved.			
OutputDelay	3:0	R	Dh	N/A (Hard-coded)
	Typical latency in frames. Number of samples between when the signal is received from the HD Audio link and when it appears as an analog signal at the pin.			

7.4.3. AFG (NID = 01h): PCMCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Ah			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:21	R	000h	N/A (Hard-coded)
	Reserved.			
B32	20	R	0h	N/A (Hard-coded)
	32 bit audio format support: 1 = yes, 0 = no.			
B24	19	R	1h	N/A (Hard-coded)
	24 bit audio format support: 1 = yes, 0 = no.			
B20	18	R	1h	N/A (Hard-coded)
	20 bit audio format support: 1 = yes, 0 = no.			

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Field Name	Bits	R/W	Default	Reset
B16	17	R	1h	N/A (Hard-coded)
	16 bit audio format support: 1 = yes, 0 = no.			
B8	16	R	0h	N/A (Hard-coded)
	8 bit audio format support: 1 = yes, 0 = no.			
Rsvd1	15:12	R	0h	N/A (Hard-coded)
	Reserved.			
R12	11	R	0h	N/A (Hard-coded)
	384kHz rate support: 1 = yes, 0 = no.			
R11	10	R	1h	N/A (Hard-coded)
	192kHz rate support: 1 = yes, 0 = no.			
R10	9	R	0h	N/A (Hard-coded)
	176.4kHz rate support: 1 = yes, 0 = no.			
R9	8	R	1h	N/A (Hard-coded)
	96kHz rate support: 1 = yes, 0 = no.			
R8	7	R	1h	N/A (Hard-coded)
	88.2kHz rate support: 1 = yes, 0 = no.			
R7	6	R	1h	N/A (Hard-coded)
	48kHz rate support: 1 = yes, 0 = no.			
R6	5	R	1h	N/A (Hard-coded)
	44.1kHz rate support: 1 = yes, 0 = no.			
R5	4	R	0h	N/A (Hard-coded)
	32kHz rate support: 1 = yes, 0 = no.			
R4	3	R	0h	N/A (Hard-coded)
	22.05kHz rate support: 1 = yes, 0 = no.			
R3	2	R	0h	N/A (Hard-coded)
	16kHz rate support: 1 = yes, 0 = no.			

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Field Name	Bits	R/W	Default	Reset
R2	1	R	0h	N/A (Hard-coded)
	11.025kHz rate support: 1 = yes, 0 = no.			
R1	0	R	0h	N/A (Hard-coded)
	8kHz rate support: 1 = yes, 0 = no.			

7.4.4. AFG (NID = 01h): StreamCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Bh			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:3	R	00000000h	N/A (Hard-coded)
	Reserved.			
AC3	2	R	0h	N/A (Hard-coded)
	AC-3 formatted data support: 1 = yes, 0 = no.			
Float32	1	R	0h	N/A (Hard-coded)
	Float32 formatted data support: 1 = yes, 0 = no.			
PCM	0	R	1h	N/A (Hard-coded)
	PCM-formatted data support: 1 = yes, 0 = no.			

7.4.5. AFG (NID = 01h): InAmpCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Dh			

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Field Name	Bits	R/W	Default	Reset
Mute	31	R	0h	N/A (Hard-coded)
	Mute support: 1 = yes, 0 = no.			
Rsvd3	30:23	R	00h	N/A (Hard-coded)
	Reserved.			
StepSize	22:16	R	27h	N/A (Hard-coded)
	Size of each step in the gain range: 0 to 127 = .25dB to 32dB, in .25dB steps.			
Rsvd2	15	R	0h	N/A (Hard-coded)
	Reserved.			
NumSteps	14:8	R	03h	N/A (Hard-coded)
	Number of gains steps (number of possible settings - 1).			
Rsvd1	7	R	0h	N/A (Hard-coded)
	Reserved.			
Offset	6:0	R	00h	N/A (Hard-coded)
	Indicates which step is 0dB			

7.4.6. AFG (NID = 01h): PwrStateCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Fh			

Field Name	Bits	R/W	Default	Reset
EPSS	31	R	1h	N/A (Hard-coded)
	Extended power states support: 1 = yes, 0 = no.			
ClkStop	30	R	1h	N/A (Hard-coded)
	D3 clock stop support: 1 = yes, 0 = no.			

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Field Name	Bits	R/W	Default	Reset
LPD3Sup	29	R	1h	N/A (Hard-coded)
	Codec state intended during system S3 state: 0 = D3Hot, 1 = D3Cold			
Rsvd	28:5	R	000000h	N/A (Hard-coded)
	Reserved.			
D3ColdSup	4	R	1h	N/A (Hard-coded)
	D3Cold power state support: 1 = yes, 0 = no.			
D3Sup	3	R	1h	N/A (Hard-coded)
	D3 power state support: 1 = yes, 0 = no.			
D2Sup	2	R	1h	N/A (Hard-coded)
	D2 power state support: 1 = yes, 0 = no.			
D1Sup	1	R	1h	N/A (Hard-coded)
	D1 power state support: 1 = yes, 0 = no.			
D0Sup	0	R	1h	N/A (Hard-coded)
	D0 power state support: 1 = yes, 0 = no.			

7.4.7. AFG (NID = 01h): GPIOCnt

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0011h			

Field Name	Bits	R/W	Default	Reset
GPIWake	31	R	1h	N/A (Hard-coded)
	Wake capability. Assuming the Wake Enable Mask controls are enabled, GPIO's configured as inputs can cause a wake (generate a Status Change event on the link) when there is a change in level on the pin.			
GPIUnsol	30	R	1h	N/A (Hard-coded)
	GPIO unsolicited response support: 1 = yes, 0 = no.			
Rsvd	29:24	R	00h	N/A (Hard-coded)
	Reserved.			

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Field Name	Bits	R/W	Default	Reset
NumGPIs	23:16	R	00h	N/A (Hard-coded)
	Number of GPI pins supported by function group.			
NumGPOs	15:8	R	00h	N/A (Hard-coded)
	Number of GPO pins supported by function group.			
NumGPIOs	7:0	R	48QFN=07h 40QFN=03h	N/A (Hard-coded)
	Number of GPIO pins supported by function group. Note different default by package options.			

7.4.8. AFG (NID = 01h): OutAmpCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0012h			

Field Name	Bits	R/W	Default	Reset
Mute	31	R	1h	N/A (Hard-coded)
	Mute support: 1 = yes, 0 = no.			
Rsvd3	30:23	R	00h	N/A (Hard-coded)
	Reserved.			
StepSize	22:16	R	02h	N/A (Hard-coded)
	Size of each step in the gain range: 0 to 127 = .25dB to 32dB, in .25dB steps.			
Rsvd2	15	R	0h	N/A (Hard-coded)
	Reserved.			
NumSteps	14:8	R	7Fh	N/A (Hard-coded)
	Number of gains steps (number of possible settings - 1).			
Rsvd1	7	R	0h	N/A (Hard-coded)
	Reserved.			

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Field Name	Bits	R/W	Default	Reset
Offset	6:0	R	7Fh	N/A (Hard-coded)
	Indicates which step is 0dB			

7.4.9. AFG (NID = 01h): PwrState

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				705h
Get	F0500h			

Field Name	Bits	R/W	Default	Reset
Rsvd3	31:11	R	000000h	N/A (Hard-coded)
	Reserved.			
SettingsReset	10	R	1h	POR - DAFG - ULR
	Indicates if any persistent settings in this Function Group have been reset. Cleared by PwrState 'Get' to this Widget.			
ClkStopOK	9	R	1h	POR - DAFG - ULR
	Bit clock can currently be removed: 1 = yes, 0 = no.			
Error	8	R	0h	POR - DAFG - ULR
	Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state.			
Rsvd2	7	R	0h	N/A (Hard-coded)
	Reserved.			
Act	6:4	R	3h	POR - DAFG - LR
	Actual power state of this widget.			
Rsvd1	3	R	0h	N/A (Hard-coded)
	Reserved.			
Set	2:0	RW	3h	POR - DAFG - LR
	Current power state setting for this widget.			

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7.4.10. AFG (NID = 01h): UnsolResp

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				708h
Get	F0800h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
En	7	RW	0h	POR - DAFG - ULR
	Unsolicited response enable: 1 = enabled, 0 = disabled.			
Rsvd1	6	R	0h	N/A (Hard-coded)
	Reserved.			
Tag	5:0	RW	00h	POR - DAFG - ULR
	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.			

7.4.11. AFG (NID = 01h): GPIO

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				715h
Get	F1500h			

Please note that the 40QFN package version only supports GPIO0, GPIO1 and GPIO2.

Field Name	Bits	R/W	Default	Reset
Rsvd	31:7	R	00000000h	N/A (Hard-coded)
	Reserved.			
Data6	6	RW	0h	POR-DAFG-ULR
	Data for GPIO6. If this GPIO bit is configured as Sticky (edge-sensitive) imput, it can be cleared by writing “0”. For details of read back value, refer to HD Audio spec. section 7.3.3.22.			

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Field Name	Bits	R/W	Default	Reset
Data5	5	RW	0h	POR-DAFG-ULR
	Data for GPIO5. If this GPIO bit is configured as Sticky (edge-sensitive) imput, it can be cleared by writing “0”. For details of read back value, refer to HD Audio spec. section 7.3.3.22.			
Data4	4	RW	0h	POR-DAFG-ULR
	Data for GPIO4. If this GPIO bit is configured as Sticky (edge-sensitive) imput, it can be cleared by writing “0”. For details of read back value, refer to HD Audio spec. section 7.3.3.22.			
Data3	3	RW	0h	POR-DAFG-ULR
	Data for GPIO3. If this GPIO bit is configured as Sticky (edge-sensitive) imput, it can be cleared by writing “0”. For details of read back value, refer to HD Audio spec. section 7.3.3.22.			
Data2	2	RW	0h	POR - DAFG - ULR
	Data for GPIO2. If this GPIO bit is configured as Sticky (edge-sensitive) input, it can be cleared by writing "0". For details of read back value, refer to HD Audio spec. section 7.3.3.22.			
Data1	1	RW	0h	POR - DAFG - ULR
	Data for GPIO1. If this GPIO bit is configured as Sticky (edge-sensitive) input, it can be cleared by writing "0". For details of read back value, refer to HD Audio spec. section 7.3.3.22.			
Data0	0	RW	0h	POR - DAFG - ULR
	Data for GPIO0. If this GPIO bit is configured as Sticky (edge-sensitive) input, it can be cleared by writing "0". For details of read back value, refer to HD Audio spec. section 7.3.3.22.			

7.4.12. AFG (NID = 01h): GPIOEn

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				716h
Get	F1600h			

Please note that the 40QFN package version only supports GPIO0, GPIO1 and GPIO2.

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Field Name	Bits	R/W	Default	Reset
Rsvd	31:7	R	00000000h	N/A (Hard-coded)
	Reserved.			
Mask6	6	RW	0h	POR - DAFG - ULR
	Enable for GPIO6: 0 = pin is disabled (Hi-Z state); 1 = pin is enabled; behavior determined by GPIO Direction control.			
Mask5	5	RW	0h	POR - DAFG - ULR
	Enable for GPIO5: 0 = pin is disabled (Hi-Z state); 1 = pin is enabled; behavior determined by GPIO Direction control.			
Mask4	4	RW	0h	POR - DAFG - ULR
	Enable for GPIO4: 0 = pin is disabled (Hi-Z state); 1 = pin is enabled; behavior determined by GPIO Direction control.			
Mask3	3	RW	0h	POR - DAFG - ULR
	Enable for GPIO3: 0 = pin is disabled (Hi-Z state); 1 = pin is enabled; behavior determined by GPIO Direction control.			
Mask2	2	RW	0h	POR - DAFG - ULR
	Enable for GPIO2: 0 = pin is disabled (Hi-Z state); 1 = pin is enabled; behavior determined by GPIO Direction control.			
Mask1	1	RW	0h	POR - DAFG - ULR
	Enable for GPIO1: 0 = pin is disabled (Hi-Z state); 1 = pin is enabled; behavior determined by GPIO Direction control.			
Mask0	0	RW	0h	POR - DAFG - ULR
	Enable for GPIO0: 0 = pin is disabled (Hi-Z state); 1 = pin is enabled; behavior determined by GPIO Direction control.			

7.4.13. AFG (NID = 01h): GPIODir

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				717h
Get	F1700h			

Please note that the 40QFN package version only supports GPIO0, GPIO1 and GPIO2.

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Field Name	Bits	R/W	Default	Reset
Rsvd	31:7	R	00000000h	N/A (Hard-coded)
	Reserved.			
Control6	6	RW	0h	POR - DAFG - ULR
	Direction control for GPIO6: 0 = GPIO is configured as input; 1 = GPIO is configured as output.			
Control5	5	RW	0h	POR - DAFG - ULR
	Direction control for GPIO5: 0 = GPIO is configured as input; 1 = GPIO is configured as output.			
Control4	4	RW	0h	POR - DAFG - ULR
	Direction control for GPIO4: 0 = GPIO is configured as input; 1 = GPIO is configured as output.			
Control3	3	RW	0h	POR - DAFG - ULR
	Direction control for GPIO3: 0 = GPIO is configured as input; 1 = GPIO is configured as output.			
Control2	2	RW	0h	POR - DAFG - ULR
	Direction control for GPIO2: 0 = GPIO is configured as input; 1 = GPIO is configured as output.			
Control1	1	RW	0h	POR - DAFG - ULR
	Direction control for GPIO1: 0 = GPIO is configured as input; 1 = GPIO is configured as output.			
Control0	0	RW	0h	POR - DAFG - ULR
	Direction control for GPIO0: 0 = GPIO is configured as input; 1 = GPIO is configured as output.			

7.4.14. AFG (NID = 01h): GPIOWakeEn

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				718h
Get	F1800h			

Please note that the 40QFN package version only supports GPIO0, GPIO1 and GPIO2.

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Field Name	Bits	R/W	Default	Reset
Rsvd	31:7	R	00000000h	N/A (Hard-coded)
	Reserved.			
W6	6	RW	0h	POR - DAFG - ULR
	Wake enable for GPIO6: 0 = wake-up event is disabled; 1 = When HD Audio link is powered down (RST# is asserted), a wake-up event will trigger a Status Change Request event on the link.			
W5	5	RW	0h	POR - DAFG - ULR
	Wake enable for GPIO5: 0 = wake-up event is disabled; 1 = When HD Audio link is powered down (RST# is asserted), a wake-up event will trigger a Status Change Request event on the link.			
W4	4	RW	0h	POR - DAFG - ULR
	Wake enable for GPIO4: 0 = wake-up event is disabled; 1 = When HD Audio link is powered down (RST# is asserted), a wake-up event will trigger a Status Change Request event on the link.			
W3	3	RW	0h	POR - DAFG - ULR
	Wake enable for GPIO3: 0 = wake-up event is disabled; 1 = When HD Audio link is powered down (RST# is asserted), a wake-up event will trigger a Status Change Request event on the link.			
W2	2	RW	0h	POR - DAFG - ULR
	Wake enable for GPIO2: 0 = wake-up event is disabled; 1 = When HD Audio link is powered down (RST# is asserted), a wake-up event will trigger a Status Change Request event on the link.			
W1	1	RW	0h	POR - DAFG - ULR
	Wake enable for GPIO1: 0 = wake-up event is disabled; 1 = When HD Audio link is powered down (RST# is asserted), a wake-up event will trigger a Status Change Request event on the link.			
W0	0	RW	0h	POR - DAFG - ULR
	Wake enable for GPIO0: 0 = wake-up event is disabled; 1 = When HD Audio link is powered down (RST# is asserted), a wake-up event will trigger a Status Change Request event on the link.			

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7.4.15. AFG (NID = 01h): GPIOUnsol

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				719h
Get	F1900h			

Please note that the 40QFN package version only supports GPIO0, GPIO1 and GPIO2.

Field Name	Bits	R/W	Default	Reset
Rsvd	31:7	R	00000000h	N/A (Hard-coded)
	Reserved.			
EnMask6	6	RW	0h	POR - DAFG - ULR
	Unsolicited enable mask for GPIO6. If set, and the Unsolicited Response control for this widget has been enabled, an unsolicited response will be sent when GPIO2 is configured as input and changes state.			
EnMask5	5	RW	0h	POR - DAFG - ULR
	Unsolicited enable mask for GPIO5. If set, and the Unsolicited Response control for this widget has been enabled, an unsolicited response will be sent when GPIO2 is configured as input and changes state.			
EnMask4	4	RW	0h	POR - DAFG - ULR
	Unsolicited enable mask for GPIO4. If set, and the Unsolicited Response control for this widget has been enabled, an unsolicited response will be sent when GPIO2 is configured as input and changes state.			
EnMask3	3	RW	0h	POR - DAFG - ULR
	Unsolicited enable mask for GPIO3. If set, and the Unsolicited Response control for this widget has been enabled, an unsolicited response will be sent when GPIO2 is configured as input and changes state.			
EnMask2	2	RW	0h	POR - DAFG - ULR
	Unsolicited enable mask for GPIO2. If set, and the Unsolicited Response control for this widget has been enabled, an unsolicited response will be sent when GPIO2 is configured as input and changes state.			
EnMask1	1	RW	0h	POR - DAFG - ULR
	Unsolicited enable mask for GPIO1. If set, and the Unsolicited Response control for this widget has been enabled, an unsolicited response will be sent when GPIO1 is configured as input and changes state.			

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Field Name	Bits	R/W	Default	Reset
EnMask0	0	RW	0h	POR - DAFG - ULR
	Unsolicited enable mask for GPIO0. If set, and the Unsolicited Response control for this widget has been enabled, an unsolicited response will be sent when GPIO0 is configured as input and changes state.			

7.4.16. AFG (NID = 01h): GPIOSticky

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				71Ah
Get	F1A00h			

Please note that the 40QFN package version only supports GPIO0, GPIO1 and GPIO2.

Field Name	Bits	R/W	Default	Reset
Rsvd	31:7	R	00000000h	N/A (Hard-coded)
	Reserved.			
Mask6	6	RW	0h	POR - DAFG - ULR
	GPIO6 input type (when configured as input): 0 = Non-Sticky (level-sensitive); 1 = Sticky (edge-sensitive).			
Mask5	5	RW	0h	POR - DAFG - ULR
	GPIO5input type (when configured as input): 0 = Non-Sticky (level-sensitive); 1 = Sticky (edge-sensitive).			
Mask4	4	RW	0h	POR - DAFG - ULR
	GPIO4 input type (when configured as input): 0 = Non-Sticky (level-sensitive); 1 = Sticky (edge-sensitive).			
Mask3	3	RW	0h	POR - DAFG - ULR
	GPIO3 input type (when configured as input): 0 = Non-Sticky (level-sensitive); 1 = Sticky (edge-sensitive).			
Mask2	2	RW	0h	POR - DAFG - ULR
	GPIO2 input type (when configured as input): 0 = Non-Sticky (level-sensitive); 1 = Sticky (edge-sensitive).			

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Field Name	Bits	R/W	Default	Reset
Mask1	1	RW	0h	POR - DAFG - ULR
	GPIO1 input type (when configured as input): 0 = Non-Sticky (level-sensitive); 1 = Sticky (edge-sensitive).			
Mask0	0	RW	0h	POR - DAFG - ULR
	GPIO0 input type (when configured as input): 0 = Non-Sticky (level-sensitive); 1 = Sticky (edge-sensitive).			

7.4.17. AFG (NID = 01h): SubID

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set	723h	722h	721h	720h
Get	F2300h / F2200h / F2100h / F2000h			

Field Name	Bits	R/W	Default	Reset
Subsys3	31:24	RW	00h	POR
	Subsystem ID (byte 3)			
Subsys2	23:16	RW	00h	POR
	Subsystem ID (byte 2)			
Subsys1	15:8	RW	01h	POR
	Subsystem ID (byte 1)			
Assembly	7:0	RW	00h	POR
	Assembly ID (Not applicable to codec vendors).			

7.4.18. AFG (NID = 01h): GPIOPIrty

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				770h
Get	F7000h			

Please note that the 40QFN package version only supports GPIO0, GPIO1 and GPIO2

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Field Name	Bits	R/W	Default	Reset
Rsvd	31:7	R	00000000h	N/A (Hard-coded)
	Reserved.			
GP6	6	RW	1h	POR - DAFG - ULR
	GPIO6 Polarity: If configured as output or non-sticky input: 0 = inverting 1 = non-inverting If configured as sticky input: 0 = falling edges will be detected 1 = rising edges will be detected			
GP5	5	RW	1h	POR - DAFG - ULR
	GPIO5 Polarity: If configured as output or non-sticky input: 0 = inverting 1 = non-inverting If configured as sticky input: 0 = falling edges will be detected 1 = rising edges will be detected			
GP4	4	RW	1h	POR - DAFG - ULR
	GPIO4 Polarity: If configured as output or non-sticky input: 0 = inverting 1 = non-inverting If configured as sticky input: 0 = falling edges will be detected 1 = rising edges will be detected			
GP3	3	RW	1h	POR - DAFG - ULR
	GPIO3 Polarity: If configured as output or non-sticky input: 0 = inverting 1 = non-inverting If configured as sticky input: 0 = falling edges will be detected 1 = rising edges will be detected			

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Field Name	Bits	R/W	Default	Reset
GP2	2	RW	1h	POR - DAFG - ULR
	GPIO2 Polarity: If configured as output or non-sticky input: 0 = inverting 1 = non-inverting If configured as sticky input: 0 = falling edges will be detected 1 = rising edges will be detected			
GP1	1	RW	1h	POR - DAFG - ULR
	GPIO1 Polarity: If configured as output or non-sticky input: 0 = inverting 1 = non-inverting If configured as sticky input: 0 = falling edges will be detected 1 = rising edges will be detected			
GP0	0	RW	1h	POR - DAFG - ULR
	GPIO0 Polarity: If configured as output or non-sticky input: 0 = inverting 1 = non-inverting If configured as sticky input: 0 = falling edges will be detected 1 = rising edges will be detected			

7.4.19. AFG (NID = 01h): GPIODrive

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				771h
Get	F7100h			

Please note that the 40QFN package version only supports GPIO0, GPIO1 and GPIO2

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Field Name	Bits	R/W	Default	Reset
Rsvd	31:7	R	00000000h	N/A (Hard-coded)
	Reserved.			
OD6	6	RW	0h	POR - DAFG - ULR
	GPIO6 Drive Mode: 0 = push-pull (drive 0 and 1); 1 = open drain (drive 0, float for 1).			
OD5	5	RW	0h	POR - DAFG - ULR
	GPIO5 Drive Mode: 0 = push-pull (drive 0 and 1); 1 = open drain (drive 0, float for 1).			
OD4	4	RW	0h	POR - DAFG - ULR
	GPIO4 Drive Mode: 0 = push-pull (drive 0 and 1); 1 = open drain (drive 0, float for 1).			
OD3	3	RW	0h	POR - DAFG - ULR
	GPIO3 Drive Mode: 0 = push-pull (drive 0 and 1); 1 = open drain (drive 0, float for 1).			
OD2	2	RW	0h	POR - DAFG - ULR
	GPIO2 Drive Mode: 0 = push-pull (drive 0 and 1); 1 = open drain (drive 0, float for 1).			
OD1	1	RW	0h	POR - DAFG - ULR
	GPIO1 Drive Mode: 0 = push-pull (drive 0 and 1); 1 = open drain (drive 0, float for 1).			
OD0	0	RW	0h	POR - DAFG - ULR
	GPIO0 Drive Mode: 0 = push-pull (drive 0 and 1); 1 = open-drain (drive 0, float for 1).			

7.4.20. AFG (NID = 01h): DMic

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				778h
Get	F7800h			

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Field Name	Bits	R/W	Default	Reset
Rsvd	31:6	R	0000000h	N/A (Hard-coded)
	Reserved.			
Mono1	5	RW	0h	POR
	DMic1 mono select: 0 = stereo operation, 1 = mono operation (left channel duplicated to the right channel).			
Mono0	4	RW	0h	POR
	DMic0 mono select: 0 = stereo operation, 1 = mono operation (left channel duplicated to the right channel).			
PhAdj	3:2	RW	0h	POR
	Selects what phase of the DMic clock the data should be latched: 0h = left data rising edge/right data falling edge 1h = left data center of high/right data center of low 2h = left data falling edge/right data rising edge 3h = left data center of low/right data center of high			
Rate	1:0	RW	2h	POR
	Selects the DMic clock rate: 0h = 4.704MHz 1h = 3.528MHz 2h = 2.352MHz 3h = 1.176MHz.			

7.4.21. AFG (NID = 01h): DACMode

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				780h
Get	F8000h			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:9	R	000000h	N/A (Hard-coded)
	Reserved.			

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Field Name	Bits	R/W	Default	Reset
Atten3dB	8	RW	1h	POR - S&DAFG - LR
	Attenuate DAC path signal by 3dB			
SDMSettleDisable	7	RW	0h	POR - S&DAFG - LR
	SDM wait-to-settle disable: 1 = at mute, the SDM switches to the mute pattern immediately 0 = at mute, the SDM switches to the mute pattern after settling (can take up to ~45ms)			
SDMCoeffSel	6	RW	0h	POR - S&DAFG - LR
	DAC SDM coefficient select (stages 1, 2, 3): 1 = 1/16, 1/2, 1/4 0 = 1/16, 1/4, 1/2			
SDMLFHalf	5	RW	0h	POR - S&DAFG - LR
	DAC SDM local feedback coefficient select: 1 = 1/4096, 0 = 1/2048.			
SDMLFDisable	4	RW	0h	POR - S&DAFG - LR
	DAC SDM local feedback disable: 1 = local feedback disabled, 0 = local feedback enabled.			
InvertValid	3	RW	0h	POR - S&DAFG - LR
	DAC Valid Invert: 1 = 7.056MHz valid strobe is inverted, 0 = 7.056MHz valid strobe is not inverted.			
InvertData	2	RW	0h	POR - S&DAFG - LR
	DAC Data Invert: 1 = 1-bit outputs are inverted, 0 = 1-bit outputs are not inverted.			
Atten6dBDisable	1	RW	1h	POR - S&DAFG - LR
	Disable built-in -6dB digital attenuation: 1 = -6dB disabled, 0 = -6dB enabled.			
Fade	0	RW	1h	POR - S&DAFG - LR
	DAC Gain Fade Enable: 1 = gain will be slowly faded from old value to new value (~10ms) 0 = gain will jump immediately to new value.			

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7.4.22. AFG (NID = 01h): ADCMode

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				784h
Get	F8400h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:4	R	0000000h	N/A (Hard-coded)
	Reserved.			
InvertValid	3	RW	0h	POR - S&DAFG - LR
	ADC Valid Invert: 1 = 14.112MHz valid strobe is inverted, 0 = 14.112MHz valid strobe is not inverted.			
InvertData	2	RW	0h	POR - S&DAFG - LR
	ADC Data Invert: 1 = 1-bit inputs are inverted, 0 = 1-bit inputs are not inverted.			
Rsvd1	1:0	R	0h	N/A (Hard-coded)
	Reserved.			

7.4.23. AFG (NID = 01h): EAPD

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				788h
Get	F8800h			

Field Name	Bits	R/W	Default	Reset
Rsvd3	31:15	R	00000h	N/A (Hard-coded)
	Reserved.			
HPBSDInv	14	RW	0h	POR
	HP Amp Shutdown Invert: 0 = Amp will power down (or mute) when EAPD pin is low 1 = Amp will power down (or mute) when EAPD pin is high			

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Field Name	Bits	R/W	Default	Reset
HPBSDMode	13	RW	0h	POR
	HP Amp Shutdown Mode: 0 = Amp will mute when disabled 1 = Amp will enter a low power state when disabled			
HPBSD	12	RW	0h	POR
	HP Amp Shutdown Control Select: 0 = Amp controlled by EAPD pin only 1 = Amp controlled by power state only			
Rsvd2	11	R	0h	N/A (Hard-coded)
	Reserved.			
HPASDInv	10	RW	0h	POR
	HP Amp Shutdown Invert: 0 = Amp will power down (or mute) when EAPD pin is low 1 = Amp will power down (or mute) when EAPD pin is high			
HPASDMode	9	RW	0h	POR
	HP Amp Shutdown Mode: 0 = Amp will mute when disabled 1 = Amp will enter a low power state when disabled			
HPASD	8	RW	0h	POR
	HP Amp Shutdown Control Select: 0 = Amp controlled by EAPD pin only 1 = Amp controlled by power state only			
Rsvd1	7:2	R	0h	N/A (Hard-coded)
	Reserved.			
PinMode	1:0	RW	0h	POR
	EAPD Pin Mode: 00b = Open Drain I/O (Value at pin is wired-AND of EAPD bit and external signal) 01b = CMOS Output (Value of EAPD bit is forced at pin) 1xb = CMOS Input (External signal controls internal amps, EAPD bit ignored)			

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7.4.24. AFG (NID = 01h): PortUse

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				7C0h
Get	FC000h			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	0000000h	N/A (Hard-coded)
	Reserved.			
PortH	7	RW	0h	POR
	Port H usage: 0 = connected as an output, 1 = either not connected or connected as an input.			
PortG	6	RW	0h	POR
	Port G usage: 0 = connected as an output, 1 = either not connected or connected as an input.			
PortF	5	RW	0h	POR
	Port F usage: 0 = connected as an output, 1 = either not connected or connected as an input.			
PortE	4	RW	0h	POR
	Port E usage: 0 = connected as an output, 1 = either not connected or connected as an input.			
PortD	3	RW	0h	POR
	Port D usage: 0 = connected as an output, 1 = either not connected or connected as an input.			
PortC	2	RW	0h	POR
	Port C usage: 0 = connected as an output, 1 = either not connected or connected as an input.			
PortB	1	RW	0h	POR
	Port B usage: 0 = connected as an output, 1 = either not connected or connected as an input.			

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Field Name	Bits	R/W	Default	Reset
PortA	0	RW	0h	POR
	Port A usage: 0 = connected as an output, 1 = either not connected or connected as an input.			

7.4.25. AFG (NID = 01h): VSPwrState

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				7D8h
Get	FD800h			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:2	R	00000000h	N/A (Hard-coded)
	Reserved.			
D5	1	RW	0h	POR - ELR
	Vendor specific D5 power state, only entered once the part is already in D3cold (this bit must be set before the command to enter D3cold). If set, this bit overrides the D4 bit (bit 0). Includes the power savings of D4, but additionally powers down GPIO pins, the VAG amp, and the HP amps. Exits this power state via POR or rising edge of Link Reset.			
D4	0	RW	0h	POR - ELR
	Vendor specific D4 power state, only entered once the part is already in D3cold (this bit must be set before the command to enter D3cold). If the D5 bit (bit 1) is set, this bit is overridden. Includes the power savings of D3cold, but additionally powers down the HDA interface (no responses). Exit this power state via POR or rising edge of Link Reset.			

7.4.26. AFG (NID = 01h): AnaPort

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set			7EDh	7ECh
Get	FEC00h			

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Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	0000000h	N/A (Hard-coded)
	Reserved.			
HPwd	7	RW	0h	POR - S&DAFG - ULR
	Power down Port H.			
GPwd	6	RW	0h	POR - S&DAFG - ULR
	Power down Port G.			
FPwd	5	RW	0h	POR - S&DAFG - ULR
	Power down Port F.			
EPwd	4	RW	0h	POR - S&DAFG - ULR
	Power down Port E.			
DPwd	3	RW	0h	POR - S&DAFG - ULR
	Power down Port D.			
CPwd	2	RW	0h	POR - S&DAFG - ULR
	Power down Port C.			
BPwd	1	RW	0h	POR - S&DAFG - ULR
	Power down Port B.			
APwd	0	RW	0h	POR - S&DAFG - ULR
	Power down Port A.			

7.4.27. AFG (NID = 01h): AnaBeep

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				7EEh
Get	FEE00h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:7	R	0000000h	N/A (Hard-coded)
	Reserved.			

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Field Name	Bits	R/W	Default	Reset
BeepDetect	6	R	0h	POR - DAFG - ULR
	0: no beep present; 1: beep present			
Gain	5:4	RW	3h	POR
	Analog PC Beep Gain: 0h = -24dB, 1h = -18dB, 2h = -12dB, 3h = -6dB.			
CntSel	3:2	RW	0h	POR
	Select counter delay.0h=64ms,1h = 128ms, 2h = 256ms, 3h = 512ms			
Mode	1:0	RW	2h	POR
	Analog PC Beep Mode: 00b = Always disabled 01b = Always enabled 1xb = Enabled during HDA Link Reset only			

7.4.28. AFG (NID = 01h): Reset

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				7FFh
Get	FFF00h			

Field Name	Bits	R/W	Default	Reset
Rsvd1	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
Execute	7:0	W	00h	N/A (Hard-coded)
	Function Reset. Function Group reset is executed when the Set verb 7FF is written with 8-bit payload of 00h. The codec should issue a response to acknowledge receipt of the verb, and then reset the affected Function Group and all associated widgets to their power-on reset values. Some controls such as Configuration Default controls should not be reset. Overlaps Response.			

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7.5. PortA (NID = 0Ah): WCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0009h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:24	R	00h	N/A (Hard-coded)
	Reserved.			
Type	23:20	R	4h	N/A (Hard-coded)
	Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined			
Delay	19:16	R	0h	N/A (Hard-coded)
	Number of sample delays through widget.			
Rsvd1	15:12	R	0h	N/A (Hard-coded)
	Reserved.			
SwapCap	11	R	0h	N/A (Hard-coded)
	Left/right swap support: 1 = yes, 0 = no.			
PwrCntrl	10	R	1h	N/A (Hard-coded)
	Power state support: 1 = yes, 0 = no.			
Dig	9	R	0h	N/A (Hard-coded)
	Digital stream support: 1 = yes (digital), 0 = no (analog).			

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Field Name	Bits	R/W	Default	Reset
ConnList	8	R	1h	N/A (Hard-coded)
	Connection list present: 1 = yes, 0 = no.			
UnSolCap	7	R	1h	N/A (Hard-coded)
	Unsolicited response support: 1 = yes, 0 = no.			
ProcWidget	6	R	0h	N/A (Hard-coded)
	Processing state support: 1 = yes, 0 = no.			
Stripe	5	R	0h	N/A (Hard-coded)
	Striping support: 1 = yes, 0 = no.			
FormatOvrd	4	R	0h	N/A (Hard-coded)
	Stream format override: 1 = yes, 0 = no.			
AmpParOvrd	3	R	0h	N/A (Hard-coded)
	Amplifier capabilities override: 1 = yes, no.			
OutAmpPrsnt	2	R	0h	N/A (Hard-coded)
	Output amp present: 1 = yes, 0 = no.			
InAmpPrsnt	1	R	1h	N/A (Hard-coded)
	Input amp present: 1 = yes, 0 = no.			
Stereo	0	R	1h	N/A (Hard-coded)
	Stereo stream support: 1 = yes (stereo), 0 = no (mono).			

7.5.1. PortA (NID = 0Ah): PinCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Ch			

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Field Name	Bits	R/W	Default	Reset
Rsvd2	31:17	R	0000h	N/A (Hard-coded)
	Reserved.			
EapdCap	16	R	1h	N/A (Hard-coded)
	EAPD support: 1 = yes, 0 = no.			
VrefCntrl	15:8	R	17h	N/A (Hard-coded)
	Vref support: bit 7 = Reserved bit 6 = Reserved bit 5 = 100% support (1 = yes, 0 = no) bit 4 = 80% support (1 = yes, 0 = no) bit 3 = Reserved bit 2 = GND support (1 = yes, 0 = no) bit 1 = 50% support (1 = yes, 0 = no) bit 0 = Hi-Z support (1 = yes, 0 = no)			
Rsvd1	7	R	0h	N/A (Hard-coded)
	Reserved.			
BalancedIO	6	R	0h	N/A (Hard-coded)
	Balanced I/O support: 1 = yes, 0 = no.			
InCap	5	R	1h	N/A (Hard-coded)
	Input support: 1 = yes, 0 = no.			
OutCap	4	R	1h	N/A (Hard-coded)
	Output support: 1 = yes, 0 = no.			
HdphDrvCap	3	R	1h	N/A (Hard-coded)
	Headphone amp present: 1 = yes, 0 = no.			
PresDtctCap	2	R	1h	N/A (Hard-coded)
	Presence detection support: 1 = yes, 0 = no.			
TrigRqd	1	R	0h	N/A (Hard-coded)
	Trigger required for impedance sense: 1 = yes, 0 = no.			

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Field Name	Bits	R/W	Default	Reset
ImpSenseCap	0	R	0h	N/A (Hard-coded)
	Impedance sense support: 1 = yes, 0 = no.			

7.5.2. PortA (NID = 0Ah): ConLst

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Eh			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
LForm	7	R	0h	N/A (Hard-coded)
	Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries.			
ConL	6:0	R	04h	N/A (Hard-coded)
	Number of NID entries in connection list.			

7.5.3. PortA (NID = 0Ah): ConLstEntry0

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0200h			

Field Name	Bits	R/W	Default	Reset
ConL3	31:24	R	19h	N/A (Hard-coded)
	DAC4 Converter widget (0x19)			

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Field Name	Bits	R/W	Default	Reset
ConL2	23:16	R	1Eh	N/A (Hard-coded)
	MixerOutVol Selector widget (0x1E)			
ConL1Range	15	R	1h	N/A (Hard-coded)
	1 = ConL0..ConL1 defines a range of selectable inputs.			
ConL1	14:8	R	18h	N/A (Hard-coded)
	DAC3 Converter widget (0x18)			
ConL0	7:0	R	15h	N/A (Hard-coded)
	DAC0 Converter widget (0x15)			

7.5.4. PortA (NID = 0Ah): InAmpLeft

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				360h
Get	B2000h			

Field Name	Bits	R/W	Default	Reset
Rsvd1	31:2	R	00000000h	N/A (Hard-coded)
	Reserved.			
Gain	1:0	R	0h	POR - DAFG - ULR
	Amp gain step number (see InAmpCap parameter pertaining to this widget).			

7.5.5. PortA (NID = 0Ah): InAmpRight

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				350h
Get	B0000h			

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Field Name	Bits	R/W	Default	Reset
Rsvd1	31:2	R	00000000h	N/A (Hard-coded)
	Reserved.			
Gain	1:0	R	0h	POR - DAFG - ULR
	Amp gain step number (see InAmpCap parameter pertaining to this widget).			

7.5.6. PortA (NID = 0Ah): ConSelectCtrl

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				701h
Get	F0100h			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:3	R	00000000h	N/A (Hard-coded)
	Reserved.			
Index	2:0	RW	0h	POR - DAFG - ULR
	Connection select control index.			

7.5.7. PortA (NID = 0Ah): PwrState

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				705h
Get	F0500h			

Field Name	Bits	R/W	Default	Reset
Rsvd4	31:11	R	000000h	N/A (Hard-coded)
	Reserved.			

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Field Name	Bits	R/W	Default	Reset
SettingsReset	10	R	1h	POR - DAFG - ULR
	Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget.			
Rsvd3	9	R	0h	N/A (Hard-coded)
	Reserved.			
Error	8	R	0h	POR - DAFG - ULR
	Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state.			
Rsvd2	7:6	R	0h	N/A (Hard-coded)
	Reserved.			
Act	5:4	R	3h	POR - DAFG - LR
	Actual power state of this widget.			
Rsvd1	3:2	R	0h	N/A (Hard-coded)
	Reserved.			
Set	1:0	RW	0h	POR - DAFG - LR
	Current power state setting for this widget.			

7.5.8. PortA (NID = 0Ah): PinWCntrl

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				707h
Get	F0700h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
HPhnEn	7	RW	0h	POR - DAFG - ULR
	Headphone amp enable: 1 = enabled, 0 = disabled.			

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Field Name	Bits	R/W	Default	Reset
OutEn	6	RW	0h	POR - DAFG - ULR
	Output enable: 1 = enabled, 0 = disabled.			
InEn	5	R	0h	POR - DAFG - ULR
	Input enable: 1 = enabled, 0 = disabled.			
Rsvd1	4:3	R	0h	N/A (Hard-coded)
	Reserved.			
VRefEn	2:0	R	0h	POR - DAFG - ULR
	Vref selection (See VrefCntrl field of PinCap parameter for supported selections): 000b= HI-Z 001b= 50% 010b= GND 011b= Reserved 100b= 80% 101b= 100% 110b= Reserved 111b= Reserved			

7.5.9. PortA (NID = 0Ah): UnsolResp

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				708h
Get	F0800h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
En	7	RW	0h	POR - DAFG - ULR
	Unsolicited response enable (also enables Wake events for this Widget): 1 = enabled, 0 = disabled.			
Rsvd1	6	R	0h	N/A (Hard-coded)
	Reserved.			

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Field Name	Bits	R/W	Default	Reset
Tag	5:0	RW	00h	POR - DAFG - ULR
	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.			

7.5.10. PortA (NID = 0Ah): ChSense

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				709h
Get	F0900h			

Field Name	Bits	R/W	Default	Reset
PresDtct	31	R	0h	POR
	Presence detection indicator: 1 = presence detected; 0 = presence not detected.			
Rsvd	30:0	R	00000000h	N/A (Hard-coded)
	Reserved.			

7.5.11. PortA (NID = 0Ah): EAPDBTLLR

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				70Ch
Get	F0C00h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:2	R	00000000h	N/A (Hard-coded)
	Reserved.			
EAPD	1	RW	1h	POR - DAFG - ULR
	EAPD control: 1 = set EAPD pin to 1 (powered) up if this pin is powered up, 0 = set EAPD pin to 0.			

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Field Name	Bits	R/W	Default	Reset
Rsvd1	0	R	0h	N/A (Hard-coded)
	Reserved.			

7.5.12. PortA (NID = 0Ah): ConfigDefault

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set	71Fh	71Eh	71Dh	71Ch
Get	F1F00h / F1E00h / F1D00h / F1C00h			

Field Name	Bits	R/W	Default	Reset
PortConnectivity	31:30	RW	0h	POR
	Port connectivity: 0h = Port complex is connected to a jack 1h = No physical connection for port 2h = Fixed function device is attached 3h = Both jack and internal device attached (info in all other fields refers to integrated device, any presence detection refers to jack)			
Location	29:24	RW	02h	POR
	Location Bits [5..4]: 0h = External on primary chassis 1h = Internal 2h = Separate chassis 3h = Other Bits [3..0]: 0h = N/A 1h = Rear 2h = Front 3h = Left 4h = Right 5h = Top 6h = Bottom 7h-9h = Special Ah-Fh = Reserved			

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Field Name	Bits	R/W	Default	Reset
Device	23:20	RW	2h	POR
	Default device: 0h = Line out 1h = Speaker 2h = HP out 3h = CD 4h = SPDIF Out 5h = Digital other out 6h = Modem line side 7h = Modem handset side 8h = Line in 9h = Aux Ah = Mic in Bh = Telephony Ch = SPDIF In Dh = Digital other in Eh = Reserved Fh = Other			
ConnectionType	19:16	RW	1h	POR
	Connection type: 0h = Unknown 1h = 1/8" stereo/mono 2h = 1/4" stereo/mono 3h = ATAPI internal 4h = RCA 5h = Optical 6h = Other digital 7h = Other analog 8h = Multichannel analog (DIN) 9h = XLR/Professional Ah = RJ-11 (modem) Bh = Combination Ch-Eh = Reserved Fh = Other			

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Field Name	Bits	R/W	Default	Reset
Color	15:12	RW	4h	POR
	Color: 0h = Unknown 1h = Black 2h = Grey 3h = Blue 4h = Green 5h = Red 6h = Orange 7h = Yellow 8h = Purple 9h = Pink Ah-Dh = Reserved Eh = White Fh = Other			
Misc	11:8	RW	0h	POR
	Miscellaneous: Bits [3..1] = Reserved Bit 0 = Jack detect override			
Association	7:4	RW	1h	POR
	Default assocation.			
Sequence	3:0	RW	0h	POR
	Sequence.			

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7.6. PortB (NID = 0Bh): WCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0009h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:24	R	00h	N/A (Hard-coded)
	Reserved.			
Type	23:20	R	4h	N/A (Hard-coded)
	Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined			
Delay	19:16	R	0h	N/A (Hard-coded)
	Number of sample delays through widget.			
Rsvd1	15:12	R	0h	N/A (Hard-coded)
	Reserved.			
SwapCap	11	R	0h	N/A (Hard-coded)
	Left/right swap support: 1 = yes, 0 = no.			
PwrCntrl	10	R	1h	N/A (Hard-coded)
	Power state support: 1 = yes, 0 = no.			
Dig	9	R	0h	N/A (Hard-coded)
	Digital stream support: 1 = yes (digital), 0 = no (analog).			
ConnList	8	R	1h	N/A (Hard-coded)
	Connection list present: 1 = yes, 0 = no.			

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Field Name	Bits	R/W	Default	Reset
UnSolCap	7	R	1h	N/A (Hard-coded)
	Unsolicited response support: 1 = yes, 0 = no.			
ProcWidget	6	R	0h	N/A (Hard-coded)
	Processing state support: 1 = yes, 0 = no.			
Stripe	5	R	0h	N/A (Hard-coded)
	Striping support: 1 = yes, 0 = no.			
FormatOvrd	4	R	0h	N/A (Hard-coded)
	Stream format override: 1 = yes, 0 = no.			
AmpParOvrd	3	R	0h	N/A (Hard-coded)
	Amplifier capabilities override: 1 = yes, no.			
OutAmpPrsnt	2	R	0h	N/A (Hard-coded)
	Output amp present: 1 = yes, 0 = no.			
InAmpPrsnt	1	R	1h	N/A (Hard-coded)
	Input amp present: 1 = yes, 0 = no.			
Stereo	0	R	1h	N/A (Hard-coded)
	Stereo stream support: 1 = yes (stereo), 0 = no (mono).			

7.6.1. PortB (NID = 0Bh): PinCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Ch			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:17	R	0000h	N/A (Hard-coded)
	Reserved.			

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Field Name	Bits	R/W	Default	Reset
EapdCap	16	R	1h	N/A (Hard-coded)
	EAPD support: 1 = yes, 0 = no.			
VrefCntrl	15:8	R	17h	N/A (Hard-coded)
	Vref support: bit 7 = Reserved bit 6 = Reserved bit 5 = 100% support (1 = yes, 0 = no) bit 4 = 80% support (1 = yes, 0 = no) bit 3 = Reserved bit 2 = GND support (1 = yes, 0 = no) bit 1 = 50% support (1 = yes, 0 = no) bit 0 = Hi-Z support (1 = yes, 0 = no)			
Rsvd1	7	R	0h	N/A (Hard-coded)
	Reserved.			
BalancedIO	6	R	0h	N/A (Hard-coded)
	Balanced I/O support: 1 = yes, 0 = no.			
InCap	5	R	1h	N/A (Hard-coded)
	Input support: 1 = yes, 0 = no.			
OutCap	4	R	1h	N/A (Hard-coded)
	Output support: 1 = yes, 0 = no.			
HdphDrvCap	3	R	1h	N/A (Hard-coded)
	Headphone amp present: 1 = yes, 0 = no.			
PresDtctCap	2	R	1h	N/A (Hard-coded)
	Presence detection support: 1 = yes, 0 = no.			
TrigRqd	1	R	0h	N/A (Hard-coded)
	Trigger required for impedance sense: 1 = yes, 0 = no.			
ImpSenseCap	0	R	0h	N/A (Hard-coded)
	Impedance sense support: 1 = yes, 0 = no.			

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7.6.2. PortB (NID = 0Bh): ConLst

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Eh			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
LForm	7	R	0h	N/A (Hard-coded)
	Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries.			
ConL	6:0	R	04h	N/A (Hard-coded)
	Number of NID entries in connection list.			

7.6.3. PortB (NID = 0Bh): ConLstEntry0

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0200h			

Field Name	Bits	R/W	Default	Reset
ConL3	31:24	R	19h	N/A (Hard-coded)
	DAC4 Converter widget (0x19)			
ConL2	23:16	R	1Eh	N/A (Hard-coded)
	MixerOutVol Selector widget (0x1E)			
ConL1Range	14:8	R	1h	N/A (Hard-coded)
	1 = ConL0..ConL1 defines a range of selectable inputs.			

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Field Name	Bits	R/W	Default	Reset
ConL1	15:8	R	18h	N/A (Hard-coded)
	DAC3 Converter widget (0x18)			
ConL0	7:0	R	15h	N/A (Hard-coded)
	DAC0 Converter widget (0x15)			

7.6.4. PortB (NID = 0Bh): ConSelectCtrl

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				701h
Get	F0100h			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:2	R	00000000h	N/A (Hard-coded)
	Reserved.			
Index	1:0	RW	0h	POR - DAFG - ULR
	Connection select control index.			

7.6.5. PortB (NID = 0Bh): InAmpLeft

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				360h
Get	B2000h			

Field Name	Bits	R/W	Default	Reset
Rsvd1	31:2	R	00000000h	N/A (Hard-coded)
	Reserved.			

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Field Name	Bits	R/W	Default	Reset
Gain	1:0	RW	0h	POR - DAFG - ULR
	Amp gain step number (see InAmpCap parameter pertaining to this widget).			

7.6.6. PortB (NID = 0Bh): InAmpRight

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				350h
Get	B0000h			

Field Name	Bits	R/W	Default	Reset
Rsvd1	31:2	R	00000000h	N/A (Hard-coded)
	Reserved.			
Gain	1:0	RW	0h	POR - DAFG - ULR
	Amp gain step number (see InAmpCap parameter pertaining to this widget).			

7.6.7. PortB (NID = 0Bh): PwrState

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				705h
Get	F0500h			

Field Name	Bits	R/W	Default	Reset
Rsvd4	31:11	R	000000h	N/A (Hard-coded)
	Reserved.			
SettingsReset	10	R	1h	POR - DAFG - ULR
	Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget.			

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Field Name	Bits	R/W	Default	Reset
Rsvd3	9	R	0h	N/A (Hard-coded)
	Reserved.			
Error	8	R	0h	POR - DAFG - ULR
	Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state.			
Rsvd2	7:6	R	0h	N/A (Hard-coded)
	Reserved.			
Act	5:4	R	3h	POR - DAFG - LR
	Actual power state of this widget.			
Rsvd1	3:2	R	0h	N/A (Hard-coded)
	Reserved.			
Set	1:0	RW	0h	POR - DAFG - LR
	Current power state setting for this widget.			

7.6.8. PortB (NID = 0Bh): PinWCntrl

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				707h
Get	F0700h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
HPhnEn	7	RW	0h	POR - DAFG - ULR
	Headphone amp enable: 1 = enabled, 0 = disabled.			
OutEn	6	RW	0h	POR - DAFG - ULR
	Output enable: 1 = enabled, 0 = disabled.			

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Field Name	Bits	R/W	Default	Reset
InEn	5	RW	0h	POR - DAFG - ULR
	Output enable: 1 = enabled, 0 = disabled.			
Rsvd1	4:3	RW	00h	N/A (Hard-coded)
	Reserved.			
VRefEn	2:0	RW	0h	POR - DAFG - ULR
	Vref selection (See VrefCntrl field of PinCap parameter for supported selections): 000b= HI-Z 001b= 50% 010b= GND 011b= Reserved 100b= 80% 101b= 100% 110b= Reserved 111b= Reserved			

7.6.9. PortB (NID = 0Bh): UnsolResp

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				708h
Get	F0800h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
En	7	RW	0h	POR - DAFG - ULR
	Unsolicited response enable (also enables Wake events for this Widget): 1 = enabled, 0 = disabled.			
Rsvd1	6	R	0h	N/A (Hard-coded)
	Reserved.			

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Field Name	Bits	R/W	Default	Reset
Tag	5:0	RW	00h	POR - DAFG - ULR
	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.			

7.6.10. PortB (NID = 0Bh): ChSense

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				709h
Get	F0900h			

Field Name	Bits	R/W	Default	Reset
PresDtct	31	R	0h	POR
	Presence detection indicator: 1 = presence detected; 0 = presence not detected.			
Rsvd	30:0	R	00000000h	N/A (Hard-coded)
	Reserved.			

7.6.11. PortB (NID = 0Bh): EAPDBTLLR

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				70Ch
Get	F0C00h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:2	R	00000000h	N/A (Hard-coded)
	Reserved.			
EAPD	1	RW	1h	POR - DAFG - ULR
	EAPD control: 1 = set EAPD pin to 1 (powered) up if this pin is powered up, 0 = set EAPD pin to 0.			

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Field Name	Bits	R/W	Default	Reset
Rsvd1	0	R	0h	N/A (Hard-coded)
	Reserved.			

7.6.12. PortB (NID = 0Bh): ConfigDefault

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set	71Fh	71Eh	71Dh	71Ch
Get	F1F00h / F1E00h / F1D00h / F1C00h			

Field Name	Bits	R/W	Default	Reset
PortConnectivity	31:30	RW	0h	POR
	Port connectivity: 0h = Port complex is connected to a jack 1h = No physical connection for port 2h = Fixed function device is attached 3h = Both jack and internal device attached (info in all other fields refers to integrated device, any presence detection refers to jack)			
Location	29:24	RW	02h	POR
	Location Bits [5..4]: 0h = External on primary chassis 1h = Internal 2h = Separate chassis 3h = Other Bits [3..0]: 0h = N/A 1h = Rear 2h = Front 3h = Left 4h = Right 5h = Top 6h = Bottom 7h-9h = Special Ah-Fh = Reserved			

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Field Name	Bits	R/W	Default	Reset
Device	23:20	RW	Ah	POR
	Default device: 0h = Line out 1h = Speaker 2h = HP out 3h = CD 4h = SPDIF Out 5h = Digital other out 6h = Modem line side 7h = Modem handset side 8h = Line in 9h = Aux Ah = Mic in Bh = Telephony Ch = SPDIF In Dh = Digital other in Eh = Reserved Fh = Other			
ConnectionType	19:16	RW	1h	POR
	Connection type: 0h = Unknown 1h = 1/8" stereo/mono 2h = 1/4" stereo/mono 3h = ATAPI internal 4h = RCA 5h = Optical 6h = Other digital 7h = Other analog 8h = Multichannel analog (DIN) 9h = XLR/Professional Ah = RJ-11 (modem) Bh = Combination Ch-Eh = Reserved Fh = Other			

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Field Name	Bits	R/W	Default	Reset
Color	15:12	RW	9h	POR
	Color: 0h = Unknown 1h = Black 2h = Grey 3h = Blue 4h = Green 5h = Red 6h = Orange 7h = Yellow 8h = Purple 9h = Pink Ah-Dh = Reserved Eh = White Fh = Other			
Misc	11:8	RW	0h	POR
	Miscellaneous: Bits [3..1] = Reserved Bit 0 = Jack detect override			
Association	7:4	RW	2h	POR
	Default assocation.			
Sequence	3:0	RW	0h	POR
	Sequence.			

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7.7. PortC (NID = 0Ch): WCap

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:24	R	00h	N/A (Hard-coded)
	Reserved.			
Type	23:20	R	4h	N/A (Hard-coded)
	Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined			
Delay	19:16	R	0h	N/A (Hard-coded)
	Number of sample delays through widget.			
Rsvd1	15:12	R	0h	N/A (Hard-coded)
	Reserved.			
SwapCap	11	R	0h	N/A (Hard-coded)
	Left/right swap support: 1 = yes, 0 = no.			
PwrCntrl	10	R	1h	N/A (Hard-coded)
	Power state support: 1 = yes, 0 = no.			
Dig	9	R	0h	N/A (Hard-coded)
	Digital stream support: 1 = yes (digital), 0 = no (analog).			
ConnList	8	R	1h	N/A (Hard-coded)
	Connection list present: 1 = yes, 0 = no.			
UnSolCap	7	R	1h	N/A (Hard-coded)
	Unsolicited response support: 1 = yes, 0 = no.			
ProcWidget	6	R	0h	N/A (Hard-coded)
	Processing state support: 1 = yes, 0 = no.			

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7.7. PortC (NID = 0Ch): WCap

Field Name	Bits	R/W	Default	Reset
Stripe	5	R	0h	N/A (Hard-coded)
	Striping support: 1 = yes, 0 = no.			
FormatOvrd	4	R	0h	N/A (Hard-coded)
	Stream format override: 1 = yes, 0 = no.			
AmpParOvrd	3	R	0h	N/A (Hard-coded)
	Amplifier capabilities override: 1 = yes, no.			
OutAmpPrsnt	2	R	0h	N/A (Hard-coded)
	Output amp present: 1 = yes, 0 = no.			
InAmpPrsnt	1	R	1h	N/A (Hard-coded)
	Input amp present: 1 = yes, 0 = no.			
Stereo	0	R	1h	N/A (Hard-coded)
	Stereo stream support: 1 = yes (stereo), 0 = no (mono).			

7.7.1. PortC (NID = 0Ch): PinCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Ch			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:17	R	0000h	N/A (Hard-coded)
	Reserved.			
EapdCap	16	R	1h	N/A (Hard-coded)
	EAPD support: 1 = yes, 0 = no.			

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Field Name	Bits	R/W	Default	Reset
VrefCntrl	15:8	R	00h	N/A (Hard-coded)
	Vref support: bit 7 = Reserved bit 6 = Reserved bit 5 = 100% support (1 = yes, 0 = no) bit 4 = 80% support (1 = yes, 0 = no) bit 3 = Reserved bit 2 = GND support (1 = yes, 0 = no) bit 1 = 50% support (1 = yes, 0 = no) bit 0 = Hi-Z support (1 = yes, 0 = no)			
Rsvd1	7	R	0h	N/A (Hard-coded)
	Reserved.			
BalancedIO	6	R	0h	N/A (Hard-coded)
	Balanced I/O support: 1 = yes, 0 = no.			
InCap	5	R	1h	N/A (Hard-coded)
	Input support: 1 = yes, 0 = no.			
OutCap	4	R	1h	N/A (Hard-coded)
	Output support: 1 = yes, 0 = no.			
HdphDrvCap	3	R	0h	N/A (Hard-coded)
	Headphone amp present: 1 = yes, 0 = no.			
PresDtctCap	2	R	1h	N/A (Hard-coded)
	Presence detection support: 1 = yes, 0 = no.			
TrigRqd	1	R	0h	N/A (Hard-coded)
	Trigger required for impedance sense: 1 = yes, 0 = no.			
ImpSenseCap	0	R	0h	N/A (Hard-coded)
	Impedance sense support: 1 = yes, 0 = no.			

7.7.2. PortC (NID = 0Ch): ConLst

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				

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7.7.2. PortC (NID = 0Ch): ConLst

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Get	F000Eh			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
LForm	7	R	0h	N/A (Hard-coded)
	Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries.			
ConL	6:0	R	04h	N/A (Hard-coded)
	Number of NID entries in connection list.			

7.7.3. PortC (NID = 0Ch): ConLstEntry0

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0200h			

Field Name	Bits	R/W	Default	Reset
ConL3	31:24	R	19h	N/A (Hard-coded)
	DAC4 Converter widget (0x19)			
ConL2	23:16	R	1Eh	N/A (Hard-coded)
	MixerOutVol Selector widget (0x1E)			
ConL1Range	15	R	1h	N/A (Hard-coded)
	= ConL0..ConL1 defines a range of selectable inputs.			
ConL1	14:8	R	16h	N/A (Hard-coded)
	DAC3 Converter widget (0x16)			

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Field Name	Bits	R/W	Default	Reset
ConL0	7:0	R	15h	N/A (Hard-coded)
	DAC0 Converter widget (0x15)			

7.7.4. PortC (NID = 0Ch): InAmpLeft

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				360h
Get	B2000h			

Field Name	Bits	R/W	Default	Reset
Rsvd1	31:2	R	00000000h	N/A (Hard-coded)
	Reserved.			
Gain	1:0	RW	0h	POR - DAFG - ULR
	Amp gain step number (see InAmpCap parameter pertaining to this widget).			

7.7.5. PortC (NID = 0Ch): InAmpRight

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				350h
Get	B0000h			

Field Name	Bits	R/W	Default	Reset
Rsvd1	31:2	R	00000000h	N/A (Hard-coded)
	Reserved.			
Gain	1:0	RW	0h	POR - DAFG - ULR
	Amp gain step number (see InAmpCap parameter pertaining to this widget).			

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7.7.6. PortC (NID = 0Ch): ConSelectCtrl

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				701h
Get	F0100h			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:2	R	00000000h	N/A (Hard-coded)
	Reserved.			
Index	1:0	RW	0h	POR - DAFG - ULR
	Connection select control index.			

7.7.7. PortC (NID = 0Ch): PwrState

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				705h
Get	F0500h			

Field Name	Bits	R/W	Default	Reset
Rsvd4	31:11	R	000000h	N/A (Hard-coded)
	Reserved.			
SettingsReset	10	R	1h	POR - DAFG - ULR
	Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget.			
Rsvd3	9	R	0h	N/A (Hard-coded)
	Reserved.			
Error	8	R	0h	POR - DAFG - ULR
	Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state.			

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Field Name	Bits	R/W	Default	Reset
Rsvd2	7:6	R	0h	N/A (Hard-coded)
	Reserved.			
Act	5:4	R	3h	POR - DAFG - LR
	Actual power state of this widget.			
Rsvd1	3:2	R	0h	N/A (Hard-coded)
	Reserved.			
Set	1:0	RW	0h	POR - DAFG - LR
	Current power state setting for this widget.			

7.7.8. PortC (NID = 0Ch): PinWCntrl

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				707h
Get	F0700h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:7	R	000000h	N/A (Hard-coded)
	Reserved.			
OutEn	6	RW	0h	POR - DAFG - ULR
	Output enable: 1 = enabled, 0 = disabled.			
InEn	5	RW	0h	POR - DAFG - ULR
	Input enable: 1 = enabled, 0 = disabled.			
Rsvd1	4:3	RW	00h	N/A (Hard-coded)
	Reserved.			
VRefEn	2:0	RW	0h	POR - DAFG - ULR

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Field Name	Bits	R/W	Default	Reset
	Vref selection (See VrefCntrl field of PinCap parameter for supported selections): 000b= HI-Z 001b= 50% 010b= GND 011b= Reserved 100b= 80% 101b= 100% 110b= Reserved 111b= Reserved			

7.7.9. PortC (NID = 0Ch): UnsolResp

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				708h
Get	F0800h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
En	7	RW	0h	POR - DAFG - ULR
	Unsolicited response enable (also enables Wake events for this Widget): 1 = enabled, 0 = disabled.			
Rsvd1	6	R	0h	N/A (Hard-coded)
	Reserved.			
Tag	5:0	RW	00h	POR - DAFG - ULR
	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.			

7.7.10. PortC (NID = 0Ch): ChSense

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				709h
Get	F0900h			

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Field Name	Bits	R/W	Default	Reset
PresDtct	31	R	0h	POR
	Presence detection indicator: 1 = presence detected; 0 = presence not detected.			
Rsvd	30:0	R	00000000h	N/A (Hard-coded)
	Reserved.			

7.7.11. PortC (NID = 0Ch): EAPDBTLLR

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				70Ch
Get	F0C00h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:2	R	00000000h	N/A (Hard-coded)
	Reserved.			
EAPD	1	RW	1h	POR - DAFG - ULR
	EAPD control: 1 = set EAPD pin to 1 (powered) up if this pin is powered up, 0 = set EAPD pin to 0.			
Rsvd1	0	R	0h	N/A (Hard-coded)
	Reserved.			

7.7.12. PortC (NID = 0Ch): ConfigDefault

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set	71Fh	71Eh	71Dh	71Ch
Get	F1F00h / F1E00h / F1D00h / F1C00h			

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Field Name	Bits	R/W	Default	Reset
PortConnectivity	31:30	RW	0h	POR
	Port connectivity: 0h = Port complex is connected to a jack 1h = No physical connection for port 2h = Fixed function device is attached 3h = Both jack and internal device attached (info in all other fields refers to integrated device, any presence detection refers to jack)			
Location	29:24	RW	01h	POR
	Location Bits [5..4]: 0h = External on primary chassis 1h = Internal 2h = Separate chassis 3h = Other Bits [3..0]: 0h = N/A 1h = Rear 2h = Front 3h = Left 4h = Right 5h = Top 6h = Bottom 7h-9h = Special Ah-Fh = Reserved			

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Field Name	Bits	R/W	Default	Reset
Device	23:20	RW	8h	POR
	Default device: 0h = Line out 1h = Speaker 2h = HP out 3h = CD 4h = SPDIF Out 5h = Digital other out 6h = Modem line side 7h = Modem handset side 8h = Line in 9h = Aux Ah = Mic in Bh = Telephony Ch = SPDIF In Dh = Digital other in Eh = Reserved Fh = Other			
ConnectionType	19:16	RW	1h	POR
	Connection type: 0h = Unknown 1h = 1/8" stereo/mono 2h = 1/4" stereo/mono 3h = ATAPI internal 4h = RCA 5h = Optical 6h = Other digital 7h = Other analog 8h = Multichannel analog (DIN) 9h = XLR/Professional Ah = RJ-11 (modem) Bh = Combination Ch-Eh = Reserved Fh = Other			

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Field Name	Bits	R/W	Default	Reset
Color	15:12	RW	3h	POR
	Color: 0h = Unknown 1h = Black 2h = Grey 3h = Blue 4h = Green 5h = Red 6h = Orange 7h = Yellow 8h = Purple 9h = Pink Ah-Dh = Reserved Eh = White Fh = Other			
Misc	11:8	RW	0h	POR
	Miscellaneous: Bits [3..1] = Reserved Bit 0 = Jack detect override			
Association	7:4	RW	4h	POR
	Default assocation.			
Sequence	3:0	RW	0h	POR
	Sequence.			

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7.8. PortD (NID = 0Dh): WCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0009h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:24	R	00h	N/A (Hard-coded)
	Reserved.			
Type	23:20	R	4h	N/A (Hard-coded)
	Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined			
Delay	19:16	R	0h	N/A (Hard-coded)
	Number of sample delays through widget.			
Rsvd1	15:12	R	0h	N/A (Hard-coded)
	Reserved.			
SwapCap	11	R	0h	N/A (Hard-coded)
	Left/right swap support: 1 = yes, 0 = no.			
PwrCntrl	10	R	1h	N/A (Hard-coded)
	Power state support: 1 = yes, 0 = no.			
Dig	9	R	0h	N/A (Hard-coded)
	Digital stream support: 1 = yes (digital), 0 = no (analog).			
ConnList	8	R	1h	N/A (Hard-coded)
	Connection list present: 1 = yes, 0 = no.			

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Field Name	Bits	R/W	Default	Reset
UnSolCap	7	R	1h	N/A (Hard-coded)
	Unsolicited response support: 1 = yes, 0 = no.			
ProcWidget	6	R	0h	N/A (Hard-coded)
	Processing state support: 1 = yes, 0 = no.			
Stripe	5	R	0h	N/A (Hard-coded)
	Striping support: 1 = yes, 0 = no.			
FormatOvrd	4	R	0h	N/A (Hard-coded)
	Stream format override: 1 = yes, 0 = no.			
AmpParOvrd	3	R	0h	N/A (Hard-coded)
	Amplifier capabilities override: 1 = yes, no.			
OutAmpPrsnt	2	R	0h	N/A (Hard-coded)
	Output amp present: 1 = yes, 0 = no.			
InAmpPrsnt	1	R	1h	N/A (Hard-coded)
	Input amp present: 1 = yes, 0 = no.			
Stereo	0	R	1h	N/A (Hard-coded)
	Stereo stream support: 1 = yes (stereo), 0 = no (mono).			

7.8.1. PortD (NID = 0Dh): PinCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Ch			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:17	R	0000h	N/A (Hard-coded)
	Reserved.			

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Field Name	Bits	R/W	Default	Reset
EapdCap	16	R	1h	N/A (Hard-coded)
	EAPD support: 1 = yes, 0 = no.			
VrefCntrl	15:8	R	00h	N/A (Hard-coded)
	Vref support: bit 7 = Reserved bit 6 = Reserved bit 5 = 100% support (1 = yes, 0 = no) bit 4 = 80% support (1 = yes, 0 = no) bit 3 = Reserved bit 2 = GND support (1 = yes, 0 = no) bit 1 = 50% support (1 = yes, 0 = no) bit 0 = Hi-Z support (1 = yes, 0 = no)			
Rsvd1	7	R	0h	N/A (Hard-coded)
	Reserved.			
BalancedIO	6	R	0h	N/A (Hard-coded)
	Balanced I/O support: 1 = yes, 0 = no.			
InCap	5	R	1h	N/A (Hard-coded)
	Input support: 1 = yes, 0 = no.			
OutCap	4	R	1h	N/A (Hard-coded)
	Output support: 1 = yes, 0 = no.			
HdphDrvCap	3	R	1h	N/A (Hard-coded)
	Headphone amp present: 1 = yes, 0 = no.			
PresDtctCap	2	R	1h	N/A (Hard-coded)
	Presence detection support: 1 = yes, 0 = no.			
TrigRqd	1	R	0h	N/A (Hard-coded)
	Trigger required for impedance sense: 1 = yes, 0 = no.			
ImpSenseCap	0	R	0h	N/A (Hard-coded)
	Impedance sense support: 1 = yes, 0 = no.			

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7.8.2. PortD (NID = 0Dh): ConLst

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Eh			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
LForm	7	R	0h	N/A (Hard-coded)
	Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries.			
ConL	6:0	R	04h	N/A (Hard-coded)
	Number of NID entries in connection list.			

7.8.3. PortD (NID = 0Dh): ConLstEntry0

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0200h			

Field Name	Bits	R/W	Default	Reset
ConL3	31:24	R	19h	N/A (Hard-coded)
	DAC4 Converter widget (0x19)			
ConL2	23:16	R	1Eh	N/A (Hard-coded)
	MixerOutVol Selector widget (0x1E)			
ConL1Range	14:8	R	1h	N/A (Hard-coded)
	1 = ConL0..ConL1 defines a range of selectable inputs.			

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Field Name	Bits	R/W	Default	Reset
ConL1	15:8	R	18h	N/A (Hard-coded)
	DAC3 Converter widget (0x18)			
ConL0	7:0	R	15h	N/A (Hard-coded)
	DAC0 Converter widget (0x15)			

7.8.4. PortD (NID = 0Dh): InAmpLeft

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				360h
Get	B2000h			

Field Name	Bits	R/W	Default	Reset
Rsvd1	31:2	R	00000000h	N/A (Hard-coded)
	Reserved.			
Gain	1:0	RW	0h	POR - DAFG - ULR
	Amp gain step number (see InAmpCap parameter pertaining to this widget).			

7.8.5. PortD (NID = 0Dh): InAmpRight

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				350h
Get	B0000h			

Field Name	Bits	R/W	Default	Reset
Rsvd1	31:2	R	00000000h	N/A (Hard-coded)
	Reserved.			

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Field Name	Bits	R/W	Default	Reset
Gain	1:0	RW	0h	POR - DAFG - ULR
	Amp gain step number (see InAmpCap parameter pertaining to this widget).			

7.8.6. PortD (NID = 0Dh): ConSelectCtrl

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				701h
Get	F0100h			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:2	R	00000000h	N/A (Hard-coded)
	Reserved.			
Index	1:0	RW	0h	POR - DAFG - ULR
	Connection select control index.			

7.8.7. PortD (NID = 0Dh): PwrState

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				705h
Get	F0500h			

Field Name	Bits	R/W	Default	Reset
Rsvd4	31:11	R	000000h	N/A (Hard-coded)
	Reserved.			
SettingsReset	10	R	1h	POR - DAFG - ULR
	Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget.			

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Field Name	Bits	R/W	Default	Reset
Rsvd3	9	R	0h	N/A (Hard-coded)
	Reserved.			
Error	8	R	0h	POR - DAFG - ULR
	Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state.			
Rsvd2	7:6	R	0h	N/A (Hard-coded)
	Reserved.			
Act	5:4	R	3h	POR - DAFG - LR
	Actual power state of this widget.			
Rsvd1	3:2	R	0h	N/A (Hard-coded)
	Reserved.			
Set	1:0	RW	0h	POR - DAFG - LR
	Current power state setting for this widget.			

7.8.8. PortD (NID = 0Dh): PinWCntrl

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				707h
Get	F0700h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
HPhnEn	7	RW	0h	POR - DAFG - ULR
	Headphone amp enable: 1 = enabled, 0 = disabled			
OutEn	6	RW	0h	POR - DAFG - ULR
	Output enable: 1 = enabled, 0 = disabled.			

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Field Name	Bits	R/W	Default	Reset
InEn	5	RW‘	0h	POR - DAFG - ULR
	Input enable: 1 = enabled, 0 = disabled			
Rsvd1	4:0	R	0h	N/A (Hard-coded)
	Reserved.			

7.8.9. PortD (NID = 0Dh): UnsolResp

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				708h
Get	F0800h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
En	7	RW	0h	POR - DAFG - ULR
	Unsolicited response enable (also enables Wake events for this Widget): 1 = enabled, 0 = disabled.			
Rsvd1	6	R	0h	N/A (Hard-coded)
	Reserved.			
Tag	5:0	RW	00h	POR - DAFG - ULR
	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.			

7.8.10. PortD (NID = 0Dh): ChSense

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				709h
Get	F0900h			

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Field Name	Bits	R/W	Default	Reset
PresDtct	31	R	0h	POR
	Presence detection indicator: 1 = presence detected; 0 = presence not detected.			
Rsvd	30:0	R	00000000h	N/A (Hard-coded)
	Reserved.			

7.8.11. PortD (NID = 0Dh): EAPDBTLLR

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				70Ch
Get	F0C00h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:2	R	00000000h	N/A (Hard-coded)
	Reserved.			
EAPD	1	RW	1h	POR - DAFG - ULR
	EAPD control: 1 = set EAPD pin to 1 (powered) up if this pin is powered up, 0 = set EAPD pin to 0.			
Rsvd1	0	R	0h	N/A (Hard-coded)
	Reserved.			

7.8.12. PortD (NID = 0Dh): ConfigDefault

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set	71Fh	71Eh	71Dh	71Ch
Get	F1F00h / F1E00h / F1D00h / F1C00h			

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Field Name	Bits	R/W	Default	Reset
PortConnectivity	31:30	RW	0h	POR
	Port connectivity: 0h = Port complex is connected to a jack 1h = No physical connection for port 2h = Fixed function device is attached 3h = Both jack and internal device attached (info in all other fields refers to integrated device, any presence detection refers to jack)			
Location	29:24	RW	01h	POR
	Location Bits [5..4]: 0h = External on primary chassis 1h = Internal 2h = Separate chassis 3h = Other Bits [3..0]: 0h = N/A 1h = Rear 2h = Front 3h = Left 4h = Right 5h = Top 6h = Bottom 7h-9h = Special Ah-Fh = Reserved			

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Field Name	Bits	R/W	Default	Reset
Device	23:20	RW	0h	POR
	Default device: 0h = Line out 1h = Speaker 2h = HP out 3h = CD 4h = SPDIF Out 5h = Digital other out 6h = Modem line side 7h = Modem handset side 8h = Line in 9h = Aux Ah = Mic in Bh = Telephony Ch = SPDIF In Dh = Digital other in Eh = Reserved Fh = Other			
ConnectionType	19:16	RW	1h	POR
	Connection type: 0h = Unknown 1h = 1/8" stereo/mono 2h = 1/4" stereo/mono 3h = ATAPI internal 4h = RCA 5h = Optical 6h = Other digital 7h = Other analog 8h = Multichannel analog (DIN) 9h = XLR/Professional Ah = RJ-11 (modem) Bh = Combination Ch-Eh = Reserved Fh = Other			

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Field Name	Bits	R/W	Default	Reset
Color	15:12	RW	4h	POR
	Color: 0h = Unknown 1h = Black 2h = Grey 3h = Blue 4h = Green 5h = Red 6h = Orange 7h = Yellow 8h = Purple 9h = Pink Ah-Dh = Reserved Eh = White Fh = Other			
Misc	11:8	RW	0h	POR
	Miscellaneous: Bits [3..1] = Reserved Bit 0 = Jack detect override			
Association	7:4	RW	3h	POR
	Default assocation.			
Sequence	3:0	RW	0h	POR
	Sequence.			

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7.9. PortE (NID = 0Eh): WCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0009h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:24	R	00h	N/A (Hard-coded)
	Reserved.			
Type	23:20	R	4h	N/A (Hard-coded)
	Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined			
Delay	19:16	R	0h	N/A (Hard-coded)
	Number of sample delays through widget.			
Rsvd1	15:12	R	0h	N/A (Hard-coded)
	Reserved.			
SwapCap	11	R	0h	N/A (Hard-coded)
	Left/right swap support: 1 = yes, 0 = no.			
PwrCntrl	10	R	1h	N/A (Hard-coded)
	Power state support: 1 = yes, 0 = no.			
Dig	9	R	0h	N/A (Hard-coded)
	Digital stream support: 1 = yes (digital), 0 = no (analog).			
ConnList	8	R	1h	N/A (Hard-coded)
	Connection list present: 1 = yes, 0 = no.			

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Field Name	Bits	R/W	Default	Reset
UnSolCap	7	R	1h	N/A (Hard-coded)
	Unsolicited response support: 1 = yes, 0 = no.			
ProcWidget	6	R	0h	N/A (Hard-coded)
	Processing state support: 1 = yes, 0 = no.			
Stripe	5	R	0h	N/A (Hard-coded)
	Striping support: 1 = yes, 0 = no.			
FormatOvrd	4	R	0h	N/A (Hard-coded)
	Stream format override: 1 = yes, 0 = no.			
AmpParOvrd	3	R	0h	N/A (Hard-coded)
	Amplifier capabilities override: 1 = yes, no.			
OutAmpPrsnt	2	R	0h	N/A (Hard-coded)
	Output amp present: 1 = yes, 0 = no.			
InAmpPrsnt	1	R	1h	N/A (Hard-coded)
	Input amp present: 1 = yes, 0 = no.			
Stereo	0	R	1h	N/A (Hard-coded)
	Stereo stream support: 1 = yes (stereo), 0 = no (mono).			

7.9.1. PortE (NID = 0Eh): PinCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Ch			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:17	R	0000h	N/A (Hard-coded)
	Reserved.			

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Field Name	Bits	R/W	Default	Reset
EapdCap	16	R	1h	N/A (Hard-coded)
	EAPD support: 1 = yes, 0 = no.			
VrefCntrl	15:8	R	17h	N/A (Hard-coded)
	Vref support: bit 7 = Reserved bit 6 = Reserved bit 5 = 100% support (1 = yes, 0 = no) bit 4 = 80% support (1 = yes, 0 = no) bit 3 = Reserved bit 2 = GND support (1 = yes, 0 = no) bit 1 = 50% support (1 = yes, 0 = no) bit 0 = Hi-Z support (1 = yes, 0 = no)			
Rsvd1	7	R	0h	N/A (Hard-coded)
	Reserved.			
BalancedIO	6	R	0h	N/A (Hard-coded)
	Balanced I/O support: 1 = yes, 0 = no.			
InCap	5	R	1h	N/A (Hard-coded)
	Input support: 1 = yes, 0 = no.			
OutCap	4	R	1h	N/A (Hard-coded)
	Output support: 1 = yes, 0 = no.			
HdphDrvCap	3	R	0h	N/A (Hard-coded)
	Headphone amp present: 1 = yes, 0 = no.			
PresDtctCap	2	R	1h	N/A (Hard-coded)
	Presence detection support: 1 = yes, 0 = no.			
TrigRqd	1	R	0h	N/A (Hard-coded)
	Trigger required for impedance sense: 1 = yes, 0 = no.			
ImpSenseCap	0	R	0h	N/A (Hard-coded)
	Impedance sense support: 1 = yes, 0 = no.			

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7.9.2. PortE (NID = 0Eh): ConLst

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Eh			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
LForm	7	R	0h	N/A (Hard-coded)
	Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries.			
ConL	6:0	R	04h	N/A (Hard-coded)
	Number of NID entries in connection list.			

7.9.3. PortE (NID = 0Eh): ConLstEntry0

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0200h			

Field Name	Bits	R/W	Default	Reset
ConL3	31:24	R	19h	N/A (Hard-coded)
	DAC4 Converter widget (0x19)			
ConL2	23:16	R	1Eh	N/A (Hard-coded)
	MixerOutVol Selector widget (0x1E)			
ConL1Range	14:8	R	1h	N/A (Hard-coded)
	1 = ConL0..ConL1 defines a range of selectable inputs.			

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Field Name	Bits	R/W	Default	Reset
ConL1	15:8	R	18h	N/A (Hard-coded)
	DAC3 Converter widget (0x18)			
ConL0	7:0	R	15h	N/A (Hard-coded)
	DAC0 Converter widget (0x15)			

7.9.4. PortE (NID = 0Eh): InAmpLeft

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				360h
Get	B2000h			

Field Name	Bits	R/W	Default	Reset
Rsvd1	31:2	R	00000000h	N/A (Hard-coded)
	Reserved.			
Gain	1:0	RW	0h	POR - DAFG - ULR
	Amp gain step number (see InAmpCap parameter pertaining to this widget).			

7.9.5. PortE (NID = 0Eh): InAmpRight

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				350h
Get	B0000h			

Field Name	Bits	R/W	Default	Reset
Rsvd1	31:2	R	00000000h	N/A (Hard-coded)
	Reserved.			
Gain	1:0	RW	0h	POR - DAFG - ULR
	Amp gain step number (see InAmpCap parameter pertaining to this widget).			

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7.9.6. PortE (NID = 0Eh): ConSelectCtrl

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				701h
Get	F0100h			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:2	R	00000000h	N/A (Hard-coded)
	Reserved.			
Index	1:0	RW	0h	POR - DAFG - ULR
	Connection select control index.			

7.9.7. PortE (NID = 0Eh): PwrState

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				705h
Get	F0500h			

Field Name	Bits	R/W	Default	Reset
Rsvd4	31:11	R	000000h	N/A (Hard-coded)
	Reserved.			
SettingsReset	10	R	1h	POR - DAFG - ULR
	Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget.			
Rsvd3	9	R	0h	N/A (Hard-coded)
	Reserved.			
Error	8	R	0h	POR - DAFG - ULR
	Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state.			

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Field Name	Bits	R/W	Default	Reset
Rsvd2	7:6	R	0h	N/A (Hard-coded)
	Reserved.			
Act	5:4	R	3h	POR - DAFG - LR
	Actual power state of this widget.			
Rsvd1	3:2	R	0h	N/A (Hard-coded)
	Reserved.			
Set	1:0	RW	0h	POR - DAFG - LR
	Current power state setting for this widget.			

7.9.8. PortE (NID = 0Eh): PinWCntrl

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				707h
Get	F0700h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:7	R	000000h	N/A (Hard-coded)
	Reserved.			
OutEn	6	RW	0h	POR - DAFG - ULR
	Output enable: 1 = enabled, 0 = disabled.			
InEn	5	RW	1h	POR - DAFG - ULR
	Input enable: 1 = enabled, 0 = disabled.			
Rsvd1	4:3	R	0h	N/A (Hard-coded)
	Reserved.			
VRefEn	2.0	RW	0h	POR - DAFG - ULR

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Field Name	Bits	R/W	Default	Reset
	Vref selection (See VrefCntrl field of PinCap parameter for supported selections): 000b= HI-Z 001b= 50% 010b= GND 011b= Reserved 100b= 80% 101b= 100% 110b= Reserved 111b= Reserved			

7.9.9. PortE (NID = 0Eh): UnsolResp

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				708h
Get	F0800h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
En	7	RW	0h	POR - DAFG - ULR
	Unsolicited response enable (also enables Wake events for this Widget): 1 = enabled, 0 = disabled.			
Rsvd1	6	R	0h	N/A (Hard-coded)
	Reserved.			
Tag	5:0	RW	00h	POR - DAFG - ULR
	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.			

7.9.10. PortE (NID = 0Eh): ChSense

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				709h
Get	F0900h			

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Field Name	Bits	R/W	Default	Reset
PresDtct	31	R	0h	POR
	Presence detection indicator: 1 = presence detected; 0 = presence not detected.			
Rsvd	30:0	R	00000000h	N/A (Hard-coded)
	Reserved.			

7.9.11. PortE (NID = 0Eh): EAPDBTLLR

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				70Ch
Get	F0C00h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:2	R	00000000h	N/A (Hard-coded)
	Reserved.			
EAPD	1	RW	1h	POR - DAFG - ULR
	EAPD control: 1 = set EAPD pin to 1 (powered) up if this pin is powered up, 0 = set EAPD pin to 0.			
Rsvd1	0	R	0h	N/A (Hard-coded)
	Reserved.			

7.9.12. PortE (NID = 0Eh): ConfigDefault

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set	71Fh	71Eh	71Dh	71Ch
Get	F1F00h / F1E00h / F1D00h / F1C00h			

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Field Name	Bits	R/W	Default	Reset
PortConnectivity	31:30	RW	0h	POR
	Port connectivity: 0h = Port complex is connected to a jack 1h = No physical connection for port 2h = Fixed function device is attached 3h = Both jack and internal device attached (info in all other fields refers to integrated device, any presence detection refers to jack)			
Location	29:24	RW	01h	POR
	Location Bits [5..4]: 0h = External on primary chassis 1h = Internal 2h = Separate chassis 3h = Other Bits [3..0]: 0h = N/A 1h = Rear 2h = Front 3h = Left 4h = Right 5h = Top 6h = Bottom 7h-9h = Special Ah-Fh = Reserved			

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Field Name	Bits	R/W	Default	Reset
Device	23:20	RW	Ah	POR
	Default device: 0h = Line out 1h = Speaker 2h = HP out 3h = CD 4h = SPDIF Out 5h = Digital other out 6h = Modem line side 7h = Modem handset side 8h = Line in 9h = Aux Ah = Mic in Bh = Telephony Ch = SPDIF In Dh = Digital other in Eh = Reserved Fh = Other			
ConnectionType	19:16	RW	1h	POR
	Connection type: 0h = Unknown 1h = 1/8" stereo/mono 2h = 1/4" stereo/mono 3h = ATAPI internal 4h = RCA 5h = Optical 6h = Other digital 7h = Other analog 8h = Multichannel analog (DIN) 9h = XLR/Professional Ah = RJ-11 (modem) Bh = Combination Ch-Eh = Reserved Fh = Other			

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Field Name	Bits	R/W	Default	Reset
Color	15:12	RW	9h	POR
	Color: 0h = Unknown 1h = Black 2h = Grey 3h = Blue 4h = Green 5h = Red 6h = Orange 7h = Yellow 8h = Purple 9h = Pink Ah-Dh = Reserved Eh = White Fh = Other			
Misc	11:8	RW	0h	POR
	Miscellaneous: Bits [3..1] = Reserved Bit 0 = Jack detect override			
Association	7:4	RW	4h	POR
	Default assocation.			
Sequence	3:0	RW	Eh	POR
	Sequence.			

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7.10. PortF (NID = 0Fh): WCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0009h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:24	R	00h	N/A (Hard-coded)
	Reserved.			
Type	23:20	R	4h	N/A (Hard-coded)
	Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined			
Delay	19:16	R	0h	N/A (Hard-coded)
	Number of sample delays through widget.			
Rsvd1	15:12	R	0h	N/A (Hard-coded)
	Reserved.			
SwapCap	11	R	0h	N/A (Hard-coded)
	Left/right swap support: 1 = yes, 0 = no.			
PwrCntrl	10	R	1h	N/A (Hard-coded)
	Power state support: 1 = yes, 0 = no.			
Dig	9	R	0h	N/A (Hard-coded)
	Digital stream support: 1 = yes (digital), 0 = no (analog).			
ConnList	8	R	1h	N/A (Hard-coded)
	Connection list present: 1 = yes, 0 = no.			

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Field Name	Bits	R/W	Default	Reset
UnSolCap	7	R	1h	N/A (Hard-coded)
	Unsolicited response support: 1 = yes, 0 = no.			
ProcWidget	6	R	0h	N/A (Hard-coded)
	Processing state support: 1 = yes, 0 = no.			
Stripe	5	R	0h	N/A (Hard-coded)
	Striping support: 1 = yes, 0 = no.			
FormatOvrd	4	R	0h	N/A (Hard-coded)
	Stream format override: 1 = yes, 0 = no.			
AmpParOvrd	3	R	0h	N/A (Hard-coded)
	Amplifier capabilities override: 1 = yes, no.			
OutAmpPrsnt	2	R	0h	N/A (Hard-coded)
	Output amp present: 1 = yes, 0 = no.			
InAmpPrsnt	1	R	1h	N/A (Hard-coded)
	Input amp present: 1 = yes, 0 = no.			
Stereo	0	R	1h	N/A (Hard-coded)
	Stereo stream support: 1 = yes (stereo), 0 = no (mono).			

7.10.1. PortF (NID = 0Fh): PinCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Ch			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:17	R	0000h	N/A (Hard-coded)
	Reserved.			

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Field Name	Bits	R/W	Default	Reset
EapdCap	16	R	1h	N/A (Hard-coded)
	EAPD support: 1 = yes, 0 = no.			
VrefCntrl	15:8	R	00h	N/A (Hard-coded)
	Vref support: bit 7 = Reserved bit 6 = Reserved bit 5 = 100% support (1 = yes, 0 = no) bit 4 = 80% support (1 = yes, 0 = no) bit 3 = Reserved bit 2 = GND support (1 = yes, 0 = no) bit 1 = 50% support (1 = yes, 0 = no) bit 0 = Hi-Z support (1 = yes, 0 = no)			
Rsvd1	7	R	0h	N/A (Hard-coded)
	Reserved.			
BalancedIO	6	R	0h	N/A (Hard-coded)
	Balanced I/O support: 1 = yes, 0 = no.			
InCap	5	R	1h	N/A (Hard-coded)
	Input support: 1 = yes, 0 = no.			
OutCap	4	R	1h	N/A (Hard-coded)
	Output support: 1 = yes, 0 = no.			
HdphDrvCap	3	R	0h	N/A (Hard-coded)
	Headphone amp present: 1 = yes, 0 = no.			
PresDtctCap	2	R	1h	N/A (Hard-coded)
	Presence detection support: 1 = yes, 0 = no.			
TrigRqd	1	R	0h	N/A (Hard-coded)
	Trigger required for impedance sense: 1 = yes, 0 = no.			
ImpSenseCap	0	R	0h	N/A (Hard-coded)
	Impedance sense support: 1 = yes, 0 = no.			

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7.10.2. PortF (NID = 0Fh): ConLst

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Eh			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
LForm	7	R	0h	N/A (Hard-coded)
	Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries.			
ConL	6:0	R	04h	N/A (Hard-coded)
	Number of NID entries in connection list.			

7.10.3. PortF (NID = 0Fh): ConLstEntry0

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0200h			

Field Name	Bits	R/W	Default	Reset
ConL3	31:24	R	19h	N/A (Hard-coded)
	DAC4 Converter widget (0x19)			
ConL2	23:16	R	1Eh	N/A (Hard-coded)
	MixerOutVol Selector widget (0x1E)			
ConL1Range	14:8	R	1h	N/A (Hard-coded)
	1 = ConL0..ConL1 defines a range of selectable inputs.			

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Field Name	Bits	R/W	Default	Reset
ConL1	15:8	R	18h	N/A (Hard-coded)
	DAC3 Converter widget (0x18)			
ConL0	7:0	R	15h	N/A (Hard-coded)
	DAC0 Converter widget (0x15)			

7.10.4. PortF (NID = 0Fh): InAmpLeft

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				360h
Get	B2000h			

Field Name	Bits	R/W	Default	Reset
Rsvd1	31:2	R	00000000h	N/A (Hard-coded)
	Reserved.			
Gain	1:0	RW	0h	POR - DAFG - ULR
	Amp gain step number (see InAmpCap parameter pertaining to this widget).			

7.10.5. PortF (NID = 0Fh): InAmpRight

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				350h
Get	B0000h			

Field Name	Bits	R/W	Default	Reset
Rsvd1	31:2	R	00000000h	N/A (Hard-coded)
	Reserved.			
Gain	1:0	RW	0h	POR - DAFG - ULR
	Amp gain step number (see InAmpCap parameter pertaining to this widget).			

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7.10.6. PortF (NID = 0Fh): ConSelectCtrl

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				701h
Get	F0100h			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:2	R	00000000h	N/A (Hard-coded)
	Reserved.			
Index	1:0	RW	0h	POR - DAFG - ULR
	Connection select control index.			

7.10.7. PortF (NID = 0Fh): PwrState

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				705h
Get	F0500h			

Field Name	Bits	R/W	Default	Reset
Rsvd4	31:11	R	000000h	N/A (Hard-coded)
	Reserved.			
SettingsReset	10	R	1h	POR - DAFG - ULR
	Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget.			
Rsvd3	9	R	0h	N/A (Hard-coded)
	Reserved.			
Error	8	R	0h	POR - DAFG - ULR
	Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state.			

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Field Name	Bits	R/W	Default	Reset
Rsvd2	7:6	R	0h	N/A (Hard-coded)
	Reserved.			
Act	5:4	R	3h	POR - DAFG - LR
	Actual power state of this widget.			
Rsvd1	3:2	R	0h	N/A (Hard-coded)
	Reserved.			
Set	1:0	RW	0h	POR - DAFG - LR
	Current power state setting for this widget.			

7.10.8. PortF (NID = 0Fh): PinWCntrl

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				707h
Get	F0700h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:7	R	000000h	N/A (Hard-coded)
	Reserved.			
OutEn	6	RW	0h	POR - DAFG - ULR
	Output enable: 1 = enabled, 0 = disabled.			
InEn	5	RW	0h	POR - DAFG - ULR
	Input enable: 1 = enabled, 0 = disabled.			
Rsvd1	4:0	R	0h	N/A (Hard-coded)
	Reserved.			

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7.10.9. PortF (NID = 0Fh): UnsolResp

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				708h
Get	F0800h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
En	7	RW	0h	POR - DAFG - ULR
	Unsolicited response enable (also enables Wake events for this Widget): 1 = enabled, 0 = disabled.			
Rsvd1	6	R	0h	N/A (Hard-coded)
	Reserved.			
Tag	5:0	RW	00h	POR - DAFG - ULR
	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.			

7.10.10. PortF (NID = 0Fh): ChSense

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				709h
Get	F0900h			

Field Name	Bits	R/W	Default	Reset
PresDtct	31	R	0h	POR
	Presence detection indicator: 1 = presence detected; 0 = presence not detected.			
Rsvd	30:0	R	00000000h	N/A (Hard-coded)
	Reserved.			

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7.10.11. PortF (NID = 0Fh): EAPDBTLLR

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				70Ch
Get	F0C00h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:2	R	00000000h	N/A (Hard-coded)
	Reserved.			
EAPD	1	RW	1h	POR - DAFG - ULR
	EAPD control: 1 = set EAPD pin to 1 (powered) up if this pin is powered up, 0 = set EAPD pin to 0.			
Rsvd1	0	R	0h	N/A (Hard-coded)
	Reserved.			

7.10.12. PortF (NID = 0Fh): ConfigDefault

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set	71Fh	71Eh	71Dh	71Ch
Get	F1F00h / F1E00h / F1D00h / F1C00h			

Field Name	Bits	R/W	Default	Reset
PortConnectivity	31:30	RW	0h	POR
	Port connectivity: 0h = Port complex is connected to a jack 1h = No physical connection for port 2h = Fixed function device is attached 3h = Both jack and internal device attached (info in all other fields refers to integrated device, any presence detection refers to jack)			

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Field Name	Bits	R/W	Default	Reset
Location	29:24	RW	01h	POR
	Location Bits [5..4]: 0h = External on primary chassis 1h = Internal 2h = Separate chassis 3h = Other Bits [3..0]: 0h = N/A 1h = Rear 2h = Front 3h = Left 4h = Right 5h = Top 6h = Bottom 7h-9h = Special Ah-Fh = Reserved			
Device	23:20	RW	0h	POR
	Default device: 0h = Line out 1h = Speaker 2h = HP out 3h = CD 4h = SPDIF Out 5h = Digital other out 6h = Modem line side 7h = Modem handset side 8h = Line in 9h = Aux Ah = Mic in Bh = Telephony Ch = SPDIF In Dh = Digital other in Eh = Reserved Fh = Other			

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Field Name	Bits	R/W	Default	Reset
ConnectionType	19:16	RW	1h	POR
	Connection type: 0h = Unknown 1h = 1/8" stereo/mono 2h = 1/4" stereo/mono 3h = ATAPI internal 4h = RCA 5h = Optical 6h = Other digital 7h = Other analog 8h = Multichannel analog (DIN) 9h = XLR/Professional Ah = RJ-11 (modem) Bh = Combination Ch-Eh = Reserved Fh = Other			
Color	15:12	RW	1h	POR
	Color: 0h = Unknown 1h = Black 2h = Grey 3h = Blue 4h = Green 5h = Red 6h = Orange 7h = Yellow 8h = Purple 9h = Pink Ah-Dh = Reserved Eh = White Fh = Other			
Misc	11:8	RW	0h	POR
	Miscellaneous: Bits [3..1] = Reserved Bit 0 = Jack detect override			
Association	7:4	RW	3h	POR
	Default assocation.			
Sequence	3:0	RW	2h	POR
	Sequence.			

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7.11. PortG (NID = 10h): WCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0009h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:24	R	00h	N/A (Hard-coded)
	Reserved.			
Type	23:20	R	4h	N/A (Hard-coded)
	Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined			
Delay	19:16	R	0h	N/A (Hard-coded)
	Number of sample delays through widget.			
Rsvd1	15:12	R	0h	N/A (Hard-coded)
	Reserved.			
SwapCap	11	R	0h	N/A (Hard-coded)
	Left/right swap support: 1 = yes, 0 = no.			
PwrCntrl	10	R	1h	N/A (Hard-coded)
	Power state support: 1 = yes, 0 = no.			
Dig	9	R	0h	N/A (Hard-coded)
	Digital stream support: 1 = yes (digital), 0 = no (analog).			
ConnList	8	R	1h	N/A (Hard-coded)
	Connection list present: 1 = yes, 0 = no.			

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Field Name	Bits	R/W	Default	Reset
UnSolCap	7	R	1h	N/A (Hard-coded)
	Unsolicited response support: 1 = yes, 0 = no.			
ProcWidget	6	R	0h	N/A (Hard-coded)
	Processing state support: 1 = yes, 0 = no.			
Stripe	5	R	0h	N/A (Hard-coded)
	Striping support: 1 = yes, 0 = no.			
FormatOvrd	4	R	0h	N/A (Hard-coded)
	Stream format override: 1 = yes, 0 = no.			
AmpParOvrd	3	R	0h	N/A (Hard-coded)
	Amplifier capabilities override: 1 = yes, no.			
OutAmpPrsnt	2	R	0h	N/A (Hard-coded)
	Output amp present: 1 = yes, 0 = no.			
InAmpPrsnt	1	R	1h	N/A (Hard-coded)
	Input amp present: 1 = yes, 0 = no.			
Stereo	0	R	1h	N/A (Hard-coded)
	Stereo stream support: 1 = yes (stereo), 0 = no (mono).			

7.11.1. PortG (NID = 10h): PinCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Ch			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:17	R	0000h	N/A (Hard-coded)
	Reserved.			

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Field Name	Bits	R/W	Default	Reset
EapdCap	16	R	1h	N/A (Hard-coded)
	EAPD support: 1 = yes, 0 = no.			
VrefCntrl	15:8	R	00h	N/A (Hard-coded)
	Vref support: bit 7 = Reserved bit 6 = Reserved bit 5 = 100% support (1 = yes, 0 = no) bit 4 = 80% support (1 = yes, 0 = no) bit 3 = Reserved bit 2 = GND support (1 = yes, 0 = no) bit 1 = 50% support (1 = yes, 0 = no) bit 0 = Hi-Z support (1 = yes, 0 = no)			
Rsvd1	7	R	0h	N/A (Hard-coded)
	Reserved.			
BalancedIO	6	R	0h	N/A (Hard-coded)
	Balanced I/O support: 1 = yes, 0 = no.			
InCap	5	R	1h	N/A (Hard-coded)
	Input support: 1 = yes, 0 = no.			
OutCap	4	R	1h	N/A (Hard-coded)
	Output support: 1 = yes, 0 = no.			
HdphDrvCap	3	R	0h	N/A (Hard-coded)
	Headphone amp present: 1 = yes, 0 = no.			
PresDtctCap	2	R	1h	N/A (Hard-coded)
	Presence detection support: 1 = yes, 0 = no.			
TrigRqd	1	R	0h	N/A (Hard-coded)
	Trigger required for impedance sense: 1 = yes, 0 = no.			
ImpSenseCap	0	R	0h	N/A (Hard-coded)
	Impedance sense support: 1 = yes, 0 = no.			

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7.11.2. PortG (NID = 10h): ConLst

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Eh			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
LForm	7	R	0h	N/A (Hard-coded)
	Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries.			
ConL	6:0	R	04h	N/A (Hard-coded)
	Number of NID entries in connection list.			

7.11.3. PortG (NID = 10h): ConLstEntry0

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0200h			

Field Name	Bits	R/W	Default	Reset
ConL3	31:24	R	19h	N/A (Hard-coded)
	DAC4 Converter widget (0x19)			
ConL2	23:16	R	1Eh	N/A (Hard-coded)
	MixerOutVol Selector widget (0x1E)			
ConL1Range	14:8	R	1h	N/A (Hard-coded)
	1 = ConL0..ConL1 defines a range of selectable inputs.			

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Field Name	Bits	R/W	Default	Reset
ConL1	15:8	R	18h	N/A (Hard-coded)
	DAC3 Converter widget (0x18)			
ConL0	7:0	R	15h	N/A (Hard-coded)
	DAC0 Converter widget (0x15)			

7.11.4. PortG (NID = 10h): InAmpLeft

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				360h
Get	B2000h			

Field Name	Bits	R/W	Default	Reset
Rsvd1	31:2	R	00000000h	N/A (Hard-coded)
	Reserved.			
Gain	1:0	RW	0h	POR - DAFG - ULR
	Amp gain step number (see InAmpCap parameter pertaining to this widget).			

7.11.5. PortG (NID = 10h): InAmpRight

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				350h
Get	B0000h			

Field Name	Bits	R/W	Default	Reset
Rsvd1	31:2	R	00000000h	N/A (Hard-coded)
	Reserved.			
Gain	1:0	RW	0h	POR - DAFG - ULR
	Amp gain step number (see InAmpCap parameter pertaining to this widget).			

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7.11.6. PortG (NID = 10h): ConSelectCtrl

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				701h
Get	F0100h			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:2	R	00000000h	N/A (Hard-coded)
	Reserved.			
Index	1:0	RW	0h	POR - DAFG - ULR
	Connection select control index.			

7.11.7. PortG (NID = 10h): PwrState

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				705h
Get	F0500h			

Field Name	Bits	R/W	Default	Reset
Rsvd4	31:11	R	000000h	N/A (Hard-coded)
	Reserved.			
SettingsReset	10	R	1h	POR - DAFG - ULR
	Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget.			
Rsvd3	9	R	0h	N/A (Hard-coded)
	Reserved.			
Error	8	R	0h	POR - DAFG - ULR
	Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state.			

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Field Name	Bits	R/W	Default	Reset
Rsvd2	7:6	R	0h	N/A (Hard-coded)
	Reserved.			
Act	5:4	R	3h	POR - DAFG - LR
	Actual power state of this widget.			
Rsvd1	3:2	R	0h	N/A (Hard-coded)
	Reserved.			
Set	1:0	RW	0h	POR - DAFG - LR
	Current power state setting for this widget.			

7.11.8. PortG (NID = 10h): PinWCntrl

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				707h
Get	F0700h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:7	R	000000h	N/A (Hard-coded)
	Reserved.			
OutEn	6	RW	0h	POR - DAFG - ULR
	Output enable: 1 = enabled, 0 = disabled.			
InEn	5	RW	1h	POR - DAFG - ULR
	Input enable: 1 = enabled, 0 = disabled.			
Rsvd1	4:0	R	00h	N/A (Hard-coded)
	Reserved.			

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7.11.9. PortG (NID = 10h): UnsolResp

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				708h
Get	F0800h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
En	7	RW	0h	POR - DAFG - ULR
	Unsolicited response enable (also enables Wake events for this Widget): 1 = enabled, 0 = disabled.			
Rsvd1	6	R	0h	N/A (Hard-coded)
	Reserved.			
Tag	5:0	RW	00h	POR - DAFG - ULR
	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.			

7.11.10. PortG (NID = 10h): ChSense

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				709h
Get	F0900h			

Field Name	Bits	R/W	Default	Reset
PresDtct	31	R	0h	POR
	Presence detection indicator: 1 = presence detected; 0 = presence not detected.			
Rsvd	30:0	R	00000000h	N/A (Hard-coded)
	Reserved.			

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7.11.11. PortG (NID = 10h): EAPDBTLLR

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				70Ch
Get	F0C00h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:2	R	00000000h	N/A (Hard-coded)
	Reserved.			
EAPD	1	RW	1h	POR - DAFG - ULR
	EAPD control: 1 = set EAPD pin to 1 (powered) up if this pin is powered up, 0 = set EAPD pin to 0.			
Rsvd1	0	R	0h	N/A (Hard-coded)
	Reserved.			

7.11.12. PortG (NID = 10h): ConfigDefault

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set	71Fh	71Eh	71Dh	71Ch
Get	F1F00h / F1E00h / F1D00h / F1C00h			

Field Name	Bits	R/W	Default	Reset
PortConnectivity	31:30	RW	0h	POR
	Port connectivity: 0h = Port complex is connected to a jack 1h = No physical connection for port 2h = Fixed function device is attached 3h = Both jack and internal device attached (info in all other fields refers to integrated device, any presence detection refers to jack)			

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Field Name	Bits	R/W	Default	Reset
Location	29:24	RW	01h	POR
	Location Bits [5..4]: 0h = External on primary chassis 1h = Internal 2h = Separate chassis 3h = Other Bits [3..0]: 0h = N/A 1h = Rear 2h = Front 3h = Left 4h = Right 5h = Top 6h = Bottom 7h-9h = Special Ah-Fh = Reserved			
Device	23:20	RW	0h	POR
	Default device: 0h = Line out 1h = Speaker 2h = HP out 3h = CD 4h = SPDIF Out 5h = Digital other out 6h = Modem line side 7h = Modem handset side 8h = Line in 9h = Aux Ah = Mic in Bh = Telephony Ch = SPDIF In Dh = Digital other in Eh = Reserved Fh = Other			

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Field Name	Bits	R/W	Default	Reset
ConnectionType	19:16	RW	1h	POR
	Connection type: 0h = Unknown 1h = 1/8" stereo/mono 2h = 1/4" stereo/mono 3h = ATAPI internal 4h = RCA 5h = Optical 6h = Other digital 7h = Other analog 8h = Multichannel analog (DIN) 9h = XLR/Professional Ah = RJ-11 (modem) Bh = Combination Ch-Eh = Reserved Fh = Other			
Color	15:12	RW	6h	POR
	Color: 0h = Unknown 1h = Black 2h = Grey 3h = Blue 4h = Green 5h = Red 6h = Orange 7h = Yellow 8h = Purple 9h = Pink Ah-Dh = Reserved Eh = White Fh = Other			
Misc	11:8	RW	0h	POR
	Miscellaneous: Bits [3..1] = Reserved Bit 0 = Jack detect override			
Association	7:4	RW	3h	POR
	Default assocation.			
Sequence	3:0	RW	1h	POR
	Sequence.			

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7.18. PortH (NID = 11h): WCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0009h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:24	R	00h	N/A (Hard-coded)
	Reserved.			
Type	23:20	R	4h	N/A (Hard-coded)
	Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined			
Delay	19:16	R	0h	N/A (Hard-coded)
	Number of sample delays through widget.			
Rsvd1	15:12	R	0h	N/A (Hard-coded)
	Reserved.			
SwapCap	11	R	0h	N/A (Hard-coded)
	Left/right swap support: 1 = yes, 0 = no.			
PwrCntrl	10	R	1h	N/A (Hard-coded)
	Power state support: 1 = yes, 0 = no.			
Dig	9	R	0h	N/A (Hard-coded)
	Digital stream support: 1 = yes (digital), 0 = no (analog).			
ConnList	8	R	1h	N/A (Hard-coded)
	Connection list present: 1 = yes, 0 = no.			

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Field Name	Bits	R/W	Default	Reset
UnSolCap	7	R	1h	N/A (Hard-coded)
	Unsolicited response support: 1 = yes, 0 = no.			
ProcWidget	6	R	0h	N/A (Hard-coded)
	Processing state support: 1 = yes, 0 = no.			
Stripe	5	R	0h	N/A (Hard-coded)
	Striping support: 1 = yes, 0 = no.			
FormatOvrd	4	R	0h	N/A (Hard-coded)
	Stream format override: 1 = yes, 0 = no.			
AmpParOvrd	3	R	0h	N/A (Hard-coded)
	Amplifier capabilities override: 1 = yes, no.			
OutAmpPrsnt	2	R	0h	N/A (Hard-coded)
	Output amp present: 1 = yes, 0 = no.			
InAmpPrsnt	1	R	1h	N/A (Hard-coded)
	Input amp present: 1 = yes, 0 = no.			
Stereo	0	R	1h	N/A (Hard-coded)
	Stereo stream support: 1 = yes (stereo), 0 = no (mono).			

7.18.1. PortH (NID = 11h): PinCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Ch			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:17	R	0000h	N/A (Hard-coded)
	Reserved.			

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Field Name	Bits	R/W	Default	Reset
EapdCap	16	R	1h	N/A (Hard-coded)
	EAPD support: 1 = yes, 0 = no.			
VrefCntrl	15:8	R	00h	N/A (Hard-coded)
	Vref support: bit 7 = Reserved bit 6 = Reserved bit 5 = 100% support (1 = yes, 0 = no) bit 4 = 80% support (1 = yes, 0 = no) bit 3 = Reserved bit 2 = GND support (1 = yes, 0 = no) bit 1 = 50% support (1 = yes, 0 = no) bit 0 = Hi-Z support (1 = yes, 0 = no)			
Rsvd1	7	R	0h	N/A (Hard-coded)
	Reserved.			
BalancedIO	6	R	0h	N/A (Hard-coded)
	Balanced I/O support: 1 = yes, 0 = no.			
InCap	5	R	1h	N/A (Hard-coded)
	Input support: 1 = yes, 0 = no.			
OutCap	4	R	1h	N/A (Hard-coded)
	Output support: 1 = yes, 0 = no.			
HdphDrvCap	3	R	0h	N/A (Hard-coded)
	Headphone amp present: 1 = yes, 0 = no.			
PresDtctCap	2	R	1h	N/A (Hard-coded)
	Presence detection support: 1 = yes, 0 = no.			
TrigRqd	1	R	0h	N/A (Hard-coded)
	Trigger required for impedance sense: 1 = yes, 0 = no.			
ImpSenseCap	0	R	0h	N/A (Hard-coded)
	Impedance sense support: 1 = yes, 0 = no.			

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7.18.2. PortH (NID = 11h): ConLst

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Eh			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
LForm	7	R	0h	N/A (Hard-coded)
	Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries.			
ConL	6:0	R	04h	N/A (Hard-coded)
	Number of NID entries in connection list.			

7.18.3. PortH (NID = 11h): ConLstEntry0

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0200h			

Field Name	Bits	R/W	Default	Reset
ConL3	31:24	R	19h	N/A (Hard-coded)
	DAC4 Converter widget (0x19)			
ConL2	23:16	R	1Eh	N/A (Hard-coded)
	MixerOutVol Selector widget (0x1E)			
ConL1Range	14:8	R	1h	N/A (Hard-coded)
	1 = ConL0..ConL1 defines a range of selectable inputs.			

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Field Name	Bits	R/W	Default	Reset
ConL1	15:8	R	18h	N/A (Hard-coded)
	DAC3 Converter widget (0x18)			
ConL0	7:0	R	15h	N/A (Hard-coded)
	DAC0 Converter widget (0x15)			

7.18.4. PortH (NID = 11h): InAmpLeft

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				360h
Get	B2000h			

Field Name	Bits	R/W	Default	Reset
Rsvd1	31:2	R	00000000h	N/A (Hard-coded)
	Reserved.			
Gain	1:0	RW	0h	POR - DAFG - ULR
	Amp gain step number (see InAmpCap parameter pertaining to this widget).			

7.18.5. PortH (NID = 11h): InAmpRight

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				350h
Get	B0000h			

Field Name	Bits	R/W	Default	Reset
Rsvd1	31:2	R	00000000h	N/A (Hard-coded)
	Reserved.			
Gain	1:0	RW	0h	POR - DAFG - ULR
	Amp gain step number (see InAmpCap parameter pertaining to this widget).			

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7.18.6. PortH (NID = 11h): ConSelectCtrl

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				701h
Get	F0100h			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:2	R	00000000h	N/A (Hard-coded)
	Reserved.			
Index	1:0	RW	0h	POR - DAFG - ULR
	Connection select control index.			

7.18.7. PortH (NID = 11h): PwrState

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				705h
Get	F0500h			

Field Name	Bits	R/W	Default	Reset
Rsvd4	31:11	R	000000h	N/A (Hard-coded)
	Reserved.			
SettingsReset	10	R	1h	POR - DAFG - ULR
	Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget.			
Rsvd3	9	R	0h	N/A (Hard-coded)
	Reserved.			
Error	8	R	0h	POR - DAFG - ULR
	Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state.			

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Field Name	Bits	R/W	Default	Reset
Rsvd2	7:6	R	0h	N/A (Hard-coded)
	Reserved.			
Act	5:4	R	3h	POR - DAFG - LR
	Actual power state of this widget.			
Rsvd1	3:2	R	0h	N/A (Hard-coded)
	Reserved.			
Set	1:0	RW	0h	POR - DAFG - LR
	Current power state setting for this widget.			

7.18.8. PortH (NID = 11h): PinWCntrl

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				707h
Get	F0700h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:7	R	000000h	N/A (Hard-coded)
	Reserved.			
OutEn	6	RW	0h	POR - DAFG - ULR
	Output enable: 1 = enabled, 0 = disabled.			
InEn	5	RW	1h	POR - DAFG - ULR
	Input enable: 1 = enabled, 0 = disabled.			
Rsvd1	4:0	R	00h	N/A (Hard-coded)
	Reserved.			

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7.18.9. PortH (NID = 11h): UnsolResp

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				708h
Get	F0800h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
En	7	RW	0h	POR - DAFG - ULR
	Unsolicited response enable (also enables Wake events for this Widget): 1 = enabled, 0 = disabled.			
Rsvd1	6	R	0h	N/A (Hard-coded)
	Reserved.			
Tag	5:0	RW	00h	POR - DAFG - ULR
	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.			

7.18.10. PortH (NID = 11h): ChSense

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				709h
Get	F0900h			

Field Name	Bits	R/W	Default	Reset
PresDtct	31	R	0h	POR
	Presence detection indicator: 1 = presence detected; 0 = presence not detected.			
Rsvd	30:0	R	00000000h	N/A (Hard-coded)
	Reserved.			

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7.18.11. PortH (NID = 11h): EAPDBTLLR

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				70Ch
Get	F0C00h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:2	R	00000000h	N/A (Hard-coded)
	Reserved.			
EAPD	1	RW	1h	POR - DAFG - ULR
	EAPD control: 1 = set EAPD pin to 1 (powered) up if this pin is powered up, 0 = set EAPD pin to 0.			
Rsvd1	0	R	0h	N/A (Hard-coded)
	Reserved.			

7.18.12. PortH (NID = 11h): ConfigDefault

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set	71Fh	71Eh	71Dh	71Ch
Get	F1F00h / F1E00h / F1D00h / F1C00h			

Field Name	Bits	R/W	Default	Reset
PortConnectivity	31:30	RW	0h	POR
	Port connectivity: 0h = Port complex is connected to a jack 1h = No physical connection for port 2h = Fixed function device is attached 3h = Both jack and internal device attached (info in all other fields refers to integrated device, any presence detection refers to jack)			

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Field Name	Bits	R/W	Default	Reset
Location	29:24	RW	01h	POR
	Location Bits [5..4]: 0h = External on primary chassis 1h = Internal 2h = Separate chassis 3h = Other Bits [3..0]: 0h = N/A 1h = Rear 2h = Front 3h = Left 4h = Right 5h = Top 6h = Bottom 7h-9h = Special Ah-Fh = Reserved			
Device	23:20	RW	0h	POR
	Default device: 0h = Line out 1h = Speaker 2h = HP out 3h = CD 4h = SPDIF Out 5h = Digital other out 6h = Modem line side 7h = Modem handset side 8h = Line in 9h = Aux Ah = Mic in Bh = Telephony Ch = SPDIF In Dh = Digital other in Eh = Reserved Fh = Other			

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Field Name	Bits	R/W	Default	Reset
ConnectionType	19:16	RW	1h	POR
	Connection type: 0h = Unknown 1h = 1/8" stereo/mono 2h = 1/4" stereo/mono 3h = ATAPI internal 4h = RCA 5h = Optical 6h = Other digital 7h = Other analog 8h = Multichannel analog (DIN) 9h = XLR/Professional Ah = RJ-11 (modem) Bh = Combination Ch-Eh = Reserved Fh = Other			
Color	15:12	RW	2h	POR
	Color: 0h = Unknown 1h = Black 2h = Grey 3h = Blue 4h = Green 5h = Red 6h = Orange 7h = Yellow 8h = Purple 9h = Pink Ah-Dh = Reserved Eh = White Fh = Other			
Misc	11:8	RW	0h	POR
	Miscellaneous: Bits [3..1] = Reserved Bit 0 = Jack detect override			
Association	7:4	RW	3h	POR
	Default assocation.			
Sequence	3:0	RW	4h	POR
	Sequence.			

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7.19. CD (NID = 12h): WCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0009h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:24	R	00h	N/A (Hard-coded)
	Reserved.			
Type	23:20	R	4h	N/A (Hard-coded)
	Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined			
Delay	19:16	R	0h	N/A (Hard-coded)
	Number of sample delays through widget.			
Rsvd1	15:12	R	0h	N/A (Hard-coded)
	Reserved.			
SwapCap	11	R	0h	N/A (Hard-coded)
	Left/right swap support: 1 = yes, 0 = no.			
PwrCntrl	10	R	1h	N/A (Hard-coded)
	Power state support: 1 = yes, 0 = no.			
DigitalStrm	9	R	0h	N/A (Hard-coded)
	Digital stream support: 1 = yes (digital), 0 = no (analog).			
ConnList	8	R	0h	N/A (Hard-coded)
	Connection list present: 1 = yes, 0 = no.			

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Field Name	Bits	R/W	Default	Reset
UnsolCap	7	R	1h	N/A (Hard-coded)
	Unsolicited response support: 1 = yes, 0 = no.			
ProcWidget	6	R	0h	N/A (Hard-coded)
	Processing state support: 1 = yes, 0 = no.			
Stripe	5	R	0h	N/A (Hard-coded)
	Striping support: 1 = yes, 0 = no.			
FormatOvrd	4	R	0h	N/A (Hard-coded)
	Stream format override: 1 = yes, 0 = no.			
AmpParOvrd	3	R	0h	N/A (Hard-coded)
	Amplifier capabilities override: 1 = yes, no.			
OutAmpPrsnt	2	R	0h	N/A (Hard-coded)
	Output amp present: 1 = yes, 0 = no.			
InAmpPrsnt	1	R	0h	N/A (Hard-coded)
	Input amp present: 1 = yes, 0 = no.			
Stereo	0	R	1h	N/A (Hard-coded)
	Stereo stream support: 1 = yes (stereo), 0 = no (mono).			

7.19.1. CD (NID = 12h): PinCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Ch			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:17	R	0000h	N/A (Hard-coded)
	Reserved.			

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Field Name	Bits	R/W	Default	Reset
EapdCap	16	R	0h	N/A (Hard-coded)
	EAPD support: 1 = yes, 0 = no.			
VRefCntrl	15:8	R	00h	N/A (Hard-coded)
	Vref support: bit 7 = Reserved bit 6 = Reserved bit 5 = 100% support (1 = yes, 0 = no) bit 4 = 80% support (1 = yes, 0 = no) bit 3 = Reserved bit 2 = GND support (1 = yes, 0 = no) bit 1 = 50% support (1 = yes, 0 = no) bit 0 = Hi-Z support (1 = yes, 0 = no)			
Rsvd1	7	R	0h	N/A (Hard-coded)
	Reserved.			
BalancedIO	6	R	0h	N/A (Hard-coded)
	Balanced I/O support: 1 = yes, 0 = no.			
InCap	5	R	1h	N/A (Hard-coded)
	Input support: 1 = yes, 0 = no.			
OutCap	4	R	0h	N/A (Hard-coded)
	Output support: 1 = yes, 0 = no.			
HPhnDrvCap	3	R	0h	N/A (Hard-coded)
	Headphone amp present: 1 = yes, 0 = no.			
PresDtctCap	2	R	0h	N/A (Hard-coded)
	Presence detection support: 1 = yes, 0 = no.			
TrigRqd	1	R	0h	N/A (Hard-coded)
	Trigger required for impedance sense: 1 = yes, 0 = no.			
ImpSenseCap	0	R	0h	N/A (Hard-coded)
	Impedance sense support: 1 = yes, 0 = no.			

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7.19.2. CD (NID = 12h): PwrState

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				705h
Get	F0500h			

Field Name	Bits	R/W	Default	Reset
Rsvd4	31:11	R	000000h	N/A (Hard-coded)
	Reserved.			
SettingsReset	10	R	1h	POR - DAFG - ULR
	Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget.			
Rsvd3	9	R	0h	N/A (Hard-coded)
	Reserved.			
Error	8	R	0h	POR - DAFG - ULR
	Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state.			
Rsvd2	7:6	R	0h	N/A (Hard-coded)
	Reserved.			
Act	5:4	R	3h	POR - DAFG - LR
	Actual power state of this widget.			
Rsvd1	3:2	R	0h	N/A (Hard-coded)
	Reserved.			
Set	1:0	RW	0h	POR - DAFG - LR
	Current power state setting for this widget.			

7.19.3. CD (NID = 12h): PinWCntrl

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				707h

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7.19.3. CD (NID = 12h): PinWCntrl

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Get	F0700h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:6	R	0000000h	N/A (Hard-coded)
	Reserved.			
InEn	5	RW	0h	POR - DAFG - ULR
	Input enable: 1 = enabled, 0 = disabled.			
Rsvd1	4:0	R	00h	N/A (Hard-coded)
	Reserved.			

7.19.4. CD (NID = 12h): ConfigDefault

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set	71Fh	71Eh	71Dh	71Ch
Get	F1F00h / F1E00h / F1D00h / F1C00h			

Field Name	Bits	R/W	Default	Reset
PortConnectivity	31:30	RW	2h	POR
	Port connectivity: 0h = Port complex is connected to a jack 1h = No physical connection for port 2h = Fixed function device is attached 3h = Both jack and internal device attached (info in all other fields refers to integrated device, any presence detection refers to jack)			

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Field Name	Bits	R/W	Default	Reset
Location	29:24	RW	19h	POR
	Location Bits [5..4]: 0h = External on primary chassis 1h = Internal 2h = Separate chassis 3h = Other Bits [3..0]: 0h = N/A 1h = Rear 2h = Front 3h = Left 4h = Right 5h = Top 6h = Bottom 7h-9h = Special Ah-Fh = Reserved			
Device	23:20	RW	3h	POR
	Default device: 0h = Line out 1h = Speaker 2h = HP out 3h = CD 4h = SPDIF Out 5h = Digital other out 6h = Modem line side 7h = Modem handset side 8h = Line in 9h = Aux Ah = Mic in Bh = Telephony Ch = SPDIF In Dh = Digital other in Eh = Reserved Fh = Other			

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Field Name	Bits	R/W	Default	Reset
ConnectionType	19:16	RW	3h	POR
	Connection type: 0h = Unknown 1h = 1/8" stereo/mono 2h = 1/4" stereo/mono 3h = ATAPI internal 4h = RCA 5h = Optical 6h = Other digital 7h = Other analog 8h = Multichannel analog (DIN) 9h = XLR/Professional Ah = RJ-11 (modem) Bh = Combination Ch-Eh = Reserved Fh = Other			
Color	15:12	RW	0h	POR
	Color: 0h = Unknown 1h = Black 2h = Grey 3h = Blue 4h = Green 5h = Red 6h = Orange 7h = Yellow 8h = Purple 9h = Pink Ah-Dh = Reserved Eh = White Fh = Other			
Misc	11:8	RW	1h	POR
	Miscellaneous: Bits [3..1] = Reserved Bit 0 = Jack detect override			
Association	7:4	RW	4h	POR
	Default assocation.			
Sequence	3:0	RW	1h	POR
	Sequence.			

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7.20. DMic0 (NID = 13h): WCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0009h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:24	R	00h	N/A (Hard-coded)
	Reserved.			
Type	23:20	R	Fh	N/A (Hard-coded)
	Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined			
Delay	19:16	R	0h	N/A (Hard-coded)
	Number of sample delays through widget.			
Rsvd1	15:12	R	0h	N/A (Hard-coded)
	Reserved.			
SwapCap	11	R	0h	N/A (Hard-coded)
	Left/right swap support: 1 = yes, 0 = no.			
PwrCntrl	10	R	0h	N/A (Hard-coded)
	Power state support: 1 = yes, 0 = no.			
DigitalStrm	9	R	0h	N/A (Hard-coded)
	Digital stream support: 1 = yes (digital), 0 = no (analog).			
ConnList	8	R	0h	N/A (Hard-coded)
	Connection list present: 1 = yes, 0 = no.			

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Field Name	Bits	R/W	Default	Reset
UnsolCap	7	R	0h	N/A (Hard-coded)
	Unsolicited response support: 1 = yes, 0 = no.			
ProcWidget	6	R	0h	N/A (Hard-coded)
	Processing state support: 1 = yes, 0 = no.			
Stripe	5	R	0h	N/A (Hard-coded)
	Striping support: 1 = yes, 0 = no.			
FormatOvrd	4	R	0h	N/A (Hard-coded)
	Stream format override: 1 = yes, 0 = no.			
AmpParOvrd	3	R	0h	N/A (Hard-coded)
	Amplifier capabilities override: 1 = yes, no.			
OutAmpPrsnt	2	R	0h	N/A (Hard-coded)
	Output amp present: 1 = yes, 0 = no.			
InAmpPrsnt	1	R	0h	N/A (Hard-coded)
	Input amp present: 1 = yes, 0 = no.			
Stereo	0	R	0h	N/A (Hard-coded)
	Stereo stream support: 1 = yes (stereo), 0 = no (mono).			

7.20.1. DMic0 (NID = 13h): PinCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Ch			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:17	R	0000h	N/A (Hard-coded)
	Reserved.			

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Field Name	Bits	R/W	Default	Reset
EapdCap	16	R	0h	N/A (Hard-coded)
	EAPD support: 1 = yes, 0 = no.			
VRefCntrl	15:8	R	00h	N/A (Hard-coded)
	Vref support: bit 7 = Reserved bit 6 = Reserved bit 5 = 100% support (1 = yes, 0 = no) bit 4 = 80% support (1 = yes, 0 = no) bit 3 = Reserved bit 2 = GND support (1 = yes, 0 = no) bit 1 = 50% support (1 = yes, 0 = no) bit 0 = Hi-Z support (1 = yes, 0 = no)			
Rsvd1	7	R	0h	N/A (Hard-coded)
	Reserved.			
BalancedIO	6	R	0h	N/A (Hard-coded)
	Balanced I/O support: 1 = yes, 0 = no.			
InCap	5	R	1h	N/A (Hard-coded)
	Input support: 1 = yes, 0 = no.			
OutCap	4	R	0h	N/A (Hard-coded)
	Output support: 1 = yes, 0 = no.			
HPhnDrvCap	3	R	0h	N/A (Hard-coded)
	Headphone amp present: 1 = yes, 0 = no.			
PresDtctCap	2	R	0h	N/A (Hard-coded)
	Presence detection support: 1 = yes, 0 = no.			
TrigRqd	1	R	0h	N/A (Hard-coded)
	Trigger required for impedance sense: 1 = yes, 0 = no.			
ImpSenseCap	0	R	0h	N/A (Hard-coded)
	Impedance sense support: 1 = yes, 0 = no.			

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7.20.2. DMic0 (NID = 13h): InAmpLeft

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				360h
Get	B2000h			

Field Name	Bits	R/W	Default	Reset
Rsvd1	31:2	R	00000000h	N/A (Hard-coded)
	Reserved.			
Gain	1:0	RW	0h	POR - DAFG - ULR
	Amp gain step number (see InAmpCap parameter pertaining to this widget).			

7.20.3. DMic0 (NID = 13h): InAmpRight

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				350h
Get	B0000h			

Field Name	Bits	R/W	Default	Reset
Rsvd1	31:2	R	00000000h	N/A (Hard-coded)
	Reserved.			
Gain	1:0	RW	0h	POR - DAFG - ULR
	Amp gain step number (see InAmpCap parameter pertaining to this widget).			

7.20.4. DMic0 (NID = 13h): PwrState

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				705h
Get	F0500h			

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Field Name	Bits	R/W	Default	Reset
Rsvd4	31:11	R	000000h	N/A (Hard-coded)
	Reserved.			
SettingsReset	10	R	1h	POR - DAFG - ULR
	Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget.			
Rsvd3	9	R	0h	N/A (Hard-coded)
	Reserved.			
Error	8	R	0h	POR - DAFG - ULR
	Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state.			
Rsvd2	7:6	R	0h	N/A (Hard-coded)
	Reserved.			
Act	5:4	R	3h	POR - DAFG - LR
	Actual power state of this widget.			
Rsvd1	3:2	R	0h	N/A (Hard-coded)
	Reserved.			
Set	1:0	RW	0h	POR - DAFG - LR
	Current power state setting for this widget.			

7.20.5. DMic0 (NID = 13h): PinWCntrl

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				707h
Get	F0700h			

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Field Name	Bits	R/W	Default	Reset
Rsvd2	31:6	R	0000000h	N/A (Hard-coded)
	Reserved.			
InEn	5	RW	0h	POR - DAFG - ULR
	Input enable: 1 = enabled, 0 = disabled.			
Rsvd1	4:0	R	00h	N/A (Hard-coded)
	Reserved.			

7.20.6. DMic0 (NID = 13h): UnsolResp

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				708h
Get	F0800h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
En	7	RW	0h	POR - DAFG - ULR
	Unsolicited response enable (also enables Wake events for this Widget): 1 = enabled, 0 = disabled.			
Rsvd1	6	R	0h	N/A (Hard-coded)
	Reserved.			
Tag	5:0	RW	00h	POR - DAFG - ULR
	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.			

7.20.7. DMic0 (NID = 13h): ConfigDefault

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set	71Fh	71Eh	71Dh	71Ch

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7.20.7. DMic0 (NID = 13h): ConfigDefault

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Get	F1F00h / F1E00h / F1D00h / F1C00h			

Field Name	Bits	R/W	Default	Reset
PortConnectivity	31:30	RW	2h	POR
	Port connectivity: 0h = Port complex is connected to a jack 1h = No physical connection for port 2h = Fixed function device is attached 3h = Both jack and internal device attached (info in all other fields refers to integrated device, any presence detection refers to jack)			
Location	29:24	RW	10h	POR
	Location Bits [5..4]: 0h = External on primary chassis 1h = Internal 2h = Separate chassis 3h = Other Bits [3..0]: 0h = N/A 1h = Rear 2h = Front 3h = Left 4h = Right 5h = Top 6h = Bottom 7h-9h = Special Ah-Fh = Reserved			

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Field Name	Bits	R/W	Default	Reset
Device	23:20	RW	Ah	POR
	Default device: 0h = Line out 1h = Speaker 2h = HP out 3h = CD 4h = SPDIF Out 5h = Digital other out 6h = Modem line side 7h = Modem handset side 8h = Line in 9h = Aux Ah = Mic in Bh = Telephony Ch = SPDIF In Dh = Digital other in Eh = Reserved Fh = Other			
ConnectionType	19:16	RW	3h	POR
	Connection type: 0h = Unknown 1h = 1/8" stereo/mono 2h = 1/4" stereo/mono 3h = ATAPI internal 4h = RCA 5h = Optical 6h = Other digital 7h = Other analog 8h = Multichannel analog (DIN) 9h = XLR/Professional Ah = RJ-11 (modem) Bh = Combination Ch-Eh = Reserved Fh = Other			

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Field Name	Bits	R/W	Default	Reset
Color	15:12	RW	0h	POR
	Color: 0h = Unknown 1h = Black 2h = Grey 3h = Blue 4h = Green 5h = Red 6h = Orange 7h = Yellow 8h = Purple 9h = Pink Ah-Dh = Reserved Eh = White Fh = Other			
Misc	11:8	RW	1h	POR
	Miscellaneous: Bits [3..1] = Reserved Bit 0 = Jack detect override			
Association	7:4	RW	4h	POR
	Default assocation.			
Sequence	3:0	RW	2h	POR
	Sequence.			

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7.21. DMic1 (NID = 14h): WCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0009h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:24	R	00h	N/A (Hard-coded)
	Reserved.			
Type	23:20	R	Fh	N/A (Hard-coded)
	Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined			
Delay	19:16	R	0h	N/A (Hard-coded)
	Number of sample delays through widget.			
Rsvd1	15:12	R	0h	N/A (Hard-coded)
	Reserved.			
SwapCap	11	R	0h	N/A (Hard-coded)
	Left/right swap support: 1 = yes, 0 = no.			
PwrCntrl	10	R	0h	N/A (Hard-coded)
	Power state support: 1 = yes, 0 = no.			
DigitalStrm	9	R	0h	N/A (Hard-coded)
	Digital stream support: 1 = yes (digital), 0 = no (analog).			
ConnList	8	R	0h	N/A (Hard-coded)
	Connection list present: 1 = yes, 0 = no.			

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Field Name	Bits	R/W	Default	Reset
UnsolCap	7	R	0h	N/A (Hard-coded)
	Unsolicited response support: 1 = yes, 0 = no.			
ProcWidget	6	R	0h	N/A (Hard-coded)
	Processing state support: 1 = yes, 0 = no.			
Stripe	5	R	0h	N/A (Hard-coded)
	Striping support: 1 = yes, 0 = no.			
FormatOvrd	4	R	0h	N/A (Hard-coded)
	Stream format override: 1 = yes, 0 = no.			
AmpParOvrd	3	R	0h	N/A (Hard-coded)
	Amplifier capabilities override: 1 = yes, no.			
OutAmpPrsnt	2	R	0h	N/A (Hard-coded)
	Output amp present: 1 = yes, 0 = no.			
InAmpPrsnt	1	R	0h	N/A (Hard-coded)
	Input amp present: 1 = yes, 0 = no.			
Stereo	0	R	0h	N/A (Hard-coded)
	Stereo stream support: 1 = yes (stereo), 0 = no (mono).			

7.21.1. DMic1 (NID = 14h): PinCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Ch			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:17	R	0000h	N/A (Hard-coded)
	Reserved.			

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Field Name	Bits	R/W	Default	Reset
EapdCap	16	R	0h	N/A (Hard-coded)
	EAPD support: 1 = yes, 0 = no.			
VRefCntrl	15:8	R	00h	N/A (Hard-coded)
	Vref support: bit 7 = Reserved bit 6 = Reserved bit 5 = 100% support (1 = yes, 0 = no) bit 4 = 80% support (1 = yes, 0 = no) bit 3 = Reserved bit 2 = GND support (1 = yes, 0 = no) bit 1 = 50% support (1 = yes, 0 = no) bit 0 = Hi-Z support (1 = yes, 0 = no)			
Rsvd1	7	R	0h	N/A (Hard-coded)
	Reserved.			
BalancedIO	6	R	0h	N/A (Hard-coded)
	Balanced I/O support: 1 = yes, 0 = no.			
InCap	5	R	1h	N/A (Hard-coded)
	Input support: 1 = yes, 0 = no.			
OutCap	4	R	0h	N/A (Hard-coded)
	Output support: 1 = yes, 0 = no.			
HPhnDrvCap	3	R	0h	N/A (Hard-coded)
	Headphone amp present: 1 = yes, 0 = no.			
PresDtctCap	2	R	0h	N/A (Hard-coded)
	Presence detection support: 1 = yes, 0 = no.			
TrigRqd	1	R	0h	N/A (Hard-coded)
	Trigger required for impedance sense: 1 = yes, 0 = no.			
ImpSenseCap	0	R	0h	N/A (Hard-coded)
	Impedance sense support: 1 = yes, 0 = no.			

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7.21.2. DMic1 (NID = 14h): InAmpLeft

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				360h
Get	B2000h			

Field Name	Bits	R/W	Default	Reset
Rsvd1	31:2	R	00000000h	N/A (Hard-coded)
	Reserved.			
Gain	1:0	RW	0h	POR - DAFG - ULR
	Amp gain step number (see InAmpCap parameter pertaining to this widget).			

7.21.3. DMic1 (NID = 14h): InAmpRight

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				350h
Get	B0000h			

Field Name	Bits	R/W	Default	Reset
Rsvd1	31:2	R	00000000h	N/A (Hard-coded)
	Reserved.			
Gain	1:0	RW	0h	POR - DAFG - ULR
	Amp gain step number (see InAmpCap parameter pertaining to this widget).			

7.21.4. DMic1 (NID = 14h): PwrState

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				705h
Get	F0500h			

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Field Name	Bits	R/W	Default	Reset
Rsvd4	31:11	R	000000h	N/A (Hard-coded)
	Reserved.			
SettingsReset	10	R	1h	POR - DAFG - ULR
	Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget.			
Rsvd3	9	R	0h	N/A (Hard-coded)
	Reserved.			
Error	8	R	0h	POR - DAFG - ULR
	Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state.			
Rsvd2	7:6	R	0h	N/A (Hard-coded)
	Reserved.			
Act	5:4	R	3h	POR - DAFG - LR
	Actual power state of this widget.			
Rsvd1	3:2	R	0h	N/A (Hard-coded)
	Reserved.			
Set	1:0	RW	0h	POR - DAFG - LR
	Current power state setting for this widget.			

7.21.5. DMic1 (NID = 14h): PinWCntrl

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				707h
Get	F0700h			

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Field Name	Bits	R/W	Default	Reset
Rsvd2	31:6	R	0000000h	N/A (Hard-coded)
	Reserved.			
InEn	5	RW	0h	POR - DAFG - ULR
	Input enable: 1 = enabled, 0 = disabled.			
Rsvd1	4:0	R	00h	N/A (Hard-coded)
	Reserved.			

7.21.6. DMic1 (NID = 14h): UnsolResp

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				708h
Get	F0800h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
En	7	RW	0h	POR - DAFG - ULR
	Unsolicited response enable (also enables Wake events for this Widget): 1 = enabled, 0 = disabled.			
Rsvd1	6	R	0h	N/A (Hard-coded)
	Reserved.			
Tag	5:0	RW	00h	POR - DAFG - ULR
	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.			

7.21.7. DMic1 (NID = 14h): ConfigDefault

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set	71Fh	71Eh	71Dh	71Ch

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7.21.7. DMic1 (NID = 14h): ConfigDefault

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Get	F1F00h / F1E00h / F1D00h / F1C00h			

Field Name	Bits	R/W	Default	Reset
PortConnectivity	31:30	RW	2h	POR
	Port connectivity: 0h = Port complex is connected to a jack 1h = No physical connection for port 2h = Fixed function device is attached 3h = Both jack and internal device attached (info in all other fields refers to integrated device, any presence detection refers to jack)			
Location	29:24	RW	10h	POR
	Location Bits [5..4]: 0h = External on primary chassis 1h = Internal 2h = Separate chassis 3h = Other Bits [3..0]: 0h = N/A 1h = Rear 2h = Front 3h = Left 4h = Right 5h = Top 6h = Bottom 7h-9h = Special Ah-Fh = Reserved			

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Field Name	Bits	R/W	Default	Reset
Device	23:20	RW	Ah	POR
	Default device: 0h = Line out 1h = Speaker 2h = HP out 3h = CD 4h = SPDIF Out 5h = Digital other out 6h = Modem line side 7h = Modem handset side 8h = Line in 9h = Aux Ah = Mic in Bh = Telephony Ch = SPDIF In Dh = Digital other in Eh = Reserved Fh = Other			
ConnectionType	19:16	RW	3h	POR
	Connection type: 0h = Unknown 1h = 1/8" stereo/mono 2h = 1/4" stereo/mono 3h = ATAPI internal 4h = RCA 5h = Optical 6h = Other digital 7h = Other analog 8h = Multichannel analog (DIN) 9h = XLR/Professional Ah = RJ-11 (modem) Bh = Combination Ch-Eh = Reserved Fh = Other			

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Field Name	Bits	R/W	Default	Reset
Color	15:12	RW	0h	POR
	Color: 0h = Unknown 1h = Black 2h = Grey 3h = Blue 4h = Green 5h = Red 6h = Orange 7h = Yellow 8h = Purple 9h = Pink Ah-Dh = Reserved Eh = White Fh = Other			
Misc	11:8	RW	1h	POR
	Miscellaneous: Bits [3..1] = Reserved Bit 0 = Jack detect override			
Association	7:4	RW	4h	POR
	Default assocation.			
Sequence	3:0	RW	3h	POR
	Sequence.			

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7.22. DAC0 (NID = 15h): WCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0009h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:24	R	00h	N/A (Hard-coded)
	Reserved.			
Type	23:20	R	0h	N/A (Hard-coded)
	Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined			
Delay	19:16	R	Dh	N/A (Hard-coded)
	Number of sample delays through widget.			
Rsvd1	15:12	R	0h	N/A (Hard-coded)
	Reserved.			
SwapCap	11	R	1h	N/A (Hard-coded)
	Left/right swap support: 1 = yes, 0 = no.			
PwrCntrl	10	R	1h	N/A (Hard-coded)
	Power state support: 1 = yes, 0 = no.			
Dig	9	R	0h	N/A (Hard-coded)
	Digital stream support: 1 = yes (digital), 0 = no (analog).			
ConnList	8	R	0h	N/A (Hard-coded)
	Connection list present: 1 = yes, 0 = no.			

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Field Name	Bits	R/W	Default	Reset
UnSolCap	7	R	0h	N/A (Hard-coded)
	Unsolicited response support: 1 = yes, 0 = no.			
ProcWidget	6	R	0h	N/A (Hard-coded)
	Processing state support: 1 = yes, 0 = no.			
Stripe	5	R	0h	N/A (Hard-coded)
	Striping support: 1 = yes, 0 = no.			
FormatOvrd	4	R	0h	N/A (Hard-coded)
	Stream format override: 1 = yes, 0 = no.			
AmpParOvrd	3	R	0h	N/A (Hard-coded)
	Amplifier capabilities override: 1 = yes, no.			
OutAmpPrsnt	2	R	1h	N/A (Hard-coded)
	Output amp present: 1 = yes, 0 = no.			
InAmpPrsnt	1	R	0h	N/A (Hard-coded)
	Input amp present: 1 = yes, 0 = no.			
Stereo	0	R	1h	N/A (Hard-coded)
	Stereo stream support: 1 = yes (stereo), 0 = no (mono).			

7.22.1. DAC0 (NID = 15h): Cnvtr

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set			2h	
Get	A0000h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:16	R	0000h	N/A (Hard-coded)
	Reserved.			

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Field Name	Bits	R/W	Default	Reset
StrmType	15	R	0h	N/A (Hard-coded)
	Stream type: 1 = Non-PCM, 0 = PCM.			
FrmtSmplRate	14	RW	0h	POR - DAFG - ULR
	Sample base rate: 1 = 44.1kHz, 0 = 48kHz.			
SmplRateMultp	13:11	RW	0h	POR - DAFG - ULR
	Sample base rate multiple: 000b= x1 (48kHz/44.1kHz or less) 001b= x2 (96kHz/88.2kHz/32kHz) 010b= x3 (144kHz) 011b= x4 (192kHz/176.4kHz) 100b-111b Reserved			
SmplRateDiv	10:8	RW	0h	POR - DAFG - ULR
	Sample base rate divider: 000b= Divide by 1 (48kHz/44.1kHz) 001b= Divide by 2 (24kHz/20.05kHz) 010b= Divide by 3 (16kHz/32kHz) 011b= Divide by 4 (11.025kHz) 100b= Divide by 5 (9.6kHz) 101b= Divide by 6 (8kHz) 110b= Divide by 7 111b= Divide by 8 (6kHz)			
Rsvd1	7	R	0h	N/A (Hard-coded)
	Reserved.			
BitsPerSmpl	6:4	RW	3h	POR - DAFG - ULR
	Bits per sample: 000b= 8 bits 001b= 16 bits 010b= 20 bits 011b= 24 bits 100b= 32 bits 101b-111b= Reserved			
NmbrChan	3:0	RW	1h	POR - DAFG - ULR
	Total number of channels in the stream assigned to this converter: 0000b-1111b= 1-16 channels.			

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7.22.2. DAC0 (NID = 15h): OutAmpLeft

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				3A0h
Get	BA000h			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
Mute	7	RW	1h	POR - DAFG - ULR
	Amp mute: 1 = muted, 0 = not muted.			
Gain	6:0	RW	7Fh	POR - DAFG - ULR
	Amp gain step number (see OutAmpCap parameter pertaining to this widget).			

7.22.3. DAC0 (NID = 15h): OutAmpRight

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				390h
Get	B8000h			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
Mute	7	RW	1h	POR - DAFG - ULR
	Amp mute: 1 = muted, 0 = not muted.			
Gain	6:0	RW	7Fh	POR - DAFG - ULR
	Amp gain step number (see OutAmpCap parameter pertaining to this widget).			

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7.22.4. DAC0 (NID = 15h): PwrState

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				705h
Get	F0500h			

Field Name	Bits	R/W	Default	Reset
Rsvd4	31:11	R	000000h	N/A (Hard-coded)
	Reserved.			
SettingsReset	10	R	1h	POR - DAFG - ULR
	Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget.			
Rsvd3	9	R	0h	N/A (Hard-coded)
	Reserved.			
Error	8	R	0h	POR - DAFG - ULR
	Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state.			
Rsvd2	7:6	R	0h	N/A (Hard-coded)
	Reserved.			
Act	5:4	R	3h	POR - DAFG - LR
	Actual power state of this widget.			
Rsvd1	3:2	R	0h	N/A (Hard-coded)
	Reserved.			
Set	1:0	RW	3h	POR - DAFG - LR
	Current power state setting for this widget.			

7.22.5. DAC0 (NID = 15h): CnvtrID

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				706h

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7.22.5. DAC0 (NID = 15h): CnvtrID

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Get	F0600h			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
Strm	7:4	RW	0h	POR - S&DAFG - LR - PS
	Stream ID: 0h = Converter "off", 1h-Fh = valid ID's.			
Ch	3:0	RW	0h	POR - S&DAFG - LR - PS
	Channel assignment ("Ch" and "Ch+1" assigned as a pair, for a stereo converter).			

7.22.6. DAC0 (NID = 15h): EAPDBTLLR

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				70Ch
Get	F0C00h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:3	R	00000000h	N/A (Hard-coded)
	Reserved.			
SwapEn	2	RW	0h	POR - DAFG - ULR
	Swap enable: 1 = L/R swap enabled, 0 = L/R swap disabled.			
Rsvd1	1:0	R	0h	N/A (Hard-coded)
	Reserved.			

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7.23. DAC1 (NID = 16h): WCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0009h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:24	R	00h	N/A (Hard-coded)
	Reserved.			
Type	23:20	R	0h	N/A (Hard-coded)
	Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined			
Delay	19:16	R	Dh	N/A (Hard-coded)
	Number of sample delays through widget.			
Rsvd1	15:12	R	0h	N/A (Hard-coded)
	Reserved.			
SwapCap	11	R	1h	N/A (Hard-coded)
	Left/right swap support: 1 = yes, 0 = no.			
PwrCntrl	10	R	1h	N/A (Hard-coded)
	Power state support: 1 = yes, 0 = no.			
Dig	9	R	0h	N/A (Hard-coded)
	Digital stream support: 1 = yes (digital), 0 = no (analog).			
ConnList	8	R	0h	N/A (Hard-coded)
	Connection list present: 1 = yes, 0 = no.			

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Field Name	Bits	R/W	Default	Reset
UnSolCap	7	R	0h	N/A (Hard-coded)
	Unsolicited response support: 1 = yes, 0 = no.			
ProcWidget	6	R	0h	N/A (Hard-coded)
	Processing state support: 1 = yes, 0 = no.			
Stripe	5	R	0h	N/A (Hard-coded)
	Striping support: 1 = yes, 0 = no.			
FormatOvrd	4	R	0h	N/A (Hard-coded)
	Stream format override: 1 = yes, 0 = no.			
AmpParOvrd	3	R	0h	N/A (Hard-coded)
	Amplifier capabilities override: 1 = yes, no.			
OutAmpPrsnt	2	R	1h	N/A (Hard-coded)
	Output amp present: 1 = yes, 0 = no.			
InAmpPrsnt	1	R	0h	N/A (Hard-coded)
	Input amp present: 1 = yes, 0 = no.			
Stereo	0	R	1h	N/A (Hard-coded)
	Stereo stream support: 1 = yes (stereo), 0 = no (mono).			

7.23.1. DAC1 (NID = 16h): Cnvtr

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set			2h	
Get	A0000h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:16	R	0000h	N/A (Hard-coded)
	Reserved.			

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Field Name	Bits	R/W	Default	Reset
StrmType	15	R	0h	N/A (Hard-coded)
	Stream type: 1 = Non-PCM, 0 = PCM.			
FrmtSmplRate	14	RW	0h	POR - DAFG - ULR
	Sample base rate: 1 = 44.1kHz, 0 = 48kHz.			
SmplRateMultp	13:11	RW	0h	POR - DAFG - ULR
	Sample base rate multiple: 000b= x1 (48kHz/44.1kHz or less) 001b= x2 (96kHz/88.2kHz/32kHz) 010b= x3 (144kHz) 011b= x4 (192kHz/176.4kHz) 100b-111b Reserved			
SmplRateDiv	10:8	RW	0h	POR - DAFG - ULR
	Sample base rate divider: 000b= Divide by 1 (48kHz/44.1kHz) 001b= Divide by 2 (24kHz/20.05kHz) 010b= Divide by 3 (16kHz/32kHz) 011b= Divide by 4 (11.025kHz) 100b= Divide by 5 (9.6kHz) 101b= Divide by 6 (8kHz) 110b= Divide by 7 111b= Divide by 8 (6kHz)			
Rsvd1	7	R	0h	N/A (Hard-coded)
	Reserved.			
BitsPerSmpl	6:4	RW	3h	POR - DAFG - ULR
	Bits per sample: 000b= 8 bits 001b= 16 bits 010b= 20 bits 011b= 24 bits 100b= 32 bits 101b-111b= Reserved			
NmbrChan	3:0	RW	1h	POR - DAFG - ULR
	Total number of channels in the stream assigned to this converter: 0000b-1111b= 1-16 channels.			

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7.23.2. DAC1 (NID = 16h): OutAmpLeft

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				3A0h
Get	BA000h			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
Mute	7	RW	1h	POR - DAFG - ULR
	Amp mute: 1 = muted, 0 = not muted.			
Gain	6:0	RW	7Fh	POR - DAFG - ULR
	Amp gain step number (see OutAmpCap parameter pertaining to this widget).			

7.23.3. DAC1 (NID = 16h): OutAmpRight

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				390h
Get	B8000h			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
Mute	7	RW	1h	POR - DAFG - ULR
	Amp mute: 1 = muted, 0 = not muted.			
Gain	6:0	RW	7Fh	POR - DAFG - ULR
	Amp gain step number (see OutAmpCap parameter pertaining to this widget).			

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7.23.4. DAC1 (NID = 16h): PwrState

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				705h
Get	F0500h			

Field Name	Bits	R/W	Default	Reset
Rsvd4	31:11	R	000000h	N/A (Hard-coded)
	Reserved.			
SettingsReset	10	R	1h	POR - DAFG - ULR
	Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget.			
Rsvd3	9	R	0h	N/A (Hard-coded)
	Reserved.			
Error	8	R	0h	POR - DAFG - ULR
	Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state.			
Rsvd2	7:6	R	0h	N/A (Hard-coded)
	Reserved.			
Act	5:4	R	3h	POR - DAFG - LR
	Actual power state of this widget.			
Rsvd1	3:2	R	0h	N/A (Hard-coded)
	Reserved.			
Set	1:0	RW	3h	POR - DAFG - LR
	Current power state setting for this widget.			

7.23.5. DAC1 (NID = 16h): CnvtrID

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				706h

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7.23.5. DAC1 (NID = 16h): CnvtrID

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Get	F0600h			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
Strm	7:4	RW	0h	POR - S&DAFG - LR - PS
	Stream ID: 0h = Converter "off", 1h-Fh = valid ID's.			
Ch	3:0	RW	0h	POR - S&DAFG - LR - PS
	Channel assignment ("Ch" and "Ch+1" assigned as a pair, for a stereo converter).			

7.23.6. DAC1 (NID = 16h): EAPDBTLLR

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				70Ch
Get	F0C00h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:3	R	00000000h	N/A (Hard-coded)
	Reserved.			
SwapEn	2	RW	0h	POR - DAFG - ULR
	Swap enable: 1 = L/R swap enabled, 0 = L/R swap disabled.			
Rsvd1	1:0	R	0h	N/A (Hard-coded)
	Reserved.			

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7.24. DAC2 (NID = 17h): WCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0009h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:24	R	00h	N/A (Hard-coded)
	Reserved.			
Type	23:20	R	0h	N/A (Hard-coded)
	Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined			
Delay	19:16	R	Dh	N/A (Hard-coded)
	Number of sample delays through widget.			
Rsvd1	15:12	R	0h	N/A (Hard-coded)
	Reserved.			
SwapCap	11	R	1h	N/A (Hard-coded)
	Left/right swap support: 1 = yes, 0 = no.			
PwrCntrl	10	R	1h	N/A (Hard-coded)
	Power state support: 1 = yes, 0 = no.			
Dig	9	R	0h	N/A (Hard-coded)
	Digital stream support: 1 = yes (digital), 0 = no (analog).			
ConnList	8	R	0h	N/A (Hard-coded)
	Connection list present: 1 = yes, 0 = no.			

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Field Name	Bits	R/W	Default	Reset
UnSolCap	7	R	0h	N/A (Hard-coded)
	Unsolicited response support: 1 = yes, 0 = no.			
ProcWidget	6	R	0h	N/A (Hard-coded)
	Processing state support: 1 = yes, 0 = no.			
Stripe	5	R	0h	N/A (Hard-coded)
	Striping support: 1 = yes, 0 = no.			
FormatOvrd	4	R	0h	N/A (Hard-coded)
	Stream format override: 1 = yes, 0 = no.			
AmpParOvrd	3	R	0h	N/A (Hard-coded)
	Amplifier capabilities override: 1 = yes, no.			
OutAmpPrsnt	2	R	1h	N/A (Hard-coded)
	Output amp present: 1 = yes, 0 = no.			
InAmpPrsnt	1	R	0h	N/A (Hard-coded)
	Input amp present: 1 = yes, 0 = no.			
Stereo	0	R	1h	N/A (Hard-coded)
	Stereo stream support: 1 = yes (stereo), 0 = no (mono).			

7.24.1. DAC2 (NID = 17h): Cnvtr

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set			2h	
Get	A0000h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:16	R	0000h	N/A (Hard-coded)
	Reserved.			

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Field Name	Bits	R/W	Default	Reset
StrmType	15	R	0h	N/A (Hard-coded)
	Stream type: 1 = Non-PCM, 0 = PCM.			
FrmtSmplRate	14	RW	0h	POR - DAFG - ULR
	Sample base rate: 1 = 44.1kHz, 0 = 48kHz.			
SmplRateMultp	13:11	RW	0h	POR - DAFG - ULR
	Sample base rate multiple: 000b= x1 (48kHz/44.1kHz or less) 001b= x2 (96kHz/88.2kHz/32kHz) 010b= x3 (144kHz) 011b= x4 (192kHz/176.4kHz) 100b-111b Reserved			
SmplRateDiv	10:8	RW	0h	POR - DAFG - ULR
	Sample base rate divider: 000b= Divide by 1 (48kHz/44.1kHz) 001b= Divide by 2 (24kHz/20.05kHz) 010b= Divide by 3 (16kHz/32kHz) 011b= Divide by 4 (11.025kHz) 100b= Divide by 5 (9.6kHz) 101b= Divide by 6 (8kHz) 110b= Divide by 7 111b= Divide by 8 (6kHz)			
Rsvd1	7	R	0h	N/A (Hard-coded)
	Reserved.			
BitsPerSmpl	6:4	RW	3h	POR - DAFG - ULR
	Bits per sample: 000b= 8 bits 001b= 16 bits 010b= 20 bits 011b= 24 bits 100b= 32 bits 101b-111b= Reserved			
NmbrChan	3:0	RW	1h	POR - DAFG - ULR
	Total number of channels in the stream assigned to this converter: 0000b-1111b= 1-16 channels.			

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7.24.2. DAC2 (NID = 17h): OutAmpLeft

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				3A0h
Get	BA000h			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
Mute	7	RW	1h	POR - DAFG - ULR
	Amp mute: 1 = muted, 0 = not muted.			
Gain	6:0	RW	7Fh	POR - DAFG - ULR
	Amp gain step number (see OutAmpCap parameter pertaining to this widget).			

7.24.3. DAC2 (NID = 17h): OutAmpRight

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				390h
Get	B8000h			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
Mute	7	RW	1h	POR - DAFG - ULR
	Amp mute: 1 = muted, 0 = not muted.			
Gain	6:0	RW	7Fh	POR - DAFG - ULR
	Amp gain step number (see OutAmpCap parameter pertaining to this widget).			

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7.24.4. DAC2 (NID = 17h): PwrState

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				705h
Get	F0500h			

Field Name	Bits	R/W	Default	Reset
Rsvd4	31:11	R	000000h	N/A (Hard-coded)
	Reserved.			
SettingsReset	10	R	1h	POR - DAFG - ULR
	Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget.			
Rsvd3	9	R	0h	N/A (Hard-coded)
	Reserved.			
Error	8	R	0h	POR - DAFG - ULR
	Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state.			
Rsvd2	7:6	R	0h	N/A (Hard-coded)
	Reserved.			
Act	5:4	R	3h	POR - DAFG - LR
	Actual power state of this widget.			
Rsvd1	3:2	R	0h	N/A (Hard-coded)
	Reserved.			
Set	1:0	RW	3h	POR - DAFG - LR
	Current power state setting for this widget.			

7.24.5. DAC2 (NID = 17h): CnvtrID

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				706h

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7.24.5. DAC2 (NID = 17h): CnvtrID

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Get	F0600h			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
Strm	7:4	RW	0h	POR - S&DAFG - LR - PS
	Stream ID: 0h = Converter "off", 1h-Fh = valid ID's.			
Ch	3:0	RW	0h	POR - S&DAFG - LR - PS
	Channel assignment ("Ch" and "Ch+1" assigned as a pair, for a stereo converter).			

7.24.6. DAC2 (NID = 17h): EAPDBTLLR

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				70Ch
Get	F0C00h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:3	R	00000000h	N/A (Hard-coded)
	Reserved.			
SwapEn	2	RW	0h	POR - DAFG - ULR
	Swap enable: 1 = L/R swap enabled, 0 = L/R swap disabled.			
Rsvd1	1:0	R	0h	N/A (Hard-coded)
	Reserved.			

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7.25. DAC3 (NID = 18h): WCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0009h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:24	R	00h	N/A (Hard-coded)
	Reserved.			
Type	23:20	R	0h	N/A (Hard-coded)
	Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined			
Delay	19:16	R	Dh	N/A (Hard-coded)
	Number of sample delays through widget.			
Rsvd1	15:12	R	0h	N/A (Hard-coded)
	Reserved.			
SwapCap	11	R	1h	N/A (Hard-coded)
	Left/right swap support: 1 = yes, 0 = no.			
PwrCntrl	10	R	1h	N/A (Hard-coded)
	Power state support: 1 = yes, 0 = no.			
Dig	9	R	0h	N/A (Hard-coded)
	Digital stream support: 1 = yes (digital), 0 = no (analog).			
ConnList	8	R	0h	N/A (Hard-coded)
	Connection list present: 1 = yes, 0 = no.			

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Field Name	Bits	R/W	Default	Reset
UnSolCap	7	R	0h	N/A (Hard-coded)
	Unsolicited response support: 1 = yes, 0 = no.			
ProcWidget	6	R	0h	N/A (Hard-coded)
	Processing state support: 1 = yes, 0 = no.			
Stripe	5	R	0h	N/A (Hard-coded)
	Striping support: 1 = yes, 0 = no.			
FormatOvrd	4	R	0h	N/A (Hard-coded)
	Stream format override: 1 = yes, 0 = no.			
AmpParOvrd	3	R	0h	N/A (Hard-coded)
	Amplifier capabilities override: 1 = yes, no.			
OutAmpPrsnt	2	R	1h	N/A (Hard-coded)
	Output amp present: 1 = yes, 0 = no.			
InAmpPrsnt	1	R	0h	N/A (Hard-coded)
	Input amp present: 1 = yes, 0 = no.			
Stereo	0	R	1h	N/A (Hard-coded)
	Stereo stream support: 1 = yes (stereo), 0 = no (mono).			

7.25.1. DAC3 (NID = 18h): Cnvtr

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set			2h	
Get	A0000h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:16	R	0000h	N/A (Hard-coded)
	Reserved.			

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Field Name	Bits	R/W	Default	Reset
StrmType	15	R	0h	N/A (Hard-coded)
	Stream type: 1 = Non-PCM, 0 = PCM.			
FrmtSmplRate	14	RW	0h	POR - DAFG - ULR
	Sample base rate: 1 = 44.1kHz, 0 = 48kHz.			
SmplRateMultp	13:11	RW	0h	POR - DAFG - ULR
	Sample base rate multiple: 000b= x1 (48kHz/44.1kHz or less) 001b= x2 (96kHz/88.2kHz/32kHz) 010b= x3 (144kHz) 011b= x4 (192kHz/176.4kHz) 100b-111b Reserved			
SmplRateDiv	10:8	RW	0h	POR - DAFG - ULR
	Sample base rate divider: 000b= Divide by 1 (48kHz/44.1kHz) 001b= Divide by 2 (24kHz/20.05kHz) 010b= Divide by 3 (16kHz/32kHz) 011b= Divide by 4 (11.025kHz) 100b= Divide by 5 (9.6kHz) 101b= Divide by 6 (8kHz) 110b= Divide by 7 111b= Divide by 8 (6kHz)			
Rsvd1	7	R	0h	N/A (Hard-coded)
	Reserved.			
BitsPerSmpl	6:4	RW	3h	POR - DAFG - ULR
	Bits per sample: 000b= 8 bits 001b= 16 bits 010b= 20 bits 011b= 24 bits 100b= 32 bits 101b-111b= Reserved			
NmbrChan	3:0	RW	1h	POR - DAFG - ULR
	Total number of channels in the stream assigned to this converter: 0000b-1111b= 1-16 channels.			

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7.25.2. DAC3 (NID = 18h): OutAmpLeft

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				3A0h
Get	BA000h			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
Mute	7	RW	1h	POR - DAFG - ULR
	Amp mute: 1 = muted, 0 = not muted.			
Gain	6:0	RW	7Fh	POR - DAFG - ULR
	Amp gain step number (see OutAmpCap parameter pertaining to this widget).			

7.25.3. DAC3 (NID = 18h): OutAmpRight

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				390h
Get	B8000h			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
Mute	7	RW	1h	POR - DAFG - ULR
	Amp mute: 1 = muted, 0 = not muted.			
Gain	6:0	RW	7Fh	POR - DAFG - ULR
	Amp gain step number (see OutAmpCap parameter pertaining to this widget).			

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7.25.4. DAC3 (NID = 18h): PwrState

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				705h
Get	F0500h			

Field Name	Bits	R/W	Default	Reset
Rsvd4	31:11	R	000000h	N/A (Hard-coded)
	Reserved.			
SettingsReset	10	R	1h	POR - DAFG - ULR
	Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget.			
Rsvd3	9	R	0h	N/A (Hard-coded)
	Reserved.			
Error	8	R	0h	POR - DAFG - ULR
	Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state.			
Rsvd2	7:6	R	0h	N/A (Hard-coded)
	Reserved.			
Act	5:4	R	3h	POR - DAFG - LR
	Actual power state of this widget.			
Rsvd1	3:2	R	0h	N/A (Hard-coded)
	Reserved.			
Set	1:0	RW	3h	POR - DAFG - LR
	Current power state setting for this widget.			

7.25.5. DAC3 (NID = 18h): CnvtrID

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				706h

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7.25.5. DAC3 (NID = 18h): CnvtrID

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Get	F0600h			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
Strm	7:4	RW	0h	POR - S&DAFG - LR - PS
	Stream ID: 0h = Converter "off", 1h-Fh = valid ID's.			
Ch	3:0	RW	0h	POR - S&DAFG - LR - PS
	Channel assignment ("Ch" and "Ch+1" assigned as a pair, for a stereo converter).			

7.25.6. DAC3 (NID = 18h): EAPDBTLLR

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				70Ch
Get	F0C00h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:3	R	00000000h	N/A (Hard-coded)
	Reserved.			
SwapEn	2	RW	0h	POR - DAFG - ULR
	Swap enable: 1 = L/R swap enabled, 0 = L/R swap disabled.			
Rsvd1	1:0	R	0h	N/A (Hard-coded)
	Reserved.			

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7.20. DAC4 (NID = 19h): WCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0009h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:24	R	00h	N/A (Hard-coded)
	Reserved.			
Type	23:20	R	0h	N/A (Hard-coded)
	Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined			
Delay	19:16	R	Dh	N/A (Hard-coded)
	Number of sample delays through widget.			
Rsvd1	15:12	R	0h	N/A (Hard-coded)
	Reserved.			
SwapCap	11	R	1h	N/A (Hard-coded)
	Left/right swap support: 1 = yes, 0 = no.			
PwrCntrl	10	R	1h	N/A (Hard-coded)
	Power state support: 1 = yes, 0 = no.			
Dig	9	R	0h	N/A (Hard-coded)
	Digital stream support: 1 = yes (digital), 0 = no (analog).			
ConnList	8	R	0h	N/A (Hard-coded)
	Connection list present: 1 = yes, 0 = no.			

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Field Name	Bits	R/W	Default	Reset
UnSolCap	7	R	0h	N/A (Hard-coded)
	Unsolicited response support: 1 = yes, 0 = no.			
ProcWidget	6	R	0h	N/A (Hard-coded)
	Processing state support: 1 = yes, 0 = no.			
Stripe	5	R	0h	N/A (Hard-coded)
	Striping support: 1 = yes, 0 = no.			
FormatOvrd	4	R	0h	N/A (Hard-coded)
	Stream format override: 1 = yes, 0 = no.			
AmpParOvrd	3	R	0h	N/A (Hard-coded)
	Amplifier capabilities override: 1 = yes, no.			
OutAmpPrsnt	2	R	1h	N/A (Hard-coded)
	Output amp present: 1 = yes, 0 = no.			
InAmpPrsnt	1	R	0h	N/A (Hard-coded)
	Input amp present: 1 = yes, 0 = no.			
Stereo	0	R	1h	N/A (Hard-coded)
	Stereo stream support: 1 = yes (stereo), 0 = no (mono).			

7.20.1. DAC4 (NID = 19h): Cnvtr

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set			2h	
Get	A0000h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:16	R	0000h	N/A (Hard-coded)
	Reserved.			

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Field Name	Bits	R/W	Default	Reset
StrmType	15	R	0h	N/A (Hard-coded)
	Stream type: 1 = Non-PCM, 0 = PCM.			
FrmtSmplRate	14	RW	0h	POR - DAFG - ULR
	Sample base rate: 1 = 44.1kHz, 0 = 48kHz.			
SmplRateMultp	13:11	RW	0h	POR - DAFG - ULR
	Sample base rate multiple: 000b= x1 (48kHz/44.1kHz or less) 001b= x2 (96kHz/88.2kHz/32kHz) 010b= x3 (144kHz) 011b= x4 (192kHz/176.4kHz) 100b-111b Reserved			
SmplRateDiv	10:8	RW	0h	POR - DAFG - ULR
	Sample base rate divider: 000b= Divide by 1 (48kHz/44.1kHz) 001b= Divide by 2 (24kHz/20.05kHz) 010b= Divide by 3 (16kHz/32kHz) 011b= Divide by 4 (11.025kHz) 100b= Divide by 5 (9.6kHz) 101b= Divide by 6 (8kHz) 110b= Divide by 7 111b= Divide by 8 (6kHz)			
Rsvd1	7	R	0h	N/A (Hard-coded)
	Reserved.			
BitsPerSmpl	6:4	RW	3h	POR - DAFG - ULR
	Bits per sample: 000b= 8 bits 001b= 16 bits 010b= 20 bits 011b= 24 bits 100b= 32 bits 101b-111b= Reserved			
NmbrChan	3:0	RW	1h	POR - DAFG - ULR
	Total number of channels in the stream assigned to this converter: 0000b-1111b= 1-16 channels.			

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7.20.2. DAC4 (NID = 19h): OutAmpLeft

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				3A0h
Get	BA000h			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
Mute	7	RW	1h	POR - DAFG - ULR
	Amp mute: 1 = muted, 0 = not muted.			
Gain	6:0	RW	7Fh	POR - DAFG - ULR
	Amp gain step number (see OutAmpCap parameter pertaining to this widget).			

7.20.3. DAC4 (NID = 19h): OutAmpRight

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				390h
Get	B8000h			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
Mute	7	RW	1h	POR - DAFG - ULR
	Amp mute: 1 = muted, 0 = not muted.			
Gain	6:0	RW	7Fh	POR - DAFG - ULR
	Amp gain step number (see OutAmpCap parameter pertaining to this widget).			

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7.20.4. DAC4 (NID = 19h): PwrState

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				705h
Get	F0500h			

Field Name	Bits	R/W	Default	Reset
Rsvd4	31:11	R	000000h	N/A (Hard-coded)
	Reserved.			
SettingsReset	10	R	1h	POR - DAFG - ULR
	Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget.			
Rsvd3	9	R	0h	N/A (Hard-coded)
	Reserved.			
Error	8	R	0h	POR - DAFG - ULR
	Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state.			
Rsvd2	7:6	R	0h	N/A (Hard-coded)
	Reserved.			
Act	5:4	R	3h	POR - DAFG - LR
	Actual power state of this widget.			
Rsvd1	3:2	R	0h	N/A (Hard-coded)
	Reserved.			
Set	1:0	RW	3h	POR - DAFG - LR
	Current power state setting for this widget.			

7.20.5. DAC4 (NID = 19h): CnvtrID

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				706h

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7.20.5. DAC4 (NID = 19h): CnvtrID

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Get	F0600h			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
Strm	7:4	RW	0h	POR - S&DAFG - LR - PS
	Stream ID: 0h = Converter "off", 1h-Fh = valid ID's.			
Ch	3:0	RW	0h	POR - S&DAFG - LR - PS
	Channel assignment ("Ch" and "Ch+1" assigned as a pair, for a stereo converter).			

7.20.6. DAC4 (NID = 19h): EAPDBTLLR

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				70Ch
Get	F0C00h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:3	R	00000000h	N/A (Hard-coded)
	Reserved.			
SwapEn	2	RW	0h	POR - DAFG - ULR
	Swap enable: 1 = L/R swap enabled, 0 = L/R swap disabled.			
Rsvd1	1:0	R	0h	N/A (Hard-coded)
	Reserved.			

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7.27. ADC0Mux (NID = 20h): WCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0009h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:24	R	00h	N/A (Hard-coded)
	Reserved.			
Type	23:20	R	3h	N/A (Hard-coded)
	Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined			
Delay	19:16	R	0h	N/A (Hard-coded)
	Number of sample delays through widget.			
Rsvd1	15:12	R	0h	N/A (Hard-coded)
	Reserved.			
SwapCap	11	R	1h	N/A (Hard-coded)
	Left/right swap support: 1 = yes, 0 = no.			
PwrCntrl	10	R	1h	N/A (Hard-coded)
	Power state support: 1 = yes, 0 = no.			
DigitalStrm	9	R	0h	N/A (Hard-coded)
	Digital stream support: 1 = yes (digital), 0 = no (analog).			
ConnList	8	R	1h	N/A (Hard-coded)
	Connection list present: 1 = yes, 0 = no.			

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Field Name	Bits	R/W	Default	Reset
UnsolCap	7	R	0h	N/A (Hard-coded)
	Unsolicited response support: 1 = yes, 0 = no.			
ProcWidget	6	R	0h	N/A (Hard-coded)
	Processing state support: 1 = yes, 0 = no.			
Stripe	5	R	0h	N/A (Hard-coded)
	Striping support: 1 = yes, 0 = no.			
FormatOvrd	4	R	0h	N/A (Hard-coded)
	Stream format override: 1 = yes, 0 = no.			
AmpParamOvrd	3	R	1h	N/A (Hard-coded)
	Amplifier capabilities override: 1 = yes, no.			
OutAmpPrsnt	2	R	1h	N/A (Hard-coded)
	Output amp present: 1 = yes, 0 = no.			
InAmpPrsnt	1	R	0h	N/A (Hard-coded)
	Input amp present: 1 = yes, 0 = no.			
Stereo	0	R	1h	N/A (Hard-coded)
	Stereo stream support: 1 = yes (stereo), 0 = no (mono).			

7.27.1. ADC0Mux (NID = 20h): ConLst

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Eh			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			

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Field Name	Bits	R/W	Default	Reset
LForm	7	R	0h	N/A (Hard-coded)
	Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries.			
ConL	6:0	R	04h in 40QFN 06h in 48QFN	N/A (Hard-coded)
	Number of NID entries in connection list.			

7.27.2. ADC0Mux (NID = 17h): ConLstEntry4

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0204h			

Field Name	Bits	R/W	Default	Reset
ConL7	31:24	R	00h	N/A (Hard-coded)
	Unused list entry.			
ConL6	23:16	R	00h	N/A (Hard-coded)
	Unused list entry.			
ConL5	15:8	R	00h in 40QFN 14h in 48QFN	N/A (Hard-coded)
	DMic1 Pin widget (0x14) for QFN48, reserved for QFN40.			
ConL4	7:0	R	00h in 40QFN 13h in 48QFN	N/A (Hard-coded)
	DMic0 Pin widget (0x13) for QFN48, reserved for QFN40.			

7.27.3. ADC0Mux (NID = 20h): ConLstEntry0

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0200h			

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Field Name	Bits	R/W	Default	Reset
ConL3	31:24	R	12h	N/A (Hard-coded)
	CD Pin widget (0x12)			
ConL2Range	23	R	1h	N/A (Hard-coded)
	ConL1 .. ConL2 define a selectalbe range input			
ConL2	22:16	R	11h	N/A (Hard-coded)
	Port H Pin widget (0x10)			
ConL1	15:8	R	0Ah	N/A (Hard-coded)
	Port A Pin widget (0x0A)			
ConL0	7:0	R	1Dh	N/A (Hard-coded)
	Mixer Summing widget (0x1D			

7.27.4. ADC0Mux (NID = 20h): OutAmpCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0012h			

Field Name	Bits	R/W	Default	Reset
Mute	31	R	1h	N/A (Hard-coded)
	Mute support: 1 = yes, 0 = no.			
Rsvd3	30:23	R	00h	N/A (Hard-coded)
	Reserved.			
StepSize	22:16	R	05h	N/A (Hard-coded)
	Size of each step in the gain range: 0 to 127 = .25dB to 32dB, in .25dB steps.			
Rsvd2	15	R	0h	N/A (Hard-coded)
	Reserved.			

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Field Name	Bits	R/W	Default	Reset
NumSteps	14:8	R	0Fh	N/A (Hard-coded)
	Number of gains steps (number of possible settings - 1).			
Rsvd1	7	R	0h	N/A (Hard-coded)
	Reserved.			
Offset	6:0	R	00h	N/A (Hard-coded)
	Indicates which step is 0dB			

7.27.5. ADC0Mux (NID = 20h): OutAmpLeft

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				3A0h
Get	BA000h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
Mute	7	RW	1h	POR - DAFG - ULR
	Amp mute: 1 = muted, 0 = not muted.			
Rsvd1	6:4	R	0h	N/A (Hard-coded)
	Reserved.			
Gain	3:0	RW	0h	POR - DAFG - ULR
	Amp gain step number (see OutAmpCap parameter pertaining to this widget).			

7.27.6. ADC0Mux (NID = 20h): OutAmpRight

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				390h
Get	B8000h			

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Field Name	Bits	R/W	Default	Reset
Rsvd2	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
Mute	7	RW	1h	POR - DAFG - ULR
	Amp mute: 1 = muted, 0 = not muted.			
Rsvd1	6:4	R	0h	N/A (Hard-coded)
	Reserved.			
Gain	3:0	RW	0h	POR - DAFG - ULR
	Amp gain step number (see OutAmpCap parameter pertaining to this widget).			

7.27.7. ADC0Mux (NID = 20h): ConSelectCtrl

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				701h
Get	F0100h			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:3	R	00000000h	N/A (Hard-coded)
	Reserved.			
Index	2:0	RW	0h	POR - DAFG - ULR
	Connection select control index.			

7.27.8. ADC0Mux (NID = 20h): PwrState

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				705h
Get	F0500h			

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Field Name	Bits	R/W	Default	Reset
Rsvd4	31:11	R	000000h	N/A (Hard-coded)
	Reserved.			
SettingsReset	10	R	1h	POR - DAFG - ULR
	Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget.			
Rsvd3	9	R	0h	N/A (Hard-coded)
	Reserved.			
Error	8	R	0h	POR - DAFG - ULR
	Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state.			
Rsvd2	7:6	R	0h	N/A (Hard-coded)
	Reserved.			
Act	5:4	R	3h	POR - DAFG - LR
	Actual power state of this widget.			
Rsvd1	3:2	R	0h	N/A (Hard-coded)
	Reserved.			
Set	1:0	RW	0h	POR - DAFG - LR
	Current power state setting for this widget.			

7.27.9. ADC0Mux (NID = 20h): EAPDBTLLR

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				70Ch
Get	F0C00h			

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Field Name	Bits	R/W	Default	Reset
Rsvd2	31:3	R	00000000h	N/A (Hard-coded)
	Reserved.			
SwapEn	2	RW	0h	POR - DAFG - ULR
	Swap enable: 1 = L/R swap enabled, 0 = L/R swap disabled.			
Rsvd1	1:0	R	0h	N/A (Hard-coded)
	Reserved.			

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7.28. ADC1Mux (NID = 21h): WCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0009h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:24	R	00h	N/A (Hard-coded)
	Reserved.			
Type	23:20	R	3h	N/A (Hard-coded)
	Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined			
Delay	19:16	R	0h	N/A (Hard-coded)
	Number of sample delays through widget.			
Rsvd1	15:12	R	0h	N/A (Hard-coded)
	Reserved.			
SwapCap	11	R	1h	N/A (Hard-coded)
	Left/right swap support: 1 = yes, 0 = no.			
PwrCntrl	10	R	1h	N/A (Hard-coded)
	Power state support: 1 = yes, 0 = no.			
DigitalStrm	9	R	0h	N/A (Hard-coded)
	Digital stream support: 1 = yes (digital), 0 = no (analog).			
ConnList	8	R	1h	N/A (Hard-coded)
	Connection list present: 1 = yes, 0 = no.			

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Field Name	Bits	R/W	Default	Reset
UnsolCap	7	R	0h	N/A (Hard-coded)
	Unsolicited response support: 1 = yes, 0 = no.			
ProcWidget	6	R	0h	N/A (Hard-coded)
	Processing state support: 1 = yes, 0 = no.			
Stripe	5	R	0h	N/A (Hard-coded)
	Striping support: 1 = yes, 0 = no.			
FormatOvrd	4	R	0h	N/A (Hard-coded)
	Stream format override: 1 = yes, 0 = no.			
AmpParamOvrd	3	R	1h	N/A (Hard-coded)
	Amplifier capabilities override: 1 = yes, no.			
OutAmpPrsnt	2	R	1h	N/A (Hard-coded)
	Output amp present: 1 = yes, 0 = no.			
InAmpPrsnt	1	R	0h	N/A (Hard-coded)
	Input amp present: 1 = yes, 0 = no.			
Stereo	0	R	1h	N/A (Hard-coded)
	Stereo stream support: 1 = yes (stereo), 0 = no (mono).			

7.28.1. ADC1Mux (NID = 21h): ConLst

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Eh			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			

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Field Name	Bits	R/W	Default	Reset
LForm	7	R	0h	N/A (Hard-coded)
	Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries.			
ConL	6:0	R	05h	N/A (Hard-coded)
	Number of NID entries in connection list.			

7.28.2. ADC1Mux (NID = 21h): ConLstEntry4

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0204h			

Field Name	Bits	R/W	Default	Reset
ConL7	31:24	R	00h	N/A (Hard-coded)
	Unused list entry.			
ConL6	23:16	R	00h	N/A (Hard-coded)
	Unused list entry			
ConL5	15:8	R	00h in 40QFN 14h in 48QFN	N/A (Hard-coded)
	DMic1 Pin widget (0x14) for QFN48, reserved for QFN40			
ConL4	7:0	R	00h in 40QFN 13h in 48QFN	N/A (Hard-coded)
	DMic0 Pin widget (0x13) for QFN48, reserved for QFN40			

7.28.3. ADC1Mux (NID = 21h): ConLstEntry0

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0200h			

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Field Name	Bits	R/W	Default	Reset
ConL3	31:24	R	1Bh	N/A (Hard-coded)
	Mixer Summing widget (0x1B)			
ConL2Range	23	R	1h	N/A (Hard-coded)
	ConL1 .. ConL2 define a selectalbe range input			
ConL2	22:16	R	11h	N/A (Hard-coded)
	Port H Pin widget (0x10)			
ConL1	15:8	R	0Ah	N/A (Hard-coded)
	Port A Pin widget (0x0A)			
ConL0	7:0	R	1Dh	N/A (Hard-coded)
	Mixer Summing widget (0x0D)			

7.28.4. ADC1Mux (NID = 21h): OutAmpCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0012h			

Field Name	Bits	R/W	Default	Reset
Mute	31	R	1h	N/A (Hard-coded)
	Mute support: 1 = yes, 0 = no.			
Rsvd3	30:23	R	00h	N/A (Hard-coded)
	Reserved.			
StepSize	22:16	R	05h	N/A (Hard-coded)
	Size of each step in the gain range: 0 to 127 = .25dB to 32dB, in .25dB steps.			
Rsvd2	15	R	0h	N/A (Hard-coded)
	Reserved.			

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Field Name	Bits	R/W	Default	Reset
NumSteps	14:8	R	0Fh	N/A (Hard-coded)
	Number of gains steps (number of possible settings - 1).			
Rsvd1	7	R	0h	N/A (Hard-coded)
	Reserved.			
Offset	6:0	R	00h	N/A (Hard-coded)
	Indicates which step is 0dB			

7.28.5. ADC1Mux (NID = 21h): OutAmpLeft

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				3A0h
Get	BA000h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
Mute	7	RW	1h	POR - DAFG - ULR
	Amp mute: 1 = muted, 0 = not muted.			
Rsvd1	6:4	R	0h	N/A (Hard-coded)
	Reserved.			
Gain	3:0	RW	0h	POR - DAFG - ULR
	Amp gain step number (see OutAmpCap parameter pertaining to this widget).			

7.28.6. ADC1Mux (NID = 21h): OutAmpRight

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				390h
Get	B8000h			

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Field Name	Bits	R/W	Default	Reset
Rsvd2	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
Mute	7	RW	1h	POR - DAFG - ULR
	Amp mute: 1 = muted, 0 = not muted.			
Rsvd1	6:4	R	0h	N/A (Hard-coded)
	Reserved.			
Gain	3:0	RW	0h	POR - DAFG - ULR
	Amp gain step number (see OutAmpCap parameter pertaining to this widget).			

7.28.7. ADC1Mux (NID = 21h): ConSelectCtrl

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				701h
Get	F0100h			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:3	R	00000000h	N/A (Hard-coded)
	Reserved.			
Index	2:0	RW	0h	POR - DAFG - ULR
	Connection select control index.			

7.28.8. ADC1Mux (NID = 21h): PwrState

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				705h
Get	F0500h			

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Field Name	Bits	R/W	Default	Reset
Rsvd4	31:11	R	000000h	N/A (Hard-coded)
	Reserved.			
SettingsReset	10	R	1h	POR - DAFG - ULR
	Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget.			
Rsvd3	9	R	0h	N/A (Hard-coded)
	Reserved.			
Error	8	R	0h	POR - DAFG - ULR
	Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state.			
Rsvd2	7:6	R	0h	N/A (Hard-coded)
	Reserved.			
Act	5:4	R	3h	POR - DAFG - LR
	Actual power state of this widget.			
Rsvd1	3:2	R	0h	N/A (Hard-coded)
	Reserved.			
Set	1:0	RW	0h	POR - DAFG - LR
	Current power state setting for this widget.			

7.28.9. ADC1Mux (NID = 21h): EAPDBTLLR

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				70Ch
Get	F0C00h			

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Field Name	Bits	R/W	Default	Reset
Rsvd2	31:3	R	00000000h	N/A (Hard-coded)
	Reserved.			
SwapEn	2	RW	0h	POR - DAFG - ULR
	Swap enable: 1 = L/R swap enabled, 0 = L/R swap disabled.			
Rsvd1	1:0	R	0h	N/A (Hard-coded)
	Reserved.			

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7.29. Dig0Pin (NID = 22h): WCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0009h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:24	R	00h	N/A (Hard-coded)
	Reserved.			
Type	23:20	R	4h	N/A (Hard-coded)
	Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined			
Delay	19:16	R	0h	N/A (Hard-coded)
	Number of sample delays through widget.			
Rsvd1	15:12	R	0h	N/A (Hard-coded)
	Reserved.			
SwapCap	11	R	0h	N/A (Hard-coded)
	Left/right swap support: 1 = yes, 0 = no.			
PwrCntrl	10	R	1h	N/A (Hard-coded)
	Power state support: 1 = yes, 0 = no.			
Dig	9	R	1h	N/A (Hard-coded)
	Digital stream support: 1 = yes (digital), 0 = no (analog).			
ConnList	8	R	1h	N/A (Hard-coded)
	Connection list present: 1 = yes, 0 = no.			

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Field Name	Bits	R/W	Default	Reset
UnSolCap	7	R	1h	N/A (Hard-coded)
	Unsolicited response support: 1 = yes, 0 = no.			
ProcWidget	6	R	0h	N/A (Hard-coded)
	Processing state support: 1 = yes, 0 = no.			
Stripe	5	R	0h	N/A (Hard-coded)
	Striping support: 1 = yes, 0 = no.			
FormatOvrd	4	R	0h	N/A (Hard-coded)
	Stream format override: 1 = yes, 0 = no.			
AmpParOvrd	3	R	0h	N/A (Hard-coded)
	Amplifier capabilities override: 1 = yes, no.			
OutAmpPrsnt	2	R	0h	N/A (Hard-coded)
	Output amp present: 1 = yes, 0 = no.			
InAmpPrsnt	1	R	0h	N/A (Hard-coded)
	Input amp present: 1 = yes, 0 = no.			
Stereo	0	R	1h	N/A (Hard-coded)
	Stereo stream support: 1 = yes (stereo), 0 = no (mono).			

7.29.1. Dig0Pin (NID = 22h): PinCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Ch			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:17	R	0000h	N/A (Hard-coded)
	Reserved.			

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Field Name	Bits	R/W	Default	Reset
EapdCap	16	R	0h	N/A (Hard-coded)
	EAPD support: 1 = yes, 0 = no.			
VrefCntrl	15:8	R	00h	N/A (Hard-coded)
	Vref support: bit 7 = Reserved bit 6 = Reserved bit 5 = 100% support (1 = yes, 0 = no) bit 4 = 80% support (1 = yes, 0 = no) bit 3 = Reserved bit 2 = GND support (1 = yes, 0 = no) bit 1 = 50% support (1 = yes, 0 = no) bit 0 = Hi-Z support (1 = yes, 0 = no)			
Rsvd1	7	R	0h	N/A (Hard-coded)
	Reserved.			
BalancedIO	6	R	0h	N/A (Hard-coded)
	Balanced I/O support: 1 = yes, 0 = no.			
InCap	5	R	0h	N/A (Hard-coded)
	Input support: 1 = yes, 0 = no.			
OutCap	4	R	1h	N/A (Hard-coded)
	Output support: 1 = yes, 0 = no.			
HdphDrvCap	3	R	0h	N/A (Hard-coded)
	Headphone amp present: 1 = yes, 0 = no.			
PresDtctCap	2	R	1h	N/A (Hard-coded)
	Presence detection support: 1 = yes, 0 = no.			
TrigRqd	1	R	0h	N/A (Hard-coded)
	Trigger required for impedance sense: 1 = yes, 0 = no.			
ImpSenseCap	0	R	0h	N/A (Hard-coded)
	Impedance sense support: 1 = yes, 0 = no.			

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7.29.2. Dig0Pin (NID = 22h): ConLst

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Eh			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
LForm	7	R	0h	N/A (Hard-coded)
	Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries.			
ConL	6:0	R	01h	N/A (Hard-coded)
	Number of NID entries in connection list.			

7.29.3. Dig0Pin (NID = 22h): ConLstEntry0

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0200h			

Field Name	Bits	R/W	Default	Reset
ConL3	31:24	R	00h	N/A (Hard-coded)
	Unused list entry.			
ConL2	23:16	R	00h	N/A (Hard-coded)
	Unused list entry.			
ConL1	15:8	R	00h	N/A (Hard-coded)
	Unused list entry.			

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Field Name	Bits	R/W	Default	Reset
ConL0	7:0	R	25h	N/A (Hard-coded)
	SPDIFOut0 Converter widget (0x25)			

7.29.4. Dig0Pin (NID = 22h): PwrState

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				705h
Get	F0500h			

Field Name	Bits	R/W	Default	Reset
Rsvd4	31:11	R	000000h	N/A (Hard-coded)
	Reserved.			
SettingsReset	10	R	1h	POR - DAFG - ULR
	Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget.			
Rsvd3	9	R	0h	N/A (Hard-coded)
	Reserved.			
Error	8	R	0h	POR - DAFG - ULR
	Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state.			
Rsvd2	7:6	R	0h	N/A (Hard-coded)
	Reserved.			
Act	5:4	R	3h	POR - DAFG - LR
	Actual power state of this widget.			
Rsvd1	3:2	R	0h	N/A (Hard-coded)
	Reserved.			
Set	1:0	RW	0h	POR - DAFG - LR
	Current power state setting for this widget.			

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7.29.5. Dig0Pin (NID = 22h): PinWCntrl

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				707h
Get	F0700h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:7	R	0000000h	N/A (Hard-coded)
	Reserved.			
OutEn	6	RW	0h	POR - DAFG - ULR
	Output enable: 1 = enabled, 0 = disabled.			
Rsvd1	5:0	R	00h	N/A (Hard-coded)
	Reserved.			

7.29.6. Dig0Pin (NID = 22h): UnsolResp

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				708h
Get	F0800h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
En	7	RW	0h	POR - DAFG - ULR
	Unsolicited response enable (also enables Wake events for this Widget): 1 = enabled, 0 = disabled.			
Rsvd1	6	R	0h	N/A (Hard-coded)
	Reserved.			

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Field Name	Bits	R/W	Default	Reset
Tag	5:0	RW	00h	POR - DAFG - ULR
	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.			

7.29.7. Dig0Pin (NID = 22h): ChSense

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				709h
Get	F0900h			

Field Name	Bits	R/W	Default	Reset
PresDtct	31	R	0h	POR
	Presence detection indicator: 1 = presence detected; 0 = presence not detected.			
Rsvd	30:0	R	00000000h	N/A (Hard-coded)
	Reserved.			

7.29.8. Dig0Pin (NID = 22h): ConfigDefault

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set	71Fh	71Eh	71Dh	71Ch
Get	F1F00h / F1E00h / F1D00h / F1C00h			

Field Name	Bits	R/W	Default	Reset
PortConnectivity	31:30	RW	0h	POR
	Port connectivity: 0h = Port complex is connected to a jack 1h = No physical connection for port 2h = Fixed function device is attached 3h = Both jack and internal device attached (info in all other fields refers to integrated device, any presence detection refers to jack)			

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Field Name	Bits	R/W	Default	Reset
Location	29:24	RW	1h	POR
	Location Bits [5..4]: 0h = External on primary chassis 1h = Internal 2h = Separate chassis 3h = Other Bits [3..0]: 0h = N/A 1h = Rear 2h = Front 3h = Left 4h = Right 5h = Top 6h = Bottom 7h-9h = Special Ah-Fh = Reserved			
Device	23:20	RW	4h	POR
	Default device: 0h = Line out 1h = Speaker 2h = HP out 3h = CD 4h = SPDIF Out 5h = Digital other out 6h = Modem line side 7h = Modem handset side 8h = Line in 9h = Aux Ah = Mic in Bh = Telephony Ch = SPDIF In Dh = Digital other in Eh = Reserved Fh = Other			

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Field Name	Bits	R/W	Default	Reset
ConnectionType	19:16	RW	5h	POR
	Connection type: 0h = Unknown 1h = 1/8" stereo/mono 2h = 1/4" stereo/mono 3h = ATAPI internal 4h = RCA 5h = Optical 6h = Other digital 7h = Other analog 8h = Multichannel analog (DIN) 9h = XLR/Professional Ah = RJ-11 (modem) Bh = Combination Ch-Eh = Reserved Fh = Other			
Color	15:12	RW	1h	POR
	Color: 0h = Unknown 1h = Black 2h = Grey 3h = Blue 4h = Green 5h = Red 6h = Orange 7h = Yellow 8h = Purple 9h = Pink Ah-Dh = Reserved Eh = White Fh = Other			
Misc	11:8	RW	1h	POR
	Miscellaneous: Bits [3..1] = Reserved Bit 0 = Jack detect override			
Association	7:4	RW	5h	POR
	Default assocation.			
Sequence	3:0	RW	0h	POR
	Sequence.			

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7.30. Dig1Pin (NID = 23h): WCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0009h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:24	R	00h	N/A (Hard-coded)
	Reserved.			
Type	23:20	R	4h	N/A (Hard-coded)
	Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined			
Delay	19:16	R	0h	N/A (Hard-coded)
	Number of sample delays through widget.			
Rsvd1	15:12	R	0h	N/A (Hard-coded)
	Reserved.			
SwapCap	11	R	0h	N/A (Hard-coded)
	Left/right swap support: 1 = yes, 0 = no.			
PwrCntrl	10	R	1h	N/A (Hard-coded)
	Power state support: 1 = yes, 0 = no.			
Dig	9	R	1h	N/A (Hard-coded)
	Digital stream support: 1 = yes (digital), 0 = no (analog).			
ConnList	8	R	1h	N/A (Hard-coded)
	Connection list present: 1 = yes, 0 = no.			

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Field Name	Bits	R/W	Default	Reset
UnSolCap	7	R	1h	N/A (Hard-coded)
	Unsolicited response support: 1 = yes, 0 = no.			
ProcWidget	6	R	0h	N/A (Hard-coded)
	Processing state support: 1 = yes, 0 = no.			
Stripe	5	R	0h	N/A (Hard-coded)
	Striping support: 1 = yes, 0 = no.			
FormatOvrd	4	R	0h	N/A (Hard-coded)
	Stream format override: 1 = yes, 0 = no.			
AmpParOvrd	3	R	0h	N/A (Hard-coded)
	Amplifier capabilities override: 1 = yes, no.			
OutAmpPrsnt	2	R	0h	N/A (Hard-coded)
	Output amp present: 1 = yes, 0 = no.			
InAmpPrsnt	1	R	0h	N/A (Hard-coded)
	Input amp present: 1 = yes, 0 = no.			
Stereo	0	R	1h	N/A (Hard-coded)
	Stereo stream support: 1 = yes (stereo), 0 = no (mono).			

7.30.1. Dig1Pin (NID = 23h): PinCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Ch			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:17	R	0000h	N/A (Hard-coded)
	Reserved.			

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Field Name	Bits	R/W	Default	Reset
EapdCap	16	R	0h	N/A (Hard-coded)
	EAPD support: 1 = yes, 0 = no.			
VrefCntrl	15:8	R	00h	N/A (Hard-coded)
	Vref support: bit 7 = Reserved bit 6 = Reserved bit 5 = 100% support (1 = yes, 0 = no) bit 4 = 80% support (1 = yes, 0 = no) bit 3 = Reserved bit 2 = GND support (1 = yes, 0 = no) bit 1 = 50% support (1 = yes, 0 = no) bit 0 = Hi-Z support (1 = yes, 0 = no)			
Rsvd1	7	R	0h	N/A (Hard-coded)
	Reserved.			
BalancedIO	6	R	0h	N/A (Hard-coded)
	Balanced I/O support: 1 = yes, 0 = no.			
InCap	5	R	1h	N/A (Hard-coded)
	Input support: 1 = yes, 0 = no.			
OutCap	4	R	1h	N/A (Hard-coded)
	Output support: 1 = yes, 0 = no.			
HdphDrvCap	3	R	0h	N/A (Hard-coded)
	Headphone amp present: 1 = yes, 0 = no.			
PresDtctCap	2	R	1h	N/A (Hard-coded)
	Presence detection support: 1 = yes, 0 = no.			
TrigRqd	1	R	0h	N/A (Hard-coded)
	Trigger required for impedance sense: 1 = yes, 0 = no.			
ImpSenseCap	0	R	0h	N/A (Hard-coded)
	Impedance sense support: 1 = yes, 0 = no.			

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7.30.2. Dig1Pin (NID = 23h): ConLst

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Eh			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
LForm	7	R	0h	N/A (Hard-coded)
	Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries.			
ConL	6:0	R	01h	N/A (Hard-coded)
	Number of NID entries in connection list.			

7.30.3. Dig1Pin (NID = 20h): ConLstEntry0

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0200h			

Field Name	Bits	R/W	Default	Reset
ConL3	31:24	R	00h	N/A (Hard-coded)
	Unused list entry.			
ConL2	23:16	R	00h	N/A (Hard-coded)
	Unused list entry.			
ConL1	15:8	R	00h	N/A (Hard-coded)
	Unused list entry.			

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Field Name	Bits	R/W	Default	Reset
ConL0	7:0	R	26h	N/A (Hard-coded)
	SPDIFOut1 Converter widget (0x26)			

7.30.4. Dig1Pin (NID = 23h): PwrState

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				705h
Get	F0500h			

Field Name	Bits	R/W	Default	Reset
Rsvd4	31:11	R	000000h	N/A (Hard-coded)
	Reserved.			
SettingsReset	10	R	1h	POR - DAFG - ULR
	Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget.			
Rsvd3	9	R	0h	N/A (Hard-coded)
	Reserved.			
Error	8	R	0h	POR - DAFG - ULR
	Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state.			
Rsvd2	7:6	R	0h	N/A (Hard-coded)
	Reserved.			
Act	5:4	R	3h	POR - DAFG - LR
	Actual power state of this widget.			
Rsvd1	3:2	R	0h	N/A (Hard-coded)
	Reserved.			
Set	1:0	RW	0h	POR - DAFG - LR
	Current power state setting for this widget.			

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7.30.5. Dig1Pin (NID = 23h): PinWCntrl

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				707h
Get	F0700h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:7	R	0000000h	N/A (Hard-coded)
	Reserved.			
OutEn	6	RW	0h	POR - DAFG - ULR
	Output enable: 1 = enabled, 0 = disabled.			
InEn	5	RW	0h	POR - DAFG - ULR
	Input enable: 1 = enabled, 0 = disabled.			
Rsvd1	4:0	R	00h	N/A (Hard-coded)
	Reserved.			

7.30.6. Dig1Pin (NID = 20h): ConfigDefault

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set	71Fh	71Eh	71Dh	71Ch
Get	F1F00h / F1E00h / F1D00h / F1C00h			

Field Name	Bits	R/W	Default	Reset
PortConnectivity	31:30	RW	2h	POR
	Port connectivity: 0h = Port complex is connected to a jack 1h = No physical connection for port 2h = Fixed function device is attached 3h = Both jack and internal device attached (info in all other fields refers to integrated device, any presence detection refers to jack)			

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Field Name	Bits	R/W	Default	Reset
Location	29:24	RW	18h	POR
	Location Bits [5..4]: 0h = External on primary chassis 1h = Internal 2h = Separate chassis 3h = Other Bits [3..0]: 0h = N/A 1h = Rear 2h = Front 3h = Left 4h = Right 5h = Top 6h = Bottom 7h-9h = Special Ah-Fh = Reserved			
Device	23:20	RW	5h	POR
	Default device: 0h = Line out 1h = Speaker 2h = HP out 3h = CD 4h = SPDIF Out 5h = Digital other out 6h = Modem line side 7h = Modem handset side 8h = Line in 9h = Aux Ah = Mic in Bh = Telephony Ch = SPDIF In Dh = Digital other in Eh = Reserved Fh = Other			

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Field Name	Bits	R/W	Default	Reset
ConnectionType	19:16	RW	6h	POR
	Connection type: 0h = Unknown 1h = 1/8" stereo/mono 2h = 1/4" stereo/mono 3h = ATAPI internal 4h = RCA 5h = Optical 6h = Other digital 7h = Other analog 8h = Multichannel analog (DIN) 9h = XLR/Professional Ah = RJ-11 (modem) Bh = Combination Ch-Eh = Reserved Fh = Other			
Color	15:12	RW	0h	POR
	Color: 0h = Unknown 1h = Black 2h = Grey 3h = Blue 4h = Green 5h = Red 6h = Orange 7h = Yellow 8h = Purple 9h = Pink Ah-Dh = Reserved Eh = White Fh = Other			
Misc	11:8	RW	1h	POR
	Miscellaneous: Bits [3..1] = Reserved Bit 0 = Jack detect override			
Association	7:4	RW	6h	POR
	Default assocation.			
Sequence	3:0	RW	0h	POR
	Sequence.			

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7.31. Dig2Pin (NID = 24h): WCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0009h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:24	R	00h	N/A (Hard-coded)
	Reserved.			
Type	23:20	R	4h	N/A (Hard-coded)
	Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined			
Delay	19:16	R	0h	N/A (Hard-coded)
	Number of sample delays through widget.			
Rsvd1	15:12	R	0h	N/A (Hard-coded)
	Reserved.			
SwapCap	11	R	0h	N/A (Hard-coded)
	Left/right swap support: 1 = yes, 0 = no.			
PwrCntrl	10	R	1h	N/A (Hard-coded)
	Power state support: 1 = yes, 0 = no.			
Dig	9	R	1h	N/A (Hard-coded)
	Digital stream support: 1 = yes (digital), 0 = no (analog).			
ConnList	8	R	1h	N/A (Hard-coded)
	Connection list present: 1 = yes, 0 = no.			

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Field Name	Bits	R/W	Default	Reset
UnSolCap	7	R	1h	N/A (Hard-coded)
	Unsolicited response support: 1 = yes, 0 = no.			
ProcWidget	6	R	0h	N/A (Hard-coded)
	Processing state support: 1 = yes, 0 = no.			
Stripe	5	R	0h	N/A (Hard-coded)
	Striping support: 1 = yes, 0 = no.			
FormatOvrd	4	R	0h	N/A (Hard-coded)
	Stream format override: 1 = yes, 0 = no.			
AmpParOvrd	3	R	0h	N/A (Hard-coded)
	Amplifier capabilities override: 1 = yes, no.			
OutAmpPrsnt	2	R	0h	N/A (Hard-coded)
	Output amp present: 1 = yes, 0 = no.			
InAmpPrsnt	1	R	0h	N/A (Hard-coded)
	Input amp present: 1 = yes, 0 = no.			
Stereo	0	R	1h	N/A (Hard-coded)
	Stereo stream support: 1 = yes (stereo), 0 = no (mono).			

7.31.1. Dig2Pin (NID = 24h): PinCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Ch			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:17	R	0000h	N/A (Hard-coded)
	Reserved.			

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Field Name	Bits	R/W	Default	Reset
EapdCap	16	R	0h	N/A (Hard-coded)
	EAPD support: 1 = yes, 0 = no.			
VrefCntrl	15:8	R	00h	N/A (Hard-coded)
	Vref support: bit 7 = Reserved bit 6 = Reserved bit 5 = 100% support (1 = yes, 0 = no) bit 4 = 80% support (1 = yes, 0 = no) bit 3 = Reserved bit 2 = GND support (1 = yes, 0 = no) bit 1 = 50% support (1 = yes, 0 = no) bit 0 = Hi-Z support (1 = yes, 0 = no)			
Rsvd1	7	R	0h	N/A (Hard-coded)
	Reserved.			
BalancedIO	6	R	0h	N/A (Hard-coded)
	Balanced I/O support: 1 = yes, 0 = no.			
InCap	5	R	1h	N/A (Hard-coded)
	Input support: 1 = yes, 0 = no.			
OutCap	4	R	1h	N/A (Hard-coded)
	Output support: 1 = yes, 0 = no.			
HdphDrvCap	3	R	0h	N/A (Hard-coded)
	Headphone amp present: 1 = yes, 0 = no.			
PresDtctCap	2	R	1h	N/A (Hard-coded)
	Presence detection support: 1 = yes, 0 = no.			
TrigRqd	1	R	0h	N/A (Hard-coded)
	Trigger required for impedance sense: 1 = yes, 0 = no.			
ImpSenseCap	0	R	0h	N/A (Hard-coded)
	Impedance sense support: 1 = yes, 0 = no.			

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7.31.2. Dig2Pin (NID = 24h): ConLst

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Eh			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
LForm	7	R	0h	N/A (Hard-coded)
	Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries.			
ConL	6:0	R	01h	N/A (Hard-coded)
	Number of NID entries in connection list.			

7.31.3. Dig1Pin (NID = 20h): ConLstEntry0

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0200h			

Field Name	Bits	R/W	Default	Reset
ConL3	31:24	R	00h	N/A (Hard-coded)
	Unused list entry.			
ConL2	23:16	R	00h	N/A (Hard-coded)
	Unused list entry.			
ConL1	15:8	R	00h	N/A (Hard-coded)
	Unused list entry.			

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Field Name	Bits	R/W	Default	Reset
ConL0	7:0	R	26h	N/A (Hard-coded)
	SPDIFOut1 Converter widget (0x26)			

7.31.4. Dig2Pin (NID = 24h): PwrState

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				705h
Get	F0500h			

Field Name	Bits	R/W	Default	Reset
Rsvd4	31:11	R	000000h	N/A (Hard-coded)
	Reserved.			
SettingsReset	10	R	1h	POR - DAFG - ULR
	Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget.			
Rsvd3	9	R	0h	N/A (Hard-coded)
	Reserved.			
Error	8	R	0h	POR - DAFG - ULR
	Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state.			
Rsvd2	7:6	R	0h	N/A (Hard-coded)
	Reserved.			
Act	5:4	R	3h	POR - DAFG - LR
	Actual power state of this widget.			
Rsvd1	3:2	R	0h	N/A (Hard-coded)
	Reserved.			
Set	1:0	RW	0h	POR - DAFG - LR
	Current power state setting for this widget.			

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7.31.5. Dig2Pin (NID = 24h): PinWCntrl

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				707h
Get	F0700h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:7	R	0000000h	N/A (Hard-coded)
	Reserved.			
OutEn	6	RW	0h	POR - DAFG - ULR
	Output enable: 1 = enabled, 0 = disabled.			
InEn	5	RW	0h	POR - DAFG - ULR
	Input enable: 1 = enabled, 0 = disabled.			
Rsvd1	4:0	R	00h	N/A (Hard-coded)
	Reserved.			

7.31.6. Dig1Pin (NID = 20h): ConfigDefault

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set	71Fh	71Eh	71Dh	71Ch
Get	F1F00h / F1E00h / F1D00h / F1C00h			

Field Name	Bits	R/W	Default	Reset
PortConnectivity	31:30	RW	2h	POR
	Port connectivity: 0h = Port complex is connected to a jack 1h = No physical connection for port 2h = Fixed function device is attached 3h = Both jack and internal device attached (info in all other fields refers to integrated device, any presence detection refers to jack)			

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Field Name	Bits	R/W	Default	Reset
Location	29:24	RW	01h	POR
	Location Bits [5..4]: 0h = External on primary chassis 1h = Internal 2h = Separate chassis 3h = Other Bits [3..0]: 0h = N/A 1h = Rear 2h = Front 3h = Left 4h = Right 5h = Top 6h = Bottom 7h-9h = Special Ah-Fh = Reserved			
Device	23:20	RW	Ch	POR
	Default device: 0h = Line out 1h = Speaker 2h = HP out 3h = CD 4h = SPDIF Out 5h = Digital other out 6h = Modem line side 7h = Modem handset side 8h = Line in 9h = Aux Ah = Mic in Bh = Telephony Ch = SPDIF In Dh = Digital other in Eh = Reserved Fh = Other			

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Field Name	Bits	R/W	Default	Reset
ConnectionType	19:16	RW	5h	POR
	Connection type: 0h = Unknown 1h = 1/8" stereo/mono 2h = 1/4" stereo/mono 3h = ATAPI internal 4h = RCA 5h = Optical 6h = Other digital 7h = Other analog 8h = Multichannel analog (DIN) 9h = XLR/Professional Ah = RJ-11 (modem) Bh = Combination Ch-Eh = Reserved Fh = Other			
Color	15:12	RW	2h	POR
	Color: 0h = Unknown 1h = Black 2h = Grey 3h = Blue 4h = Green 5h = Red 6h = Orange 7h = Yellow 8h = Purple 9h = Pink Ah-Dh = Reserved Eh = White Fh = Other			
Misc	11:8	RW	1h	POR
	Miscellaneous: Bits [3..1] = Reserved Bit 0 = Jack detect override			
Association	7:4	RW	7h	POR
	Default assocation.			
Sequence	3:0	RW	0h	POR
	Sequence.			

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7.32. SPDIFOut0 (NID = 25h): WCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0009h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:24	R	00h	N/A (Hard-coded)
	Reserved.			
Type	23:20	R	0h	N/A (Hard-coded)
	Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined			
Delay	19:16	R	4h	N/A (Hard-coded)
	Number of sample delays through widget.			
Rsvd1	15:12	R	0h	N/A (Hard-coded)
	Reserved.			
SwapCap	11	R	0h	N/A (Hard-coded)
	Left/right swap support: 1 = yes, 0 = no.			
PwrCntrl	10	R	1h	N/A (Hard-coded)
	Power state support: 1 = yes, 0 = no.			
Dig	9	R	1h	N/A (Hard-coded)
	Digital stream support: 1 = yes (digital), 0 = no (analog).			
ConnList	8	R	0h	N/A (Hard-coded)
	Connection list present: 1 = yes, 0 = no.			

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Field Name	Bits	R/W	Default	Reset
UnSolCap	7	R	0h	N/A (Hard-coded)
	Unsolicited response support: 1 = yes, 0 = no.			
ProcWidget	6	R	0h	N/A (Hard-coded)
	Processing state support: 1 = yes, 0 = no.			
Stripe	5	R	0h	N/A (Hard-coded)
	Striping support: 1 = yes, 0 = no.			
FormatOvrd	4	R	1h	N/A (Hard-coded)
	Stream format override: 1 = yes, 0 = no.			
AmpParOvrd	3	R	1h	N/A (Hard-coded)
	Amplifier capabilities override: 1 = yes, no.			
OutAmpPrsnt	2	R	1h	N/A (Hard-coded)
	Output amp present: 1 = yes, 0 = no.			
InAmpPrsnt	1	R	0h	N/A (Hard-coded)
	Input amp present: 1 = yes, 0 = no.			
Stereo	0	R	1h	N/A (Hard-coded)
	Stereo stream support: 1 = yes (stereo), 0 = no (mono).			

7.32.1. SPDIFOut0 (NID = 25h): PCMCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Ah			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:21	R	000h	N/A (Hard-coded)
	Reserved.			

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Field Name	Bits	R/W	Default	Reset
B32	20	R	0h	N/A (Hard-coded)
	32 bit audio format support: 1 = yes, 0 = no.			
B24	19	R	1h	N/A (Hard-coded)
	24 bit audio format support: 1 = yes, 0 = no.			
B20	18	R	1h	N/A (Hard-coded)
	20 bit audio format support: 1 = yes, 0 = no.			
B16	17	R	1h	N/A (Hard-coded)
	16 bit audio format support: 1 = yes, 0 = no.			
B8	16	R	0h	N/A (Hard-coded)
	8 bit audio format support: 1 = yes, 0 = no.			
Rsvd1	15:12	R	0h	N/A (Hard-coded)
	Reserved.			
R12	11	R	0h	N/A (Hard-coded)
	384kHz rate support: 1 = yes, 0 = no.			
R11	10	R	1h	N/A (Hard-coded)
	192kHz rate support: 1 = yes, 0 = no.			
R10	9	R	0h	N/A (Hard-coded)
	176.4kHz rate support: 1 = yes, 0 = no.			
R9	8	R	1h	N/A (Hard-coded)
	96kHz rate support: 1 = yes, 0 = no.			
R8	7	R	1h	N/A (Hard-coded)
	88.2kHz rate support: 1 = yes, 0 = no.			
R7	6	R	1h	N/A (Hard-coded)
	48kHz rate support: 1 = yes, 0 = no.			
R6	5	R	1h	N/A (Hard-coded)
	44.1kHz rate support: 1 = yes, 0 = no.			

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Field Name	Bits	R/W	Default	Reset
R5	4	R	0h	N/A (Hard-coded)
	32kHz rate support: 1 = yes, 0 = no.			
R4	3	R	0h	N/A (Hard-coded)
	22.05kHz rate support: 1 = yes, 0 = no.			
R3	2	R	0h	N/A (Hard-coded)
	16kHz rate support: 1 = yes, 0 = no.			
R2	1	R	0h	N/A (Hard-coded)
	11.025kHz rate support: 1 = yes, 0 = no.			
R1	0	R	0h	N/A (Hard-coded)
	8kHz rate support: 1 = yes, 0 = no.			

7.32.2. SPDIFOut0 (NID = 25h): StreamCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Bh			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:3	R	00000000h	N/A (Hard-coded)
	Reserved.			
AC3	2	R	1h	N/A (Hard-coded)
	AC-3 formatted data support: 1 = yes, 0 = no.			
Float32	1	R	0h	N/A (Hard-coded)
	Float32 formatted data support: 1 = yes, 0 = no.			
PCM	0	R	1h	N/A (Hard-coded)
	PCM-formatted data support: 1 = yes, 0 = no.			

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7.32.3. SPDIFOut0 (NID = 25h): OutAmpCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0012h			

Field Name	Bits	R/W	Default	Reset
Mute	31	R	1h	N/A (Hard-coded)
	Mute support: 1 = yes, 0 = no.			
Rsvd3	30:23	R	00h	N/A (Hard-coded)
	Reserved.			
StepSize	22:16	R	00h	N/A (Hard-coded)
	Size of each step in the gain range: 0 to 127 = .25dB to 32dB, in .25dB steps.			
Rsvd2	15	R	0h	N/A (Hard-coded)
	Reserved.			
NumSteps	14:8	R	00h	N/A (Hard-coded)
	Number of gains steps (number of possible settings - 1).			
Rsvd1	7	R	0h	N/A (Hard-coded)
	Reserved.			
Offset	6:0	R	00h	N/A (Hard-coded)
	Indicates which step is 0dB			

7.32.4. SPDIFOut0 (NID = 25h): Cnvtr

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set			2h	
Get	A0000h			

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Field Name	Bits	R/W	Default	Reset
Rsvd2	31:16	R	0000h	N/A (Hard-coded)
	Reserved.			
FrmtNonPCM	15	RW	0h	POR - DAFG - ULR
	Stream type: 1 = Non-PCM, 0 = PCM.			
FrmtSmplRate	14	RW	0h	POR - DAFG - ULR
	Sample base rate: 1 = 44.1kHz, 0 = 48kHz.			
SmplRateMultp	13:11	RW	0h	POR - DAFG - ULR
	Sample base rate multiple: 000b= x1 (48kHz/44.1kHz or less) 001b= x2 (96kHz/88.2kHz/32kHz) 010b= x3 (144kHz) 011b= x4 (192kHz/176.4kHz) 100b-111b Reserved			
SmplRateDiv	10:8	RW	0h	POR - DAFG - ULR
	Sample base rate divider: 000b= Divide by 1 (48kHz/44.1kHz) 001b= Divide by 2 (24kHz/20.05kHz) 010b= Divide by 3 (16kHz/32kHz) 011b= Divide by 4 (11.025kHz) 100b= Divide by 5 (9.6kHz) 101b= Divide by 6 (8kHz) 110b= Divide by 7 111b= Divide by 8 (6kHz)			
Rsvd1	7	R	0h	N/A (Hard-coded)
	Reserved.			
BitsPerSmpl	6:4	RW	3h	POR - DAFG - ULR
	Bits per sample: 000b= 8 bits 001b= 16 bits 010b= 20 bits 011b= 24 bits 100b= 32 bits 101b-111b= Reserved			

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Field Name	Bits	R/W	Default	Reset
NmbrChan	3:0	RW	1h	POR - DAFG - ULR
	Total number of channels in the stream assigned to this converter: 0000b-1111b= 1-16 channels.			

7.32.5. SPDIFOut0 (NID = 25h): OutAmpLeft

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				3A0h
Get	BA000h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
Mute	7	RW	0h	POR - DAFG - ULR
	Amp mute: 1 = muted, 0 = not muted.			
Rsvd1	6:0	R	00h	N/A (Hard-coded)
	Reserved.			

7.32.6. SPDIFOut0 (NID = 25h): OutAmpRight

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				390h
Get	B8000h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			

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Field Name	Bits	R/W	Default	Reset
Mute	7	RW	0h	POR - DAFG - ULR
	Amp mute: 1 = muted, 0 = not muted.			
Rsvd1	6:0	R	00h	N/A (Hard-coded)
	Reserved.			

7.32.7. SPDIFOut0 (NID = 25h): PwrState

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				705h
Get	F0500h			

Field Name	Bits	R/W	Default	Reset
Rsvd4	31:11	R	000000h	N/A (Hard-coded)
	Reserved.			
SettingsReset	10	R	1h	POR - DAFG - ULR
	Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget.			
Rsvd3	9	R	0h	N/A (Hard-coded)
	Reserved.			
Error	8	R	0h	POR - DAFG - ULR
	Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state.			
Rsvd2	7:6	R	0h	N/A (Hard-coded)
	Reserved.			
Act	5:4	R	3h	POR - DAFG - LR
	Actual power state of this widget.			
Rsvd1	3:2	R	0h	N/A (Hard-coded)
	Reserved.			

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Field Name	Bits	R/W	Default	Reset
Set	1:0	RW	3h	POR - DAFG - LR
	Current power state setting for this widget.			

7.32.8. SPDIFOut0 (NID = 25h): CnvtrID

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				706h
Get	F0600h			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
Strm	7:4	RW	0h	POR - S&DAFG - LR - PS
	Stream ID: 0h = Converter "off", 1h-Fh = valid ID's.			
Ch	3:0	RW	0h	POR - S&DAFG - LR - PS
	Channel assignment ("Ch" and "Ch+1" assigned as a pair, for a stereo converter).			

7.32.9. SPDIFOut0 (NID = 25h): DigCnvtr

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set	73Fh	73Eh	70Eh	70Dh
Get	F0E00h / F0D00h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:24	R	00h	N/A (Hard-coded)
	Reserved.			

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Field Name	Bits	R/W	Default	Reset
KeepAlive	23	RW	0h	POR - DAFG - ULR
	Keep Alive Enable: 1 = clocking information maintained during D3, 0 = clock information not required during D3.			
Rsvd1	22:15	R	00h	N/A (Hard-coded)
	Reserved.			
CC	14:8	RW	00h	POR - DAFG - ULR
	CC: Category Code.			
L	7	RW	0h	POR - DAFG - ULR
	L: Generation Level.			
PRO	6	RW	0h	POR - DAFG - ULR
	PRO: Professional.			
AUDIO	5	RW	0h	POR - DAFG - ULR
	/AUDIO: Non-Audio.			
COPY	4	RW	0h	POR - DAFG - ULR
	COPY: Copyright.			
PRE	3	RW	0h	POR - DAFG - ULR
	PRE: Preemphasis.			
VCFG	2	RW	0h	POR - DAFG - ULR
	VCFG: Validity Config.			
V	1	RW	0h	POR - DAFG - ULR
	V: Validity.			
DigEn	0	RW	0h	POR - DAFG - ULR
	Digital enable: 1 = converter enabled, 0 = converter disable.			

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7.33. SPDIFOut1 (NID = 26h): WCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0009h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:24	R	00h	N/A (Hard-coded)
	Reserved.			
Type	23:20	R	0h	N/A (Hard-coded)
	Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined			
Delay	19:16	R	4h	N/A (Hard-coded)
	Number of sample delays through widget.			
Rsvd1	15:12	R	0h	N/A (Hard-coded)
	Reserved.			
SwapCap	11	R	0h	N/A (Hard-coded)
	Left/right swap support: 1 = yes, 0 = no.			
PwrCntrl	10	R	1h	N/A (Hard-coded)
	Power state support: 1 = yes, 0 = no.			
Dig	9	R	1h	N/A (Hard-coded)
	Digital stream support: 1 = yes (digital), 0 = no (analog).			
ConnList	8	R	0h	N/A (Hard-coded)
	Connection list present: 1 = yes, 0 = no.			

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Field Name	Bits	R/W	Default	Reset
UnSolCap	7	R	0h	N/A (Hard-coded)
	Unsolicited response support: 1 = yes, 0 = no.			
ProcWidget	6	R	0h	N/A (Hard-coded)
	Processing state support: 1 = yes, 0 = no.			
Stripe	5	R	0h	N/A (Hard-coded)
	Striping support: 1 = yes, 0 = no.			
FormatOvrd	4	R	1h	N/A (Hard-coded)
	Stream format override: 1 = yes, 0 = no.			
AmpParOvrd	3	R	1h	N/A (Hard-coded)
	Amplifier capabilities override: 1 = yes, no.			
OutAmpPrsnt	2	R	1h	N/A (Hard-coded)
	Output amp present: 1 = yes, 0 = no.			
InAmpPrsnt	1	R	0h	N/A (Hard-coded)
	Input amp present: 1 = yes, 0 = no.			
Stereo	0	R	1h	N/A (Hard-coded)
	Stereo stream support: 1 = yes (stereo), 0 = no (mono).			

7.33.1. SPDIFOut1 (NID = 26h): PCMCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Ah			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:21	R	000h	N/A (Hard-coded)
	Reserved.			

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Field Name	Bits	R/W	Default	Reset
B32	20	R	0h	N/A (Hard-coded)
	32 bit audio format support: 1 = yes, 0 = no.			
B24	19	R	1h	N/A (Hard-coded)
	24 bit audio format support: 1 = yes, 0 = no.			
B20	18	R	1h	N/A (Hard-coded)
	20 bit audio format support: 1 = yes, 0 = no.			
B16	17	R	1h	N/A (Hard-coded)
	16 bit audio format support: 1 = yes, 0 = no.			
B8	16	R	0h	N/A (Hard-coded)
	8 bit audio format support: 1 = yes, 0 = no.			
Rsvd1	15:12	R	0h	N/A (Hard-coded)
	Reserved.			
R12	11	R	0h	N/A (Hard-coded)
	384kHz rate support: 1 = yes, 0 = no.			
R11	10	R	1h	N/A (Hard-coded)
	192kHz rate support: 1 = yes, 0 = no.			
R10	9	R	0h	N/A (Hard-coded)
	176.4kHz rate support: 1 = yes, 0 = no.			
R9	8	R	1h	N/A (Hard-coded)
	96kHz rate support: 1 = yes, 0 = no.			
R8	7	R	1h	N/A (Hard-coded)
	88.2kHz rate support: 1 = yes, 0 = no.			
R7	6	R	1h	N/A (Hard-coded)
	48kHz rate support: 1 = yes, 0 = no.			
R6	5	R	1h	N/A (Hard-coded)
	44.1kHz rate support: 1 = yes, 0 = no.			

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Field Name	Bits	R/W	Default	Reset
R5	4	R	0h	N/A (Hard-coded)
	32kHz rate support: 1 = yes, 0 = no.			
R4	3	R	0h	N/A (Hard-coded)
	22.05kHz rate support: 1 = yes, 0 = no.			
R3	2	R	0h	N/A (Hard-coded)
	16kHz rate support: 1 = yes, 0 = no.			
R2	1	R	0h	N/A (Hard-coded)
	11.025kHz rate support: 1 = yes, 0 = no.			
R1	0	R	0h	N/A (Hard-coded)
	8kHz rate support: 1 = yes, 0 = no.			

7.33.2. SPDIFOut1 (NID = 26h): StreamCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Bh			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:3	R	00000000h	N/A (Hard-coded)
	Reserved.			
AC3	2	R	1h	N/A (Hard-coded)
	AC-3 formatted data support: 1 = yes, 0 = no.			
Float32	1	R	0h	N/A (Hard-coded)
	Float32 formatted data support: 1 = yes, 0 = no.			
PCM	0	R	1h	N/A (Hard-coded)
	PCM-formatted data support: 1 = yes, 0 = no.			

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7.33.3. SPDIFOut1 (NID = 26h): OutAmpCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0012h			

Field Name	Bits	R/W	Default	Reset
Mute	31	R	1h	N/A (Hard-coded)
	Mute support: 1 = yes, 0 = no.			
Rsvd3	30:23	R	00h	N/A (Hard-coded)
	Reserved.			
StepSize	22:16	R	00h	N/A (Hard-coded)
	Size of each step in the gain range: 0 to 127 = .25dB to 32dB, in .25dB steps.			
Rsvd2	15	R	0h	N/A (Hard-coded)
	Reserved.			
NumSteps	14:8	R	00h	N/A (Hard-coded)
	Number of gains steps (number of possible settings - 1).			
Rsvd1	7	R	0h	N/A (Hard-coded)
	Reserved.			
Offset	6:0	R	00h	N/A (Hard-coded)
	Indicates which step is 0dB			

7.33.4. SPDIFOut1 (NID = 26h): Cnvtr

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set			2h	
Get	A0000h			

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Field Name	Bits	R/W	Default	Reset
Rsvd2	31:16	R	0000h	N/A (Hard-coded)
	Reserved.			
FrmtNonPCM	15	RW	0h	POR - DAFG - ULR
	Stream type: 1 = Non-PCM, 0 = PCM.			
FrmtSmplRate	14	RW	0h	POR - DAFG - ULR
	Sample base rate: 1 = 44.1kHz, 0 = 48kHz.			
SmplRateMultp	13:11	RW	0h	POR - DAFG - ULR
	Sample base rate multiple: 000b= x1 (48kHz/44.1kHz or less) 001b= x2 (96kHz/88.2kHz/32kHz) 010b= x3 (144kHz) 011b= x4 (192kHz/176.4kHz) 100b-111b Reserved			
SmplRateDiv	10:8	RW	0h	POR - DAFG - ULR
	Sample base rate divider: 000b= Divide by 1 (48kHz/44.1kHz) 001b= Divide by 2 (24kHz/20.05kHz) 010b= Divide by 3 (16kHz/32kHz) 011b= Divide by 4 (11.025kHz) 100b= Divide by 5 (9.6kHz) 101b= Divide by 6 (8kHz) 110b= Divide by 7 111b= Divide by 8 (6kHz)			
Rsvd1	7	R	0h	N/A (Hard-coded)
	Reserved.			
BitsPerSmpl	6:4	RW	3h	POR - DAFG - ULR
	Bits per sample: 000b= 8 bits 001b= 16 bits 010b= 20 bits 011b= 24 bits 100b= 32 bits 101b-111b= Reserved			

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Field Name	Bits	R/W	Default	Reset
NmbrChan	3:0	RW	1h	POR - DAFG - ULR
	Total number of channels in the stream assigned to this converter: 0000b-1111b= 1-16 channels.			

7.33.5. SPDIFOut1 (NID = 26h): OutAmpLeft

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				3A0h
Get	BA000h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
Mute	7	RW	0h	POR - DAFG - ULR
	Amp mute: 1 = muted, 0 = not muted.			
Rsvd1	6:0	R	00h	N/A (Hard-coded)
	Reserved.			

7.33.6. SPDIFOut1 (NID = 26h): OutAmpRight

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				390h
Get	B8000h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			

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Field Name	Bits	R/W	Default	Reset
Mute	7	RW	0h	POR - DAFG - ULR
	Amp mute: 1 = muted, 0 = not muted.			
Rsvd1	6:0	R	00h	N/A (Hard-coded)
	Reserved.			

7.33.7. SPDIFOut1 (NID = 26h): PwrState

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				705h
Get	F0500h			

Field Name	Bits	R/W	Default	Reset
Rsvd4	31:11	R	000000h	N/A (Hard-coded)
	Reserved.			
SettingsReset	10	R	1h	POR - DAFG - ULR
	Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget.			
Rsvd3	9	R	0h	N/A (Hard-coded)
	Reserved.			
Error	8	R	0h	POR - DAFG - ULR
	Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state.			
Rsvd2	7:6	R	0h	N/A (Hard-coded)
	Reserved.			
Act	5:4	R	3h	POR - DAFG - LR
	Actual power state of this widget.			
Rsvd1	3:2	R	0h	N/A (Hard-coded)
	Reserved.			

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Field Name	Bits	R/W	Default	Reset
Set	1:0	RW	3h	POR - DAFG - LR
	Current power state setting for this widget.			

7.33.8. SPDIFOut1 (NID = 26h): CnvtrID

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				706h
Get	F0600h			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
Strm	7:4	RW	0h	POR - S&DAFG - LR - PS
	Stream ID: 0h = Converter "off", 1h-Fh = valid ID's.			
Ch	3:0	RW	0h	POR - S&DAFG - LR - PS
	Channel assignment ("Ch" and "Ch+1" assigned as a pair, for a stereo converter).			

7.33.9. SPDIFOut1 (NID = 26h): DigCnvtr

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set	73Fh	73Eh	70Eh	70Dh
Get	F0E00h / F0D00h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:24	R	00h	N/A (Hard-coded)
	Reserved.			

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Field Name	Bits	R/W	Default	Reset
KeepAlive	23	RW	0h	POR - DAFG - ULR
	Keep Alive Enable: 1 = clocking information maintained during D3, 0 = clock information not required during D3.			
Rsvd1	22:15	R	00h	N/A (Hard-coded)
	Reserved.			
CC	14:8	RW	00h	POR - DAFG - ULR
	CC: Category Code.			
L	7	RW	0h	POR - DAFG - ULR
	L: Generation Level.			
PRO	6	RW	0h	POR - DAFG - ULR
	PRO: Professional.			
AUDIO	5	RW	0h	POR - DAFG - ULR
	/AUDIO: Non-Audio.			
COPY	4	RW	0h	POR - DAFG - ULR
	COPY: Copyright.			
PRE	3	RW	0h	POR - DAFG - ULR
	PRE: Preemphasis.			
VCFG	2	RW	0h	POR - DAFG - ULR
	VCFG: Validity Config.			
V	1	RW	0h	POR - DAFG - ULR
	V: Validity.			
DigEn	0	RW	0h	POR - DAFG - ULR
	Digital enable: 1 = converter enabled, 0 = converter disable.			

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7.34. SPDIFIn (NID = 27h): WCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0009h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:24	R	00h	N/A (Hard-coded)
	Reserved.			
Type	23:20	R	1h	N/A (Hard-coded)
	Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined			
Delay	19:16	R	4h	N/A (Hard-coded)
	Number of sample delays through widget.			
Rsvd1	15:12	R	0h	N/A (Hard-coded)
	Reserved.			
SwapCap	11	R	0h	N/A (Hard-coded)
	Left/right swap support: 1 = yes, 0 = no.			
PwrCntrl	10	R	1h	N/A (Hard-coded)
	Power state support: 1 = yes, 0 = no.			
Dig	9	R	1h	N/A (Hard-coded)
	Digital stream support: 1 = yes (digital), 0 = no (analog).			
ConnList	8	R	1h	N/A (Hard-coded)
	Connection list present: 1 = yes, 0 = no.			

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Field Name	Bits	R/W	Default	Reset
UnSolCap	7	R	0h	N/A (Hard-coded)
	Unsolicited response support: 1 = yes, 0 = no.			
ProcWidget	6	R	0h	N/A (Hard-coded)
	Processing state support: 1 = yes, 0 = no.			
Stripe	5	R	0h	N/A (Hard-coded)
	Striping support: 1 = yes, 0 = no.			
FormatOvrd	4	R	1h	N/A (Hard-coded)
	Stream format override: 1 = yes, 0 = no.			
AmpParOvrd	3	R	1h	N/A (Hard-coded)
	Amplifier capabilities override: 1 = yes, no.			
OutAmpPrsnt	2	R	0h	N/A (Hard-coded)
	Output amp present: 1 = yes, 0 = no.			
InAmpPrsnt	1	R	1h	N/A (Hard-coded)
	Input amp present: 1 = yes, 0 = no.			
Stereo	0	R	1h	N/A (Hard-coded)
	Stereo stream support: 1 = yes (stereo), 0 = no (mono).			

7.34.1. SPDIFIn (NID = 27h): PCMCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Ah			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:21	R	000h	N/A (Hard-coded)
	Reserved.			

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Field Name	Bits	R/W	Default	Reset
B32	20	R	0h	N/A (Hard-coded)
	32 bit audio format support: 1 = yes, 0 = no.			
B24	19	R	1h	N/A (Hard-coded)
	24 bit audio format support: 1 = yes, 0 = no.			
B20	18	R	1h	N/A (Hard-coded)
	20 bit audio format support: 1 = yes, 0 = no.			
B16	17	R	1h	N/A (Hard-coded)
	16 bit audio format support: 1 = yes, 0 = no.			
B8	16	R	0h	N/A (Hard-coded)
	8 bit audio format support: 1 = yes, 0 = no.			
Rsvd1	15:12	R	0h	N/A (Hard-coded)
	Reserved.			
R12	11	R	0h	N/A (Hard-coded)
	384kHz rate support: 1 = yes, 0 = no.			
R11	10	R	0h	N/A (Hard-coded)
	192kHz rate support: 1 = yes, 0 = no.			
R10	9	R	0h	N/A (Hard-coded)
	176.4kHz rate support: 1 = yes, 0 = no.			
R9	8	R	1h	N/A (Hard-coded)
	96kHz rate support: 1 = yes, 0 = no.			
R8	7	R	0h	N/A (Hard-coded)
	88.2kHz rate support: 1 = yes, 0 = no.			
R7	6	R	1h	N/A (Hard-coded)
	48kHz rate support: 1 = yes, 0 = no.			
R6	5	R	1h	N/A (Hard-coded)
	44.1kHz rate support: 1 = yes, 0 = no.			

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Field Name	Bits	R/W	Default	Reset
R5	4	R	0h	N/A (Hard-coded)
	32kHz rate support: 1 = yes, 0 = no.			
R4	3	R	0h	N/A (Hard-coded)
	22.05kHz rate support: 1 = yes, 0 = no.			
R3	2	R	0h	N/A (Hard-coded)
	16kHz rate support: 1 = yes, 0 = no.			
R2	1	R	0h	N/A (Hard-coded)
	11.025kHz rate support: 1 = yes, 0 = no.			
R1	0	R	0h	N/A (Hard-coded)
	8kHz rate support: 1 = yes, 0 = no.			

7.34.2. SPDIFIn (NID = 27h): StreamCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Bh			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:3	R	00000000h	N/A (Hard-coded)
	Reserved.			
AC3	2	R	1h	N/A (Hard-coded)
	AC-3 formatted data support: 1 = yes, 0 = no.			
Float32	1	R	0h	N/A (Hard-coded)
	Float32 formatted data support: 1 = yes, 0 = no.			
PCM	0	R	1h	N/A (Hard-coded)
	PCM-formatted data support: 1 = yes, 0 = no.			

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7.34.3. SPDIFIn (NID = 27h): Cnvtr

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set			2h	
Get	A0000h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:16	R	0000h	N/A (Hard-coded)
	Reserved.			
FrmtNonPCM	15	RW	0h	POR - DAFG - ULR
	Stream type: 1 = Non-PCM, 0 = PCM.			
FrmtSmplRate	14	RW	0h	POR - DAFG - ULR
	Sample base rate: 1 = 44.1kHz, 0 = 48kHz.			
SmplRateMultp	13:11	RW	0h	POR - DAFG - ULR
	Sample base rate multiple: 000b= x1 (48kHz/44.1kHz or less) 001b= x2 (96kHz/88.2kHz/32kHz) 010b= x3 (144kHz) 011b= x4 (192kHz/176.4kHz) 100b-111b Reserved			
SmplRateDiv	10:8	RW	0h	POR - DAFG - ULR
	Sample base rate divider: 000b= Divide by 1 (48kHz/44.1kHz) 001b= Divide by 2 (24kHz/20.05kHz) 010b= Divide by 3 (16kHz/32kHz) 011b= Divide by 4 (11.025kHz) 100b= Divide by 5 (9.6kHz) 101b= Divide by 6 (8kHz) 110b= Divide by 7 111b= Divide by 8 (6kHz)			
Rsvd1	7	R	0h	N/A (Hard-coded)
	Reserved.			

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Field Name	Bits	R/W	Default	Reset
BitsPerSmpl	6:4	RW	3h	POR - DAFG - ULR
	Bits per sample: 000b= 8 bits 001b= 16 bits 010b= 20 bits 011b= 24 bits 100b= 32 bits 101b-111b= Reserved			
NmbrChan	3:0	RW	1h	POR - DAFG - ULR
	Total number of channels in the stream assigned to this converter: 0000b-1111b= 1-16 channels.			

7.34.4. SPDIFIn (NID = 27h): ConLst

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Eh			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
LForm	7	R	0h	N/A (Hard-coded)
	Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries.			
ConL	6:0	R	01h	N/A (Hard-coded)
	Number of NID entries in connection list.			

7.34.5. SPDIFIn (NID = 27h): ConLstEntry0

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0200h			

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Field Name	Bits	R/W	Default	Reset
ConL3	31:24	R	00h	N/A (Hard-coded)
	Unused			
ConL2	23:16	R	00h	N/A (Hard-coded)
	Unused			
ConL1	15:8	R	00h	N/A (Hard-coded)
	Unused			
ConL0	7:0	R	24h	N/A (Hard-coded)
	Dig2Pin pin widget (0x24			

7.34.6. SPDIFIn (NID = 27h): PwrState

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				705h
Get	F0500h			

Field Name	Bits	R/W	Default	Reset
Rsvd4	31:11	R	000000h	N/A (Hard-coded)
	Reserved.			
SettingsReset	10	R	1h	POR - DAFG - ULR
	Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget.			
Rsvd3	9	R	0h	N/A (Hard-coded)
	Reserved.			
Error	8	R	0h	POR - DAFG - ULR
	Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state.			

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Field Name	Bits	R/W	Default	Reset
Rsvd2	7:6	R	0h	N/A (Hard-coded)
	Reserved.			
Act	5:4	R	3h	POR - DAFG - LR
	Actual power state of this widget.			
Rsvd1	3:2	R	0h	N/A (Hard-coded)
	Reserved.			
Set	1:0	RW	3h	POR - DAFG - LR
	Current power state setting for this widget.			

7.34.7. SPDIFIn (NID = 27h): CnvtrID

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				706h
Get	F0600h			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
Strm	7:4	RW	0h	POR - S&DAFG - LR - PS
	Stream ID: 0h = Converter "off", 1h-Fh = valid ID's.			
Ch	3:0	RW	0h	POR - S&DAFG - LR - PS
	Channel assignment ("Ch" and "Ch+1" assigned as a pair, for a stereo converter).			

7.34.8. SPDIFIn (NID = 27h): DigCnvtr

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set	73Fh	73Eh	70Eh	70Dh

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7.34.8. SPDIFIn (NID = 27h): DigCnvtr

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Get	F0E00h / F0D00h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:24	R	00h	N/A (Hard-coded)
	Reserved.			
KeepAlive	23	RW	0h	POR - DAFG - ULR
	Keep Alive Enable: 1 = clocking information maintained during D3, 0 = clock information not required during D3.			
Rsvd1	22:15	R	00h	N/A (Hard-coded)
	Reserved.			
CC	14:8	RW	00h	POR - DAFG - ULR
	CC: Category Code.			
L	7	RW	0h	POR - DAFG - ULR
	L: Generation Level.			
PRO	6	RW	0h	POR - DAFG - ULR
	PRO: Professional.			
AUDIO	5	RW	0h	POR - DAFG - ULR
	/AUDIO: Non-Audio.			
COPY	4	RW	0h	POR - DAFG - ULR
	COPY: Copyright.			
PRE	3	RW	0h	POR - DAFG - ULR
	PRE: Preemphasis.			
VCFG	2	RW	0h	POR - DAFG - ULR
	VCFG: Validity Config.			
V	1	RW	0h	POR - DAFG - ULR
	V: Validity.			

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Field Name	Bits	R/W	Default	Reset
DigEn	0	RW	0h	POR - DAFG - ULR
	Digital enable: 1 = converter enabled, 0 = converter disable.			

7.34.9. SPDIFIn (NID = 27h): InAmpCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Dh			

Field Name	Bits	R/W	Default	Reset
Mute	31	R	1h	N/A (Hard-coded)
	Mute support: 1 = yes, 0 = no.			
Rsvd3	30:23	R	00h	N/A (Hard-coded)
	Reserved.			
StepSize	22:16	R	05h	N/A (Hard-coded)
	Size of each step in the gain range: 0 to 127 = .25dB to 32dB, in .25dB steps.			
Rsvd2	15	R	0h	N/A (Hard-coded)
	Reserved.			
NumSteps	14:8	R	00h	N/A (Hard-coded)
	Number of gains steps (number of possible settings - 1).			
Rsvd1	7	R	0h	N/A (Hard-coded)
	Reserved.			
Offset	6:0	R	00h	N/A (Hard-coded)
	Indicates which step is 0dB			

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7.34.10. SPDIFIn (NID = 27h): InAmpLeft

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				360h
Get	B2000h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
Mute	7	RW	0h	POR - DAFG - ULR
	Amp mute: 1 = muted, 0 = not muted			
Rsvd1	6:0	R	0h	N/A (Hard-coded)
	Reserved.			

7.34.11. SPDIFIn (NID = 27h): InAmpRight

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				350h
Get	B0000h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
Mute	7	RW	0h	POR - DAFG - ULR
	Amp mute: 1 = muted, 0 = not muted			
Rsvd1	6:0	R	0h	N/A (Hard-coded)
	Reserved.			

7.34.12. SPDIFIn (NID = 27h): VS

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				7E8h
Get	FE800h			

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Field Name	Bits	R/W	Default	Reset
RcvSmplRate	31:29	R	7h	POR - DAFG - ULR
	Received Sample Rate: 000b = 44.1kHz 001b = 48kHz 010b = 88.2kHz 011b = 96kHz 100b = 176.4kHz 101b = 192kHz 11Xb = Invalid Rate			
Rsvd2	28:26	R	0h	POR - DAFG - ULR
	Reserved.			
OrigFS	25:22	R	0h	POR - DAFG - ULR
	Original Sample Rate (per IEC60958-3 spec): 0000b = Original sampling frequency not indicated 0001b = 192kHz 0010b = 12kHz 0011b = 176.4kHz 0100b = Reserved 0101b = 96kHz 0110b = 8kHz 0111b = 88.2kHz 1000b = 16kHz 1001b = 24kHz 1010b = 11.025kHz 1011b = 22.05kHz 1100b = 32kHz 1101b = 48khz 1110b = Reserved 1111b = 44.1kHz			
CA	21:20	R	0h	POR - DAFG - ULR
	Clock Accuracy (per IEC60958-3 spec): 00b = Level II 01b = Level I 10b = Level III 11b = Reserved			

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Field Name	Bits	R/W	Default	Reset
FS	19:16	R	0h	POR - DAFG - ULR
	Sample Rate (per IEC60958-3 spec): 0000b = 44.1kHz 0001b = Original sampling frequency not indicated 0010b = 48kHz 0011b = 32kHz 0100b = 22.05kHz 0101b = Reserved 0110b = 24kHz 0111b = Reserved 1000b = 88.2kHz 1001b = Reserved 1010b = 96kHz 1011b = Reserved 1100b = 176.4kHz 1101b = Reserved 1110b = 192kHz 1111b = Reserved			
CN	15:12	R	0h	POR - DAFG - ULR
	Channel Number (per IEC60958-3 spec): 0000b = Do not take into account 0001b = Channel 1 (Left channel for stereo channel format) 0010b = Channel 2 (Right channel for stereo channel format) 0011b-1111b = Channel 3-15			
SamplWrdL	11:9	R	0h	POR - DAFG - ULR
	Sample Word Length (per IEC60958-3 spec): 000b = Word length not indicated 001b = Max length - 4 010b = Max length - 2 011b = Reserved 100b = Max length - 1 101b = Max length - 0 110b = Max length - 3 111b = Reserved			
MaxWrdL	8	R	0h	POR - DAFG - ULR
	Max Word Length (per IEC60958-3 spec): 0 = 20 bits, 1 = 24 bits.			
NoBlkChk	7	RW	0h	POR - DAFG - ULR
	Disable Sample Block Checking.			
Rsvd	6:5	R	0h	N/A (Hard-coded)
	Reserved.			

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Field Name	Bits	R/W	Default	Reset
ParityLimit	4:3	RW	0h	POR - DAFG - ULR
	SPDIFIn Parity Limit (DPLL loses lock when the set number of parity errors per block is detected): 00b = 4 Parity errors 01b = 3 Parity errors 10b = 2 Parity errors 11b = 1 Parity errors			
SPRun	2	R	0h	POR - DAFG - ULR
	SPDIFIn Running 0 = no signal on SPDIFIn Pin, 1 = Signal on SPDIFIn pin.			
SiPerr	1	RW	0h	POR - DAFG - ULR
	SPDIFIn Parity Error: 0 = No error detected, 1 = Error detected (write 0 to clear). Not affected by ParityLimit.			
CopyInv	0	RW	0h	POR - DAFG - ULR
	Copyright Invert: 0 = Do not invert COPY bit, 1 = Invert COPY bit..			

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7.35. InPort0Mux (NID = 28h): WCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0009h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:24	R	00h	N/A (Hard-coded)
	Reserved.			
Type	23:20	R	3h	N/A (Hard-coded)
	Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined			
Delay	19:16	R	0h	N/A (Hard-coded)
	Number of sample delays through widget.			
Rsvd1	15:12	R	0h	N/A (Hard-coded)
	Reserved.			
SwapCap	11	R	0h	N/A (Hard-coded)
	Left/right swap support: 1 = yes, 0 = no.			
PwrCntrl	10	R	1h	N/A (Hard-coded)
	Power state support: 1 = yes, 0 = no.			
DigitalStrm	9	R	0h	N/A (Hard-coded)
	Digital stream support: 1 = yes (digital), 0 = no (analog).			
ConnList	8	R	1h	N/A (Hard-coded)
	Connection list present: 1 = yes, 0 = no.			

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Field Name	Bits	R/W	Default	Reset
UnsolCap	7	R	0h	N/A (Hard-coded)
	Unsolicited response support: 1 = yes, 0 = no.			
ProcWidget	6	R	0h	N/A (Hard-coded)
	Processing state support: 1 = yes, 0 = no.			
Stripe	5	R	0h	N/A (Hard-coded)
	Striping support: 1 = yes, 0 = no.			
FormatOvrd	4	R	0h	N/A (Hard-coded)
	Stream format override: 1 = yes, 0 = no.			
AmpParamOvrd	3	R	0h	N/A (Hard-coded)
	Amplifier capabilities override: 1 = yes, no.			
OutAmpPrsnt	2	R	0h	N/A (Hard-coded)
	Output amp present: 1 = yes, 0 = no.			
InAmpPrsnt	1	R	0h	N/A (Hard-coded)
	Input amp present: 1 = yes, 0 = no.			
Stereo	0	R	1h	N/A (Hard-coded)
	Stereo stream support: 1 = yes (stereo), 0 = no (mono).			

7.35.1. InPort0Mux (NID = 28h): ConLst

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Eh			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			

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Field Name	Bits	R/W	Default	Reset
LForm	7	R	0h	N/A (Hard-coded)
	Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries.			
ConL	6:0	R	04h	N/A (Hard-coded)
	Number of NID entries in connection list.			

7.35.2. InPort0Mux (NID = 28h): ConLstEntry0

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0200h			

Field Name	Bits	R/W	Default	Reset
ConL3	31:24	R	0Fh	N/A (Hard-coded)
	Port Fwidget (0x0F)			
ConL2	23:16	R	0Dh	N/A (Hard-coded)
	Port D Pin widget (0x0D)			
ConL1	15:8	R	0Bh	N/A (Hard-coded)
	Port B Pin widget (0x0B)			
ConL0	7:0	R	0Ah	N/A (Hard-coded)
	Port A Pin widget (0x0A)			

7.35.3. InPort0Mux (NID = 28h): ConSelectCtrl

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				701h
Get	F0100h			

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Field Name	Bits	R/W	Default	Reset
Rsvd	31:3	R	00000000h	N/A (Hard-coded)
	Reserved.			
Index	2:0	RW	0h	POR - DAFG - ULR
	Connection select control index.			

7.35.4. InPort0Mux (NID = 28h): PwrState

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				705h
Get	F0500h			

Field Name	Bits	R/W	Default	Reset
Rsvd4	31:11	R	000000h	N/A (Hard-coded)
	Reserved.			
SettingsReset	10	R	1h	POR - DAFG - ULR
	Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget.			
Rsvd3	9	R	0h	N/A (Hard-coded)
	Reserved.			
Error	8	R	0h	POR - DAFG - ULR
	Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state.			
Rsvd2	7:6	R	0h	N/A (Hard-coded)
	Reserved.			
Act	5:4	R	3h	POR - DAFG - LR
	Actual power state of this widget.			

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Field Name	Bits	R/W	Default	Reset
Rsvd1	3:2	R	0h	N/A (Hard-coded)
	Reserved.			
Set	1:0	RW	0h	POR - DAFG - LR
	Current power state setting for this widget.			

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7.36. InPort1Mux (NID = 29h): WCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0009h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:24	R	00h	N/A (Hard-coded)
	Reserved.			
Type	23:20	R	3h	N/A (Hard-coded)
	Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined			
Delay	19:16	R	0h	N/A (Hard-coded)
	Number of sample delays through widget.			
Rsvd1	15:12	R	0h	N/A (Hard-coded)
	Reserved.			
SwapCap	11	R	0h	N/A (Hard-coded)
	Left/right swap support: 1 = yes, 0 = no.			
PwrCntrl	10	R	1h	N/A (Hard-coded)
	Power state support: 1 = yes, 0 = no.			
DigitalStrm	9	R	0h	N/A (Hard-coded)
	Digital stream support: 1 = yes (digital), 0 = no (analog).			
ConnList	8	R	1h	N/A (Hard-coded)
	Connection list present: 1 = yes, 0 = no.			

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Field Name	Bits	R/W	Default	Reset
UnsolCap	7	R	0h	N/A (Hard-coded)
	Unsolicited response support: 1 = yes, 0 = no.			
ProcWidget	6	R	0h	N/A (Hard-coded)
	Processing state support: 1 = yes, 0 = no.			
Stripe	5	R	0h	N/A (Hard-coded)
	Striping support: 1 = yes, 0 = no.			
FormatOvrd	4	R	0h	N/A (Hard-coded)
	Stream format override: 1 = yes, 0 = no.			
AmpParamOvrd	3	R	0h	N/A (Hard-coded)
	Amplifier capabilities override: 1 = yes, no.			
OutAmpPrsnt	2	R	0h	N/A (Hard-coded)
	Output amp present: 1 = yes, 0 = no.			
InAmpPrsnt	1	R	0h	N/A (Hard-coded)
	Input amp present: 1 = yes, 0 = no.			
Stereo	0	R	1h	N/A (Hard-coded)
	Stereo stream support: 1 = yes (stereo), 0 = no (mono).			

7.36.1. InPort1Mux (NID = 29h): ConLst

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Eh			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			

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Field Name	Bits	R/W	Default	Reset
LForm	7	R	0h	N/A (Hard-coded)
	Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries.			
ConL	6:0	R	04h	N/A (Hard-coded)
	Number of NID entries in connection list.			

7.36.2. InPort1Mux (NID = 29h): ConLstEntry0

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0200h			

Field Name	Bits	R/W	Default	Reset
ConL3	31:24	R	11h	N/A (Hard-coded)
	Port H Pin widget (0x11)			
ConL2	23:16	R	10h	N/A (Hard-coded)
	Port G Pin widget (0x10)			
ConL1	15:8	R	0Eh	N/A (Hard-coded)
	Port E Pin widget (0x0E)			
ConL0	7:0	R	0Ah	N/A (Hard-coded)
	Port A Pin widget (0x0A)			

7.36.3. InPort1Mux (NID = 29h): ConSelectCtrl

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				701h
Get	F0100h			

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Field Name	Bits	R/W	Default	Reset
Rsvd	31:3	R	00000000h	N/A (Hard-coded)
	Reserved.			
Index	2:0	RW	0h	POR - DAFG - ULR
	Connection select control index.			

7.36.4. InPort1Mux (NID = 29h): PwrState

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				705h
Get	F0500h			

Field Name	Bits	R/W	Default	Reset
Rsvd4	31:11	R	000000h	N/A (Hard-coded)
	Reserved.			
SettingsReset	10	R	1h	POR - DAFG - ULR
	Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget.			
Rsvd3	9	R	0h	N/A (Hard-coded)
	Reserved.			
Error	8	R	0h	POR - DAFG - ULR
	Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state.			
Rsvd2	7:6	R	0h	N/A (Hard-coded)
	Reserved.			
Act	5:4	R	3h	POR - DAFG - LR
	Actual power state of this widget.			

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Field Name	Bits	R/W	Default	Reset
Rsvd1	3:2	R	0h	N/A (Hard-coded)
	Reserved.			
Set	1:0	RW	0h	POR - DAFG - LR
	Current power state setting for this widget.			

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7.12. ADC0 (NID = 1Ah): WCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0009h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:24	R	00h	N/A (Hard-coded)
	Reserved.			
Type	23:20	R	1h	N/A (Hard-coded)
	Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined			
Delay	19:16	R	Dh	N/A (Hard-coded)
	Number of sample delays through widget.			
Rsvd1	15:12	R	0h	N/A (Hard-coded)
	Reserved.			
SwapCap	11	R	0h	N/A (Hard-coded)
	Left/right swap support: 1 = yes, 0 = no.			
PwrCntrl	10	R	1h	N/A (Hard-coded)
	Power state support: 1 = yes, 0 = no.			
Dig	9	R	0h	N/A (Hard-coded)
	Digital stream support: 1 = yes (digital), 0 = no (analog).			

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Field Name	Bits	R/W	Default	Reset
ConnList	8	R	1h	N/A (Hard-coded)
	Connection list present: 1 = yes, 0 = no.			
UnSolCap	7	R	0h	N/A (Hard-coded)
	Unsolicited response support: 1 = yes, 0 = no.			
ProcWidget	6	R	1h	N/A (Hard-coded)
	Processing state support: 1 = yes, 0 = no.			
Stripe	5	R	0h	N/A (Hard-coded)
	Striping support: 1 = yes, 0 = no.			
FormatOvrd	4	R	0h	N/A (Hard-coded)
	Stream format override: 1 = yes, 0 = no.			
AmpParOvrd	3	R	0h	N/A (Hard-coded)
	Amplifier capabilities override: 1 = yes, no.			
OutAmpPrsnt	2	R	0h	N/A (Hard-coded)
	Output amp present: 1 = yes, 0 = no.			
InAmpPrsnt	1	R	0h	N/A (Hard-coded)
	Input amp present: 1 = yes, 0 = no.			
Stereo	0	R	1h	N/A (Hard-coded)
	Stereo stream support: 1 = yes (stereo), 0 = no (mono).			

7.12.1. ADC0 (NID = 1Ah): ConLst

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Eh			

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Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
LForm	7	R	0h	N/A (Hard-coded)
	Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries.			
ConL	6:0	R	01h	N/A (Hard-coded)
	Number of NID entries in connection list.			

7.12.2. ADC0 (NID = 1Ah): ConLstEntry0

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0200h			

Field Name	Bits	R/W	Default	Reset
ConL3	31:24	R	00h	N/A (Hard-coded)
	Unused list entry.			
ConL2	23:16	R	00h	N/A (Hard-coded)
	Unused list entry.			
ConL1	15:8	R	00h	N/A (Hard-coded)
	Unused list entry.			
ConL0	7:0	R	20h	N/A (Hard-coded)
	ADC0Mux Selector widget (0x20)			

7.12.3. ADC0 (NID = 1Ah): Cnvtr

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set			2h	

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7.12.3. ADC0 (NID = 1Ah): Cnvtr

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Get	A0000h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:16	R	0000h	N/A (Hard-coded)
	Reserved.			
StrmType	15	R	0h	N/A (Hard-coded)
	Stream type: 1 = Non-PCM, 0 = PCM.			
FrmtSmplRate	14	RW	0h	POR - DAFG - ULR
	Sample base rate: 1 = 44.1kHz, 0 = 48kHz.			
SmplRateMultp	13:11	RW	0h	POR - DAFG - ULR
	Sample base rate multiple: 000b= x1 (48kHz/44.1kHz or less) 001b= x2 (96kHz/88.2kHz/32kHz) 010b= x3 (144kHz) 011b= x4 (192kHz/176.4kHz) 100b-111b Reserved			
SmplRateDiv	10:8	RW	0h	POR - DAFG - ULR
	Sample base rate divider: 000b= Divide by 1 (48kHz/44.1kHz) 001b= Divide by 2 (24kHz/20.05kHz) 010b= Divide by 3 (16kHz/32kHz) 011b= Divide by 4 (11.025kHz) 100b= Divide by 5 (9.6kHz) 101b= Divide by 6 (8kHz) 110b= Divide by 7 111b= Divide by 8 (6kHz)			
Rsvd1	7	R	0h	N/A (Hard-coded)
	Reserved.			

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Field Name	Bits	R/W	Default	Reset
BitsPerSmpl	6:4	RW	3h	POR - DAFG - ULR
	Bits per sample: 000b= 8 bits 001b= 16 bits 010b= 20 bits 011b= 24 bits 100b= 32 bits 101b-111b= Reserved			
NmbrChan	3:0	RW	1h	POR - DAFG - ULR
	Total number of channels in the stream assigned to this converter: 0000b-1111b= 1-16 channels.			

7.12.4. ADC0 (NID = 1Ah): ProcState

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				703h
Get	F0300h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
HPFOCDIS	7	RW	0h	POR - DAFG - ULR
	HPF offset calculation disable. 1 = calculation disabled; 0 = calculation enabled.			
Rsvd1	6:2	R	00h	N/A (Hard-coded)
	Reserved.			
ADCHPFByp	1:0	RW	1h	POR - DAFG - ULR
	Processing State: 00b= bypass the ADC HPF ("off"), 01b-11b= ADC HPF is enabled ("on" or "benign").			

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7.12.5. ADC0 (NID = 1Ah): PwrState

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				705h
Get	F0500h			

Field Name	Bits	R/W	Default	Reset
Rsvd4	31:11	R	000000h	N/A (Hard-coded)
	Reserved.			
SettingsReset	10	R	1h	POR - DAFG - ULR
	Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget.			
Rsvd3	9	R	0h	N/A (Hard-coded)
	Reserved.			
Error	8	R	0h	POR - DAFG - ULR
	Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state.			
Rsvd2	7:6	R	0h	N/A (Hard-coded)
	Reserved.			
Act	5:4	R	3h	POR - DAFG - LR
	Actual power state of this widget.			
Rsvd1	3:2	R	0h	N/A (Hard-coded)
	Reserved.			
Set	1:0	RW	3h	POR - DAFG - LR
	Current power state setting for this widget.			

7.12.6. ADC0 (NID = 1Ah): CnvtrID

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				706h

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7.12.6. ADC0 (NID = 1Ah): CnvtrID

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Get	F0600h			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
Strm	7:4	RW	0h	POR - S&DAFG - LR - PS
	Stream ID: 0h = Converter "off", 1h-Fh = valid ID's.			
Ch	3:0	RW	0h	POR - S&DAFG - LR - PS
	Channel assignment ("Ch" and "Ch+1" assigned as a pair, for a stereo converter).			

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7.13. ADC1 (NID = 1Bh): WCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0009h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:24	R	00h	N/A (Hard-coded)
	Reserved.			
Type	23:20	R	1h	N/A (Hard-coded)
	Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined			
Delay	19:16	R	Dh	N/A (Hard-coded)
	Number of sample delays through widget.			
Rsvd1	15:12	R	0h	N/A (Hard-coded)
	Reserved.			
SwapCap	11	R	0h	N/A (Hard-coded)
	Left/right swap support: 1 = yes, 0 = no.			
PwrCntrl	10	R	1h	N/A (Hard-coded)
	Power state support: 1 = yes, 0 = no.			
Dig	9	R	0h	N/A (Hard-coded)
	Digital stream support: 1 = yes (digital), 0 = no (analog).			
ConnList	8	R	1h	N/A (Hard-coded)
	Connection list present: 1 = yes, 0 = no.			

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Field Name	Bits	R/W	Default	Reset
UnSolCap	7	R	0h	N/A (Hard-coded)
	Unsolicited response support: 1 = yes, 0 = no.			
ProcWidget	6	R	1h	N/A (Hard-coded)
	Processing state support: 1 = yes, 0 = no.			
Stripe	5	R	0h	N/A (Hard-coded)
	Striping support: 1 = yes, 0 = no.			
FormatOvrd	4	R	0h	N/A (Hard-coded)
	Stream format override: 1 = yes, 0 = no.			
AmpParOvrd	3	R	0h	N/A (Hard-coded)
	Amplifier capabilities override: 1 = yes, no.			
OutAmpPrsnt	2	R	0h	N/A (Hard-coded)
	Output amp present: 1 = yes, 0 = no.			
InAmpPrsnt	1	R	0h	N/A (Hard-coded)
	Input amp present: 1 = yes, 0 = no.			
Stereo	0	R	1h	N/A (Hard-coded)
	Stereo stream support: 1 = yes (stereo), 0 = no (mono).			

7.13.1. ADC1 (NID = 1Bh): ConLst

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Eh			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			

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Field Name	Bits	R/W	Default	Reset
LForm	7	R	0h	N/A (Hard-coded)
	Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries.			
ConL	6:0	R	01h	N/A (Hard-coded)
	Number of NID entries in connection list.			

7.13.2. ADC1 (NID = 1Bh): ConLstEntry0

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0200h			

Field Name	Bits	R/W	Default	Reset
ConL3	31:24	R	00h	N/A (Hard-coded)
	Unused list entry.			
ConL2	23:16	R	00h	N/A (Hard-coded)
	Unused list entry.			
ConL1	15:8	R	00h	N/A (Hard-coded)
	Unused list entry.			
ConL0	7:0	R	21h	N/A (Hard-coded)
	ADC1Mux widget (0x21)			

7.13.3. ADC1 (NID = 1Bh): Cnvtr

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set			2h	
Get	A0000h			

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Field Name	Bits	R/W	Default	Reset
Rsvd2	31:16	R	0000h	N/A (Hard-coded)
	Reserved.			
StrmType	15	R	0h	N/A (Hard-coded)
	Stream type: 1 = Non-PCM, 0 = PCM.			
FrmtSmplRate	14	RW	0h	POR - DAFG - ULR
	Sample base rate: 1 = 44.1kHz, 0 = 48kHz.			
SmplRateMultp	13:11	RW	0h	POR - DAFG - ULR
	Sample base rate multiple: 000b= x1 (48kHz/44.1kHz or less) 001b= x2 (96kHz/88.2kHz/32kHz) 010b= x3 (144kHz) 011b= x4 (192kHz/176.4kHz) 100b-111b Reserved			
SmplRateDiv	10:8	RW	0h	POR - DAFG - ULR
	Sample base rate divider: 000b= Divide by 1 (48kHz/44.1kHz) 001b= Divide by 2 (24kHz/20.05kHz) 010b= Divide by 3 (16kHz/32kHz) 011b= Divide by 4 (11.025kHz) 100b= Divide by 5 (9.6kHz) 101b= Divide by 6 (8kHz) 110b= Divide by 7 111b= Divide by 8 (6kHz)			
Rsvd1	7	R	0h	N/A (Hard-coded)
	Reserved.			
BitsPerSmpl	6:4	RW	3h	POR - DAFG - ULR
	Bits per sample: 000b= 8 bits 001b= 16 bits 010b= 20 bits 011b= 24 bits 100b= 32 bits 101b-111b= Reserved			

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Field Name	Bits	R/W	Default	Reset
NmbrChan	3:0	RW	1h	POR - DAFG - ULR
	Total number of channels in the stream assigned to this converter: 0000b-1111b= 1-16 channels.			

7.13.4. ADC1 (NID = 1Bh): ProcState

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				703h
Get	F0300h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
HPFOCDIS	7	RW	0h	POR - DAFG - ULR
	HPF offset calculation disable. 1 = calculation disabled; 0 = calculation enabled.			
Rsvd1	6:2	R	00h	N/A (Hard-coded)
	Reserved.			
ADCHPFByp	1:0	RW	1h	POR - DAFG - ULR
	Processing State: 00b= bypass the ADC HPF ("off"), 01b-11b= ADC HPF is enabled ("on" or "benign").			

7.13.5. ADC1 (NID = 1Bh): PwrState

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				705h
Get	F0500h			

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Field Name	Bits	R/W	Default	Reset
Rsvd4	31:11	R	000000h	N/A (Hard-coded)
	Reserved.			
SettingsReset	10	R	1h	POR - DAFG - ULR
	Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget.			
Rsvd3	9	R	0h	N/A (Hard-coded)
	Reserved.			
Error	8	R	0h	POR - DAFG - ULR
	Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state.			
Rsvd2	7:6	R	0h	N/A (Hard-coded)
	Reserved.			
Act	5:4	R	3h	POR - DAFG - LR
	Actual power state of this widget.			
Rsvd1	3:2	R	0h	N/A (Hard-coded)
	Reserved.			
Set	1:0	RW	3h	POR - DAFG - LR
	Current power state setting for this widget.			

7.13.6. ADC1 (NID = 1Bh): CnvtrID

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				706h
Get	F0600h			

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Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
Strm	7:4	RW	0h	POR - S&DAFG - LR - PS
	Stream ID: 0h = Converter "off", 1h-Fh = valid ID's.			
Ch	3:0	RW	0h	POR - S&DAFG - LR - PS
	Channel assignment ("Ch" and "Ch+1" assigned as a pair, for a stereo converter).			

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7.14. DigBeep (NID = 1Ch): WCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0009h			

Field Name	Bits	R/W	Default	Reset
Rsvd4	31:24	R	00h	N/A (Hard-coded)
	Reserved.			
Type	23:20	R	7h	N/A (Hard-coded)
	Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined			
Rsvd3	19:11	R	0h	N/A (Hard-coded)
	Reserved.			
PwrCntrl	10	R	1h	N/A (Hard-coded)
	Power state support: 1 = yes, 0 = no."			
Rsvd2	9:4	R	0h	N/A (Hard-coded)
	Reserved			
AmpParOvrd	3	R	1h	N/A (Hard-coded)
	Amplifier capabilities override: 1 = yes, no.			
OutAmpPrsnt	2	R	1h	N/A (Hard-coded)
	Output amp present: 1 = yes, 0 = no.			
Rsvd1	1:0	R	0h	N/A (Hard-coded)
	Reserved.			

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7.14.1. DigBeep (NID = 1Ch): OutAmpCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0012h			

Field Name	Bits	R/W	Default	Reset
Mute	31	R	1h	N/A (Hard-coded)
	Mute support: 1 = yes, 0 = no.			
Rsvd3	30:23	R	00h	N/A (Hard-coded)
	Reserved.			
StepSize	22:16	R	17h	N/A (Hard-coded)
	Size of each step in the gain range: 0 to 127 = .25dB to 32dB, in .25dB steps.			
Rsvd2	15	R	0h	N/A (Hard-coded)
	Reserved.			
NumSteps	14:8	R	03h	N/A (Hard-coded)
	Number of gains steps (number of possible settings - 1).			
Rsvd1	7	R	0h	N/A (Hard-coded)
	Reserved.			
Offset	6:0	R	03h	N/A (Hard-coded)
	Indicates which step is 0dB			

7.14.2. DigBeep (NID = 1Ch): OutAmpLeft

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				3A0h
Get	BA000h			

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Field Name	Bits	R/W	Default	Reset
Rsvd2	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
Mute	7	RW	0h	POR - DAFG - ULR
	Amp mute: 1 = muted, 0 = not muted.			
Rsvd1	6:2	R	00h	N/A (Hard-coded)
	Reserved.			
Gain	1:0	RW	1h	POR - DAFG - ULR
	Amp gain step number (see OutAmpCap parameter pertaining to this widget).			

7.14.3. DigBeep (NID = 1Ch): PwrState

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				705h
Get	F0500h			

Field Name	Bits	R/W	Default	Reset
Rsvd4	31:11	R	000000h	N/A (Hard-coded)
	Reserved.			
SettingsReset	10	R	1h	POR - DAFG - ULR
	Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget.			
Rsvd3	9	R	0h	N/A (Hard-coded)
	Reserved.			
Error	8	R	0h	POR - DAFG - ULR
	Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state.			

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Field Name	Bits	R/W	Default	Reset
Rsvd2	7:6	R	0h	N/A (Hard-coded)
	Reserved.			
Act	5:4	R	3h	POR - DAFG - LR
	Actual power state of this widget.			
Rsvd1	3:2	R	0h	N/A (Hard-coded)
	Reserved.			
Set	1:0	RW	0h	POR - DAFG - LR
	Current power state setting for this widget.			

7.14.4. DigBeep (NID = 1Ch): Gen

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				70Ah
Get	F0A00h			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
Divider	7:0	RW	00h	POR - DAFG - LR
	Enable internal PC-Beep generation. Divider == 00h disables internal PC Beep generation and enables normal operation of the codec. Divider != 00h generates the beep tone on all Pin Complexes that are currently configured as outputs. The HD Audio spec states that the beep tone frequency = (48kHz HD Audio SYNC rate) / (4*Divider), producing tones from 47 Hz to 12 kHz (logarithmic scale).			

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7.15. Mixer (NID = 1Dh): WCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0009h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:24	R	00h	N/A (Hard-coded)
	Reserved.			
Type	23:20	R	2h	N/A (Hard-coded)
	Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined			
Delay	19:16	R	0h	N/A (Hard-coded)
	Number of sample delays through widget.			
Rsvd1	15:12	R	0h	N/A (Hard-coded)
	Reserved.			
SwapCap	11	R	0h	N/A (Hard-coded)
	Left/right swap support: 1 = yes, 0 = no.			
PwrCntrl	10	R	1h	N/A (Hard-coded)
	Power state support: 1 = yes, 0 = no.			
Dig	9	R	0h	N/A (Hard-coded)
	Digital stream support: 1 = yes (digital), 0 = no (analog).			
ConnList	8	R	1h	N/A (Hard-coded)
	Connection list present: 1 = yes, 0 = no.			

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Field Name	Bits	R/W	Default	Reset
UnSolCap	7	R	0h	N/A (Hard-coded)
	Unsolicited response support: 1 = yes, 0 = no.			
ProcWidget	6	R	0h	N/A (Hard-coded)
	Processing state support: 1 = yes, 0 = no.			
Stripe	5	R	0h	N/A (Hard-coded)
	Striping support: 1 = yes, 0 = no.			
FormatOvrd	4	R	0h	N/A (Hard-coded)
	Stream format override: 1 = yes, 0 = no.			
AmpParOvrd	3	R	1h	N/A (Hard-coded)
	Amplifier capabilities override: 1 = yes, no.			
OutAmpPrsnt	2	R	0h	N/A (Hard-coded)
	Output amp present: 1 = yes, 0 = no.			
InAmpPrsnt	1	R	1h	N/A (Hard-coded)
	Input amp present: 1 = yes, 0 = no.			
Stereo	0	R	1h	N/A (Hard-coded)
	Stereo stream support: 1 = yes (stereo), 0 = no (mono).			

7.15.1. Mixer (NID = 1Dh): InAmpCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Dh			

Field Name	Bits	R/W	Default	Reset
Mute	31	R	1h	N/A (Hard-coded)
	Mute support: 1 = yes, 0 = no.			

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Field Name	Bits	R/W	Default	Reset
Rsvd3	30:23	R	00h	N/A (Hard-coded)
	Reserved.			
StepSize	22:16	R	05h	N/A (Hard-coded)
	Size of each step in the gain range: 0 to 127 = .25dB to 32dB, in .25dB steps.			
Rsvd2	15	R	0h	N/A (Hard-coded)
	Reserved.			
NumSteps	14:8	R	1Fh	N/A (Hard-coded)
	Number of gains steps (number of possible settings - 1).			
Rsvd1	7	R	0h	N/A (Hard-coded)
	Reserved.			
Offset	6:0	R	17h	N/A (Hard-coded)
	Indicates which step is 0dB			

7.15.2. Mixer (NID = 1Dh): ConLst

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Eh			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
LForm	7	R	0h	N/A (Hard-coded)
	Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries.			
ConL	6:0	R	03h	N/A (Hard-coded)
	Number of NID entries in connection list.			

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7.15.3. Mixer (NID = 1Dh): ConLstEntry0

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0200h			

Field Name	Bits	R/W	Default	Reset
ConL3	31:24	R	00h	N/A (Hard-coded)
	Unused			
ConL2	23:16	R	12h	N/A (Hard-coded)
	CD widget (0x12). Uses InAmpLeft4/InAmpRight4 controls.			
ConL1Range	15	R	1h	N/A (Hard-coded)
	ConL0..ConL1 define a range of selectable input			
ConL1	14:8	R	2Bh	N/A (Hard-coded)
	Inport3 Mux widget (0x2B). Uses InAmpLeft3/InAmpRight3 controls			
ConL0	7:0	R	28h	N/A (Hard-coded)
	Port C Pin widget (0x0C). Uses InAmpLeft0/InAmpRight0 controls.			

7.15.4. Mixer (NID = 1Dh): InAmpLeft0

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				360h
Get	B2000h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
Mute	7	RW	1h	POR - DAFG - ULR
	Amp mute: 1 = muted, 0 = not muted.			

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Field Name	Bits	R/W	Default	Reset
Rsvd1	6:5	R	0h	N/A (Hard-coded)
	Reserved.			
Gain	4:0	RW	17h	POR - DAFG - ULR
	Amp gain step number (see InAmpCap parameter pertaining to this widget).			

7.15.5. Mixer (NID = 1Dh): InAmpRight0

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				350h
Get	B0000h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
Mute	7	RW	1h	POR - DAFG - ULR
	Amp mute: 1 = muted, 0 = not muted.			
Rsvd1	6:5	R	0h	N/A (Hard-coded)
	Reserved.			
Gain	4:0	RW	17h	POR - DAFG - ULR
	Amp gain step number (see InAmpCap parameter pertaining to this widget).			

7.15.6. Mixer (NID = 1Dh): InAmpLeft1

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				361h
Get	B2001h			

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Field Name	Bits	R/W	Default	Reset
Rsvd2	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
Mute	7	RW	1h	POR - DAFG - ULR
	Amp mute: 1 = muted, 0 = not muted.			
Rsvd1	6:5	R	0h	N/A (Hard-coded)
	Reserved.			
Gain	4:0	RW	17h	POR - DAFG - ULR
	Amp gain step number (see InAmpCap parameter pertaining to this widget).			

7.15.7. Mixer (NID = 1Dh): InAmpRight1

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				351h
Get	B0001h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
Mute	7	RW	1h	POR - DAFG - ULR
	Amp mute: 1 = muted, 0 = not muted.			
Rsvd1	6:5	R	0h	N/A (Hard-coded)
	Reserved.			
Gain	4:0	RW	17h	POR - DAFG - ULR
	Amp gain step number (see InAmpCap parameter pertaining to this widget).			

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7.15.8. Mixer (NID = 1Dh): InAmpLeft2

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				362h
Get	B2002h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
Mute	7	RW	1h	POR - DAFG - ULR
	Amp mute: 1 = muted, 0 = not muted.			
Rsvd1	6:5	R	0h	N/A (Hard-coded)
	Reserved.			
Gain	4:0	RW	17h	POR - DAFG - ULR
	Amp gain step number (see InAmpCap parameter pertaining to this widget).			

7.15.9. Mixer (NID = 1Dh): InAmpRight2

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				352h
Get	B0002h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
Mute	7	RW	1h	POR - DAFG - ULR
	Amp mute: 1 = muted, 0 = not muted.			
Rsvd1	6:5	R	0h	N/A (Hard-coded)
	Reserved.			

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Field Name	Bits	R/W	Default	Reset
Gain	4:0	RW	17h	POR - DAFG - ULR
	Amp gain step number (see InAmpCap parameter pertaining to this widget).			

7.15.10. Mixer (NID = 1Dh): InAmpLeft3

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				363h
Get	B2003h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
Mute	7	RW	1h	POR - DAFG - ULR
	Amp mute: 1 = muted, 0 = not muted.			
Rsvd1	6:5	R	0h	N/A (Hard-coded)
	Reserved.			
Gain	4:0	RW	17h	POR - DAFG - ULR
	Amp gain step number (see InAmpCap parameter pertaining to this widget).			

7.15.11. Mixer (NID = 1Dh): InAmpRight3

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				353h
Get	B0003h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			

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Field Name	Bits	R/W	Default	Reset
Mute	7	RW	1h	POR - DAFG - ULR
	Amp mute: 1 = muted, 0 = not muted.			
Rsvd1	6:5	R	0h	N/A (Hard-coded)
	Reserved.			
Gain	4:0	RW	17h	POR - DAFG - ULR
	Amp gain step number (see InAmpCap parameter pertaining to this widget).			

7.15.12. Mixer (NID = 1Dh): InAmpLeft4

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				364h
Get	B2004h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
Mute	7	RW	1h	POR - DAFG - ULR
	Amp mute: 1 = muted, 0 = not muted.			
Rsvd1	6:5	R	0h	N/A (Hard-coded)
	Reserved.			
Gain	4:0	RW	17h	POR - DAFG - ULR
	Amp gain step number (see InAmpCap parameter pertaining to this widget).			

7.15.13. Mixer (NID = 1Dh): InAmpRight4

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				354h
Get	B0004h			

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Field Name	Bits	R/W	Default	Reset
Rsvd2	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
Mute	7	RW	1h	POR - DAFG - ULR
	Amp mute: 1 = muted, 0 = not muted.			
Rsvd1	6:5	R	0h	N/A (Hard-coded)
	Reserved.			
Gain	4:0	RW	17h	POR - DAFG - ULR
	Amp gain step number (see InAmpCap parameter pertaining to this widget).			

7.15.14. Mixer (NID = 1Dh): PwrState

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				705h
Get	F0500h			

Field Name	Bits	R/W	Default	Reset
Rsvd4	31:11	R	000000h	N/A (Hard-coded)
	Reserved.			
SettingsReset	10	R	1h	POR - DAFG - ULR
	Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget.			
Rsvd3	9	R	0h	N/A (Hard-coded)
	Reserved.			
Error	8	R	0h	POR - DAFG - ULR
	Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state.			

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Field Name	Bits	R/W	Default	Reset
Rsvd2	7:6	R	0h	N/A (Hard-coded)
	Reserved.			
Act	5:4	R	3h	POR - DAFG - LR
	Actual power state of this widget.			
Rsvd1	3:2	R	0h	N/A (Hard-coded)
	Reserved.			
Set	1:0	RW	0h	POR - DAFG - LR
	Current power state setting for this widget.			

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7.16. MixerOutVol (NID = 1Eh): WCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0009h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:24	R	00h	N/A (Hard-coded)
	Reserved.			
Type	23:20	R	3h	N/A (Hard-coded)
	Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined			
Delay	19:16	R	0h	N/A (Hard-coded)
	Number of sample delays through widget.			
Rsvd1	15:12	R	0h	N/A (Hard-coded)
	Reserved.			
SwapCap	11	R	0h	N/A (Hard-coded)
	Left/right swap support: 1 = yes, 0 = no.			
PwrCntrl	10	R	1h	N/A (Hard-coded)
	Power state support: 1 = yes, 0 = no.			
Dig	9	R	0h	N/A (Hard-coded)
	Digital stream support: 1 = yes (digital), 0 = no (analog).			
ConnList	8	R	1h	N/A (Hard-coded)
	Connection list present: 1 = yes, 0 = no.			

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Field Name	Bits	R/W	Default	Reset
UnSolCap	7	R	0h	N/A (Hard-coded)
	Unsolicited response support: 1 = yes, 0 = no.			
ProcWidget	6	R	0h	N/A (Hard-coded)
	Processing state support: 1 = yes, 0 = no.			
Stripe	5	R	0h	N/A (Hard-coded)
	Striping support: 1 = yes, 0 = no.			
FormatOvrd	4	R	0h	N/A (Hard-coded)
	Stream format override: 1 = yes, 0 = no.			
AmpParOvrd	3	R	1h	N/A (Hard-coded)
	Amplifier capabilities override: 1 = yes, no.			
OutAmpPrsnt	2	R	1h	N/A (Hard-coded)
	Output amp present: 1 = yes, 0 = no.			
InAmpPrsnt	1	R	0h	N/A (Hard-coded)
	Input amp present: 1 = yes, 0 = no.			
Stereo	0	R	1h	N/A (Hard-coded)
	Stereo stream support: 1 = yes (stereo), 0 = no (mono).			

7.16.1. MixerOutVol (NID = 1Eh): ConLst

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Eh			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			

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Field Name	Bits	R/W	Default	Reset
LForm	7	R	0h	N/A (Hard-coded)
	Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries.			
ConL	6:0	R	01h	N/A (Hard-coded)
	Number of NID entries in connection list.			

7.16.2. MixerOutVol (NID = 1Eh): ConLstEntry0

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0200h			

Field Name	Bits	R/W	Default	Reset
ConL3	31:24	R	00h	N/A (Hard-coded)
	Unused list entry.			
ConL2	23:16	R	00h	N/A (Hard-coded)
	Unused list entry.			
ConL1	15:8	R	00h	N/A (Hard-coded)
	Unused list entry.			
ConL0	7:0	R	1Dh	N/A (Hard-coded)
	Mixer Summing widget (0x1D)			

7.16.3. MixerOutVol (NID = 1Dh): OutAmpCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0012h			

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Field Name	Bits	R/W	Default	Reset
Mute	31	R	1h	N/A (Hard-coded)
	Mute support: 1 = yes, 0 = no.			
Rsvd3	30:23	R	00h	N/A (Hard-coded)
	Reserved.			
StepSize	22:16	R	05h	N/A (Hard-coded)
	Size of each step in the gain range: 0 to 127 = .25dB to 32dB, in .25dB steps.			
Rsvd2	15	R	0h	N/A (Hard-coded)
	Reserved.			
NumSteps	14:8	R	1Fh	N/A (Hard-coded)
	Number of gains steps (number of possible settings - 1).			
Rsvd1	7	R	0h	N/A (Hard-coded)
	Reserved.			
Offset	6:0	R	1Fh	N/A (Hard-coded)
	Indicates which step is 0dB			

7.16.4. MixerOutVol (NID = 1Dh): OutAmpLeft

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				3A0h
Get	BA000h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
Mute	7	RW	1h	POR - DAFG - ULR
	Amp mute: 1 = muted, 0 = not muted.			

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Field Name	Bits	R/W	Default	Reset
Rsvd1	6:5	R	0h	N/A (Hard-coded)
	Reserved.			
Gain	4:0	RW	1Fh	POR - DAFG - ULR
	Amp gain step number (see OutAmpCap parameter pertaining to this widget).			

7.16.5. MixerOutVol (NID = 1Dh): OutAmpRight

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				390h
Get	B8000h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			
Mute	7	RW	1h	POR - DAFG - ULR
	Amp mute: 1 = muted, 0 = not muted.			
Rsvd1	6:5	R	0h	N/A (Hard-coded)
	Reserved.			
Gain	4:0	RW	1Fh	POR - DAFG - ULR
	Amp gain step number (see OutAmpCap parameter pertaining to this widget).			

7.16.6. MixerOutVol (NID = 1Dh): PwrState

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				705h
Get	F0500h			

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Field Name	Bits	R/W	Default	Reset
Rsvd4	31:11	R	000000h	N/A (Hard-coded)
	Reserved.			
SettingsReset	10	R	1h	POR - DAFG - ULR
	Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget.			
Rsvd3	9	R	0h	N/A (Hard-coded)
	Reserved.			
Error	8	R	0h	POR - DAFG - ULR
	Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state.			
Rsvd2	7:6	R	0h	N/A (Hard-coded)
	Reserved.			
Act	5:4	R	3h	POR - DAFG - LR
	Actual power state of this widget.			
Rsvd1	3:2	R	0h	N/A (Hard-coded)
	Reserved.			
Set	1:0	RW	0h	POR - DAFG - LR
	Current power state setting for this widget.			

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7.17. Vendor Reserved (NID = 1Fh)

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7.37. InPort2Mux (NID = 2Ah): WCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0009h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:24	R	00h	N/A (Hard-coded)
	Reserved.			
Type	23:20	R	3h	N/A (Hard-coded)
	Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined			
Delay	19:16	R	0h	N/A (Hard-coded)
	Number of sample delays through widget.			
Rsvd1	15:12	R	0h	N/A (Hard-coded)
	Reserved.			
SwapCap	11	R	0h	N/A (Hard-coded)
	Left/right swap support: 1 = yes, 0 = no.			
PwrCntrl	10	R	1h	N/A (Hard-coded)
	Power state support: 1 = yes, 0 = no.			
DigitalStrm	9	R	0h	N/A (Hard-coded)
	Digital stream support: 1 = yes (digital), 0 = no (analog).			
ConnList	8	R	1h	N/A (Hard-coded)
	Connection list present: 1 = yes, 0 = no.			

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Field Name	Bits	R/W	Default	Reset
UnsolCap	7	R	0h	N/A (Hard-coded)
	Unsolicited response support: 1 = yes, 0 = no.			
ProcWidget	6	R	0h	N/A (Hard-coded)
	Processing state support: 1 = yes, 0 = no.			
Stripe	5	R	0h	N/A (Hard-coded)
	Striping support: 1 = yes, 0 = no.			
FormatOvrd	4	R	0h	N/A (Hard-coded)
	Stream format override: 1 = yes, 0 = no.			
AmpParamOvrd	3	R	0h	N/A (Hard-coded)
	Amplifier capabilities override: 1 = yes, no.			
OutAmpPrsnt	2	R	0h	N/A (Hard-coded)
	Output amp present: 1 = yes, 0 = no.			
InAmpPrsnt	1	R	0h	N/A (Hard-coded)
	Input amp present: 1 = yes, 0 = no.			
Stereo	0	R	1h	N/A (Hard-coded)
	Stereo stream support: 1 = yes (stereo), 0 = no (mono).			

7.37.1. InPort2Mux (NID = 2Ah): ConLst

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Eh			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			

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Field Name	Bits	R/W	Default	Reset
LForm	7	R	0h	N/A (Hard-coded)
	Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries.			
ConL	6:0	R	04h	N/A (Hard-coded)
	Number of NID entries in connection list.			

7.37.2. InPort2Mux (NID = 2Ah): ConLstEntry0

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0200h			

Field Name	Bits	R/W	Default	Reset
ConL3	31:24	R	11h	N/A (Hard-coded)
	Port H Pin widget (0x11)Port H Pin widget (0x11)			
ConL2	23:16	R	10h	N/A (Hard-coded)
	Port G Pin widget (0x10)			
ConL1	15:8	R	0Ch	N/A (Hard-coded)
	Port C Pin widget (0x0C)			
ConL0	7:0	R	0Bh	N/A (Hard-coded)
	Port B Pin widget (0x0B)			

7.37.3. InPort2Mux (NID = 2Ah): ConSelectCtrl

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				701h
Get	F0100h			

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Field Name	Bits	R/W	Default	Reset
Rsvd	31:3	R	00000000h	N/A (Hard-coded)
	Reserved.			
Index	2:0	RW	0h	POR - DAFG - ULR
	Connection select control index.			

7.37.4. InPort2Mux (NID = 2Ah): PwrState

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				705h
Get	F0500h			

Field Name	Bits	R/W	Default	Reset
Rsvd4	31:11	R	000000h	N/A (Hard-coded)
	Reserved.			
SettingsReset	10	R	1h	POR - DAFG - ULR
	Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget.			
Rsvd3	9	R	0h	N/A (Hard-coded)
	Reserved.			
Error	8	R	0h	POR - DAFG - ULR
	Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state.			
Rsvd2	7:6	R	0h	N/A (Hard-coded)
	Reserved.			
Act	5:4	R	3h	POR - DAFG - LR
	Actual power state of this widget.			

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Field Name	Bits	R/W	Default	Reset
Rsvd1	3:2	R	0h	N/A (Hard-coded)
	Reserved.			
Set	1:0	RW	0h	POR - DAFG - LR
	Current power state setting for this widget.			

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7.38. InPort3Mux (NID = 2Bh): WCap

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0009h			

Field Name	Bits	R/W	Default	Reset
Rsvd2	31:24	R	00h	N/A (Hard-coded)
	Reserved.			
Type	23:20	R	3h	N/A (Hard-coded)
	Widget type: 0h = Out Converter 1h = In Converter 2h = Summing (Mixer) 3h = Selector (Mux) 4h = Pin Complex 5h = Power 6h = Volume Knob 7h = Beep Generator 8h-Eh = Reserved Fh = Vendor Defined			
Delay	19:16	R	0h	N/A (Hard-coded)
	Number of sample delays through widget.			
Rsvd1	15:12	R	0h	N/A (Hard-coded)
	Reserved.			
SwapCap	11	R	0h	N/A (Hard-coded)
	Left/right swap support: 1 = yes, 0 = no.			
PwrCntrl	10	R	1h	N/A (Hard-coded)
	Power state support: 1 = yes, 0 = no.			
DigitalStrm	9	R	0h	N/A (Hard-coded)
	Digital stream support: 1 = yes (digital), 0 = no (analog).			
ConnList	8	R	1h	N/A (Hard-coded)
	Connection list present: 1 = yes, 0 = no.			

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Field Name	Bits	R/W	Default	Reset
UnsolCap	7	R	0h	N/A (Hard-coded)
	Unsolicited response support: 1 = yes, 0 = no.			
ProcWidget	6	R	0h	N/A (Hard-coded)
	Processing state support: 1 = yes, 0 = no.			
Stripe	5	R	0h	N/A (Hard-coded)
	Striping support: 1 = yes, 0 = no.			
FormatOvrd	4	R	0h	N/A (Hard-coded)
	Stream format override: 1 = yes, 0 = no.			
AmpParamOvrd	3	R	0h	N/A (Hard-coded)
	Amplifier capabilities override: 1 = yes, no.			
OutAmpPrsnt	2	R	0h	N/A (Hard-coded)
	Output amp present: 1 = yes, 0 = no.			
InAmpPrsnt	1	R	0h	N/A (Hard-coded)
	Input amp present: 1 = yes, 0 = no.			
Stereo	0	R	1h	N/A (Hard-coded)
	Stereo stream support: 1 = yes (stereo), 0 = no (mono).			

7.38.1. InPort3Mux (NID = 2Bh): ConLst

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F000Eh			

Field Name	Bits	R/W	Default	Reset
Rsvd	31:8	R	000000h	N/A (Hard-coded)
	Reserved.			

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Field Name	Bits	R/W	Default	Reset
LForm	7	R	0h	N/A (Hard-coded)
	Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries.			
ConL	6:0	R	04h	N/A (Hard-coded)
	Number of NID entries in connection list.			

7.38.2. InPort3Mux (NID = 2Bh): ConLstEntry0

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				
Get	F0200h			

Field Name	Bits	R/W	Default	Reset
ConL3	31:24	R	18h	N/A (Hard-coded)
	DAC3 widget (0x18)			
ConL2	23:16	R	17h	N/A (Hard-coded)
	DAC2 widget (0x17)			
ConL1	15:8	R	16h	N/A (Hard-coded)
	DAC1 widget (0x16)			
ConL0	7:0	R	15h	N/A (Hard-coded)
	DAC0 widget (0x15			

7.38.3. InPort3Mux (NID = 2Bh): ConSelectCtrl

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				701h
Get	F0100h			

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Field Name	Bits	R/W	Default	Reset
Rsvd	31:3	R	00000000h	N/A (Hard-coded)
	Reserved.			
Index	2:0	RW	0h	POR - DAFG - ULR
	Connection select control index.			

7.38.4. InPort3Mux (NID = 2Bh): PwrState

Reg	Byte 4 (Bits 31:24)	Byte 3 (Bits 23:16)	Byte 2 (Bits 15:8)	Byte 1 (Bits 7:0)
Set				705h
Get	F0500h			

Field Name	Bits	R/W	Default	Reset
Rsvd4	31:11	R	000000h	N/A (Hard-coded)
	Reserved.			
SettingsReset	10	R	1h	POR - DAFG - ULR
	Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget.			
Rsvd3	9	R	0h	N/A (Hard-coded)
	Reserved.			
Error	8	R	0h	POR - DAFG - ULR
	Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state.			
Rsvd2	7:6	R	0h	N/A (Hard-coded)
	Reserved.			
Act	5:4	R	3h	POR - DAFG - LR
	Actual power state of this widget.			

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Field Name	Bits	R/W	Default	Reset
Rsvd1	3:2	R	0h	N/A (Hard-coded)
	Reserved.			
Set	1:0	RW	0h	POR - DAFG - LR
	Current power state setting for this widget.			

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8. PINOUTS AND PACKAGING

8.1. 48QFP

8.1.1. 48 QFP Pin Assignment

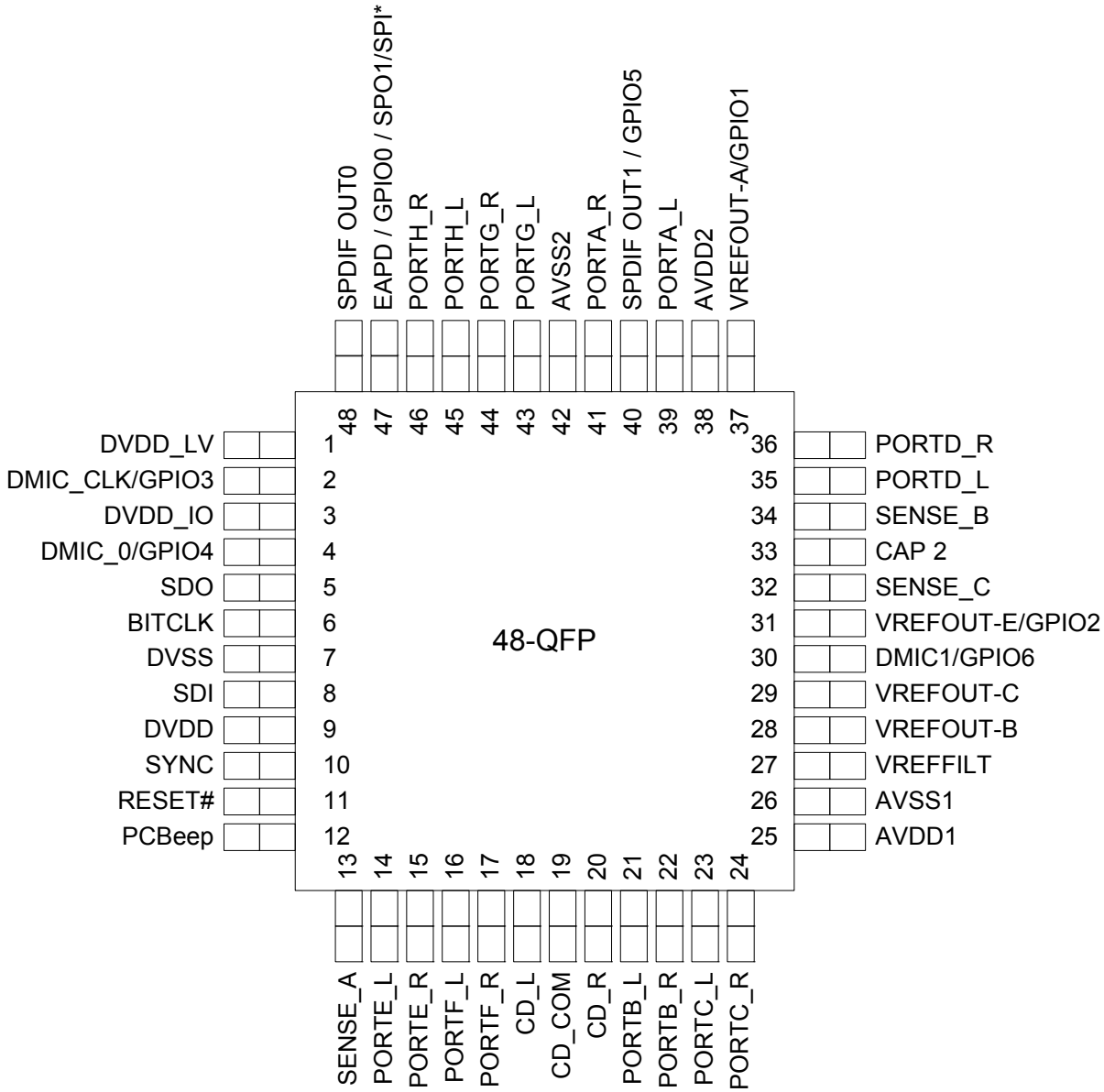


Figure 14. Pin Assignment

8.1.2. 48QFP Pin Table

Pin Name	Pin Function	I/O	Internal Pull-up Pull-down	48 pin location
DVDD_LV	1.5V Digital Core Regulator Filter Cap	O(Power)	None	1

Table 31. 48QFP Pin Table

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Pin Name	Pin Function	I/O	Internal Pull-up Pull-down	48 pin location
DMIC_CLK/GPIO3	Digital Mic Clock Output/GPIO3	I/O(Digital)	60K Pull-down	2
DVDD_IO	Reference Voltage (1.5V or 3.3V)	I(Power)	None	3
DMIC0/GPIO4	Digital Mic 01 Input/GPIO4	I/O(Digital)	60K Pull-down	4
SDATA_OUT	HD Audio Serial Data output from controller	I(Digital)	None	5
BITCLK	HD Audio Bit Clock	I(Digital)	None	6
DVSS	Digital Ground	I(Digital)	None	7
SDATA_IN	HD Audio Serial Data Input to controller	I/O(Digital)	None	8
DVDD	Digital Vdd= 3.3V	I(Power)	None	9
SYNC	HD Audio Frame Sync	I(Digital)	None	10
RESET#	HD Audio Reset	I(Digital)	None	11
PCBeep	PC Beep Input	I(Analog)	None	12
SENSE_A	Jack insertion detection	I(Analog)	None	13
PORTE_L	Port E Left	I/O(Analog)	None	14
PORTE_R	Port E Right	I/O(Analog)	None	15
PORTF_L	Port F Left	I/O(Analog)	None	16
PORTF_R	Port F Right	I/O(Analog)	None	17
CD Left	CD Left	I(Analog)	None	18
CD Common	CD L/R return	I(Analog)	None	19
CD Right	CD Right	I(Analog)	None	20
PORTB_L (HP)	Port B Output Left	I/O(Analog)	None	21
PORTB_R (HP)	Port B Output Right	I/O(Analog)	None	22
PORTC_L	Port C Left	I/O(Analog)	None	23
PORTC_R	Port C Right	I/O(Analog)	None	24
AVDD1	Analog Vdd=5.0V or 3.3V	I(Analog)	None	25
AVSS1	Analog Ground	I(Analog)	None	26
VREFFILT	Analog Virtual Ground	O(Analog)	None	27
VREFOUT-B	Reference Voltage out drive (intended for mic bias)	O(Analog)	None	28
VREFOUT-C	Reference Voltage out drive (intended for mic bias)	O (Analog)	None	29
DMIC1 / GPIO6	Digital Mic 23 Input/GPIO6	I/O (Analog)	60K Pull-down	30
VREFOUT-E / GPIO2	Reference Voltage out drive (intended for mic bias) or General Purpose I/O	O(Analog)	None	31
SENSE_C	Jack insertion detection	I(Analog)	None	32
CAP 2	ADC reference bypass capacitor	O(Analog)	None	33
SENSE_B	Jack insertion detection	I(Analog)	None	34
PORTD_L (HP)	Port D Output Left	I/O(Analog)	None	35
PORTD_R (HP)	Port D Output Right	I/O(Analog)	None	36

Table 31. 48QFP Pin Table

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Pin Name	Pin Function	I/O	Internal Pull-up Pull-down	48 pin location
VREFOUT-A / GPIO1	Reference Voltage out drive (intended for mic bias) or General Purpose I/O	O(Analog)	None	37
AVDD2	Analog Supply for VREG	I(Power)	None	38
PORTA_L (HP)	Port A Output Left	I/O(Analog)	None	39
SPDIFOUT1/ GPIO5	SPDIF Output, or General Purpose I/O	I/O(AVDD supply)	60K Pull-down	40
PORTA_R (HP)	Port A Output Right	I/O(Analog)	None	41
AVSS	Analog Ground	I(Power)	None	42
PORTG_L	Port G Left	I/O(Analog)	None	43
PORTG_R	Port G Right	I/O(Analog)	None	44
PORTH_L	Port H Left	I/O(Analog)	None	45
PORTH_R	Port H Right	I/O(Analog)	None	46
EAPD/SPDIF_IN/GPIO0/SPDIF_OUT 1	EAPD, SPDIF input, SPDIF output 1, GPIO0	I/O(Digital)	60K Pull-Up/Down	47
SPDIFOUT0	SPDIF 0utput	O(Digital)	60K pull-down	48

Table 31. 48QFP Pin Table

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8.1.3. 48QFP Package Outline and Package Dimensions

Package dimensions are kept current with JEDEC Publication No. 95

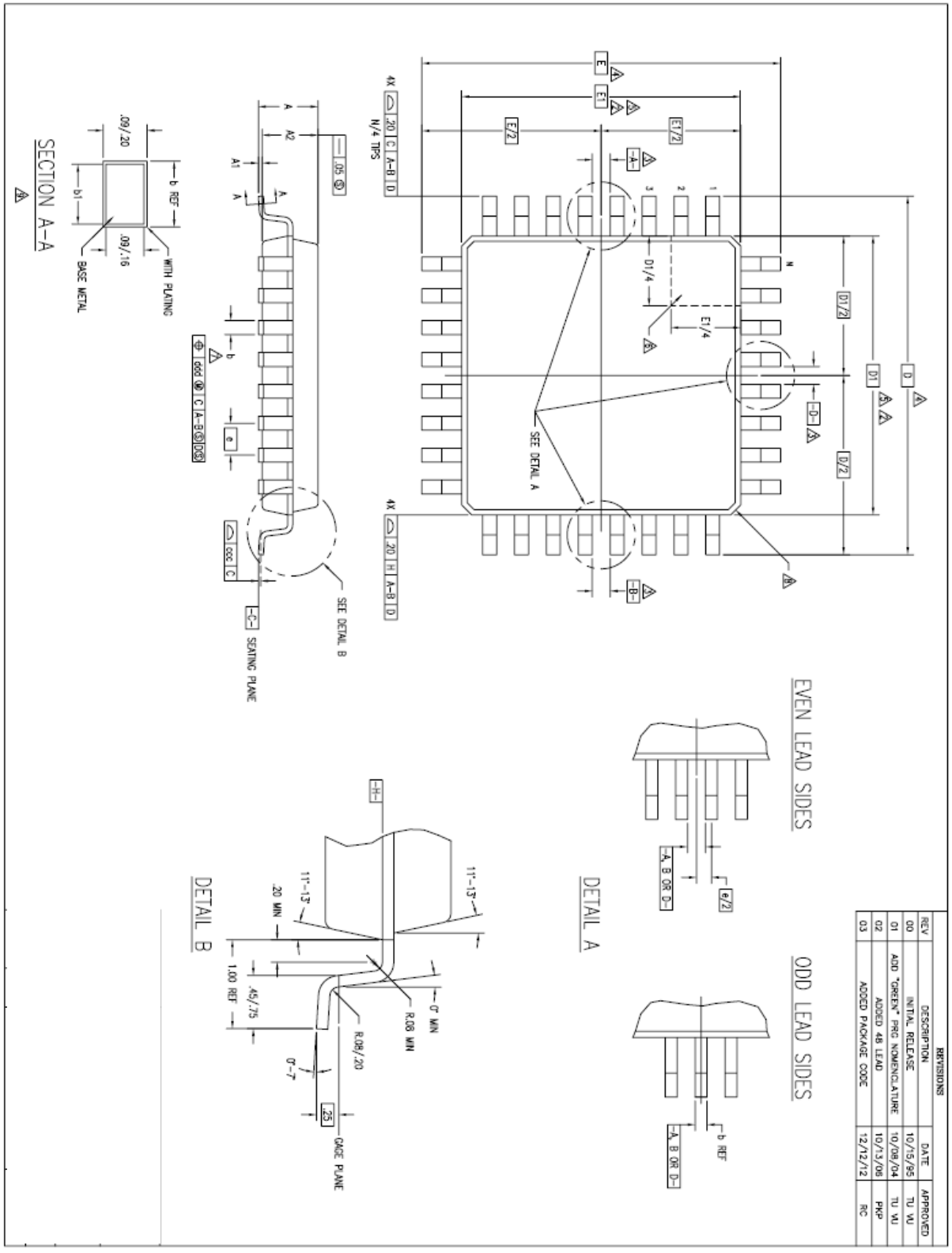


Figure 15. 48QFP Package Diagram

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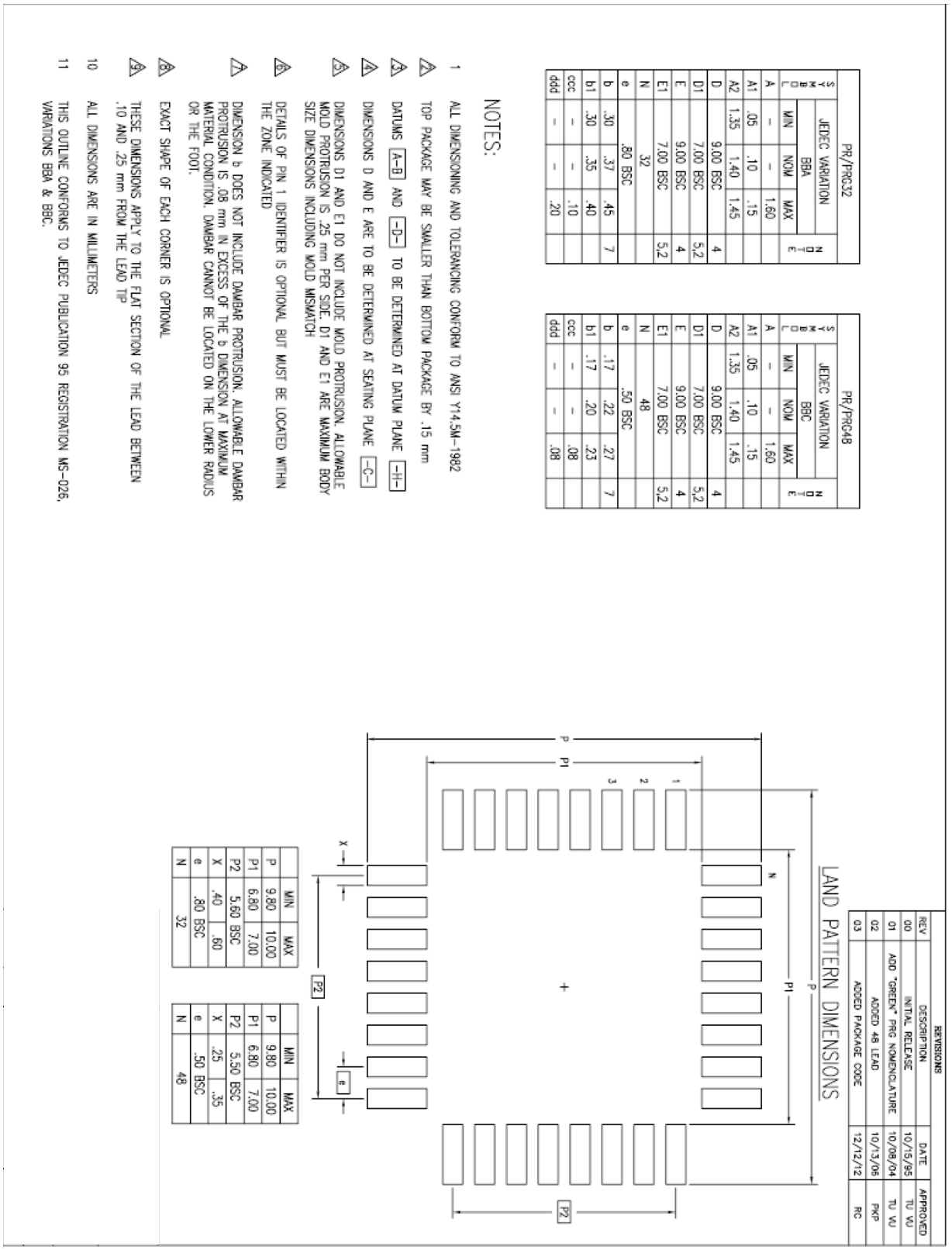


Figure 16. 48QFP Package Diagram (cont)

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8.2. 40QFN

8.2.1. 40QFN Pin Assignment

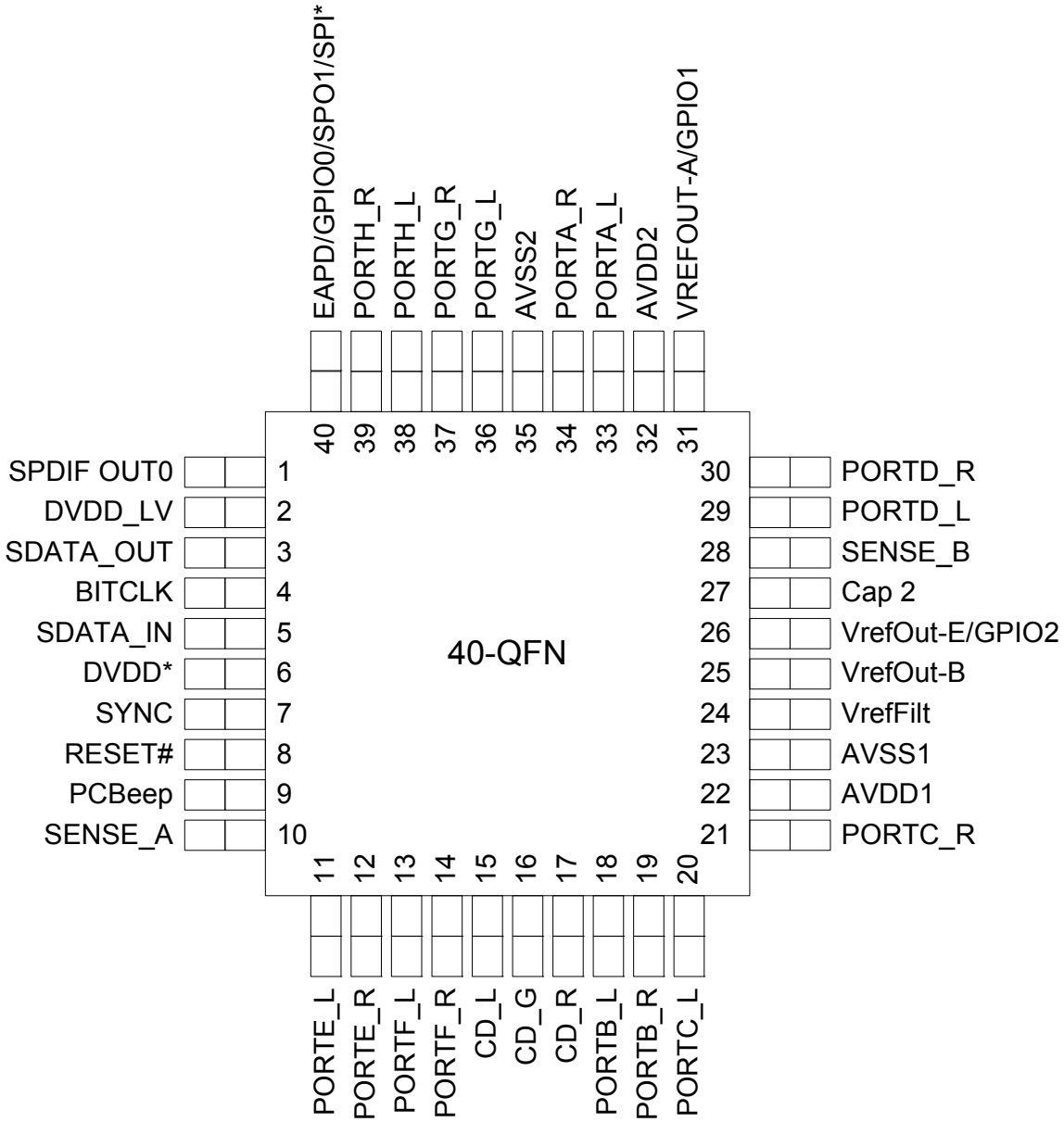


Figure 17. Pin Assignment

The DAP pad must be connected to DVSS on the 40-pin package.

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8.2.2. 40QFN Pin Table)

Pin Name	Pin Function	I/O	Internal Pull-up Pull-down	40 pin location
SPDIFOUT0	SPDIF 0utput	O(Digital)	60K pull-down	1
DVDD_LV	1.5V Digital Core Regulator Filter Cap	O(Power)	None	2
SDATA_OUT	HD Audio Serial Data output from controller	I(Digital)	None	3
BITCLK	HD Audio Bit Clock	I(Digital)	None	4
SDATA_IN	HD Audio Serial Data Input to controller	I/O(Digital)	None	5
DVDD	Digital Vdd= 3.3V	I(Power)	None	6
SYNC	HD Audio Frame Sync	I(Digital)	None	7
RESET#	HD Audio Reset	I(Digital)	None	8
PCBeep	PC Beep input	I(Analog)	None	9
SENSE_A	Jack insertion detection	I(Analog)	None	10
PORTE_L	Port E Left	I/O(Analog)	None	11
PORTE_R	Port E Right	I/O(Analog)	None	12
PORTF_L	Port F Left	I/O(Analog)	None	13
PORTF_R	Port F Right	I/O(Analog)	None	14
CD Left	CD Left	I(Analog)	None	15
CD Common	CD L/R return	I(Analog)	None	16
CD Right	CD Right	I(Analog)	None	17
PORTB_L (HP)	Port B Output Left	I/O(Analog)	None	18
PORTB_R (HP)	Port B Output Right	I/O(Analog)	None	19
PORTC_L	Port C Left	I/O(Analog)	None	20
PORTC_R	Port C Right	I/O(Analog)	None	21
AVDD1	Analog Vdd=5.0V or 3.3V	I(Analog)	None	22
AVSS1	Analog Ground	I(Analog)	None	23
VREFFILT	Analog Virtual Ground	O(Analog)	None	24
VREFOUT-B	Reference Voltage out drive (intended for mic bias)	O(Analog)	None	25
VREFOUT-E / GPIO2	Reference Voltage out drive (intended for mic bias) or General Purpose I/O	O(Analog)	None	26
CAP 2	ADC reference bypass capacitor	O(Analog)	None	27
SENSE_B	Jack insertion detection	I(Analog)	None	28
PORTD_L (HP)	Port D Output Left	I/O(Analog)	None	29
PORTD_R (HP)	Port D Output Right	I/O(Analog)	None	30
VREFOUT-A / GPIO1	Reference Voltage out drive (intended for mic bias) or General Purpose I/O	O(Analog)	None	31
AVDD2	Analog Supply for VREG	I(Power)	None	32
PORTA_L (HP)	Port A Output Left	I/O(Analog)	None	33
PORTA_R (HP)	Port A Output Right	I/O(Analog)	None	34

Table 32. 40QFN Pin Table

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Pin Name	Pin Function	I/O	Internal Pull-up Pull-down	40 pin location
AVSS	Analog Ground	I(Power)	None	35
PORTG_L	Port G Left	I/O(Analog)	None	36
PORTG_R	Port G Right	I/O(Analog)	None	37
PORTH_L	Port H Left	I/O(Analog)	None	38
PORTH_R	Port H Right	I/O(Analog)	None	39
EAPD/SPDIF_IN/GPIO0/SPDIF_OUT1	EAPD, SPDIF input, SPDIF output 1, GPIO0	I/O(Digital)	60K Pull-Up/Down	40
The DAP pad must be connected to DVSS on the 40-pin package				

Table 32. 40QFN Pin Table

8.2.3. 40QFN Package Outline and Package Dimensions

Package dimensions are kept current with JEDEC Publication No. 95

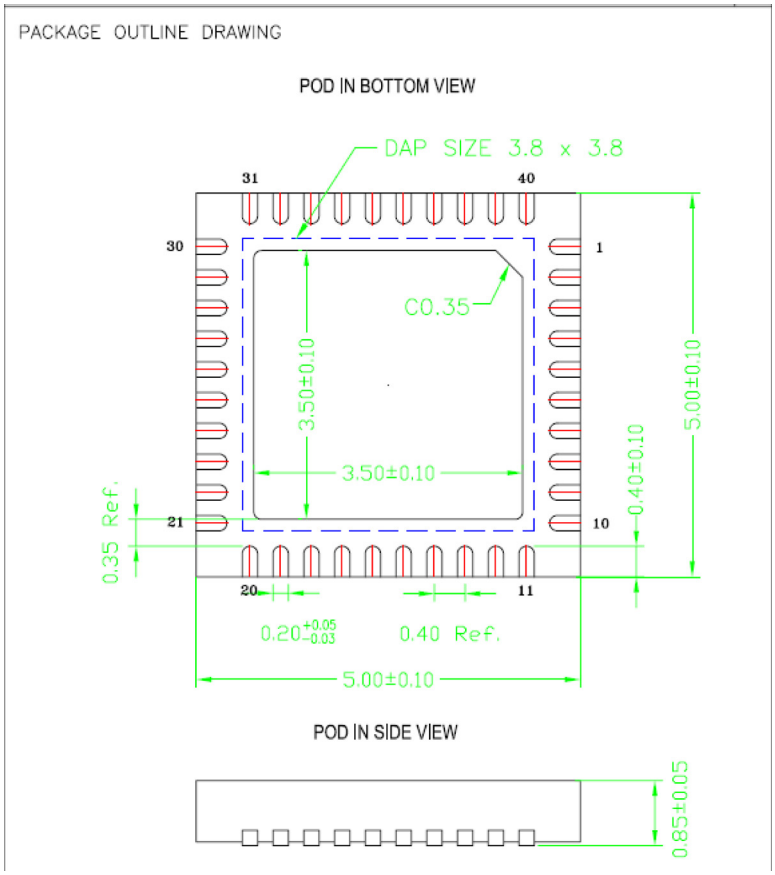


Figure 18. 40QFN Package Diagram

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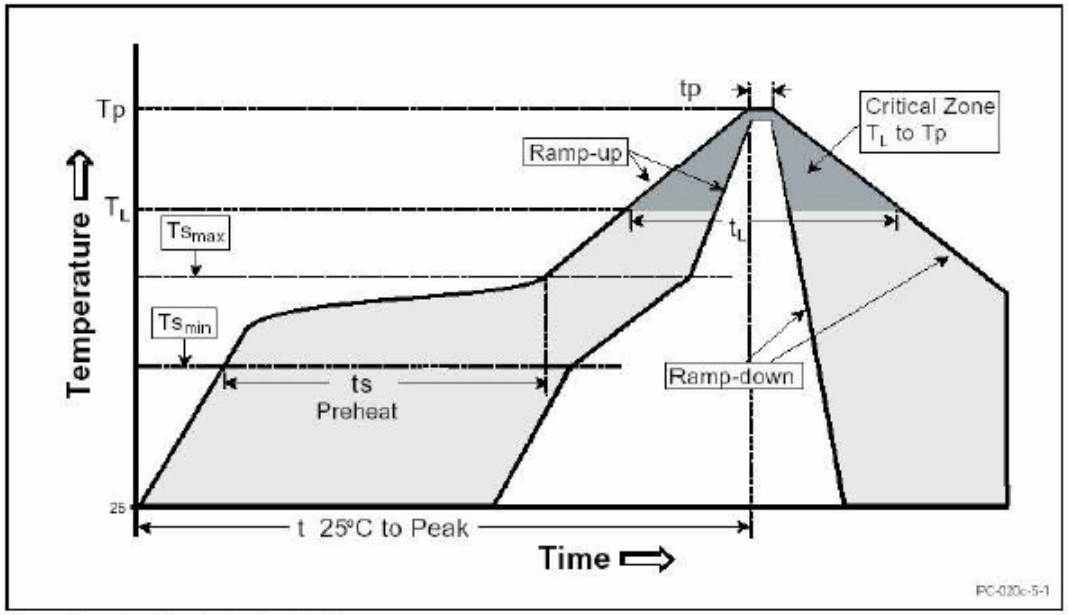
8.3. 48QFP and 40QFN Standard Reflow Profile Data

Note: These devices can be hand soldered at 360 °C for 3 to 5 seconds.

FROM: IPC / JEDEC J-STD-020C "Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices" (www.jedec.org/download).

Profile Feature		Pb Free Assembly
Average Ramp-Up Rate (Ts_{max} - Tp)		3 °C / second max
Preheat:	Temperature Min (Ts_{min}) Temperature Max (Ts_{max}) Time (ts_{min} - ts_{max})	150 °C 200 °C 60 - 180 seconds
Time maintained above:	Temperature (T_L) Time (t_L)	217 °C 60 - 150 seconds
Peak / Classification Temperature (Tp)		See "Package Classification Reflow Temperatures"
Time within 5 °C of actual Peak Temperature (tp)		20 - 40 seconds
Ramp-Down rate		6 °C / second max
Time 25 °C to Peak Temperature		8 minutes max
Note: All temperatures refer to topside of the package, measured on the package body surface.		

Table 33. Standard Reflow Profile



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10. DOCUMENT REVISION HISTORY

Revision	Date	Description of Change
1.0	September 2011	Initial release
1.1	Septembert 2014	Released in TSI format

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www.temposemi.com
8627 N. MoPac Expwy Suite 130
Austin, Texas 78759

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