

NB100LVEP56

2.5V / 3.3V ECL DUAL Differential 2:1 Multiplexer

Description

The NB100LVEP56 is a dual, fully differential 2:1 multiplexer. The differential data path makes the device ideal for multiplexing low skew clock or differential data signals. The device features both individual and common select inputs to address both data path and random logic applications. Common and individual selects can accept both LVECL and LVCMOS input voltage levels. Multiple V_{BB} pins are provided.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input operation, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μ F capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

Features

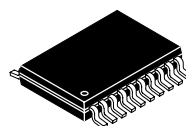
- Maximum Input Clock Frequency > 2.5 GHz Typical
- Maximum Input Data Rate > 2.5 Gb/s Typical
- 525 ps Typical Propagation Delays
- Low Profile QFN Package
- PECL Mode Operating Range:
 $V_{CC} = 2.375$ V to 3.8 V with $V_{EE} = 0$ V
- NECL Mode Operating Range:
 $V_{CC} = 0$ V with $V_{EE} = -2.375$ V to -3.8 V
- Separate, Common Select, and Individual Select
(Compatible with ECL and CMOS Input Voltage Levels)
- Q Output Will Default LOW with Inputs Open or at V_{EE}
- Multiple V_{BB} Outputs
- Pb-Free Packages are Available



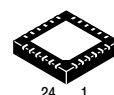
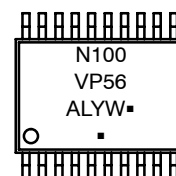
ON Semiconductor®

<http://onsemi.com>

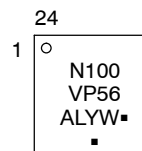
MARKING DIAGRAMS*



TSSOP-20
DT SUFFIX
CASE 948E



24 PIN QFN
MN SUFFIX
CASE 485L



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

NB100LVEP56

Table 1. PIN FUNCTION DESCRIPTION

| Pin No. | | Name | I/O | Default State | Description |
|---------|--------------|--|-----------------|---------------|---|
| TSSOP | QFN | | | | |
| 14,20 | 3,9,18,19,20 | V _{CC} | - | - | Positive Supply Voltage. All VCC Pins must be Externally Connected to Power Supply to Guarantee Proper Operation. |
| 11 | 15,24 | V _{EE} | - | - | Negative Supply Voltage. All VEE Pins must be Externally Connected to Power Supply to Guarantee Proper Operation. |
| 3,8 | 6,12 | V _{BB0} , V _{BB1} | - | - | ECL Reference Voltage Output |
| 1 | 4 | D0a | ECL Input | Low | Noninverted Differential Data a Input to MUX 0. Internal 75 kΩ to V _{EE} . |
| 2 | 5 | $\overline{D0a}$ | ECL Input | High | Inverted Differential Data a Input to MUX 0. Internal 75 kΩ to V _{EE} and 37 kΩ to V _{CC} . |
| 4 | 7 | D0b | ECL Input | Low | Noninverted Differential Data b Input to MUX 0. Internal 75 kΩ to V _{EE} . |
| 5 | 8 | $\overline{D0b}$ | ECL Input | High | Inverted Differential Data b Input to MUX 0. Internal 75 kΩ to V _{EE} and 37 kΩ to V _{CC} . |
| 6 | 10 | D1a | ECL Input | Low | Noninverted Differential Data a Input to MUX 1. Internal 75 kΩ to V _{EE} . |
| 7 | 11 | $\overline{D1a}$ | ECL Input | High | Inverted Differential Data a Input to MUX 1. Internal 75 kΩ to V _{EE} and 37 kΩ to V _{CC} . |
| 9 | 13 | D1b | ECL Input | Low | Noninverted Differential Data b Input to MUX 1. Internal 75 kΩ to V _{EE} . |
| 10 | 14 | $\overline{D1b}$ | ECL Input | High | Inverted Differential Data b Input to MUX 1. Internal 75 kΩ to V _{EE} and 37 kΩ to V _{CC} . |
| 19 | 2 | Q0 | ECL Output | - | Noninverted Differential Output MUX 0. Typically Terminated with 50 Ω to V _{TT} = V _{CC} - 2.0 V. |
| 18 | 1 | $\overline{Q0}$ | ECL Output | - | Inverted Differential Output MUX 0. Typically Terminated with 50 Ω to V _{TT} = V _{CC} - 2.0 V. |
| 13 | 17 | Q1 | ECL Output | - | Noninverted Differential Output MUX 1. Typically Terminated with 50 Ω to V _{TT} = V _{CC} - 2.0 V. |
| 12 | 16 | $\overline{Q1}$ | ECL Output | - | Inverted Differential Output MUX 1. Typically Terminated with 50 Ω to V _{TT} = V _{CC} - 2.0 V. |
| 17 | 23 | SEL0 | ECL, CMOS Input | Low | Noninverted Differential Select Input to MUX 0. Internal 75 Ω to V _{EE} . |
| 16 | 22 | COM_SEL | ECL, CMOS Input | Low | Noninverted Differential Common Select Input to Both MUX. Internal 75 Ω to V _{EE} . |
| 15 | 21 | SEL1 | ECL, CMOS Input | Low | Noninverted Differential Select Input to MUX 1. Internal 75 Ω to V _{EE} . |
| N/A | - | EP | - | - | Exposed Pad. (Note 1) |

1. The thermally conductive exposed pad on the package bottom (see case drawing) must be attached to a heat sinking conduit.

NB100LVEP56

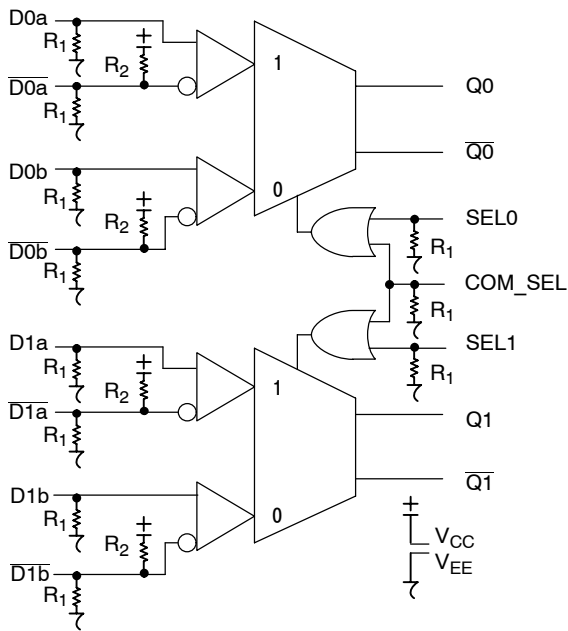


Figure 1. Logic Diagram

Table 2. TRUTH TABLE

| SEL0 | SEL1 | COM_SEL | Q0, Q0̄ | Q1, Q1̄ |
|------|------|---------|---------|---------|
| X | X | H | a | a |
| L | L | L | b | b |
| L | H | L | b | a |
| H | H | L | a | a |
| H | L | L | a | b |

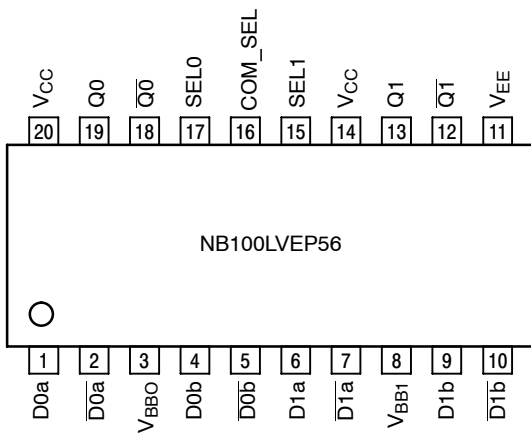


Figure 2. TSSOP-20 Lead Pinout (Top View)

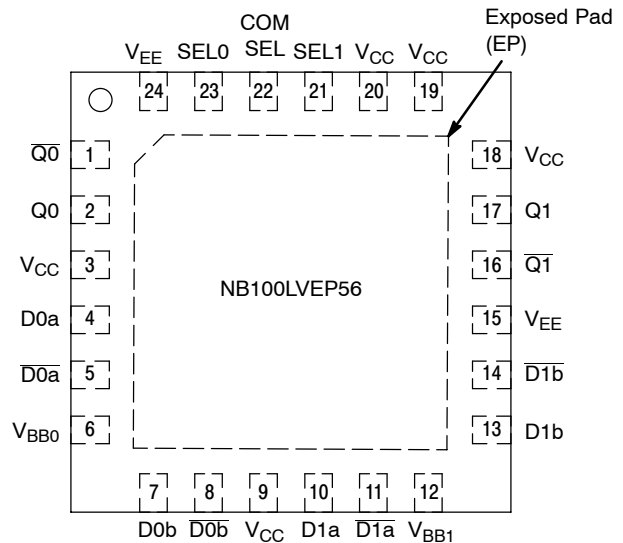


Figure 3. QFN-24 Lead Pinout (Top View)

Table 3. ATTRIBUTES

| Characteristics | | Value | |
|--|------------------------|----------------------|--------------------|
| Internal Input Pulldown Resistor | (R1) | 75 kΩ | |
| Internal Input Pullup Resistor | (R2) | 37 kΩ | |
| ESD Protection | Human Body Model | > 2 kV | |
| | Machine Model | > 150 V | |
| | Charged Device Model | > 2 kV | |
| Moisture Sensitivity (Note 1) | | Pb Pkg | Pb-Free Pkg |
| | TSSOP-20 QFN-24 | Level 1 Level 1 | Level 1 Level 1 |
| Flammability Rating | Oxygen Index: 28 to 34 | UL 94 V-0 @ 0.125 in | |
| Transistor Count | | 354 Devices | |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test | | | |

1. For additional information, see Application Note AND8003/D.

NB100LVEP56

Table 4. MAXIMUM RATINGS

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|------------------|--|--|--|----------------|--------------|
| V _{CC} | Positive Mode Power Supply | V _{EE} = 0 V | | 6 | V |
| V _{EE} | Negative Mode Power Supply | V _{CC} = 0 V | | -6 | V |
| V _I | Positive Mode Input Voltage Negative Mode Input Voltage | V _{EE} = 0 V V _{CC} = 0 V | V _I ≤ V _{CC} V _I ≥ V _{EE} | 6 -6 | V V |
| I _{out} | Output Current | Continuous Surge | | 50 100 | mA mA |
| I _{BB} | V _{BB} Sink/Source | | | ±0.5 | mA |
| T _A | Operating Temperature Range | | | -40 to +85 | °C |
| T _{stg} | Storage Temperature Range | | | -65 to +150 | °C |
| θ _{JA} | Thermal Resistance (Junction-to-Ambient) JEDEC 51-3 (1S - Single Layer Test Board) | 0 lfpm 500 lfpm | TSSOP-20 TSSOP-20 | 140 50 | °C/W °C/W |
| θ _{JA} | Thermal Resistance (Junction-to-Ambient) JEDEC 51-6 (2S2P-Multi Layer Test Board) with Filled Thermal Vias | 0 lfpm 500 lfpm | QFN-24 QFN-24 | 37 32 | °C/W °C/W |
| θ _{JC} | Thermal Resistance (Junction-to-Case) | Standard Board | TSSOP-20 QFN-24 | 23 to 41 11 | °C/W |
| T _{sol} | Wave Solder Pb Pb-Free | | | 265 265 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 5. DC CHARACTERISTICS, PECL V_{CC} = 2.5 V, V_{EE} = 0 V (Note 2)

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|--------------------|--|------------------------|---------------------|-------------------------|------------------------|------|-------------------------|------------------------|------|-------------------------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I _{EE} | Negative Power Supply Current | 35 | 45 | 55 | 35 | 45 | 55 | 35 | 48 | 58 | mA |
| V _{OH} | Output HIGH Voltage (Note 3) | 1355 | 1480 | 1605 | 1355 | 1480 | 1605 | 1355 | 1480 | 1605 | mV |
| V _{OL} | Output LOW Voltage (Note 3) | 555 | 775 | 900 | 555 | 775 | 900 | 555 | 775 | 900 | mV |
| V _{IH} | Input HIGH Voltage (SEL0, SEL1, COM_SEL) Input HIGH Voltage (D Inputs) (Note 4) | 1335 1335 | | V _{CC} 1620 | 1335 1335 | | V _{CC} 1620 | 1275 1275 | | V _{CC} 1620 | mV |
| V _{IL} | Input LOW Voltage (SEL0, SEL1, COM_SEL) Input LOW Voltage (D Inputs) (Note 4) | V _{EE} 555 | | 875 875 | V _{EE} 555 | | 875 875 | V _{EE} 555 | | 875 875 | mV |
| V _{IHCMR} | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 5) | 1.2 | | 2.5 | 1.2 | | 2.5 | 1.2 | | 2.5 | V |
| I _{IH} | Input HIGH Current (@V _{IH}) | | | 150 | | | 150 | | | 150 | μA |
| I _{IL} | Input LOW Current (@V _{IL}) | D D̄ SEL | 0.5 -150 -150 | | 0.5 -150 -150 | | | 0.5 -150 -150 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary -0.125 V to +1.3 V.
- All loading with 50 Ω to V_{CC} - 2.0 V.
- Do not use V_{BB} at V_{CC} < 3.0 V.
- V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

NB100LVEP56

Table 6. DC CHARACTERISTICS, PECL $V_{CC} = 3.3\text{ V}$, $V_{EE} = 0\text{ V}$ (Note 6)

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|-------------|--|-----------------------|---------------------|------------------|---------------------|------|------------------|---------------------|------|------------------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{EE} | Negative Power Supply Current | 35 | 45 | 55 | 35 | 45 | 55 | 35 | 48 | 58 | mA |
| V_{OH} | Output HIGH Voltage (Note 7) | 2155 | 2280 | 2405 | 2155 | 2280 | 2405 | 2155 | 2280 | 2405 | mV |
| V_{OL} | Output LOW Voltage (Note 7) | 1355 | 1575 | 1700 | 1355 | 1575 | 1700 | 1355 | 1575 | 1700 | mV |
| V_{IH} | Input HIGH Voltage (SEL0, SEL1, COM_SEL) Input HIGH Voltage (D Inputs) | 2135 2135 | | V_{CC} 2420 | 2135 2135 | | V_{CC} 2420 | 2135 2135 | | V_{CC} 2420 | mV |
| V_{IL} | Input LOW Voltage (SEL0, SEL1, COM_SEL) Input LOW Voltage (D Inputs) | V_{EE} 1355 | | 1675 1675 | V_{EE} 1355 | | 1675 1675 | V_{EE} 1355 | | 1675 1675 | mV |
| V_{BB} | Output Reference Voltage (Note 8) | 1775 | 1875 | 1975 | 1775 | 1875 | 1975 | 1775 | 1875 | 1975 | mV |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 9) | 1.2 | | 3.3 | 1.2 | | 3.3 | 1.2 | | 3.3 | V |
| I_{IH} | Input HIGH Current (@ V_{IH}) | | | 150 | | | 150 | | | 150 | μA |
| I_{IL} | Input LOW Current (@ V_{IL}) | D \bar{D} SEL | 0.5 -150 -150 | | 0.5 -150 -150 | | | 0.5 -150 -150 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

6. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.5 V to -0.3 V.

7. All loading with 50 Ω to $V_{CC} - 2.0\text{ V}$.

8. Single-Ended input operation is limited to $V_{CC} \geq 3.0\text{ V}$ in PECL mode.

9. V_{IHCMR} min varies 1:1 with V_{EE} . V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 7. DC CHARACTERISTICS, NECL $V_{CC} = 0\text{ V}$, $V_{EE} = -3.8\text{ V}$ to -2.375 V (Note 10)

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|-------------|--|-----------------------|---------------------|------------------|---------------------|-------|------------------|---------------------|-------|------------------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{EE} | Negative Power Supply Current | 35 | 45 | 55 | 35 | 45 | 55 | 35 | 48 | 58 | mA |
| V_{OH} | Output HIGH Voltage (Note 11) | -1145 | -1020 | -895 | -1145 | -1020 | -895 | -1145 | -1020 | -895 | mV |
| V_{OL} | Output LOW Voltage (Note 11) | -1945 | -1725 | -1600 | -1945 | -1725 | -1600 | -1945 | -1725 | -1600 | mV |
| V_{IH} | Input HIGH Voltage (SEL0, SEL1, COM_SEL) Input HIGH Voltage (\bar{D} Inputs) | -1165 -1165 | | V_{CC} -880 | -1165 -1165 | | V_{CC} -880 | -1165 -1165 | | V_{CC} -880 | mV |
| V_{IL} | Input LOW Voltage (SEL0, SEL1, COM_SEL) Input LOW Voltage (D Inputs) | V_{EE} -1945 | | -1600 -1600 | V_{EE} -1945 | | -1600 -1600 | V_{EE} -1945 | | -1600 -1600 | mV |
| V_{BB} | Output Reference Voltage (Note 12) | -1525 | -1425 | -1325 | -1525 | -1425 | -1325 | -1525 | -1425 | -1325 | mV |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 13) | $V_{EE}+1.2$ | | 0.0 | $V_{EE}+1.2$ | | 0.0 | $V_{EE}+1.2$ | | 0.0 | V |
| I_{IH} | Input HIGH Current (@ V_{IH}) | | | 150 | | | 150 | | | 150 | μA |
| I_{IL} | Input LOW Current (@ V_{IL}) | D \bar{D} SEL | 0.5 -150 -150 | | 0.5 -150 -150 | | | 0.5 -150 -150 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

10. Input and output parameters vary 1:1 with V_{CC} .

11. All loading with 50 Ω to $V_{CC} - 2.0\text{ V}$.

12. Single-Ended input operation is limited to V_{EE} from -3.0 V to -5.5 V in NECL mode.

13. V_{IHCMR} min varies 1:1 with V_{EE} . V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

NB100LVEP56

Table 8. AC CHARACTERISTICS $V_{CC} = 0\text{ V}$; $V_{EE} = -2.375\text{ V}$ to -3.8 V or $V_{CC} = 2.375\text{ V}$ to 3.8 V ; $V_{EE} = 0\text{ V}$ (Note 14)

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|--------------------------|--|-------|-------|------|------|-------|------|------|-------|------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| V_{OUTPP} | Output Voltage Amplitude (See Figure 4) $f_{in} \leq 1\text{ GHz}$ $f_{in} = 2\text{ GHz}$ $f_{in} = 2.5\text{ GHz}$ | 525 | 700 | | 550 | 700 | | 500 | 700 | | mV |
| t_{PLH} , t_{PHL} | Propagation Delay to Output Differential D to Q, \bar{Q} SEL to Q, \bar{Q} COM_SEL to Q, \bar{Q} | 375 | 500 | 625 | 400 | 525 | 650 | 450 | 575 | 700 | ps |
| t_{Skew} | Pulse Skew (Note 15) Within Device Input Skew (Note 16) Within Device Output Skew (Note 17) Device-to-Device Skew (Note 18) | | 10 | 50 | | 10 | | | 10 | 50 | ps |
| t_{JITTER} | RMS Random Clock Jitter (Note 19) @ $\leq 1.0\text{ GHz}$ @ $\leq 1.5\text{ GHz}$ @ $\leq 2.0\text{ GHz}$ @ $\leq 2.5\text{ GHz}$ Peak-to-Peak Data Dependent Jitter (Note 20) @ 0.5 GHz @ 1.25 GHz @ 2.488 GHz | | 0.269 | 0.4 | | 0.307 | 0.4 | | 0.371 | 0.5 | ps |
| V_{INPP} | Input Voltage Swing (Differential Configuration) (Note 21) | 150 | 800 | 1200 | 150 | 800 | 1200 | 150 | 800 | 1200 | mV |
| t_r t_f | Output Rise/Fall Times @ 50 MHz (20% – 80%) Q, \bar{Q} | 60 | 110 | 150 | 60 | 120 | 170 | 90 | 140 | 230 | ps |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

14. Measured using a 750 mV source, 50% duty cycle clock source. All loading with $50\ \Omega$ to $V_{CC} - 2.0\text{ V}$. Input edge rates 150 ps (20% – 80%).
15. Pulse Skew [$t_{PLH} - t_{PHL}$]
16. Worst case difference between D0a and D0b (or between D1a or D1b), when both output come from same input.
17. Worst case difference between Q0 and Q1 outputs.
18. Skew is measured between outputs under identical transitions.
19. Additive RMS jitter with 50% Duty Cycle Clock Signal.
20. Additive Peak-to-Peak jitter with input NRZ data at PRBS $2^{31}-1$.
21. Input voltage swing is a single-ended measurement operating in differential mode.

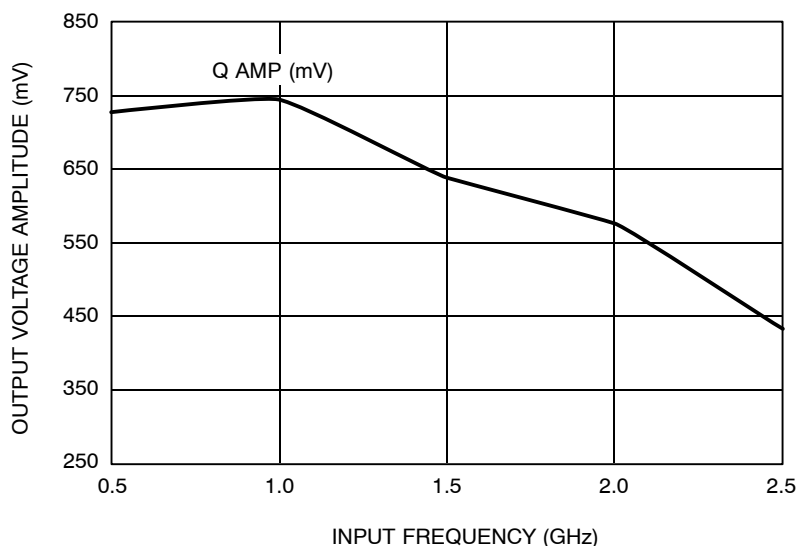


Figure 4. Output Voltage Amplitude (V_{OUTPP}) vs. Input Frequency (f_{in}) at $V_{CC} = 2.5\text{ V}$, 25°C

NB100LVEP56

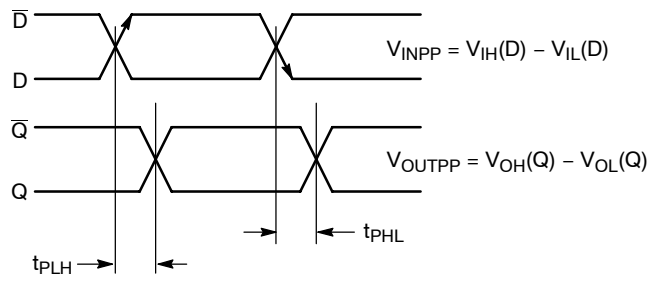


Figure 5. AC Reference Measurement

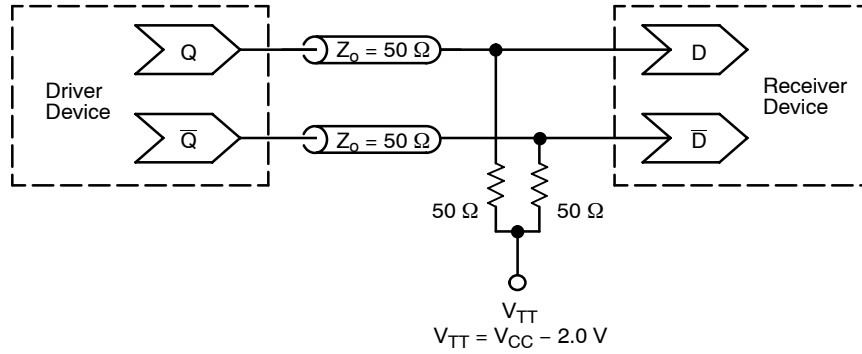


Figure 6. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020/D – Termination of ECL Logic Devices.)

NB100LVEP56

ORDERING INFORMATION

| Device | Package | Shipping† |
|------------------|---------------------|------------------|
| NB100LVEP56DT | TSSOP-20* | 75 Units / Rail |
| NB100LVEP56DTG | TSSOP-20* | 75 Units / Rail |
| NB100LVEP56DTR2 | TSSOP-20* | 2500 Tape & Reel |
| NB100LVEP56DTR2G | TSSOP-20* | 2500 Tape & Reel |
| NB100LVEP56MN | QFN-24 | 92 Units / Rail |
| NB100LVEP56MNG | QFN-24 (Pb-Free) | 92 Units / Rail |
| NB100LVEP56MNR2 | QFN-24 | 3000 Tape & Reel |
| NB100LVEP56MNR2G | QFN-24 (Pb-Free) | 3000 Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

*This package is inherently Pb-Free.

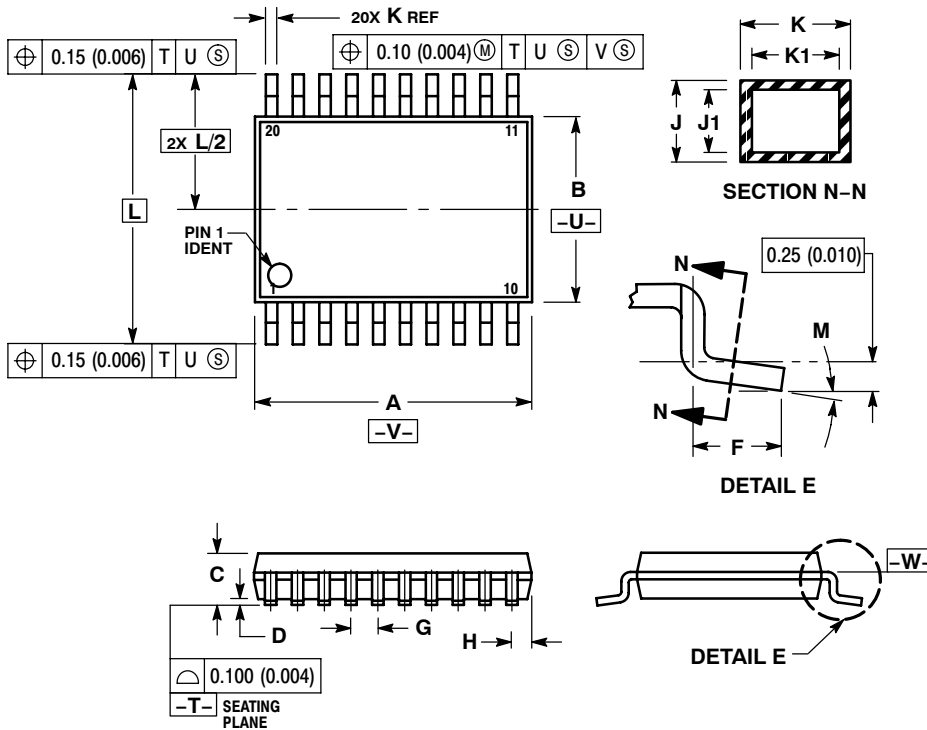
Resource Reference of Application Notes

- AN1405/D** - ECL Clock Distribution Techniques
- AN1406/D** - Designing with PECL (ECL at +5.0 V)
- AN1503/D** - ECLinPS™ I/O SPiCE Modeling Kit
- AN1504/D** - Metastability and the ECLinPS Family
- AN1568/D** - Interfacing Between LVDS and ECL
- AN1672/D** - The ECL Translator Guide
- AND8001/D** - Odd Number Counters Design
- AND8002/D** - Marking and Date Codes
- AND8020/D** - Termination of ECL Logic Devices
- AND8066/D** - Interfacing with ECLinPS
- AND8090/D** - AC Characteristics of ECL Devices

NB100LVEP56

PACKAGE DIMENSIONS

TSSOP-20
CASE 948E-02
ISSUE C

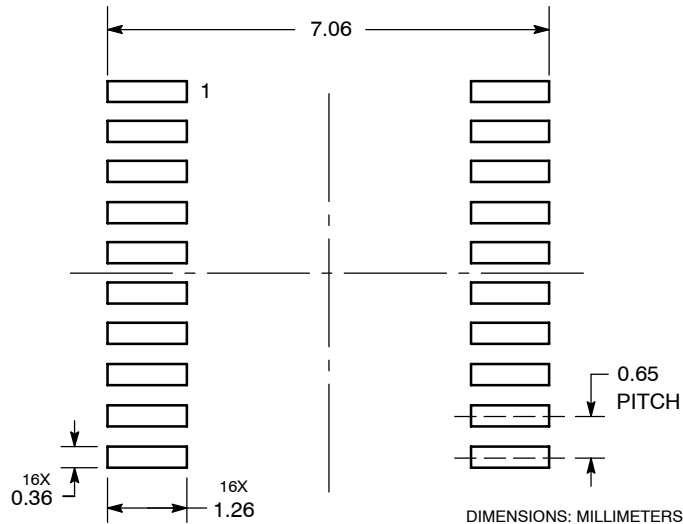


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 6.40 | 6.60 | 0.252 | 0.260 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.27 | 0.37 | 0.011 | 0.015 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

SOLDERING FOOTPRINT*

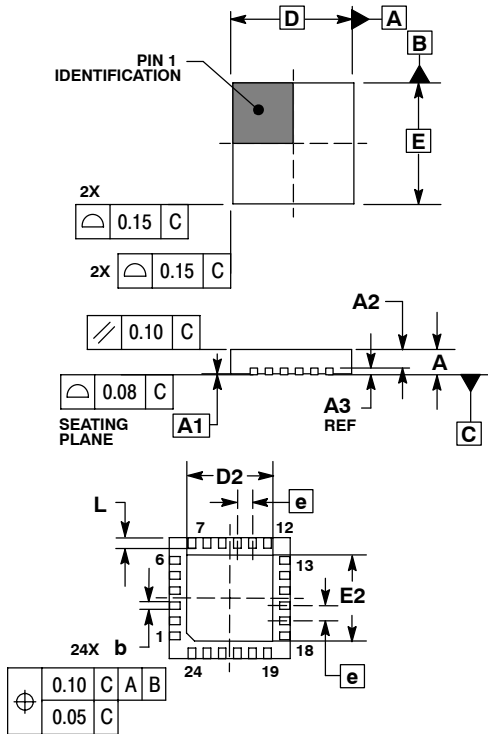


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NB100LVEP56

PACKAGE DIMENSIONS

QFN 24
MN SUFFIX
 24 PIN QFN, 4x4
 CASE 485L-01
 ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| DIM | MILLIMETERS | |
|-----|-------------|------|
| | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A2 | 0.60 | 0.80 |
| A3 | 0.20 | REF |
| b | 0.23 | 0.28 |
| D | 4.00 | BSC |
| D2 | 2.70 | 2.90 |
| E | 4.00 | BSC |
| E2 | 2.70 | 2.90 |
| e | 0.50 | BSC |
| L | 0.35 | 0.45 |

ECLinPS is a trademark of Semiconductor Components Industries, LLC (SCILLC).

ON Semiconductor and **ON** are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
 Literature Distribution Center for ON Semiconductor
 P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
 USA/Canada
Europe, Middle East and Africa Technical Support:
 Phone: 421 33 790 2910
Japan Customer Focus Center
 Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>
 For additional information, please contact your local Sales Representative



Стандарт Электрон Связь

Мы молодая и активно развивающаяся компания в области поставок электронных компонентов. Мы поставляем электронные компоненты отечественного и импортного производства напрямую от производителей и с крупнейших складов мира.

Благодаря сотрудничеству с мировыми поставщиками мы осуществляем комплексные и плановые поставки широчайшего спектра электронных компонентов.

Собственная эффективная логистика и склад в обеспечивает надежную поставку продукции в точно указанные сроки по всей России.

Мы осуществляем техническую поддержку нашим клиентам и предпродажную проверку качества продукции. На все поставляемые продукты мы предоставляем гарантию .

Осуществляем поставки продукции под контролем ВП МО РФ на предприятия военно-промышленного комплекса России , а также работаем в рамках 275 ФЗ с открытием отдельных счетов в уполномоченном банке. Система менеджмента качества компании соответствует требованиям ГОСТ ISO 9001.

Минимальные сроки поставки, гибкие цены, неограниченный ассортимент и индивидуальный подход к клиентам являются основой для выстраивания долгосрочного и эффективного сотрудничества с предприятиями радиоэлектронной промышленности, предприятиями ВПК и научно-исследовательскими институтами России.

С нами вы становитесь еще успешнее!

Наши контакты:

Телефон: +7 812 627 14 35

Электронная почта: sales@st-electron.ru

Адрес: 198099, Санкт-Петербург,
Промышленная ул, дом № 19, литера Н,
помещение 100-Н Офис 331