EVB-LAN9252-HBI+

EtherCAT® Evaluation Board User's Guide

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Object of Declaration: EVB-LAN9252-HBI+

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Derek Carlson
VP Development Tools

12-Sep-14
Date

NOTES:

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Table of Contents

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Preface

NOTICE TO CUSTOMERS

All documentation becomes dated, and this manual is no exception. Microchip tools and documentation are constantly evolving to meet customer needs, so some actual dialogs and/or tool descriptions may differ from those in this document. Please refer to our web site (www.microchip.com) to obtain the latest documentation available.

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INTRODUCTION

This chapter contains general information that will be useful to know before using the EVB-LAN9252-HBI+. Items discussed in this chapter include:

- Document Layout
- Conventions Used in this Guide
- The Microchip Web Site
- Development Systems Customer Change Notification Service
- Customer Support
- Document Revision History

DOCUMENT LAYOUT

This document describes how to use the EVB-LAN9252-HBI+ as a development tool for the Microchip LAN9252 EtherCAT® slave controller. The manual layout is as follows:

- **Chapter 1. "Overview"** – Shows a brief description of the EVB-LAN9252-HBI+.
- **Chapter 2. "Board Details & Configuration"** – Includes details and instructions for using the EVB-LAN9252-HBI+.
- **Chapter 3. "Software Development Kit"** – Includes details and instructions for using the LAN9252 EtherCAT® slave stack firmware and SDK framework.
- **Appendix A. "Evaluation Board Photo"** – This appendix shows the EVB-LAN9252-HBI+.
- **Appendix B. "Evaluation Board Schematics"** – This appendix shows the EVB-LAN9252-HBI+ schematics.
- **Appendix C. "Bill of Materials (BOM)"** – This appendix includes the EVB-LAN9252-HBI+ Bill of Materials (BOM).

CONVENTIONS USED IN THIS GUIDE

This manual uses the following documentation conventions:

DOCUMENTATION CONVENTIONS

Description	Represents	Examples
Arial font:		
Italic characters	Referenced books	*MPLAB® IDE User's Guide*
	Emphasized text	...is the *only* compiler...
Initial caps	A window	the Output window
	A dialog	the Settings dialog
	A menu selection	select Enable Programmer
Quotes	A field name in a window or dialog	"Save project before build"
Underlined, italic text with right angle bracket	A menu path	*File>Save*
Bold characters	A dialog button	Click **OK**
	A tab	Click the **Power** tab
N'Rnnnn	A number in verilog format, where N is the total number of digits, R is the radix and n is a digit.	4'b0010, 2'hF1
Text in angle brackets < >	A key on the keyboard	Press <Enter>, <F1>
Courier New font:		
Plain Courier New	Sample source code	`#define START`
	Filenames	`autoexec.bat`
	File paths	`c:\mcc18\h`
	Keywords	`_asm, _endasm, static`
	Command-line options	`-Opa+, -Opa-`
	Bit values	`0, 1`
	Constants	`0xFF, 'A'`
Italic Courier New	A variable argument	*`file`*`.o`, where *`file`* can be any valid filename
Square brackets [ ]	Optional arguments	`mcc18 [options]` *`file`* `[options]`
Curly brackets and pipe character: { | }	Choice of mutually exclusive arguments; an OR selection	`errorlevel {0|1}`
Ellipses...	Replaces repeated text	`var_name [, var_name...]`
	Represents code supplied by user	`void main (void) { ... }`

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- **Emulators** – The latest information on Microchip in-circuit emulators.This includes the MPLAB REAL ICE and MPLAB ICE 2000 in-circuit emulators.
- **In-Circuit Debuggers** – The latest information on the Microchip in-circuit debuggers. This includes MPLAB ICD 3 in-circuit debuggers and PICkit 3 debug express.
- **MPLAB IDE** – The latest information on Microchip MPLAB IDE, the Windows Integrated Development Environment for development systems tools. This list is focused on the MPLAB IDE, MPLAB IDE Project Manager, MPLAB Editor and MPLAB SIM simulator, as well as general editing and debugging features.
- **Programmers** – The latest information on Microchip programmers. These include production programmers such as MPLAB REAL ICE in-circuit emulator, MPLAB ICD 3 in-circuit debugger and MPLAB PM3 device programmers. Also included are nonproduction development programmers such as PICSTART Plus and PIC-kit 2 and 3.

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Technical support is available through the web site at:
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DOCUMENT REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS50002333C (06-17-16)	All	Updated board name to "EVB-LAN9252-HBI+" throughout document.
	Figure 1-1	Updated figure to include UART, Temp. Sensor, DAC, and ADC.
	Chapter 2. "Board Details & Configuration"	Updated Figures 1, 5, 6, 7, and 10. Added new Figure 2.
		Updated Tables 13, 14, 15, 21.
	2.1.1 "+5V Power"	Removed power supply manufacturer and part number.
	2.6 "Additional Features"	Added new section with new features.
	Chapter 3. "Software Development Kit"	Updated figures throughout chapter.
	Appendix A. "Evaluation Board Photo"	Updated appendix with new photos.
	Appendix B. "Evaluation Board Schematics"	Updated appendix with new schematics.
	Appendix C. "Bill of Materials (BOM)"	Updated appendix with updated BOM.
DS50002333B (05-12-15)	All	Updated board name to "EVB-LAN9252-HBI" throughout document, corrected misc. typos and grammatical errors.
	Section 1.2 "References"	Updated list of application notes.
	Section 2.4.4 "DIGIO/HBI/SPI+GPIO Selection"	Added additional information on DIGIO mode.
	Table 2-13, Table 2-14, and Table 2-15	Simplified table and added note under each table for clarity.
DS50002333A (02-27-15)	Initial Release of Document	

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Chapter 1. Overview

1.1 INTRODUCTION

The LAN9252 is a 2-port EtherCAT® Slave Controller (ESC) with dual integrated Ethernet PHYs which each contain a full-duplex 100BASE-TX transceiver and support 100Mbps (100BASE-TX) operation. 100BASE-FX is supported via an external fiber transceiver.

Each port receives an EtherCAT® frame, performs frame checking and forwards it to the next port. Time stamps of received frames are generated when they are received. The Loop-back function of each port forwards the frames to the next logical port if there is either no link at a port, if the port is not available, or if the loop is closed for that port. The Loop-back function of port 0 forwards the frames to the EtherCAT® Processing Unit. The loop settings can be controlled by the EtherCAT® master.

Packets are forwarded in the following order:

Port 0 -> EtherCAT® Processing Unit -> Port 1 -> Port 2.

The EtherCAT® Processing Unit (EPU) receives, analyzes and processes the EtherCAT® data stream. The main purpose of the EtherCAT® Processing unit is to enable and coordinate access to the internal registers and the memory space of the ESC, which can be addressed both from the EtherCAT® master and from the local application. Data exchange between master and slave applications is comparable to a dual-ported memory (process memory), enhanced by special functions for consistency checking (SyncManager) and data mapping (FMMU). Each FMMU performs bitwise mapping of logical EtherCAT® system addresses to physical device addresses.

The scope of this document is to describe the EVB-LAN9252-HBI+ setup, which supports a HBI/SPI+GPIO Interface and corresponding jumper configurations. The LAN9252 is connected to an RJ45 Ethernet jack with integrated magnetics for 100BASE-TX connectivity. A simplified block diagram of the EVB-LAN9252-HBI+ is shown in Figure 1-1.

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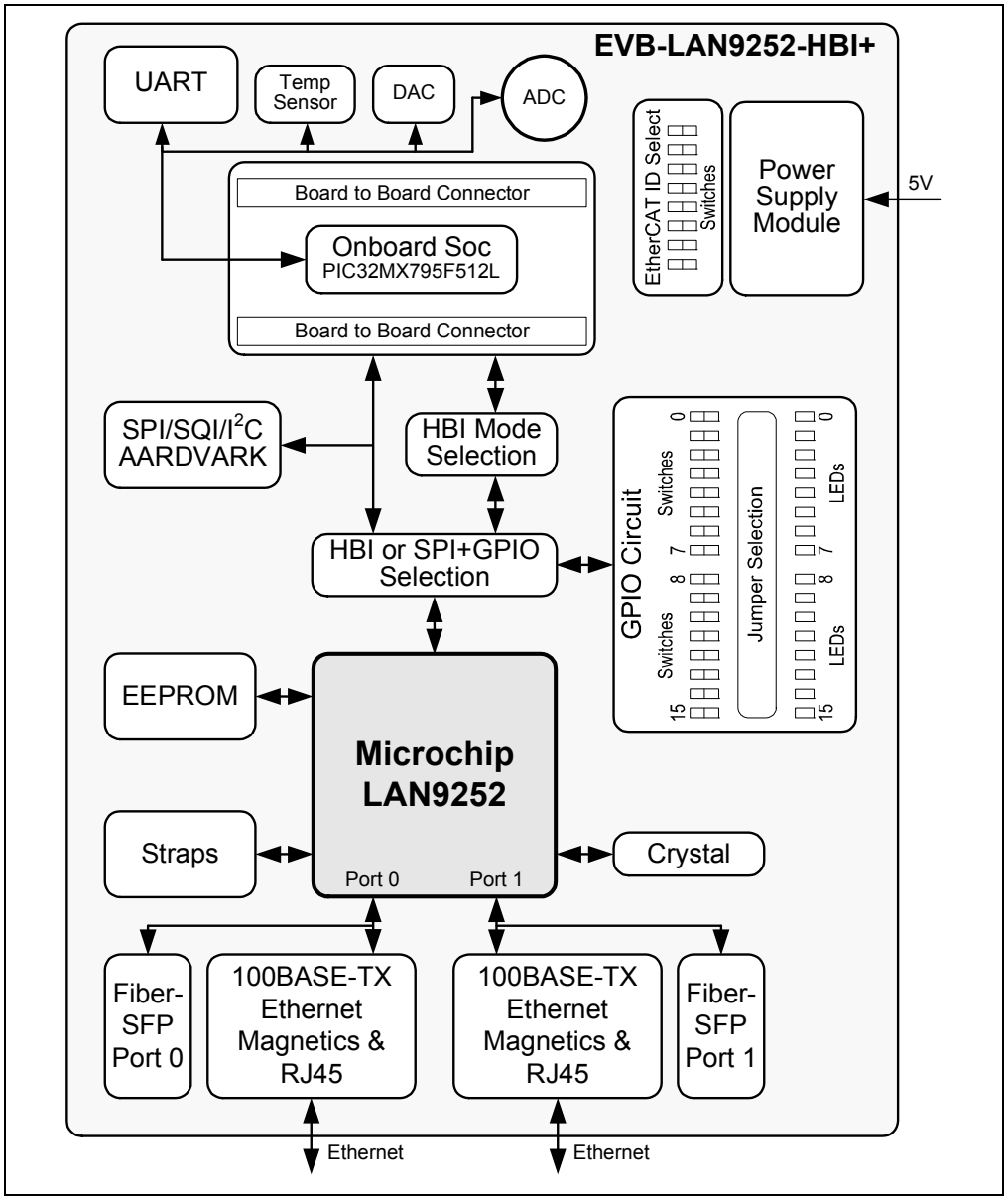
FIGURE 1-1: EVB-LAN9252-HBI+ BLOCK DIAGRAM



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1.2 REFERENCES

Concepts and material available in the following documents may be helpful when reading this document. Visit www.microchip.com for the latest documentation.

- LAN9252 Data Sheet
- AN 8.13 Suggested Magnetics
- EVB-LAN9252-HBI+ Schematics
- The following application notes:
  - AN1916 Integrating Microchip's LAN9252 SDK with Beckhoff's EtherCAT® SSC
  - AN1920 Microchip LAN9252 EEPROM Configuration and Programming
  - AN1907 Microchip LAN9252 Migration from Beckhoff ET1100

1.3 TERMS AND ABBREVIATIONS

IDE - Integrated Development Environment

ESC - EtherCAT® Slave Controller

EVB - Engineering Validation Board

HAL - Hardware Abstraction Layer

HBI - Host Bus Interface

SPI - Serial Protocol Interface

SSC - Slave Stack Code

Chapter 2. Board Details & Configuration

This chapter includes sub-sections on the following EVB-LAN9252-HBI+ details:

- Power
- Resets
- Clock
- Configuration
- Additional Features
- Limitations
- Mechanicals

2.1 POWER

2.1.1 +5V Power

Power is supplied to the LAN9252 by a +3.3V on-board regulator, which is powered by a +5V external wall adapter. The LAN9252 includes an internal +1.2V regulator which supplies power to the internal core logic. Assertion of the D1 Green LED indicates successful generation of +3.3V o/p. The SW1 switch must be in the ON position for the +5V to power the +3.3V regulator.

2.2 RESETS

2.2.1 Power-on Reset

A power-on reset occurs whenever power is initially applied to the LAN9252 or if the power is removed and reapplied to the LAN9252. This event resets all circuitry within the LAN9252. After initial power-on, the LAN9252 can be reset by pressing the reset switch SW2. The reset LED D2 will assert (red) when the LAN9252 is in reset condition. For stability, a delay of approximately 180ms is added from the +3.3V o/p to reset release.

2.2.2 Reset Out

The LAN9252 reset pin can be configured as an output to reset the SoC. The RST# pin becomes an open-drain output and is asserted for the minimum required time of 80ms.

2.2.3 GPIO Reset

The EVB-LAN9252-HBI+ provides the option to reset the LAN9252 through a PIC GPIO pin [95(RG14)]. The SW10 switch is used for this selection, as shown in Table 2-1.

TABLE 2-1: RESET CONFIGURATION SWITCH

Switch	Short Pins	Knob Position	Function
SW10	1-3	1-2	System Reset (SYS_RESETN) (Default)
SW10	1-2	1-3	GPIO Reset (RST_GPIO)

2.3 CLOCK

The EVB-LAN9252-HBI+ utilizes an external 25MHz 25ppm crystal from Cardinal Components Inc. (P/N: CSM1Z-A5B2C5-40-25.0D18-F).

2.4 CONFIGURATION

The following sub-sections describe the various board features and configuration settings. A top view of the EVB-LAN9252-HBI+ is shown in Figure 2-1. Figure 2-2 details new features.

FIGURE 2-1: EVB-LAN9252-HBI+ TOP VIEW WITH CALLOUTS

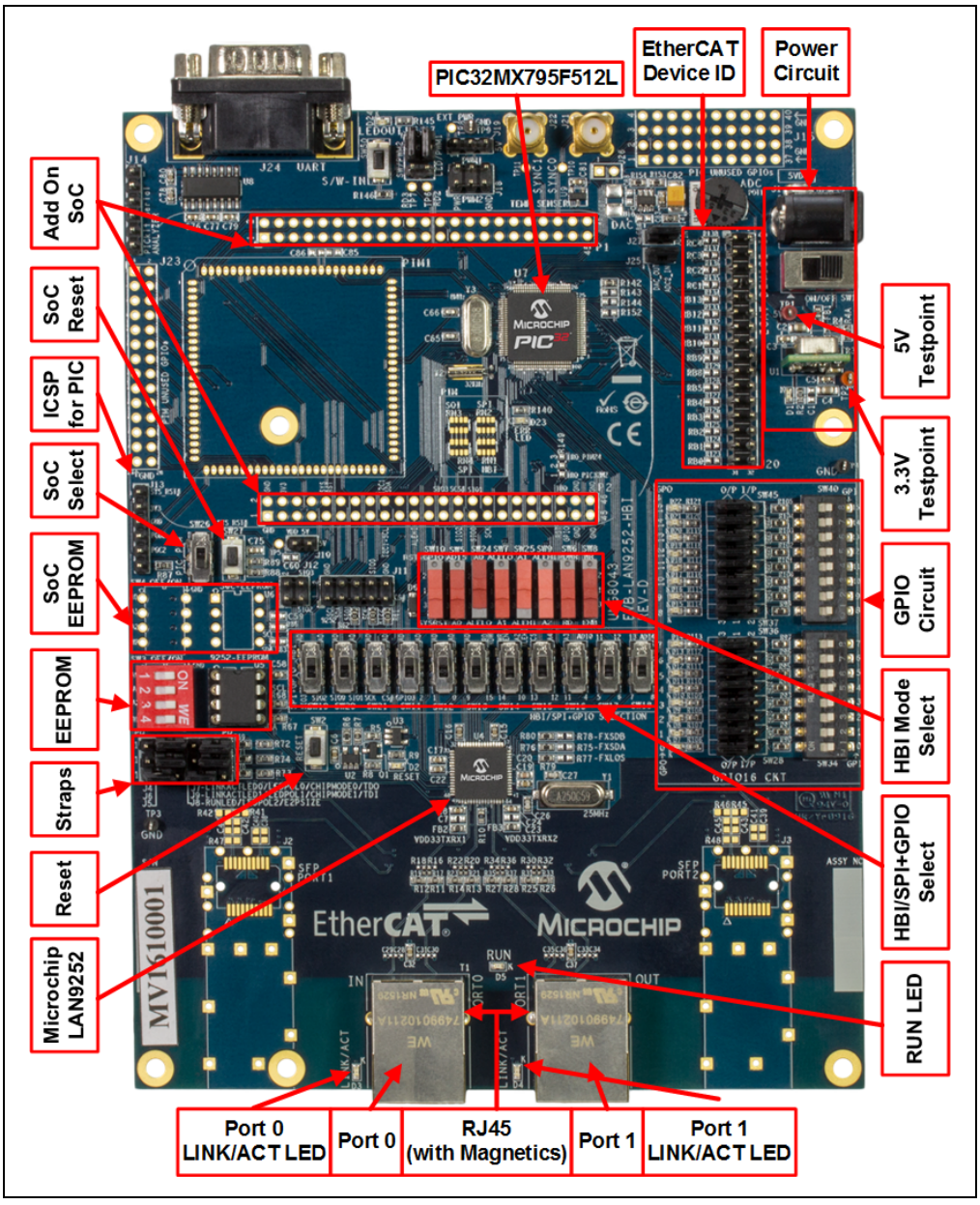
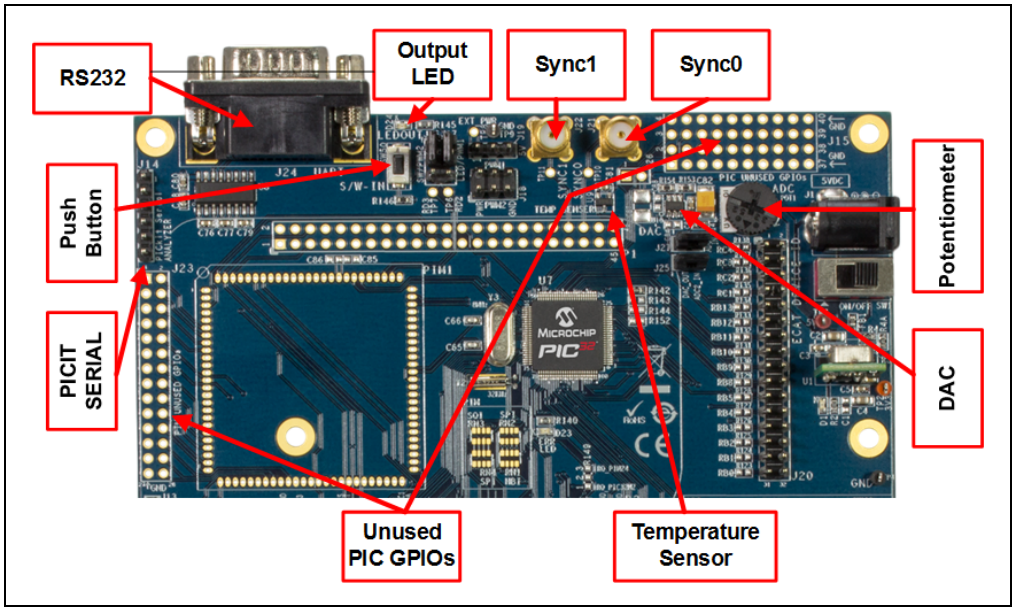


FIGURE 2-2: EVB-LAN9252-HBI+ TOP VIEW NEW FEATURE CALLOUTS



2.4.1 Strap Options

2.4.1.1 CHIP MODE SELECTION

Table 2-2 details the LAN9252 chip mode configuration straps.

TABLE 2-2: CHIP MODE CONFIGURATION STRAP

Header	Description	Pins	Settings
J4,J6,J7,J9	Chip mode configuration strap inputs. This strap determines the number of active ports and port types.	1-2 2-3	Short 1-2 for high (pull-up) (Not supported in this EVB) Short 2-3 for low (pull-down) (default)

Note: This EVB supports Chip mode 00 which is 2-port mode, where Port 0 = PHY A and Port 1 = PHY B. This requires J4, J6, J7, and J9 to be pulled-down (2-3) shorted. All other configurations are not supported with this EVB.

2.4.1.2 EEPROM SIZE CONFIGURATION

The EEPROM size configuration strap (J5 & J8) determines the supported EEPROM size range. A low selects 1Kbits (128 x 8) through 16Kbits (2K x 8)_24C16. A high selects 32Kbits (4K x 8) through 512Kbits (64K x 8) or 4Mbits (512K x 8)_24C512.

TABLE 2-3: EEPROM SIZE CONFIGURATION STRAP

Header	Description	Pins	Settings
J5, J8	EEPROM size configuration strap inputs. This strap determines the supported EEPROM size range.	1-2 2-3	Short 1-2 for high (pull-up) (default) Short 2-3 for low (pull-down)

2.4.1.3 COPPER AND FIBER STRAPS

The LAN9252 supports 100BASE-TX (Copper) and 100BASE-FX (Fiber) modes. In 100BASE-FX operation, the presence of the receive signal is indicated by the external transceiver as either an open-drain, CMOS level, Loss of Signal (SFP) or a LVPECL Signal Detect (SFF).

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This EVB supports 100BASE-TX (Copper) and SFP 100BASE-FX (Fiber) modes. By default Copper Mode is active. Fiber Mode is supported as an assembly option. To select the Copper or Fiber Mode, the respective strap and signal routing resister assembly options must to be configured.

Note: Vendor part number for SFP: Finisar/FTLF1217P2

2.4.1.3.1 Copper Mode

The EVB-LAN9252-HBI+ is set to Copper Mode by default. Table 2-4 details the required strap resistor settings for Copper Mode operation.

TABLE 2-4: COPPER MODE STRAP RESISTORS

Resistors	Description
R79 (10K)	Configures Port 0 & 1 to Copper Mode
R76, R80 (10K)	Configures Port 0 and Port 1 to Copper Mode, respectively

Note: R75, R77, and R78 must not be populated (DNP).

Additionally, the signal routing resistors detailed in Table 2-5 must be assembled for Copper Mode operation.

TABLE 2-5: COPPER MODE SIGNAL ROUTING RESISTORS

Resistors	Description
R17, R19, R21, R23	Port 0 Copper Mode enabled
R31, R33, R35, R37	Port 1 Copper mode enabled

Note: R16, R18, R20, R22, R30, R32, R34, and R36 (0402 package) must not be populated (DNP).

2.4.1.3.2 Fiber Mode

The EVB-LAN9252-HBI+ support SFP type 100BASE-FX. To enable Fiber Mode, the respective strap and signal routing resistors must be configured.

Note: Copper Mode related resistors must be DNP while Fiber Mode is active (See Section 2.4.1.3.1 “Copper Mode”).

Table 2-6 details the required strap resistor settings for Fiber Mode operation.

TABLE 2-6: FIBER MODE STRAP RESISTORS

Resistors	Description
R77 (10K)	Configures Port 0 & 1 to FX-LOS Mode
R75, R78 (10K)	Configures Port 0 and Port 1 to Fiber Mode, respectively

Note: R76, R79, and R80 must not be populated (DNP).

Additionally, the signal routing resistors detailed in Table 2-7 must be assembled for Fiber Mode operation.

TABLE 2-7: FIBER MODE SIGNAL ROUTING RESISTORS

Resistors	Description
R16, R18, R20, R22	Port 0 Fiber Mode enabled
R30, R32, R34, R36	Port 1 Fiber mode enabled

Note: R17, R19, R21, R23, R31, R33, R35, and R37 (0402 package) must not be populated (DNP).

2.4.1.3.3 FX-LOS Fiber Mode Strap

FX-LOS strap details are shown in Table 2-8. These strap settings determine if the ports are to operate in FX-LOS Fiber Mode or FX-SD/Copper Mode.

TABLE 2-8: FX-LOS MODE STRAP SETTINGS

R77 (10K)	R79 (10K)	Reference Voltage (V)	Function
Populate	DNP	3.3	A level above 2V selects FX-LOS for Port 0 and Port 1
Populate	Populate	1.5	A level greater than 1.5V and below 2V selects FX-LOS for Port 0 and FX-SD / copper twisted pair for Port 1, further determined by FXSDB
DNP	Populate	0 (Default)	A level of 0V selects FX-SD / copper twisted pair for Ports 0 and 1, further determined by FXSDA and FXSDB

Note: The above strap details describe the LAN9252 function. This EVB does not support SFF Fiber Mode. Therefore, FX-SD related straps are not applicable.

2.4.2 LED Indicators

The D3 and D4 LEDs are used to indicate the Link/Activity status on the corresponding EVB ports, as detailed in Table 2-9. The Link/Act LED should be ON at each port when the cable is present. If the Link/Act LED is not ON, it indicates there is an issue with the connection or cable.

TABLE 2-9: D3 AND D4 LINK/ACTIVITY LED STATUS INDICATORS

State	Description
Off	Link is down
Flashing Green	Link is up with activity
Steady Green	Link is up with no activity

Additionally, the D5 LED is used as a RUN indicator (green) to show the AL status of the EtherCAT® State Machine (ESM), as detailed in Table 2-10.

TABLE 2-10: D5 RUN LED STATUS INDICATOR

State	Description
Off	The device is in the INITIALIZATION state
Blinking (on 200ms, off 200ms)	The device is in the PRE-OPERATIONAL state
Single Flash (on 200ms, off 1000ms)	The device is in the SAFE-OPERATIONAL state
On	The device is in the OPERATIONAL state
Flickering (on 50ms, off 50ms)	The device is booting and has not yet entered the INITIALIZATION state, or the device is in the BOOTSTRAP state and firmware download is in progress. (Optional. Off when not implemented.)

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2.4.3 EEPROM Switch

The EVB-LAN9252-HBI+ utilizes 0x50 (7-bit) I^2C slave addressing. The SW3 switch can be used to select the A0, A1, and A2 address bits, as shown in Figure 2-3 and Table 2-11. The eighth bit of the slave address determines if the master device wants to read or write to the EEPROM (24FC512).

FIGURE 2-3: SLAVE ADDRESS ALLOCATION

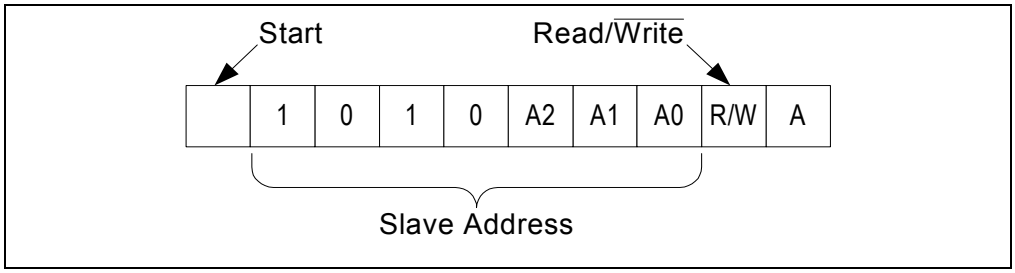


TABLE 2-11: EEPROM SWITCH

Switch	Description	Settings
SW3	I2C EEPROM address selection switch (A0, A1, A2). See Figure 2-3.	ON for logic 0 (default) OFF for logic 1

2.4.4 DIGIO/HBI/SPI+GPIO Selection

The EVB-LAN9252-HBI+ supports three LAN9252 configurations:

- DIGIO Mode
- HBI Mode
- SPI + 16 GPIO Mode

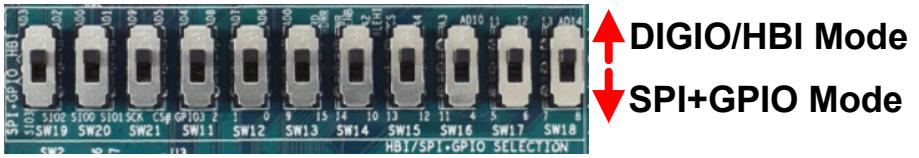
DIGIO and HBI modes use the same switch configuration. The DIGIO/HBI or SPI+GPIO configuration is selected using the DPDT SW11 to SW21 switches. By default, the EVB is set to DIGIO mode and no code is programmed to the on-board PIC32MX. In DIGIO mode, headers P1 and P2 can be used to probe the input and output control signals. It is not possible to configure the input or see to output on the LED on the EVB. Refer to Table 2-22 for a mapping of the DIGIO signals on the P1 and P2 headers.

Note: The PDI configuration which is selected in hardware must match with the PDI configuration that is chosen in the EtherCAT SDK during the SSC integration process. An appropriate PDI configuration must be set in the ESC configuration area of the EEPROM.

TABLE 2-12: HBI/SPI+GPIO SWITCH CONFIGURATIONS

Switch	Description	Settings
SW11 to SW21	Up	DIGIO/HBI Mode (Default)
SW11 to SW21	Down	SPI+GPIO Mode

FIGURE 2-4: SW11-SW21 DIGIO/HBI/SPI+GPIO MODE SELECTION



2.4.4.1 HBI MODE SELECTION

The LAN9252 supports six HBI modes. These six HBI modes (Multiplexed Modes and Indexed Modes) can be selected using the SPST switches (P/N: 450301014042-Wurth Electronics) SW5 through SW9 and SW22 through SW25. Through the switches the LAN9252 HBI signals are connected to the SoC.

Note: For switch P/N: 450301014042, pin 1 is at the middle of the switch. To short 1-2, knob position must be in the 1-3 position, and vice versa.

2.4.4.1.1 Multiplexed Modes

The following four HBI Multiplexed Modes are supported:

1. 8-bit Multiplexed single-phase mode
2. 16-bit Multiplexed single-phase mode
3. 8-bit Multiplexed dual-phase mode
4. 16-bit Multiplexed dual-phase mode

Each HBI Multiplexed Mode requires an updated ESI file, EEPROM and PDI driver with configured SSC to be programmed to the PIC32MX. For additional software information, refer to Chapter 3. "Software Development Kit".

Figure 2-5 details the switch selection for Multiplexed Mode. All four Multiplexed Modes utilize the same switch positions.

FIGURE 2-5: MULTIPLEXED HBI MODE SELECTION

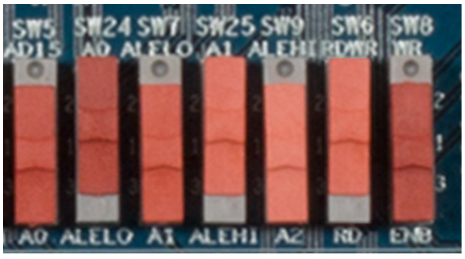


Table 2-13 details the switch selection for Multiplexed Mode.

TABLE 2-13: MULTIPLEXED HBI MODE SELECTION

Switch	Switch Knob Position	Start	Destination
SW5	Down	A0_AD15	A0_CONFIG3
SW6	Up	RD_RDWR	GPMC_DIR
SW7	Down	ALELO_A1	A1_CONFIG3
SW8	Down	WR_ENB	GPMC_DE0N_CLE
SW9	Down	ALEHI_A2	A2_CONFIG3
SW24	Up	A0_CONFIG3	GPMC_A0_ALE
SW25	Up	A1_CONFIG3	GPMC_A1_ALEHI

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Note: When the switch knob is in the down position, pins 1-2 are shorted and the dot on the switch can be seen. When the switch knob is in the up position, pins 1-3 are shorted and no dot can be seen.

2.4.4.1.2 Indexed Mode

There are 2 different Indexed modes, 8-bit and 16-bit. Each HBI Indexed Mode requires an updated ESI file, EEPROM and PDI driver with configured SSC to be programmed to the PIC32MX. For additional software information, refer to Chapter 3. “Software Development Kit”.

8-Bit Indexed Mode

Figure 2-6 details the switch selection for 8-Bit Indexed Mode.

FIGURE 2-6: 8-BIT INDEXED HBI MODE SELECTION

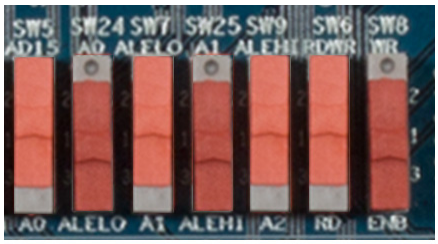

Table 2-14 details the switch selection for 8-bit Indexed HBI Mode.

TABLE 2-14: 8-BIT INDEXED HBI MODE SELECTION

Switch	Switch Knob Position	Start	Destination
SW5	Up	A0_AD15	AD15_CONFIG3
SW6	Up	RD_RDWR	GPMC_DIR
SW7	Up	ALELO_A1	ALELO_CONFIG3
SW8	Down	WR_ENB	GPMC_DE0N_CLE
SW9	Up	ALEHI_A2	ALEHI_CONFIG3
SW24	Down	ALELO_CONFIG3	GPMC_A0_ALE
SW25	Down	ALEHI_CONFIG3	GPMC_A1_ALEHI

Note: When the switch knob is in the down position, pins 1-2 are shorted and the dot on the switch can be seen. When the switch knob is in the up position, pins 1-3 are shorted and no dot can be seen.

16-Bit Indexed Mode

Figure 2-7 details the switch selection for 16-Bit Indexed Mode.

FIGURE 2-7: 16-BIT INDEXED HBI MODE SELECTION

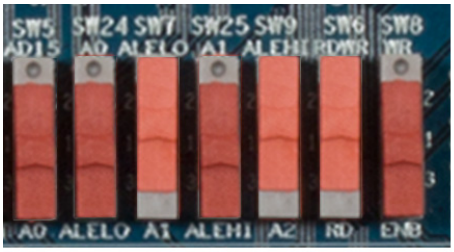

Table 2-15 details the switch selection for 16-bit Indexed HBI Mode.

TABLE 2-15: 16-BIT INDEXED HBI MODE SELECTION

Switch	Switch Knob Position	Start	Destination
SW5	Down	A0_AD15	A0_CONFIG3
SW6	Up	RD_RDWR	GPMC_DIR
SW7	Up	ALELO_A1	ALELO_CONFIG3
SW8	Down	WR_ENB	GPMC_DE0N_CLE
SW9	Up	ALEHI_A2	ALEHI_CONFIG3
SW24	X (Don't Care)	X	X
SW25	Down	ALEHI_CONFIG3	GPMC_A1_ALEHI

Note: When the switch knob is in the down position, pins 1-2 are shorted and the dot on the switch can be seen. When the switch knob is in the up position, pins 1-3 are shorted and no dot can be seen.

Note: If any other SoC is used, the user must check what modes are supported and configure the HBI mode selection switches accordingly.

2.4.4.2 SPI+GPIO SELECTION

The knob position of SW11 to SW21 must be down to select the SPI+GPIO mode. SW19, SW20, and SW21 are used to route the SPI/SQI signals from the LAN9252 to the SoC. SW11 to SW18 are used to route the 16 GPIO signals from the LAN9252 to the GPIO circuit.

TABLE 2-16: SW19-SW21 SIGNAL DEFINITIONS

Switch	Signals
SW19 (pin 2-3 & pin 5-6)	SIO3 & SIO2
SW20 (pin 2-3 & pin 5-6)	SIO0 & SIO1
SW21 (pin 2-3 & pin 5-6)	SCK & SCS#

2.4.4.2.1 SPI/SQI/I^2C Aardvark Header

J11 and J12 are used as Aardvark/SPI/SQI headers. The respective pin details are shown in Table 2-17.

TABLE 2-17: J11 & J12 HEADER PINOUT

Signal	Pin Number
SCL	J11.1
SDA	J11.3
SCK	J11.7
SCS#	J11.9
SI(SIO0)	J11.8
SO(SIO1)	J11.5
SIO2	J12.3
SIO3	J12.4

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2.4.4.3 GPIO INPUT/OUTPUT SELECTION

To enable the SPI+GPIO configuration, the SW11 to SW18 switches must be in the down position. Additionally, the following switches must be configured to select the input or output modes, as shown in Table 2-18.

TABLE 2-18: GPIO MODE SWITCH CONFIGURATIONS

Switches	Switch Knob Position	Mode
SW28 to SW33 SW35 to SW39 SW41 to SW45	Short Pins 1 and 2	INPUT Mode
SW28 to SW33 SW35 to SW39 SW41 to SW45	Short Pins 1 and 3	OUTPUT Mode

2.4.4.3.1 GPIO INPUT Mode

In INPUT Mode, Digital I/O values can be selected through dip switches SW34 and SW40:

- Logic 1 : (Default) SW34 & SW40 Off position. GPI0 to GPI15 tied to pull-up (R90 to R105)
- Logic 0 : The respective knob of 2-way, 8-position dip switch (SW34 & SW40) need to be moved to ON side. Signals can be selected individually.

2.4.4.3.2 GPIO OUTPUT Mode

In OUTPUT Mode, updated GPO values will be seen on the green LEDs (D7 to D22):

- Logic 1 : LED illuminated (green)
- Logic 0 : LED not illuminated.

Note: The LED (D7 to D22) anode is connected to ASIC.

2.4.5 SoC

The EVB-LAN9252-HBI+ supports both an on-board SoC and add-on SoC. By default, the on-board SoC is enabled. However, an external add-on SoC can be connected via the add-on SoC headers P1 and P2. The SoC selection is configured via the SW26 switch, as detailed in the following subsections.

2.4.5.1 SOC SELECTION

The SW26 switch selects the enabled SoC. The SW26 switch knob position must be down (Text = “PIC”) to select the on-board PIC. If the switch knob position is up (Text = “PIM”), then the add-on board/SoC is selected and the on-board PIC is always in the reset state. Whenever an add-on board/SoC is used, the switch knob must be in the up position.

TABLE 2-19: SOC SELECTION

Switch	Position	Settings
SW26	Down	On-board PIC enabled
SW26	Up	Add-on board/SoC enabled

2.4.5.2 ON-BOARD PIC

By default, the on-board Microchip PIC32MX795F512L (U7) is used as the default SoC. The LAN9252 can be connected to the PIC using either an HBI or SPI interface. The selection switches must be configured accordingly to enable the desired interface. Refer to Section 2.4.4 "DIGIO/HBI/SPI+GPIO Selection" and Section 2.4.4.1 "HBI Mode Selection" for additional details.

2.4.5.2.1 Reset

SW27 is used to reset the on-board PIC. The LAN9252 can also reset the SoC if the reset pin is configured to output mode. For stability, a delay of approximately 180ms is added from the 3.3V o/p to reset release.

2.4.5.2.2 ICSP Header

The on-board PIC programing is performed using the ICSP header J13. Table 2-20 details the ICSP header pinout

TABLE 2-20: J13 ICSP HEADER PINOUT

J13 Pin	Settings
1	MLCR
2	3V3
3	GND
4	PGD2
5	PGC2
6	NC

2.4.5.2.3 SoC EEPROM

The EVB-LAN9252-HBI+ provides an optional SoC EEPROM. Some SoCs may require an EEPROM. However, the PIC on-board SoC and PIC based add-on SoC boards do not require this EEPROM.

2.4.5.3 ADD-ON SOC

An add-on board can be attached to the EVB-LAN9252-HBI+ to use an add-on SoC. The add-on board must be mounted to the P1 and P2 connectors (2x23, 100mil normal gold plated berg stick). The SW26 switch must be in the up position when using an add-on SoC. Additionally, the J10 2-pin jumper must be shorted to route power to the add-on board from the EVB-LAN9252-HBI+.

2.4.5.4 ESC ID SELECT

The signals shown in Table 2-21 are provided as EtherCAT® ID selection for complex ESCs. Jumper J20 and respective pull-up resistors are used to configure the ID select signals high or low. By default, there are no resistors populated and all signals are neither high or low. When required, populating the respective jumper or resistor will change the ID select signal to low.

TABLE 2-21: ID SELECT SIGNALS

ID Selection Signal	Signal Name	PIC Pin Number	10k to Pull High	Pins to Short for Pull Low
ID0	ID0_SELECT_RB0	25	R123	32:31
ID1	ID_SELECT_RB1	24	R124	30:29
ID2	ID_SELECT_RB2	23	R125	28:27
ID3	ID_SELECT_RB3	22	R126	26:25
ID4	ID_SELECT_RB4	21	R127	24:23

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TABLE 2-21: ID SELECT SIGNALS (CONTINUED)

ID Selection Signal	Signal Name	PIC Pin Number	10k to Pull High	Pins to Short for Pull Low
ID5	ID_SELECT_RB5	20	R128	22:21
ID6	ID_SELECT_RB8	32	R129	20:19
ID7	ID_SELECT_RB9	33	R130	18:17
ID8	ID_SELECT_RB10	34	R131	16:15
ID9	ID_SELECT_RB11	35	R132	14:13
ID10	ID_SELECT_RB12	41	R133	12:11
ID11	ID_SELECT_RB13	42	R134	10:9
ID12	ID_SELECT_RC1	6	R135	8:7
ID13	ID_SELECT_RC2	7	R136	6:5
ID14	ID_SELECT_RC3	8	R137	4:3
ID15	ID_SELECT_RC4	9	R138	2:1

2.5 DIGIO & SPI+16GPIO SIGNALS ON P1 AND P2 HEADERS

2.5.1 DIGIO on P1 and P2 Headers (up to 16 bits supported)

The LAN9252 supports a DIGIO mode, where these signals can be probed on the P1 and P2 headers. To enable DIGIO mode, from the default state of the board, the SW26 switch must be changed to the PIM position (upward). The respective DIGIO signal mappings on the P1 and P2 headers are detailed in Table 2-22.

Note 1: In the default state, headers P1 and P2 are not assembled. These headers can each be populated with a Molex 87758-4616.

2: The user must ensure that the EEPROM is configured in DIGIO mode.

TABLE 2-22: DIGIO MODE P1 & P2 HEADER SIGNALS

HBI Indexed	HBI Multiplexed	DIGIO	P1/P2 Pin
RD/RD_WR	RD/RD_WR	DIGIO15	P1.8
WR/ENB	WR/ENB	DIGIO14	P1.10
CS	CS	DIGIO13	P1.26
A4	-	DIGIO12	P1.41
A3	-	DIGIO11	P1.44
A2	ALEHI	DIGIO10	P2.21
A1	ALELO	OE_EXT	P1.7
A0/D15	AD15	DIGIO9	P1.15
D14	AD14	DIGIO8	P1.16
D13	AD13	DIGIO7	P1.11
D12	AD12	DIGIO6	P1.12
D11	AD11	DIGIO5	P1.17
D10	AD10	DIGIO4	P1.14
D9	AD9	LATCH_IN	P1.13
D8	AD8	DIGIO2	P1.19
D7	AD7	DIGIO1	P1.4
D6	AD6	DIGIO0	P1.3
D5	AD5	OUTVALID	P1.22
D4	AD4	DIGIO3	P1.23

TABLE 2-22: DIGIO MODE P1 & P2 HEADER SIGNALS (CONTINUED)

HBI Indexed	HBI Multiplexed	DIGIO	P1/P2 Pin
D3	AD3	WD_TRIG	P1.6
D2	AD2	SOF	P1.5
D1	AD1	EOF	P1.24
D0	AD0	WD_STATE	P1.25

2.5.2 SPI+GPIO on P1 and P2 Headers (up to 16 bits supported)

The LAN9252 supports an SPI+16GPIO mode, where these signals can be probed on the P1 and P2 headers. To enable SPI+16GPIO mode, from the default state of the board, the SW26 switch must be changed to the PIM position (upward) and SW19, SW20, and SW21 must be changed to the downward side. The respective SPI+16GPIO signal mappings on the P1 and P2 headers are detailed in Table 2-23.

Note 1: In the default state, headers P1 and P2 are not assembled. These headers can each be populated with a Molex 87758-4616.

2: The user must ensure that the EEPROM is configured in DIGIO mode.

TABLE 2-23: SPI+16GPIO MODE P1 & P2 HEADER SIGNALS

HBI Indexed	HBI Multiplexed	SPI+16GPIO	P1/P2 Pin
RD/RD_WR	RD/RD_WR	GPI15/GPO15	P1.8
WR/ENB	WR/ENB	GPI14/GPO14	P1.10
CS	CS	GPI13/GPO13	P1.26
A4	-	GPI12/GPO12	P1.41
A3	-	GPI11/GPO11	P1.44
A2	ALEHI	GPI10/GPO10	P2.21
A0/D15	AD15	GPI9/GPO9	P1.15
D14	AD14	GPI8/GPO8	P1.16
D13	AD13	GPI7/GPO7	P1.11
D12	AD12	GPI6/GPO6	P1.12
D11	AD11	GPI5/GPO5	P1.17
D10	AD10	GPI4/GPO4	P1.14
D9	AD9	SCK	P1.13
D8	AD8	GPI2/GPO2	P1.19
D7	AD7	GPI1/GPO1	P1.4
D6	AD6	GPI0/GPO0	P1.3
D5	AD5	SCS#	P1.22
D4	AD4	GPI3/GPO3	P1.23
D3	AD3	SIO3	P1.6
D2	AD2	SIO2	P1.5
D1	AD1	SO/SIO1	P1.24
D0	AD0	SI/SIO0	P1.25

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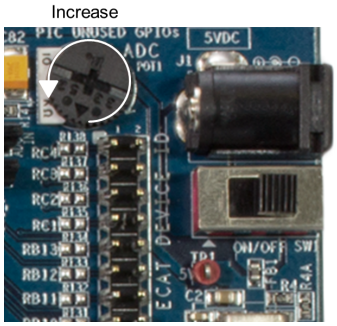
2.6 ADDITIONAL FEATURES

The EVB-LAN9252-HBI+ includes additional features that were not available in the previous revision of the board. This section details these additional features. To learn more about how to use them refer to the Quick Start guide found at microchip.com.

2.6.1 Potentiometer

The EVB-LAN9252-HBI+ includes a potentiometer, as shown in Figure 2-8. The potentiometer is used as an input to the PIC32 and is labeled as “pot1” on the board.

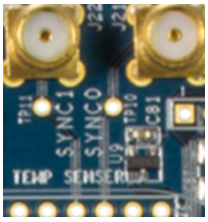
FIGURE 2-8: POTENTIOMETER POT1



2.6.2 Temperature Sensor

The EVB-LAN9252-HBI+ includes a Microchip temperature sensor (TC104AVNBTR), as shown in Figure 2-9. The temperature sensor is used as an input into the PIC32 and is labeled “U9” on the board.

FIGURE 2-9: TEMPERATURE SENSOR U9



2.6.3 UART RS-232

A RS-232 connector is present on the board as J24. This allows serial communication with the PIC32. With this connector UART communication is possible as both an input and an output.

2.6.4 DAC

Through an on-board Microchip digital to analog converter (MCP4726) it is possible to use the EtherCAT application to input a value to the DAC and get a calculated voltage output on the DAC. It it labeled as U10 on the board and can be seen next to the potentiometer.

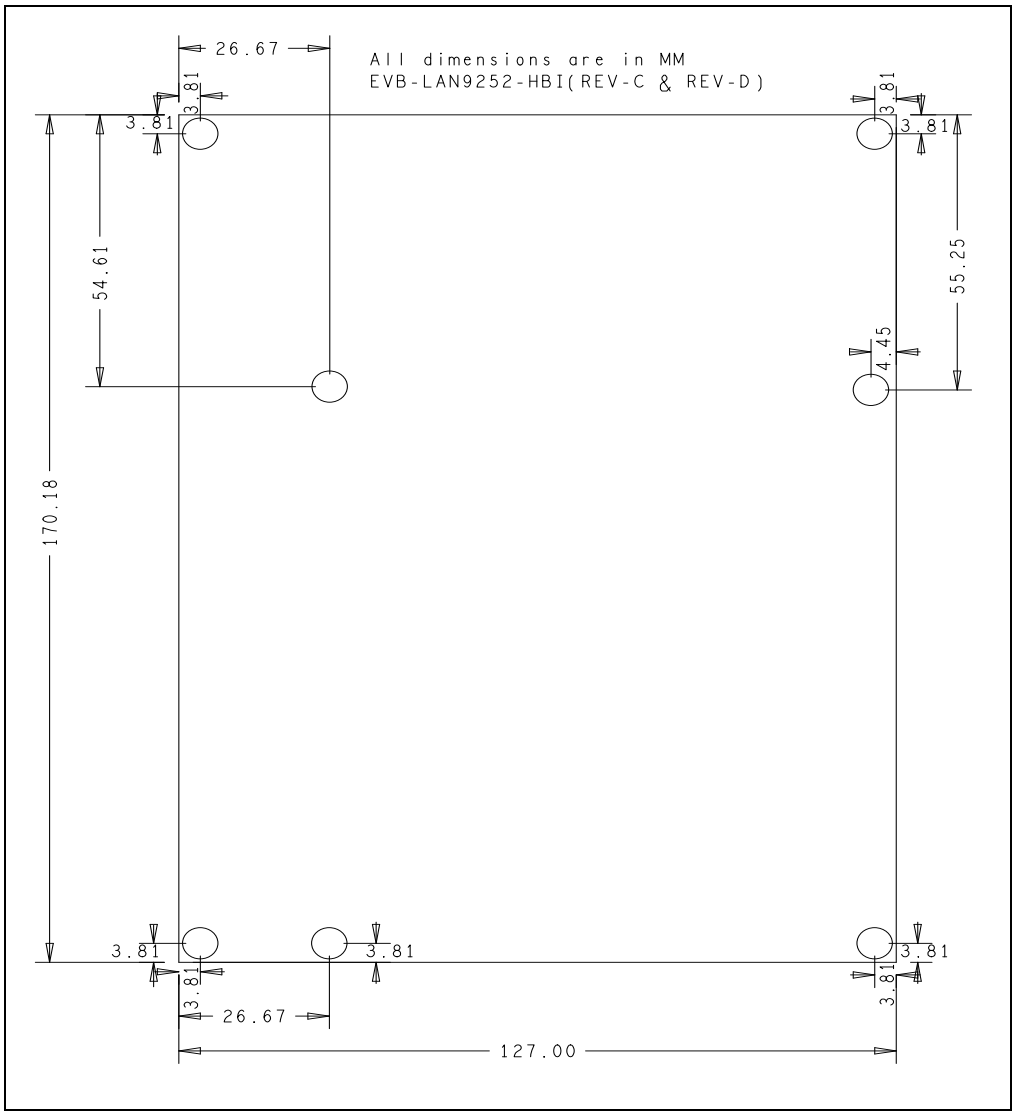
2.7 LIMITATIONS

The EVB-LAN9252-HBI+ has the following limitations:

1. While the LAN9252 supports both SFP and SFF Fiber Modes, the EVB-LAN9252-HBI+ supports only the SFP Fiber Mode.
2. SQI is not supported when using the on-board PIC32MX.

2.8 MECHANICALS

FIGURE 2-10: EVB-LAN9252-HBI+ MECHANICAL DIMENSIONS



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Chapter 3. Software Development Kit

This chapter explains the architecture of the LAN9252 EtherCAT® slave stack firmware sample and introduces the SDK framework for use with PIC32MX microcontroller for EVB-LAN9252-HBI+ development.

This chapter includes the following sub-sections:

- Prerequisites
- ESC SDK Sample Overview
- Using the Sample Project
- Programming the LAN9252 EEPROM

3.1 PREREQUISITES

3.1.1 Hardware Requirements

- EVB-LAN9252-HBI+-SPI-SQI-GPIO
- Windows Host Machine with minimum 2GB RAM
- Programmers – Aardvark I2C/SPI Host Adapter, Pickit3 Programmer

3.1.2 Software Requirements

- MPLAB IDE v2.20 or higher
- MPLAB XC Compiler v1.33 or higher
- Total Phase Flash Centre V1.31 or higher

3.2 ESC SDK SAMPLE OVERVIEW

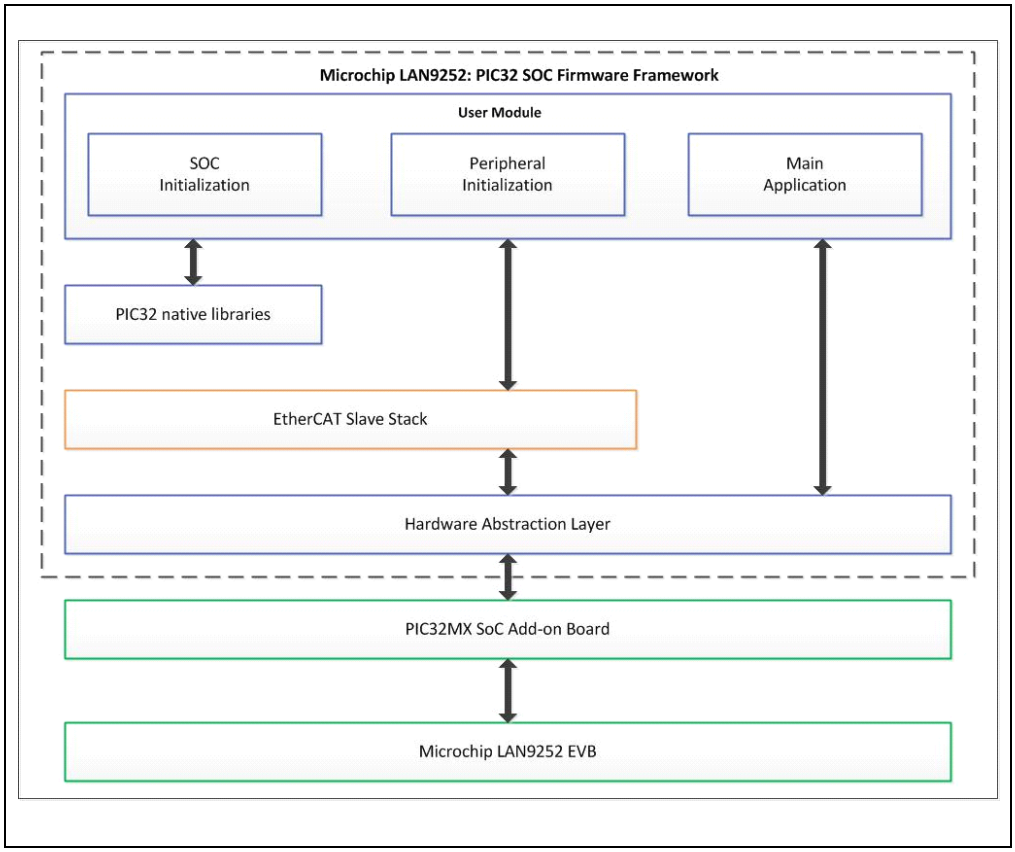
The LAN9252 ESC supports interfacing to an external SoC using an SPI or HBI interface. This PIC32 based SDK sample contains separate projects for HBI and SPI interfaces.

This software SDK is developed as a bare-metal firmware implementation (not specific to any OS) designed to access the LAN9252 ESC features via an HBI or SPI interface. The EtherCAT® slave stack portion of the source is obtained from EtherCAT Technology Group.

This software project has been tested with the EVB-LAN9252-HBI+ using the PIC32MX SoC.

Figure 3-1 provides an architectural block diagram of the SDK's various source modules. The subsequent sections detail these blocks.

FIGURE 3-1: PIC32 SOC FIRMWARE FRAMEWORK



3.2.1 User Module

3.2.1.1 SOC INITIALIZATION

This code block is part of the user application that boots the PIC microcontroller with the desired RAM configuration, clock speed, clock source and other related features of the controller, per the user's configuration.

3.2.1.2 PERIPHERAL INITIALIZATION

This code block configures and initiates the core peripherals (UART, I^2C, SPI) and external peripherals (EEPROM, LAN9252).

3.2.1.3 MAIN APPLICATION

This code block contains the code that runs the LAN9252 EtherCAT® slave module demo application.

3.2.2 EtherCAT® Slave Stack

This code block contains the EtherCAT slave stack.

3.2.3 Hardware Abstraction Layer (HAL)

This code block contains the low level layer that provides software hooks/APIs to the application module and slave stack, allowing communication between these modules and the hardware resources. For additional information, refer to the **ReadMe.txt** file located in the project source folder.

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3.3 USING THE SAMPLE PROJECT

3.3.1 MPLAB IDE Project Settings & Firmware Download

1. Once the EtherCAT SSC is integrated with LAN9252 SDK as detailed in “Integrating LAN9252 - PIC32MX SDK with EtherCAT SSC from ETG” application note, Copy it to the desired directory. (For the purposes of this document, the Desktop will be the target folder).
2. Open the MPLAB IDE and import the SSC project into the IDE.

FIGURE 3-2: MPLAB IDE OPEN PROJECT

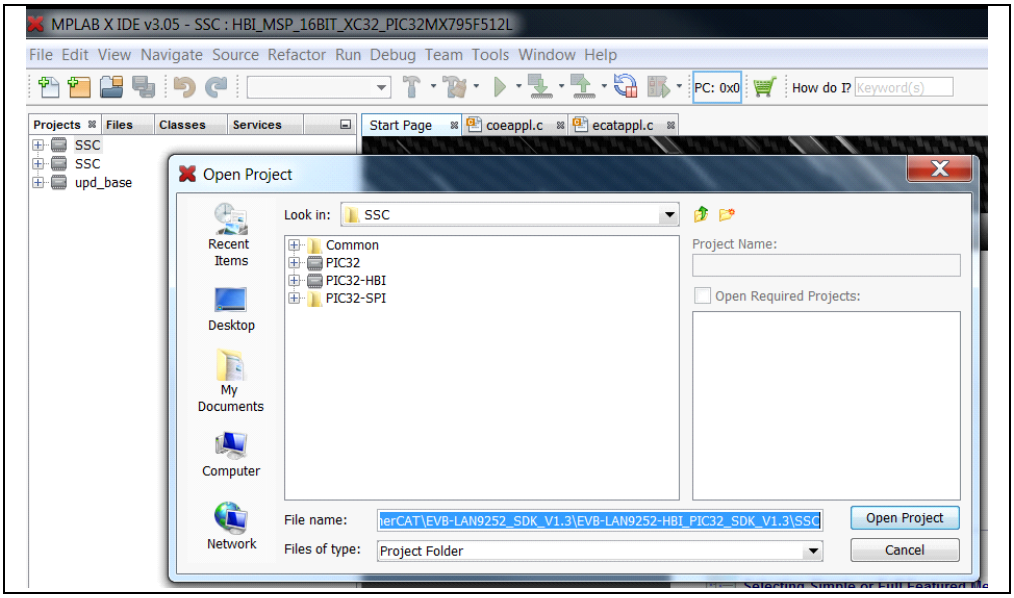
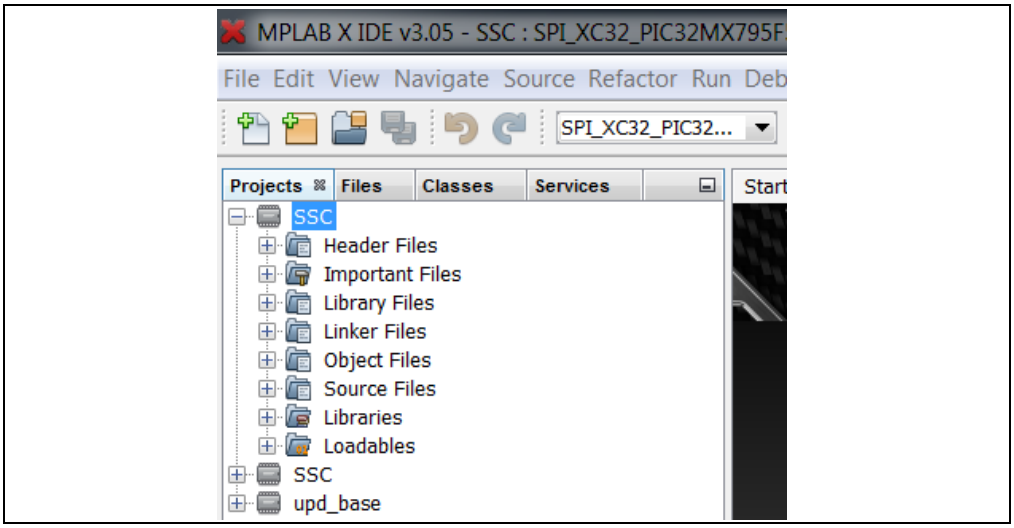


FIGURE 3-3: MPLAB IDE PROJECT DIRECTORY



The target directory contains two project folders:

- PIC32-HBI Project Folder
- PIC32 Project Folder

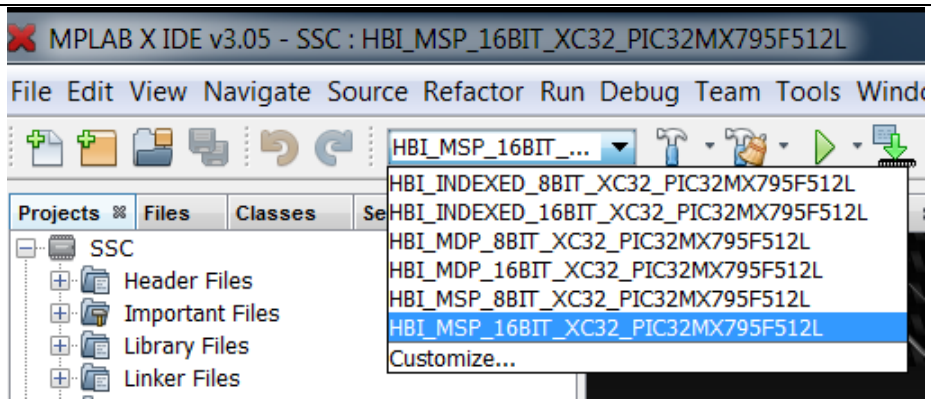
3.3.1.1 PIC32-HBI PROJECT FOLDER

The PIC32 project folder contains the sample code that enables the LAN9252's HBI interface to communicate with the SoC. HBI demo code is provided for each of the LAN9252's six HBI configurations. These configurations can be selected respectively from the configuration drop down box as shown in Figure 3-4.

TABLE 3-1: HBI CONFIGURATIONS

HBI Configuration (Project)	Description
HBI_INDEXED_8BIT_XC32_PIC32MX79F512	8-bit Indexed mode
HBI_INDEXED_16BIT_XC32_PIC32MX79F512	16-bit Indexed mode
HBI_MDP_8BIT_XC32_PIC32MX79F512	8-bit Multiplexed dual phase mode
HBI_MDP_16BIT_XC32_PIC32MX79F512	16-bit Multiplexed dual phase mode
HBI_MSP_8BIT_XC32_PIC32MX79F512	8-bit Multiplexed single phase mode
HBI_MSP_16BIT_XC32_PIC32MX79F512	16-bit Multiplexed single phase mode

FIGURE 3-4: MPLAB IDE HBI CONFIGURATION SELECTION



3.3.1.2 PIC32 PROJECT FOLDER

The PIC32-SPI project folder contains the demo code that enables the LAN9252's SPI interface to communicate with the SoC.

- Refer to the LAN9252 data sheet for more details on these HBI interface and its modes.
- Refer to Section 2.4.4 "DIGIO/HBI/SPI+GPIO Selection" for SPI jumper configurations.

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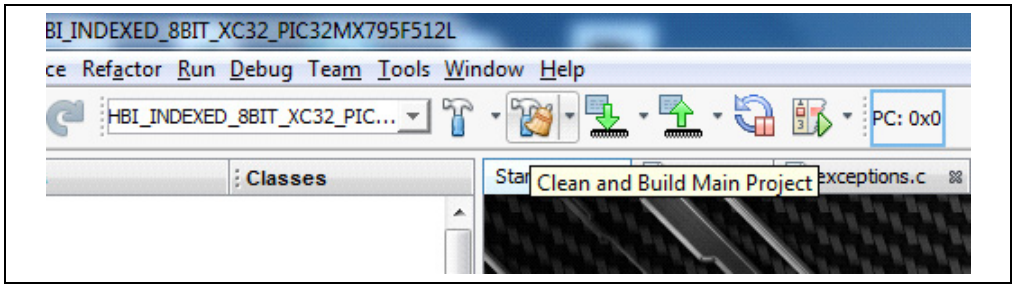
3.3.2 Compiling and Programming SoC Firmware

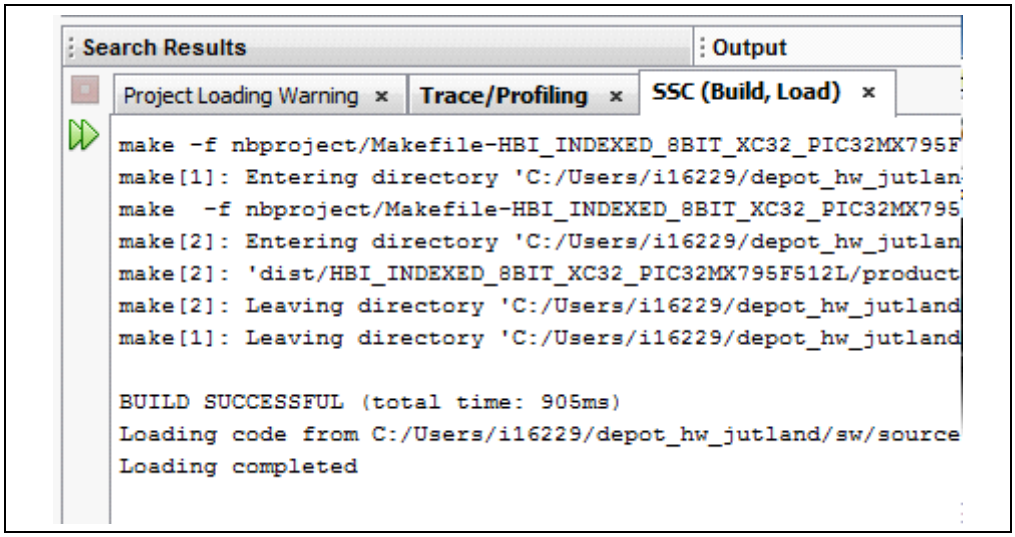
1. Compile the source code (with corresponding configuration selected if HBI project is loaded).

FIGURE 3-5: MPLAB IDE COMPILE PROJECT SELECTION



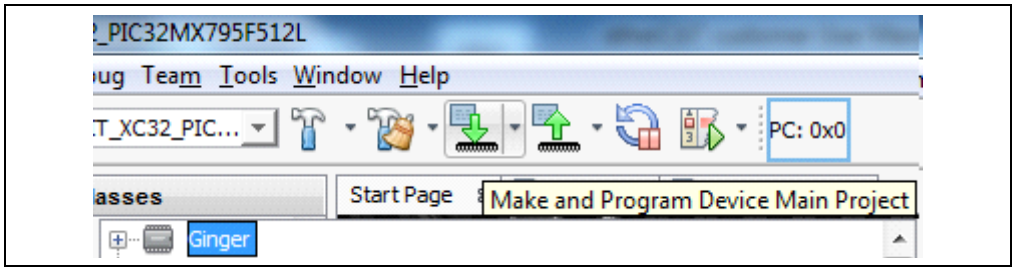
2. If the compilation is successful, the output window will display “BUILD SUCCESSFUL”, as shown in Figure 3-6.

FIGURE 3-6: MPLAB IDE BUILD SUCCESSFUL



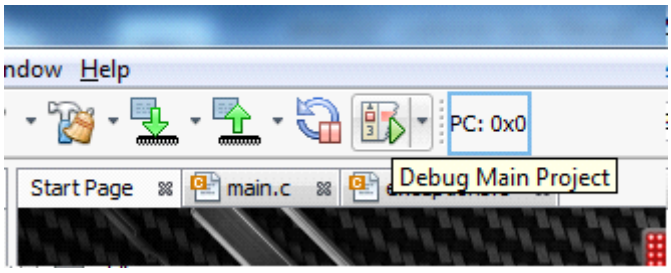
3. Before initiating the firmware download, ensure the debugger/programmer is connected to the EVB’s JTAG pins. (This demo project is debugged with the PICkit-3 In-Circuit debugger/programmer).
4. To program the PIC32 SoC, click the “Make and Program Device Main Project” button.

FIGURE 3-7: MPLAB IDE PROGRAM DEVICE



5. To debug the PIC32 SoC, click "Debug Main Project" button.

FIGURE 3-8: MPLAB IDE DEBUG DEVICE



3.4 PROGRAMMING THE LAN9252 EEPROM

The LAN9252 configures itself to the desired mode (SPI, 6 HBI modes) by reading the strap settings located in EEPROM. The LAN9252 EEPROM is programmed and validated via the TwinCAT master tool. The EEPROM can also be programmed using an external IIC Master, like AARDVARK.

3.4.1 Programming LAN9252 EEPROM using the TwinCAT Master Tool

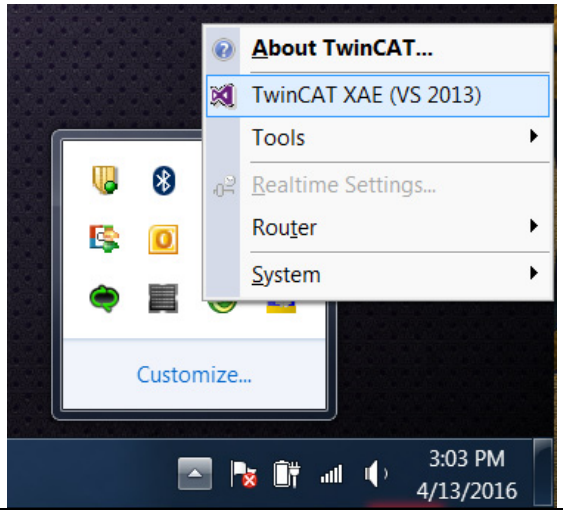
The programming procedure using the TwinCAT master tool is as follows:

Note 1: This example utilizes the TwinCAT tool. Procedures may differ when using other EtherCAT® master tools.

2: Ensure the system network properties are configured properly for the EtherCAT® frames, Ethernet cable linking your system, and EtherCAT® slave board.

1. Load the corresponding ESI file in the directory path "C:\TwinCAT\3.1\Config\Io\EtherCAT". For this demo, the ESI file for the 16-Bit Multiplexed Single-Phase Mode is used.
2. If TwinCAT installed successfully, a TwinCAT icon will be shown in the bottom-right corner of the desktop. After clicking the icon, a pop-up list will display. Select "TwinCAT XAE (VS 2013)", as shown in Figure 3-9.

FIGURE 3-9: TWINCAT SYSTEM MANAGER



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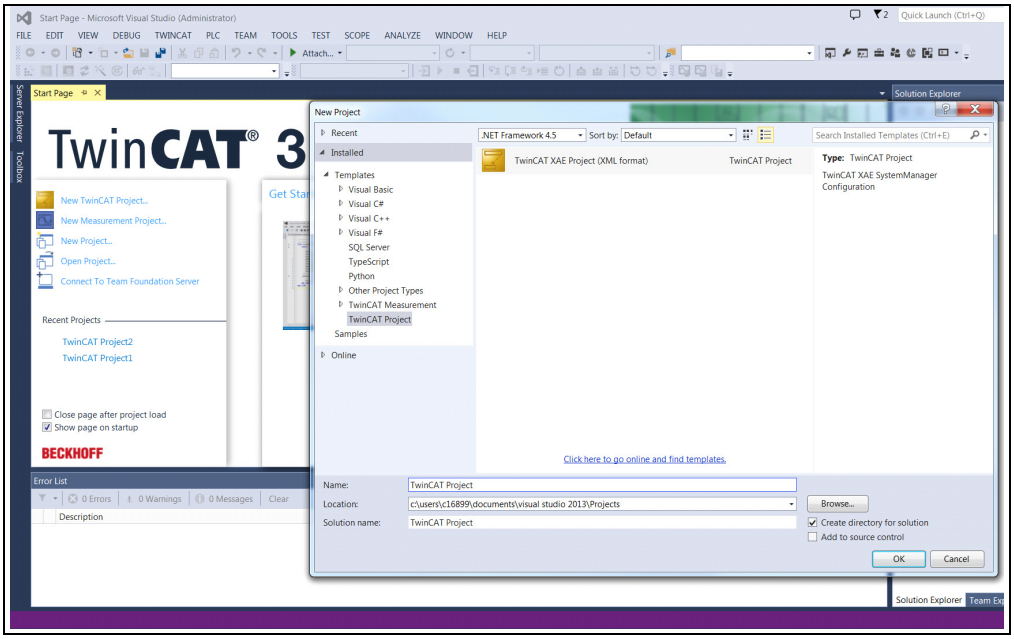
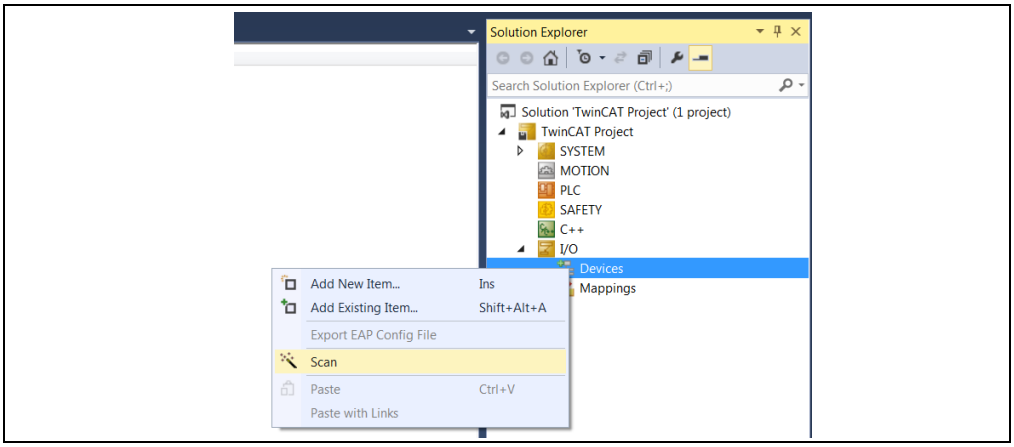
3. Click on “New TwinCAT Project” as shown in Figure 3-10. Choose a name and click “ok”.

FIGURE 3-10: TWINCAT DELETE DEVICE



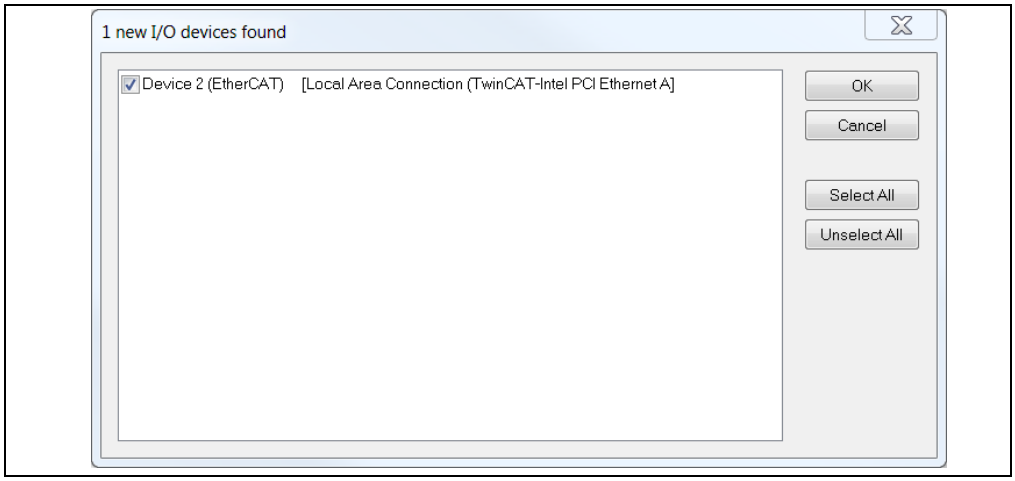
4. Scan for EtherCAT® slave devices by expanding “I/O” and right clicking “Devices” and then selecting “Scan”, as shown in Figure 3-11.

FIGURE 3-11: TWINCAT SCAN DEVICES



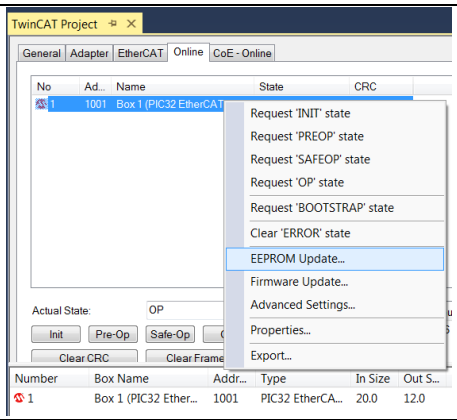
5. After scanning is complete, a window showing devices found will appear similar to Figure 3-12.

FIGURE 3-12: TWINCAT DEVICE LIST



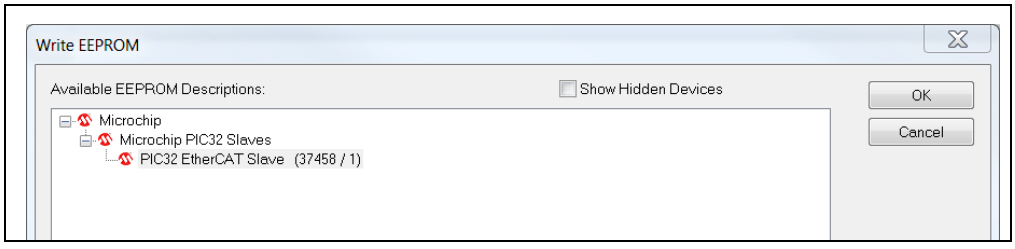
6. Click "Yes" for Scan for Boxes and "Yes" for Activate Free Run.
7. After a successful scan, click the "Device 2 (EtherCAT)" drop down bar on the left panel of the TwinCAT tool (as highlighted in Figure 3-11). Then click the "Online" tab on the right-side panel of the TwinCAT tool, as shown in Figure 3-13. Right click the LAN9252 listing and select "EEPROM Update" from the contextual menu.

FIGURE 3-13: TWINCAT EEPROM UPDATE



8. Upon selecting "EEPROM Update", the Write EEPROM window will open. Click the "OK" button to initiate EEPROM programming (Figure 3-14).

FIGURE 3-14: TWINCAT WRITE EEPROM



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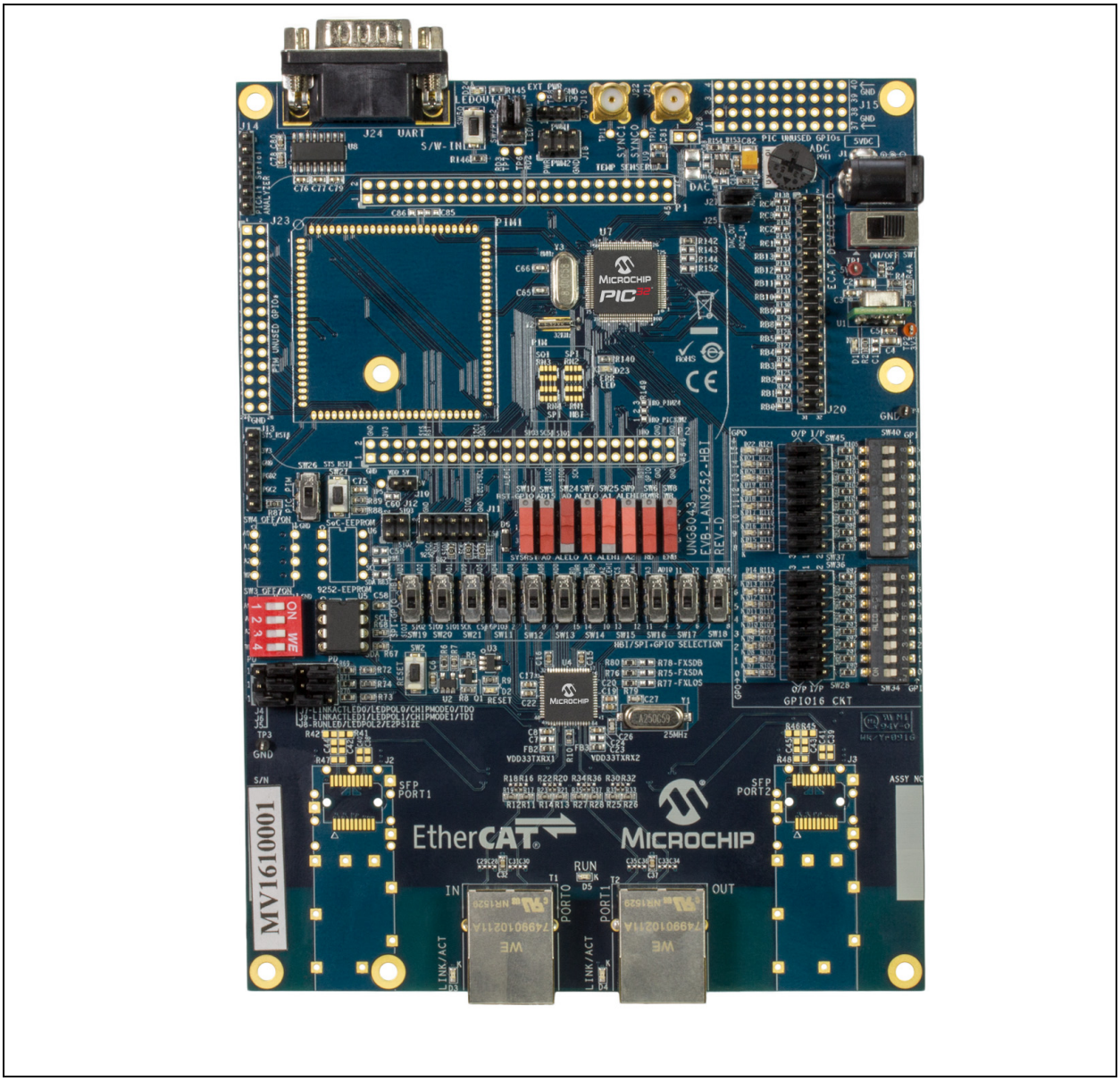
Appendix A. Evaluation Board Photo

A.1 INTRODUCTION

This appendix shows the EVB-LAN9252-HBI+ Evaluation Board.

FIGURE A-1: EVB-LAN9252-HBI+ EVALUATION BOARD



Appendix B. Evaluation Board Schematics

B.1 INTRODUCTION

This appendix shows the EVB-LAN9252-HBI+ Evaluation Board Schematics.

FIGURE B-1: EVB-LAN9252-HBI+ SCHEMATIC POWER SUPPLY & RESET

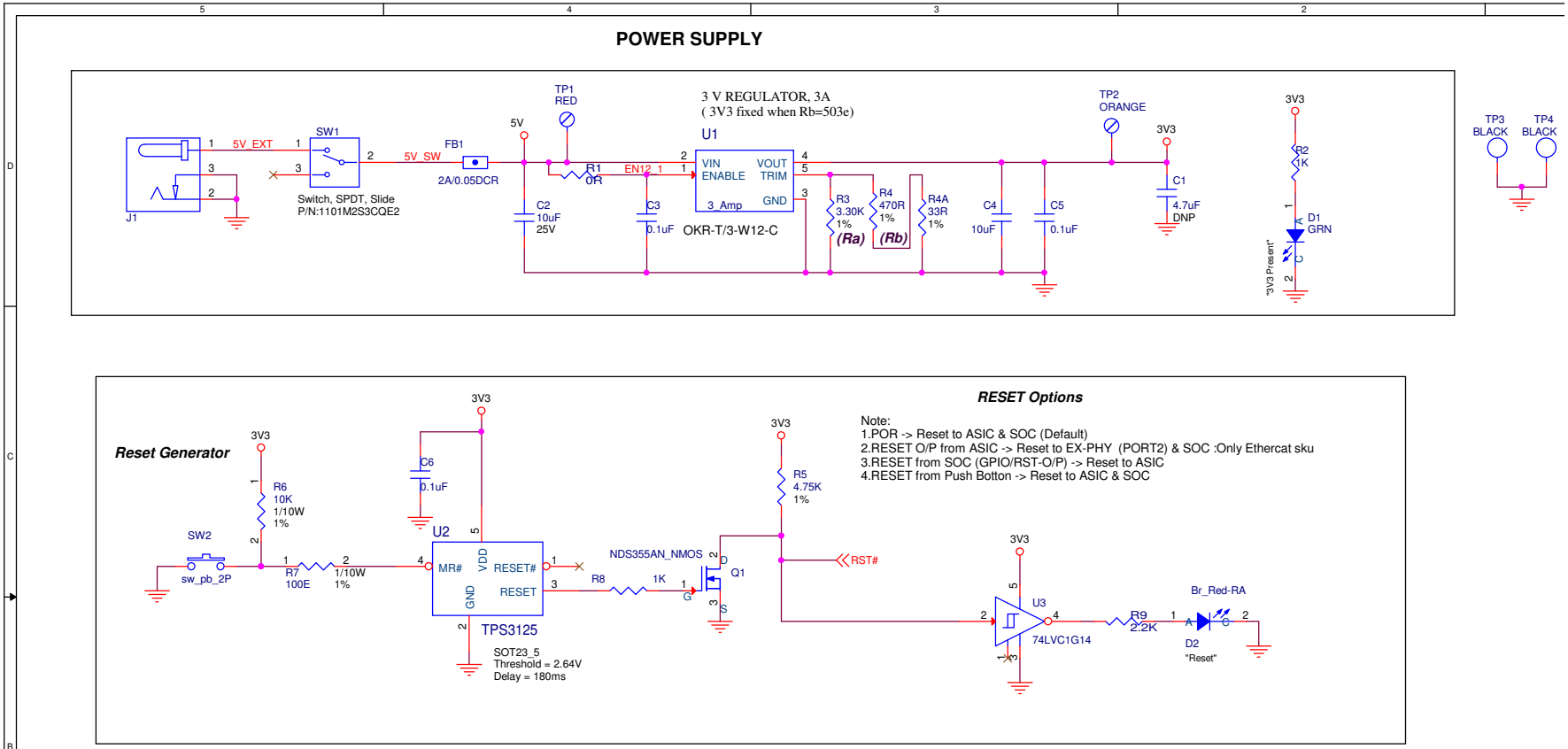


FIGURE B-2: EVB-LAN9252-HBI+ SCHEMATIC LAN9252

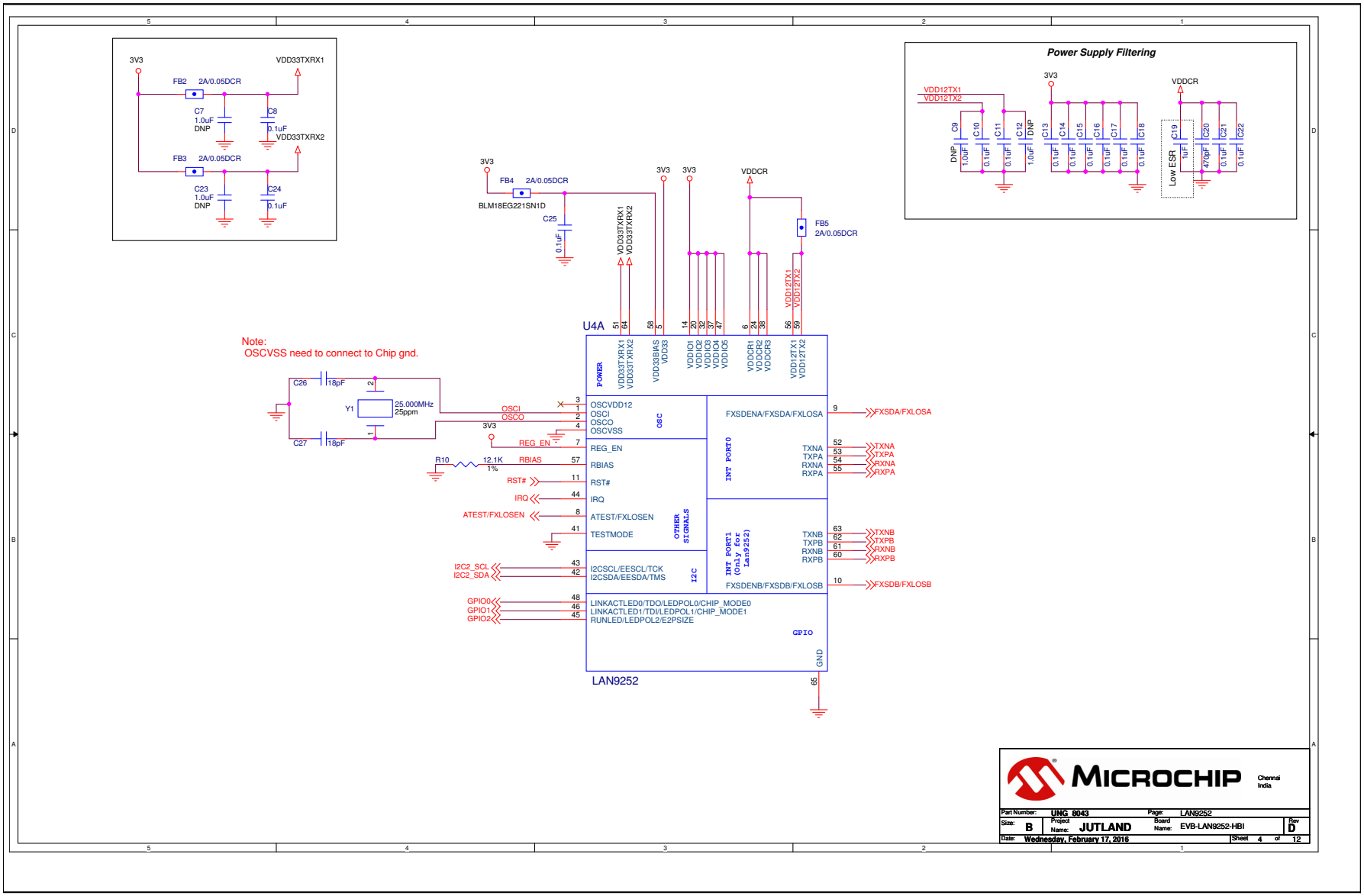


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FIGURE B-3: EVB-LAN9252-HBI+ SCHEMATIC COPPER MODE INTERFACE

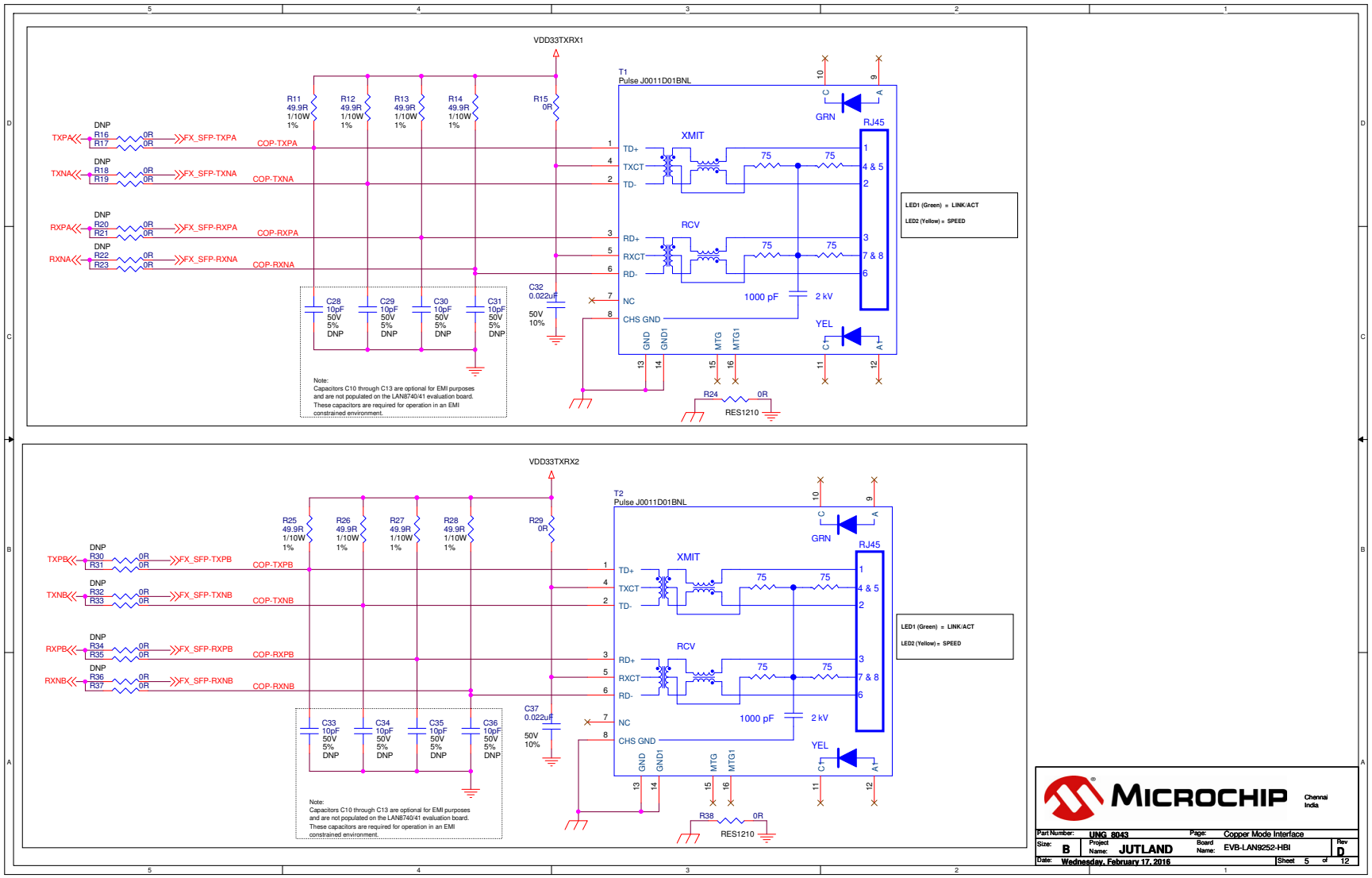

FIGURE B-4: EVB-LAN9252-HBI+ SCHEMATIC SFP INTERFACE

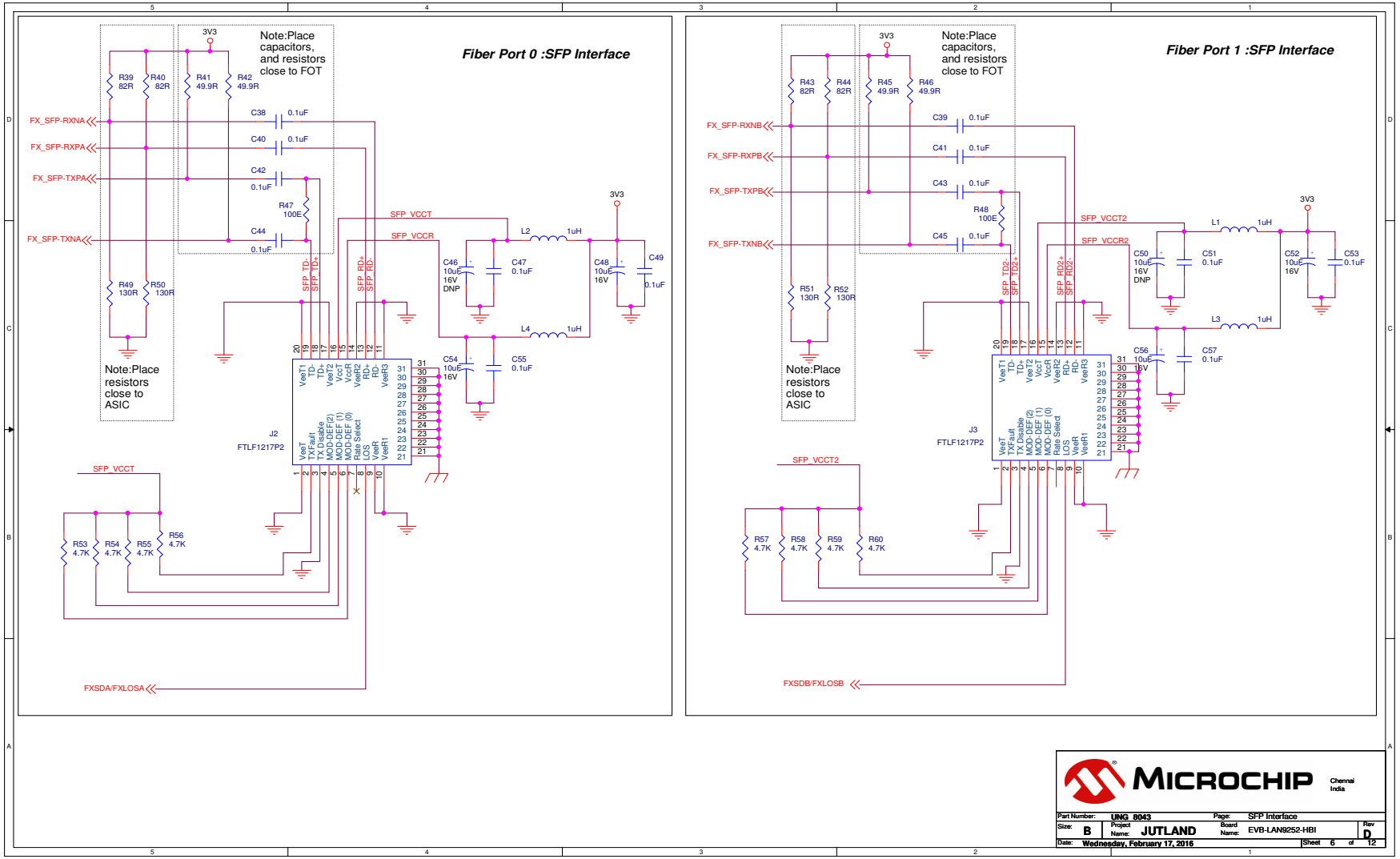

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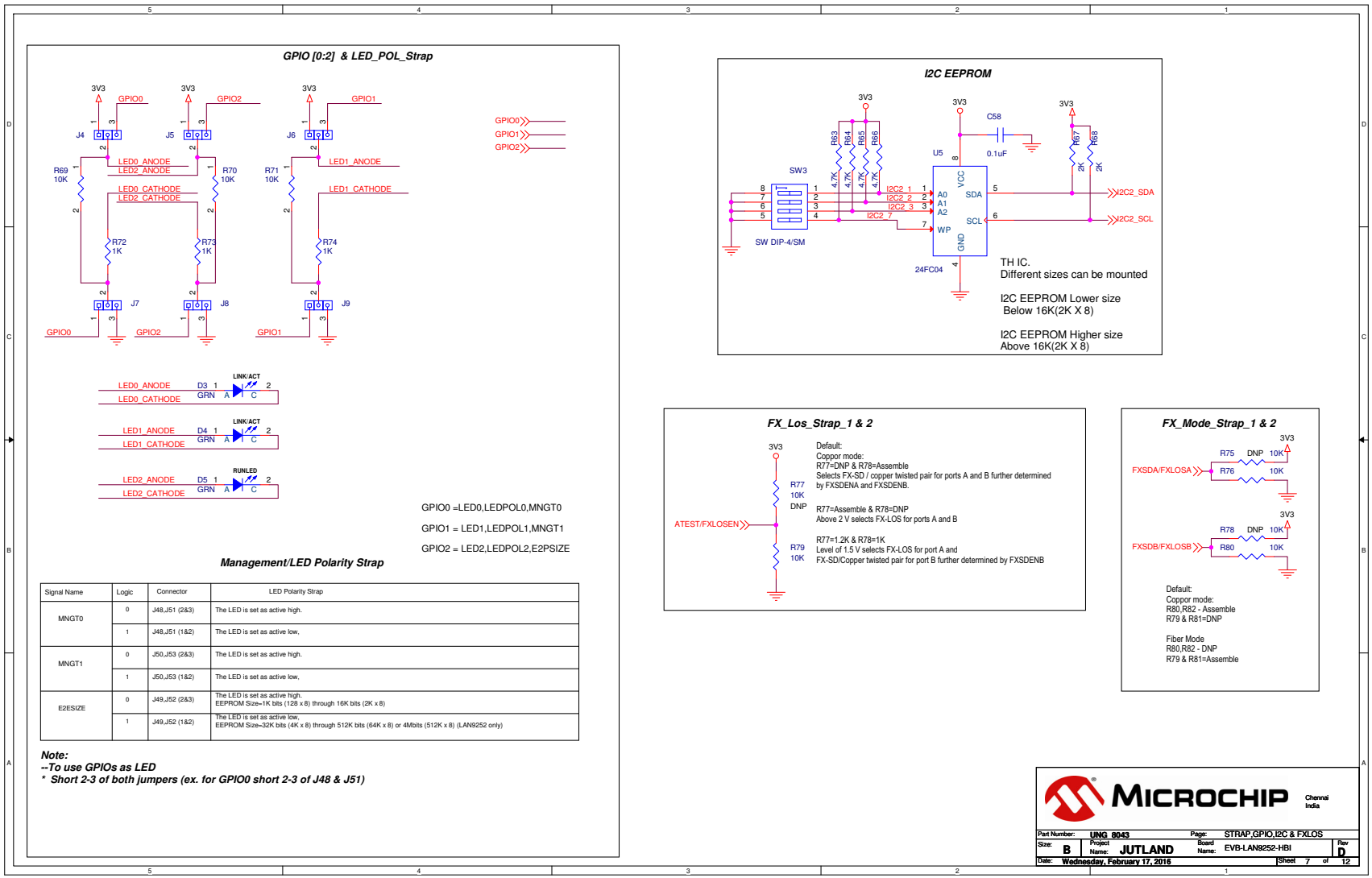
FIGURE B-5: EVB-LAN9252-HBI+ SCHEMATIC STRAP, GPIO, I2C & FXLOS



Signal Name	Logic	Connector	LED Polarity Strap
MNGT0	0	J48,J51 (2&3)	The LED is set as active high.
	1	J48,J51 (1&2)	The LED is set as active low,
MNGT1	0	J50,J53 (2&3)	The LED is set as active high.
	1	J50,J53 (1&2)	The LED is set as active low,
E2ESIZE	0	J49,J52 (2&3)	The LED is set as active high. EEPROM Size=1K bits (128 x 8) through 16K bits (2K x 8)
	1	J49,J52 (1&2)	The LED is set as active low, EEPROM Size=32K bits (4K x 8) through 512K bits (64K x 8) or 4Mbits (512K x 8) (LAN9252 only)

Note:
--To use GPIOs as LED
**** Short 2-3 of both jumpers (ex. for GPIO0 short 2-3 of J48 & J51)***

FIGURE B-6: EVB-LAN9252-HBI+ SCHEMATIC BOARD TO BOARD INTERFACE

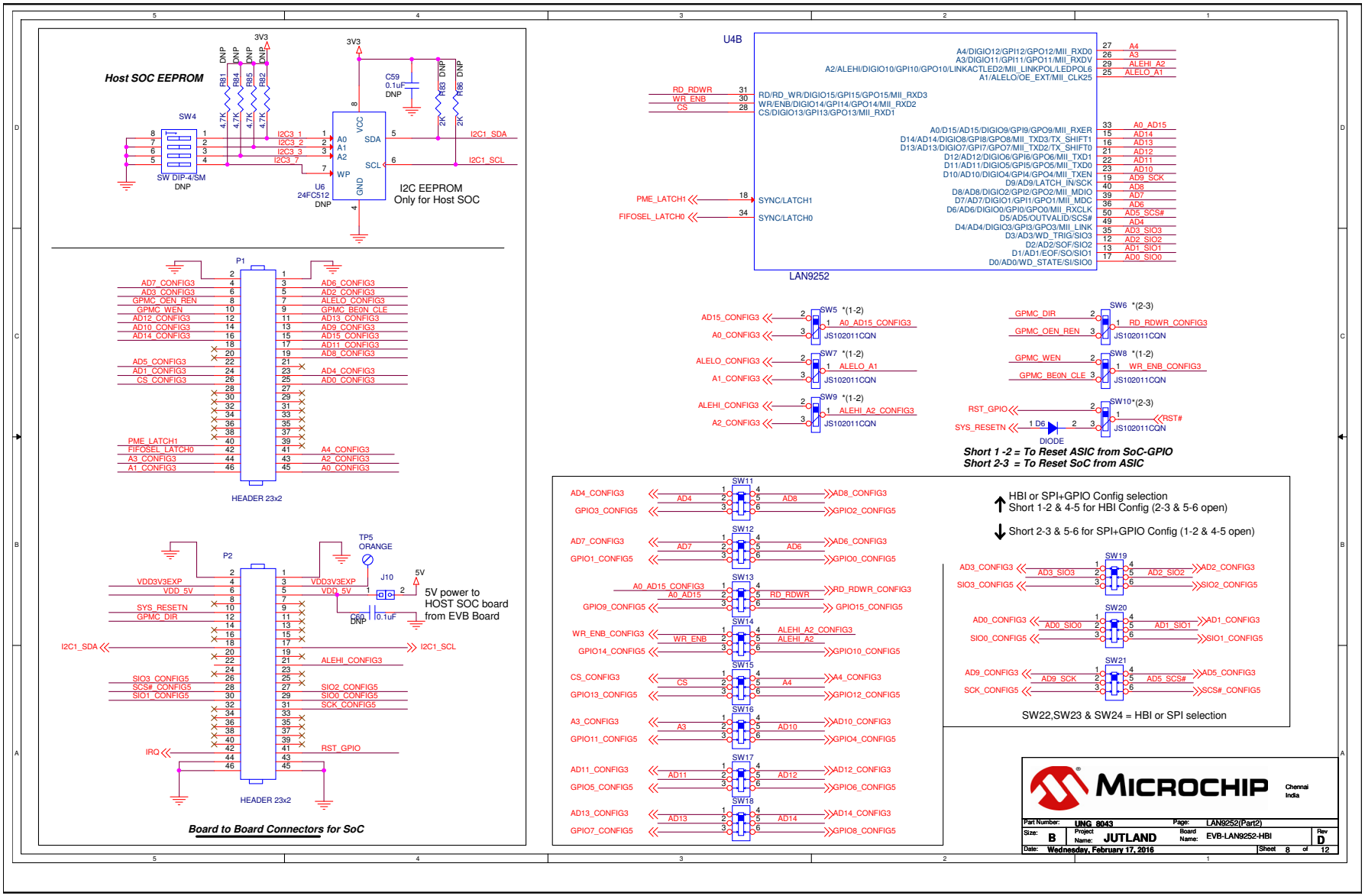


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FIGURE B-7: EVB-LAN9252-HBI+ SCHEMATIC PIC32MX

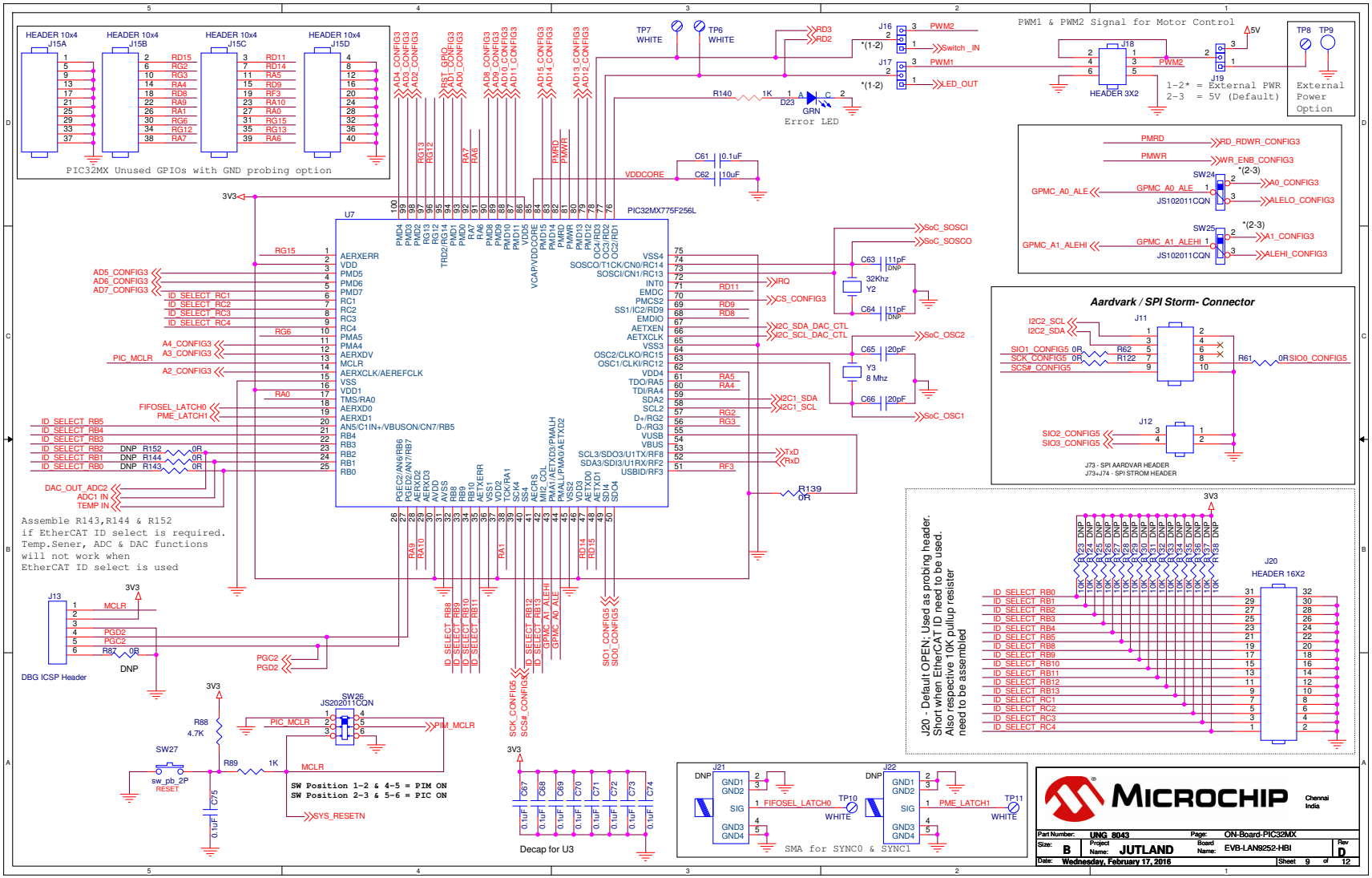

FIGURE B-8: EVB-LAN9252-HBI+ SCHEMATIC GPIOS

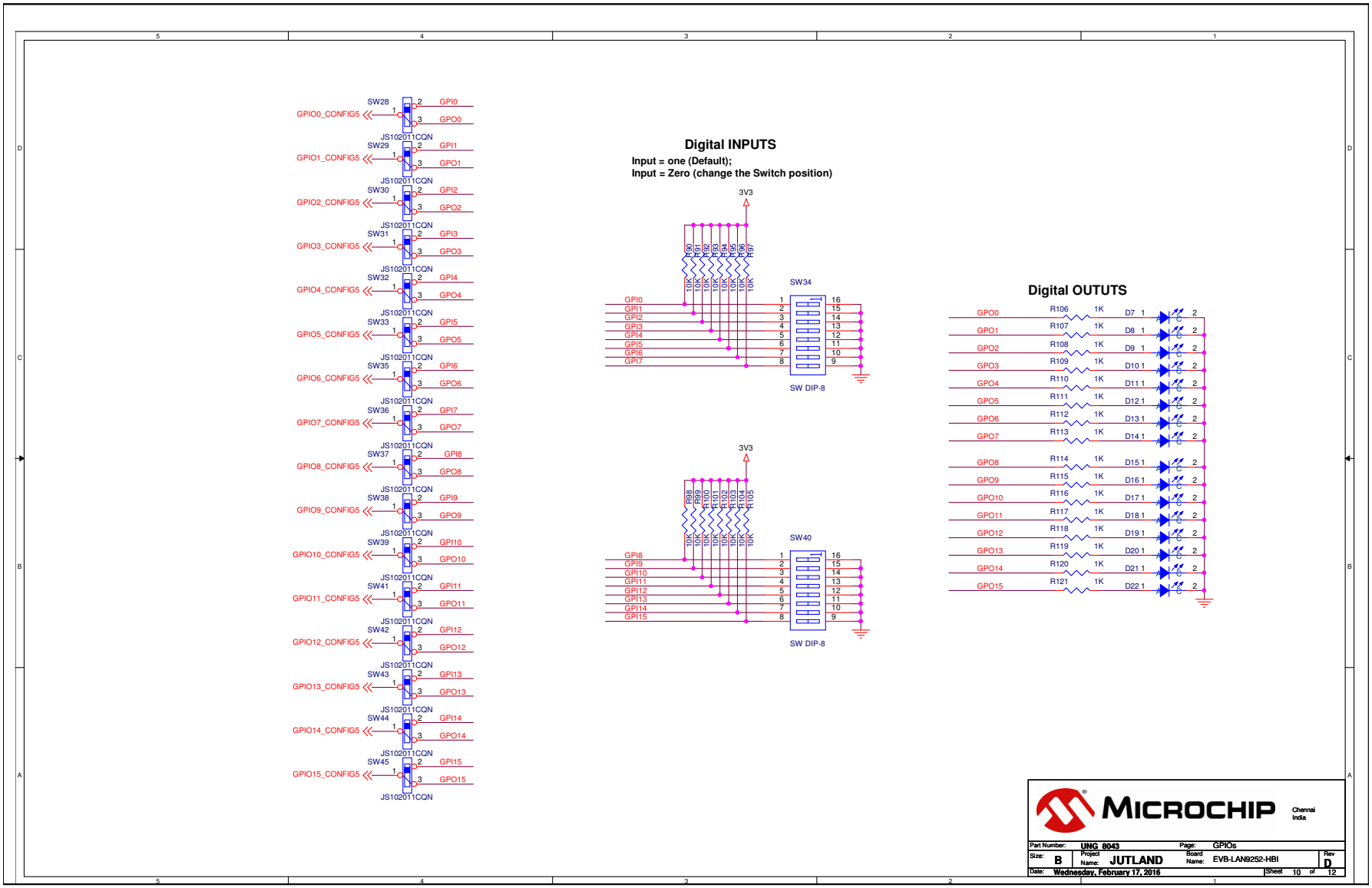

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FIGURE B-9: EVB-LAN9252-HBI+ SCHEMATIC UART, ADC, &DAC

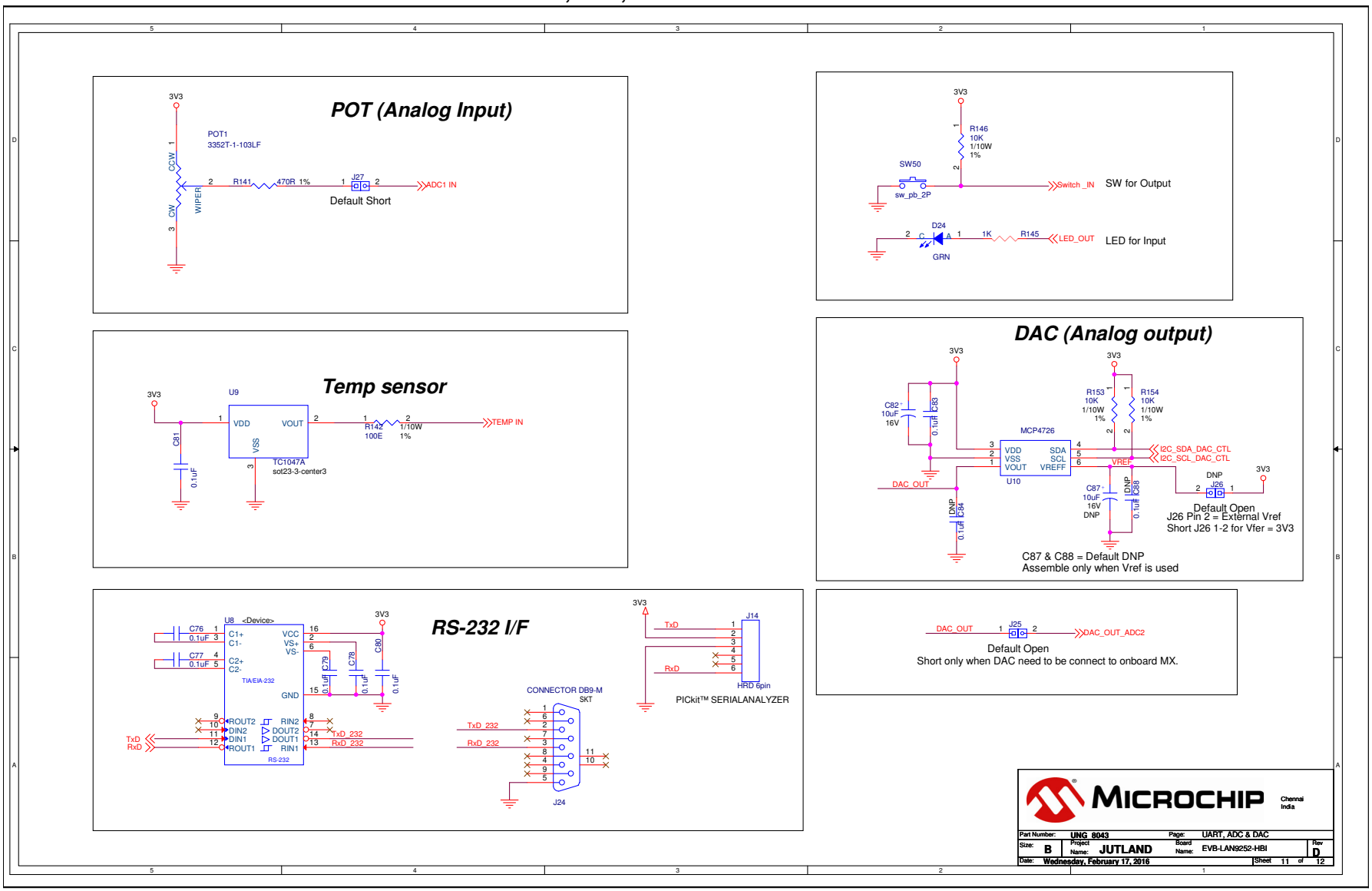

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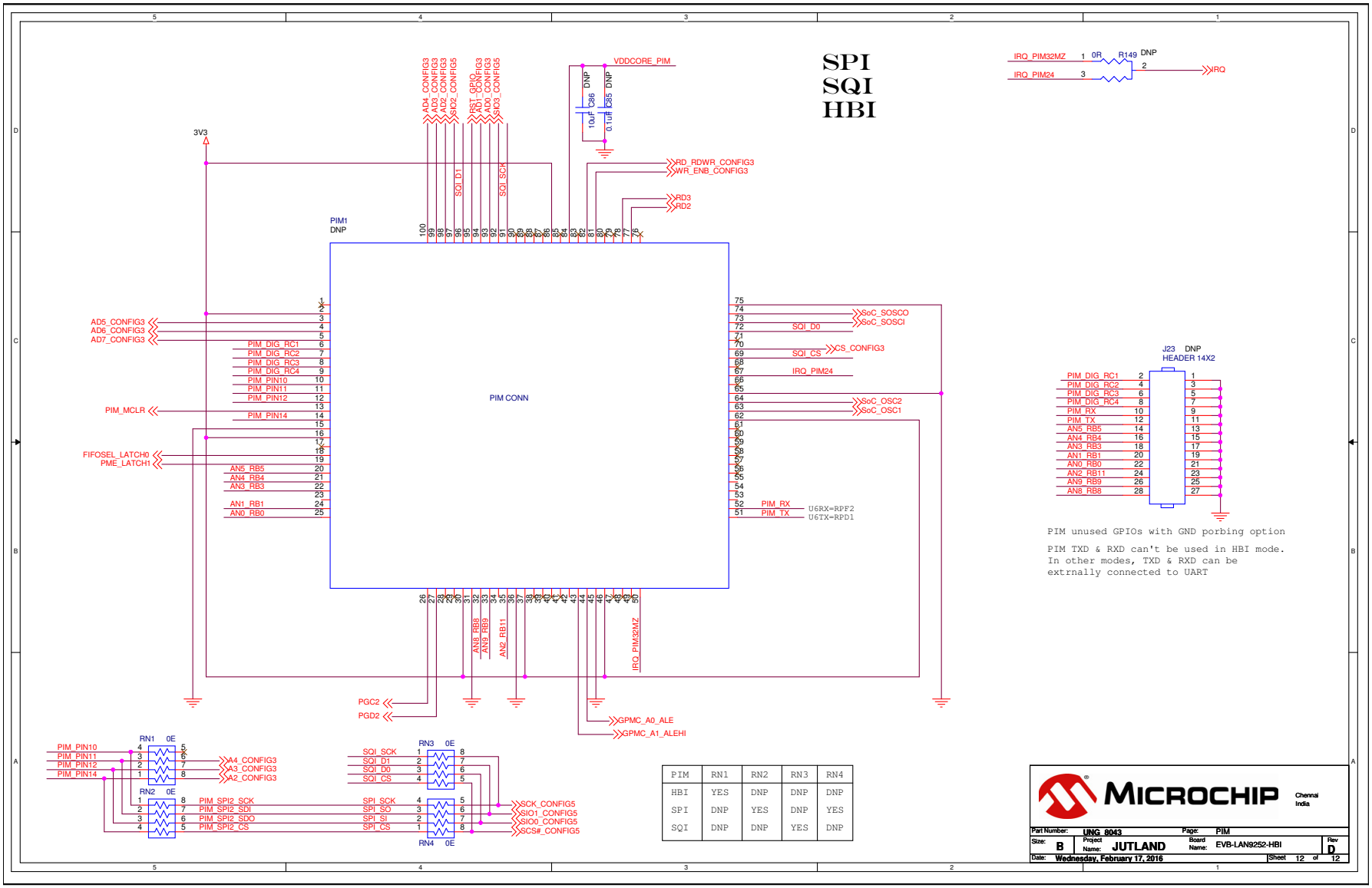
FIGURE B-10: EVB-LAN9252-HBI+ SCHEMATIC PIM



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Appendix C. Bill of Materials (BOM)

C.1 INTRODUCTION

This appendix includes the EVB-LAN9252-HBI+ Evaluation Board Bill of Materials (BOM).

Item	Qty	Reference	Part	PCB Footprint	DNP	Vender	Vender P/N
2	2	C2,C4	10uF	CAP0805	No	Murata	GRM21BR61E106KA73L
3	34	C3,C5,C6,C8,C10,C11,C13,C14,C15,C16,C17,C18,C21, C22,C24,C25,C58,C61,C67,C68,C69,C70,C71,C72,C73, C74,C75,C76,C77,C78,C79,C80,C81,C83	0.1uF	CAP0603	No	Murata	GRM188R71E104KA01D
5	1	C19	1uF	CAP0603	No	Murata	GRM188R61C105KA93D
6	1	C20	470pF	CAP0603	No	Murata	GRM188R71H471KA01D
7	2	C26,C27	18pF	CAP0603	No	Murata	GRM1885C1H180JA01D
9	2	C32,C37	0.022uF	CAP0603	No	Kemet	C0603C223K5RACTU
12	1	C62	10uF	CAP0603	No	TDK	C1608X5R0J106K080AB
13	2	C63,C64	11pF	CAP0603	No	Murata	GRM1885C1H110JA01D
14	2	C65,C66	20pF	CAP0603	No	Murata	GRM1885C1H200JA01D
15	1	C82	10uF	CAP_B_3528	No	AVX	TPSB106K016R0500
17	22	D1,D3,D4,D5,D7,D8,D9,D10,D11,D12,D13,D14,D15, D16,D17,D18,D19,D20,D21,D22,D23,D24	GRN	LED0603	No	Wurth electronics	150 060 GS7 500 0
18	1	D2	Br_Red-RA	LED0603	No	Wurth electronics	150 060 RS7 500 0
19	1	D6	DIODE	SOD123	No	Micro Commercial Co	1N4148W-TP
20	5	FB1,FB2,FB3,FB4,FB5	2A/0.05DCR	RES0603	No	Murata	BLM18EG221SN1D
21	1	J1	SKT_PWR_2R0mm_4A_THRU_RA	th_conn_pwrjack_dc-210_rt	No	Cui Stack	PJ-002AH
23	9	J4,J5,J6,J7,J8,J9,J16,J17,J19	HDR_1x3	TH_CONN_1X3P	No	FCI	68000-103HLF
24	3	J10,J25,J27	CONN_2P	th_conn_1x2p	No	FCI	68000-102HLF
25	1	J11	HEADER 5X2	TH_CONN_2X5P	No	FCI	67997-210HLF
26	1	J12	HEADER 2X2	TH_CONN_2X2P	No	FCI	67997-202HLF
27	1	J13	DBG ICSP Header	TH_CONN_1x6P	No	FCI	68000-106HLF
28	1	J14	HRD 6pin	TH_CONN_1x6P	No	FCI	68000-106HLF
30	1	J18	HEADER 3X2	TH_CONN_2X3P	No	FCI	67997-206HLF
31	1	J20	HEADER 16X2	TH_CONN_2X16P	No	FCI	67997-232HLF
32	2	J21,J22	CONN_5P	TH_CONN_SMA-J-P-H-ST-TH1	No	TE	5-1814832-1
34	1	J24	CONNECTOR DB9-M	th_conn_db9_m_rt	No	TE/AMP	5747840-4
38	1	POT1	3352T-1-103LF	TH_POT_3352T	No	Bourns Inc.	3352T-1-103LF
40	1	Q1	NDS355AN_NMOS	sot23-NDS	No	Fairchild	NDS355AN

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41	7	R1,R15,R29,R61,R62,R87,R122	0R	RES0603	No	Panasonic	ERJ-3GEY0R00V
42	24	R2,R8,R72,R73,R74,R89,R106,R107,R108,R109,R110, R111,R112,R113,R114,R115,R116,R117,R118,R119, R120,R121,R140,R145	1K	RES0603	No	Panasonic	ERJ-3GEYJ102V
43	1	R3	3.30K	RES0603	No	Yageo America	9C06031A3301FKHFT
44	2	R4,R141	470R	RES0603	No	BOURNS	CR0603-FX-4700ELF
45	1	R4A	33R	RES0603	No	BOURNS	CR0603-FX-33R0ELF
46	1	R5	4.75K	RES0603	No	Panasonic	ERJ-3EKF4751V
47	26	R6,R69,R70,R71,R146,R153,R154,R76,R79,R80,R90, R91,R92,R93,R94,R95,R96,R97,R98,R99,R100,R101, R102,R103,R104,R105	10.0K	RES0603	No	Panasonic	ERJ-3EKF1002V
48	2	R7,R142	100E	RES0603	No	Panasonic	ERJ-3EKF1000V
49	1	R9	2.2K	RES0603	No	Panasonic	ERJ-3GEYJ222V
50	1	R10	12.1K	RES0603	No	Rohm	CR03ERTF1212
51	8	R11,R12,R13,R14,R25,R26,R27,R28	49.9R	RES0603	No	Yageo America	9C06031A49R9FKHFT
53	8	R17,R19,R21,R23,R31,R33,R35,R37	0R	RES0402	No	Panasonic	ERJ-2GE0R00X
54	2	R24,R38	0R	RES1210		Vishay	CRCW12100000Z0EA
60	5	R63,R64,R65,R66,R88	4.7K	RES0603	No	Panasonic	ERJ-3EKF4701V
61	2	R67,R68	2K	RES0603	No	Panasonic	ERJ-3GEYJ202V
68	1	SW1	SW-SPDT-SLIDE	sw_ck_1101m2s3cqe2	No	C&K	1101M2S3CQE2
69	3	SW2,SW27,SW50	sw_pb_2P	sw_pb_2P	No	Panasonic	EVQ-PJU04K or EVQ-5PN04K
70	1	SW3	SW DIP-4/SM	TH_SW_DIP4	No	Wurth electronics	418117270904
72	8	SW5,SW6,SW7,SW8,SW9,SW10,SW24,SW25	JS102011CQN	TH_SW_SPST_3P_10x2p5	No	Wurth electronics	450301014042
72A	16	SW5,SW6,SW7,SW8,SW9,SW10,SW24,SW25,SW28, SW29,SW30,SW31,SW32,SW33,SW35,SW36,SW37, SW38,SW39,SW41,SW42,SW43,SW44,SW45	HDR_1x3	TH_SW_SPST_3P_10x2p5	No	FCI	68000-103HLF
73	12	SW11,SW12,SW13,SW14,SW15,SW16,SW17,SW18, SW19,SW20,SW21,SW26	JS202011CQN	TH_SW_DPDT_6P	No	C&K	JS202011CQN
74	2	SW34,SW40	SW DIP-8	SW_DIP_SMT_8P-ADE08S04	No	TE	1-1825058-9
75	1	TP1	RED	TH_TP_60D40	No	Keystone	5000
76	1	TP2	ORANGE	TH_TP_60D40	No	Keystone	5003
77	3	TP3,TP4,TP9	BLACK	TH_TP_60D40	No	Keystone	5001
80	2	T1,T2	Pulse - J0011D01BNL	th_conn_pulse_rj45_j0026	No	Pulse Electronics	J0011D01BNL

81	1	U1	3_Amp	TH_DC-DC_VERT_5PIN_P67	No	Murata	OKR-T/3-W12-C
82	1	U2	TPS3125	SOT23_5	No	TI	TPS3125L30DBVR
83	1	U3	74LVC1G14	SOT23_5	No	TI	SN74LVC1G14DBVR
84	1	U4	LAN9252	IC_QFN64	No	Microchip	LAN9252
85	1	U5	24FC512	IC_DIP8_300	No	Microchip	24FC512-I/P
87	1	U7	PIC32MX775F256L	IC_TQFP100_12x12x1-0p4mm	No	Microchip	PIC32MX795F512L-80I/PT
88	1	U8	TRS3232_SO16	IC_SO16	No	TI	TRS3232IDR
89	1	U9	TC1047A	sot23-3	No	Microchip	TC1047AVNBTR
90	1	U10	MCP4726	SOT23_6	No	Microchip	MCP4726A0T-E/CH
91	1	Y1	25.000MHz	XTAL_HCM49	No	Cardinal Components Inc.	CSM1Z-A5B2C5-40-25.0D18-F
92	1	Y2	32Khz	th_xtal_ecs-31x-13-32khz	No	ECS INC	ECS-.320-12.5-13X
93	1	Y3	8 Mhz	th_hc49us_2p	No	Citizen Finetech	HC-49/U-S8000000ABJB
DNP Components							
1	1	C1	4.7uF	CAP0603	DNP		
4	4	C7,C9,C12,C23	1.0uF	CAP0603	DNP		
8	8	C28,C29,C30,C31,C33,C34,C35,C36	10pF	CAP0402	DNP		
10	19	C38,C39,C40,C41,C42,C43,C44,C45,C47,C49,C51, C53,C55,C57,C59,C60,C84,C85,C88	0.1uF	CAP0603	DNP		
11	7	C46,C48,C50,C52,C54,C56,C87	10uF	CAP_B_3528	DNP		
16	1	C86	10uF	CAP0603	DNP		
22	2	J2,J3	FTLF1217P2	CONN_FX_SFP_FTLF1217P2	DNP		
29	1	J15	HEADER 10x4	TH_CONN_4X10P	DNP		
33	1	J23	HEADER 14X2	TH_CONN_2x14P	DNP		
35	1	J26	CONN_2P	th_conn_1x2p	DNP		
36	4	L1,L2,L3,L4	1uH	L0805	DNP		
37	1	PIM1	PIM CONN	TH_CONN_PIM100	DNP		
39	2	P1,P2	HEADER 23x2	TH_CONN_2X23P	DNP		
52	8	R16,R18,R20,R22,R30,R32,R34,R36	0R	RES0402	DNP		
55	4	R39,R40,R43,R44	82R	RES0603	DNP		
56	4	R41,R42,R45,R46	49.9R	RES0603	DNP		
57	2	R47,R48	100E	RES0603	DNP		

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58	4	R49,R50,R51,R52	130R	RES0603	DNP
59	12	R53,R54,R55,R56,R57,R58,R59,R60,R81,R82,R84,R85	4.7K	RES0603	DNP
62	19	R75,R77,R78,R123,R124,R125,R126,R127,R128,R129,R130, R131,R132,R133,R134,R135,R136,R137,R138	10K	RES0603	DNP
64	2	R83,R86	2K	RES0603	DNP
65	4	R139,R143,R144,R152	0R	RES0603	DNP
67	1	R149	0R	RES0603-3	DNP
71	1	SW4	SW DIP-4/SM	TH_SW_DIP4	DNP
78	1	TP5	ORANGE	TH_TP_60D40	DNP
79	5	TP6,TP7,TP8,TP10,TP11	WHITE	TH_TP_60D40	DNP
86	1	U6	24FC512	IC_DIP8_300	DNP

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