TEXAS INSTRUMENTS

User's Guide
SBOU082A–December 2009–Revised February 2010

PGA870EVM

This user's guide describes the characteristics, operation, and use of the PGA870EVM, an evaluation fixture for the PGA870. The PGA870 is a wideband programmable gain amplifier (PGA) for high-speed signal chain and data acquisition systems. This evaluation module (EVM) allows evaluation of all aspects of the PGA870 device. Complete circuit descriptions, schematic diagrams, and bills of material are included in this document. For more information about the PGA870, see the product data sheet (available for download at www.ti.com).

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1 Introduction

The PGA870 is a wideband PGA (available in a QFN-28 package) that has been optimized to provide high bandwidth, low distortion, and low noise, making it ideally suited as a 14-bit analog-to-digital converter (ADC) driver for wireless base station signal chain applications. The wide gain range of –11.5 dB to +20 dB can be adjusted in 0.5-dB gain steps through a 6-bit control word applied to the parallel interface.

The PGA870 evaluation fixture supports the feature and performance evaluations of the PGA870. The evaluation fixture has onboard switches for device power-up and power-down, gain setting, and gain latch modes. The PGA870EVM has SMA connectors for input and output signals and a DB25 connector to allow gain control via an external control source. Also included in the evaluation kit is an additional interface board that allows the user to control the PGA870 gain from an external USB interface, as well as graphical user interface (GUI) software that allows the user to remotely set the device gain. The PGA870 evaluation fixture requires a +5-V power supply.

Throughout this document, the acronym *EVM* and the phrases *evaluation module* and *evaluation fixture* are synonymous with the PGA870EVM.

1.1 PGA870EVM Kit Contents

The PGA870EVM kit contains:

- PGA870EVM printed circuit board (PCB)
- PGA870 USB Interface board
- USB interface cable
- CD with this document, the GUI software installer, and USB drivers

2 EVM Overview

The PGA870 evaluation fixture contains onboard switches (S3 to S9) to support manual gain selection as well as device power-up and power-down (S2). The EVM also has connectors (J3 to J8). Onboard jumper blocks (JP1 to JP10) allow selection of either the onboard switches or the connectors for off-board control. Table 1 summarizes the switch numbers and corresponding device features. Note that switches S1 to S9 put the corresponding device pins into a *high* state when the switch actuator is positioned towards the center of the board.

Table 1. PGA870EVM Switch Number and Corresponding Device Feature/Function[(1)]

EVM Switch	Device Function	Description	Jumper	EVM Connector
S1	Latch Mode	Controls latched and unlatched acquisition of the gain-control word (B0 to B5). See the device data sheet for additional information.	JP9	J8, Pin 9
S2	$\overline{\text{PD}}$ (labeled *Disable* on EVM)	A low signal disables the device analog circuitry and shuts down the forward gain path. Gain control CMOS circuitry remains active when $\overline{\text{PD}}$ is low, so the gain can be set when the device is disabled.	JP10	J8, Pin 17
S3	Gain Strobe (labeled *Clock* on EVM)	Latches gain control data (B0 to B5) depending on the Latch Mode state. See the device data sheet for additional information.	JP1 JP8	J3 (SMA)
S4	B5	Gain control word MSB. A low/high signal will decrease/increase the gain by 16 dB	JP2	J8, Pin 7
S5	B4	Gain control word bit 4. A low/high signal will decrease/increase the gain by 8 dB	JP3	J8, Pin 6
S6	B3	Gain control word bit 3. A low/high signal will decrease/increase the gain by 4 dB	JP4	J8, Pin 5
S7	B2	Gain control word bit 2. A low/high signal will decrease/increase the gain by 2 dB	JP5	J8, Pin 4
S8	B1	Gain control word bit 1. A low/high signal will decrease/increase the gain by 1 dB	JP6	J8, Pin 3

(1) Switches S1 to S9 give a high state to the corresponding device pins when the switch actuator is positioned towards the center of the board.

Table 1. PGA870EVM Switch Number and Corresponding Device Feature/Function[(1)] (continued)

EVM Switch	Device Function	Description	Jumper	EVM Connector
S9	B0	Gain control word LSB. A low/high signal will decrease/increase the gain by 0.5 dB	JP7	J8, Pin 2

Examples of various EVM jumper and switch settings are shown in Figure 1 through Figure 3.

- Figure 1 illustrates the jumper (JP1–JP10) and switch settings for an *enabled* device, with gain = 20 dB set by the EVM switches (in *unlatched* gain mode). The jumper block positions (JP1–JP10) on the back side of the DB25 connector make all of the onboard switches active (S1–S9).
- Figure 2 shows an example of the required jumper settings to allow all device functions to be controlled via the DB25 connector. The jumper block positions (JP1–JP10) on the back side of the DB25 connector make all of the onboard switches inactive (S1–S9).
- Figure 3 shows the jumper and switch settings required for the device gain to be set from a USB port via the GUI software. The Latch Mode, $\overline{PD}$, and Gain Strobe functions are controlled by onboard switches S1, S2, and S3, respectively. The jumper block positions (JP1–JP10) on the back side of the DB25 connector make the gain-setting switches inactive (S4–S9), and the Latch Mode, $\overline{PD}$, and Gain Strobe switches active (S1, S2, and S3, respectively).

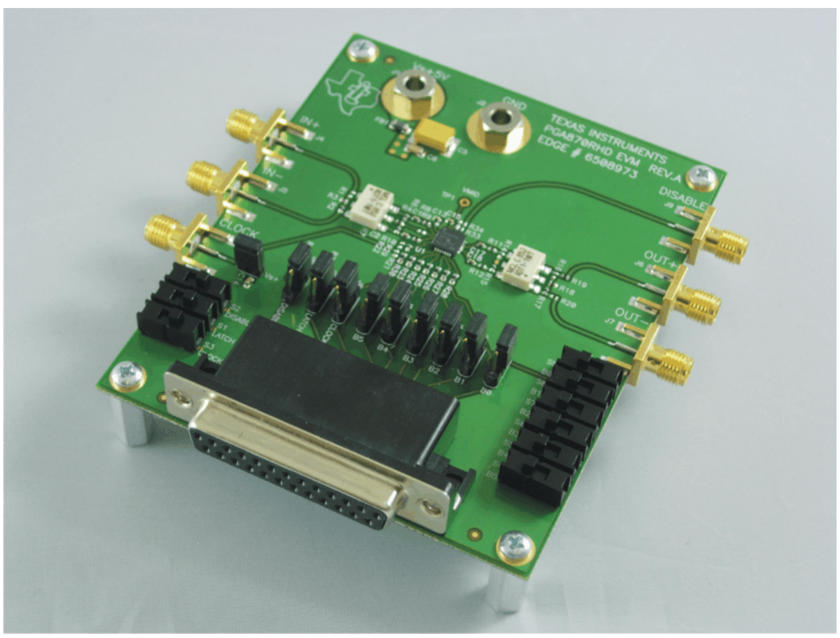


Figure 1. Switch and Jumper Block Positions for Enabled Device, Gain = 20 dB, Unlatched Gain Mode

Figure 2. Jumper Block Positions for Device Gain, Latching, and Disable to be Controlled through DB25 Connector (J8)

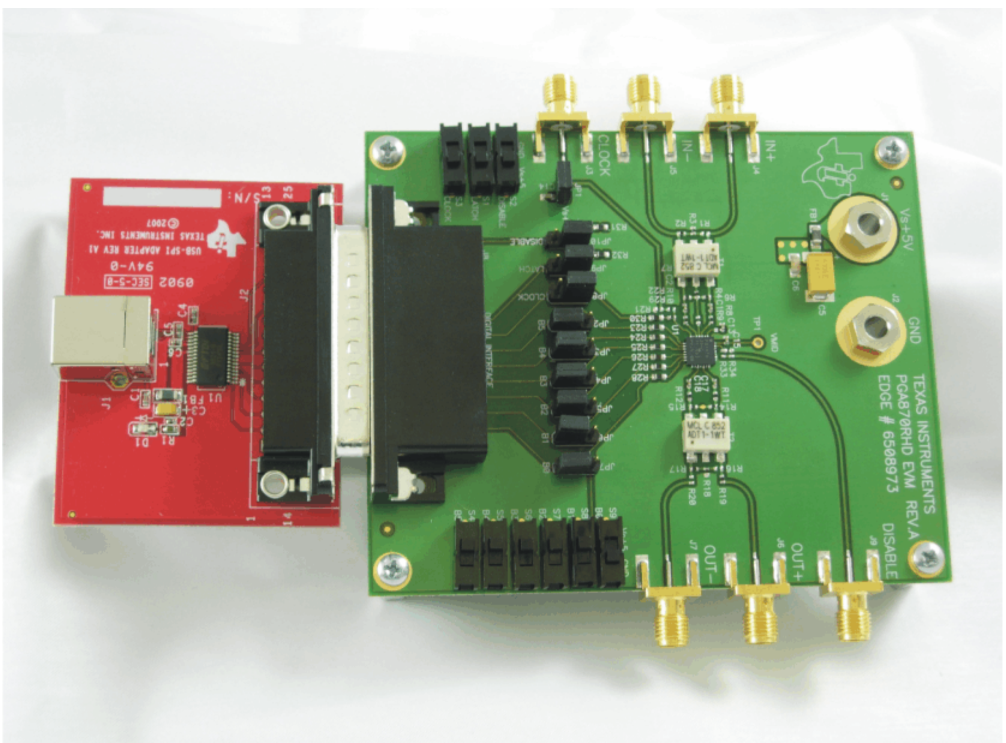


Figure 3. Switch and Jumper Block Positions for Device Gain (Unlatched Mode) Controlled through DB25 Connector and USB Interface Board

3 PGA870EVM Control Panel Graphical User Interface (GUI)

The gain of the device on the EVM may be controlled from a computer by using the PGA870 control panel GUI, the USB interface board in the EVM kit, and a USB cable. The GUI software installer (discussed in Section 4) is on the CD shipped with the EVM kit, and is also available for download through the PGA870 product folder on the TI web site. The GUI controls only the bits B0 to B5 of the gain control word. The control panel GUI does not control the Gain Strobe or Latch Mode control lines of the PGA870 itself. When using the GUI software, the Gain Strobe and Latch Mode lines must be controlled with the EVM onboard switches (S1 and S3) or with external connections.

4 GUI Software Installation and Use

To install the PGA870EVM GUI software, copy the software installer and the folder *USB_drivers* from the enclosed CD onto the Microsoft® Windows® desktop of the target computer. Double-click on the installer icon and follow the instructions to begin the installation; accept the terms of use and licensing agreements when that prompt appears. When the installation is complete, start the control panel GUI from the Windows *Start* menu by selecting **PGA870_Control_Panel.exe**. The GUI should appear, as shown in Figure 4.

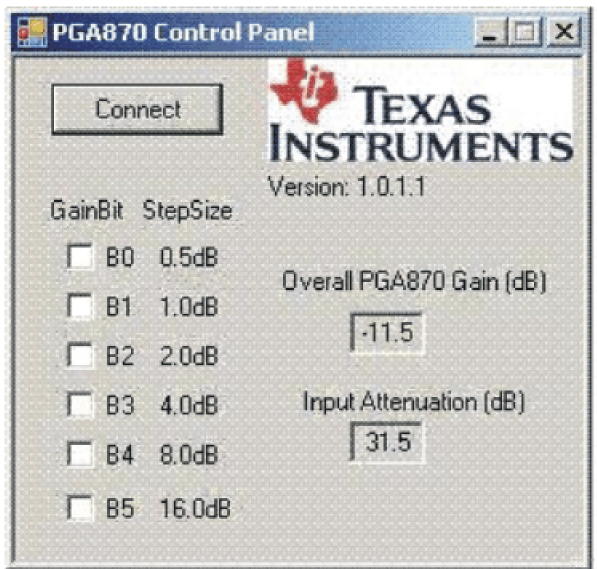


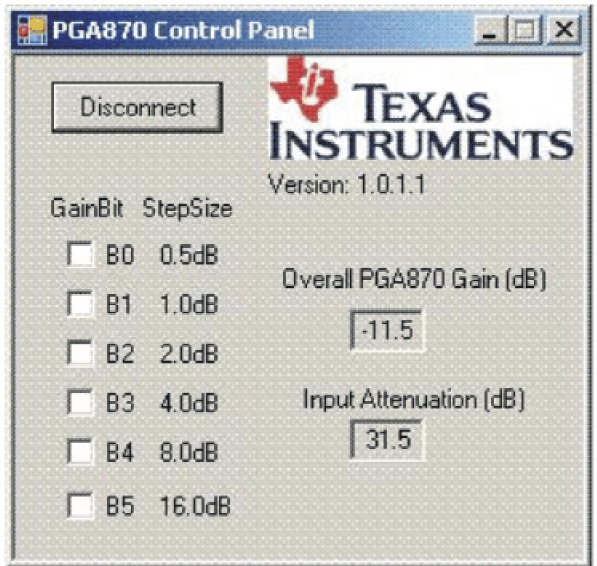
Figure 4. PGA870EVM Control Panel GUI After Installation, Before Successful Connection to PGA870EVM

Once the control panel GUI has been successfully installed, connect the USB interface board to the PGA870EVM J8 connector (DB25), and then connect the USB port to the host computer with a USB cable (provided). After connecting the USB cable, you may see a Microsoft Windows notification that *New hardware has been found*, and that new drivers are required. If you receive this notification, use the *Browse* option to direct the hardware installer to find the *USB_Drivers* folder. The driver installer may require several iterations in order to successfully complete the update process. The number of new drivers that are required depends on the host computer configuration and its unique update history.

After the GUI software installation and USB driver updates are completed, power up the PGA870EVM; make sure that the PGA870 device is in the Enabled state with switch S2, and the gain latch mode is set to *Unlatched* with switches S1 and S3.

NOTE: The EVM connection and switch (S3) labeled CLOCK provides the Gain Strobe function discussed in the product data sheet.

Once the connections are configured, click on the *Connect* button on the upper left corner of the control panel GUI. If the control panel successfully connects to the PGA870EVM, then the button label changes from **Connect** to **Disconnect** as Figure 5 shows. If the control panel software cannot connect to the PGA870EVM, the **Connect** button does not change to **Disconnect.** No other error message is generated.



Note: The button has changed from *Connect* to *Disconnect*.

Figure 5. PGA870EVM Control Panel GUI After Successful Connection to PGA870EVM

The boxes on the left side of the control panel GUI (see Figure 4) under the **GainBit** heading indicate the corresponding gain control bits as described in the PGA870 product data sheet. Bit B0 is the least significant bit (LSB) of the gain control word; it represents the smallest gain step of 0.5 dB. Bit B5 is the largest gain step (16 dB), and corresponds to the most significant gain control bit (MSB). Checking a box causes the GUI software to send a *high* signal to the corresponding gain control bit. Figure 5 corresponds to a minimum PGA870 gain of –11.5 dB.

The PGA870 gain corresponding to the gain setting (that is, the GainBit checked boxes) appears in the number field entitled, Overall PGA870 Gain (dB). The actual measured gain of the EVM may be less than the selected PGA870 gain because of losses in the resistive load and the EVM transformers.

The number field labeled **Input Attenuation (dB)** shows the equivalent loss of the PGA870 input attenuator. Consult the device data sheet for additional information.

Figure 6 shows examples of the GUI when it is connected to the PGA870EVM and used to select 20 dB of gain and 10 dB of gain, respectively.

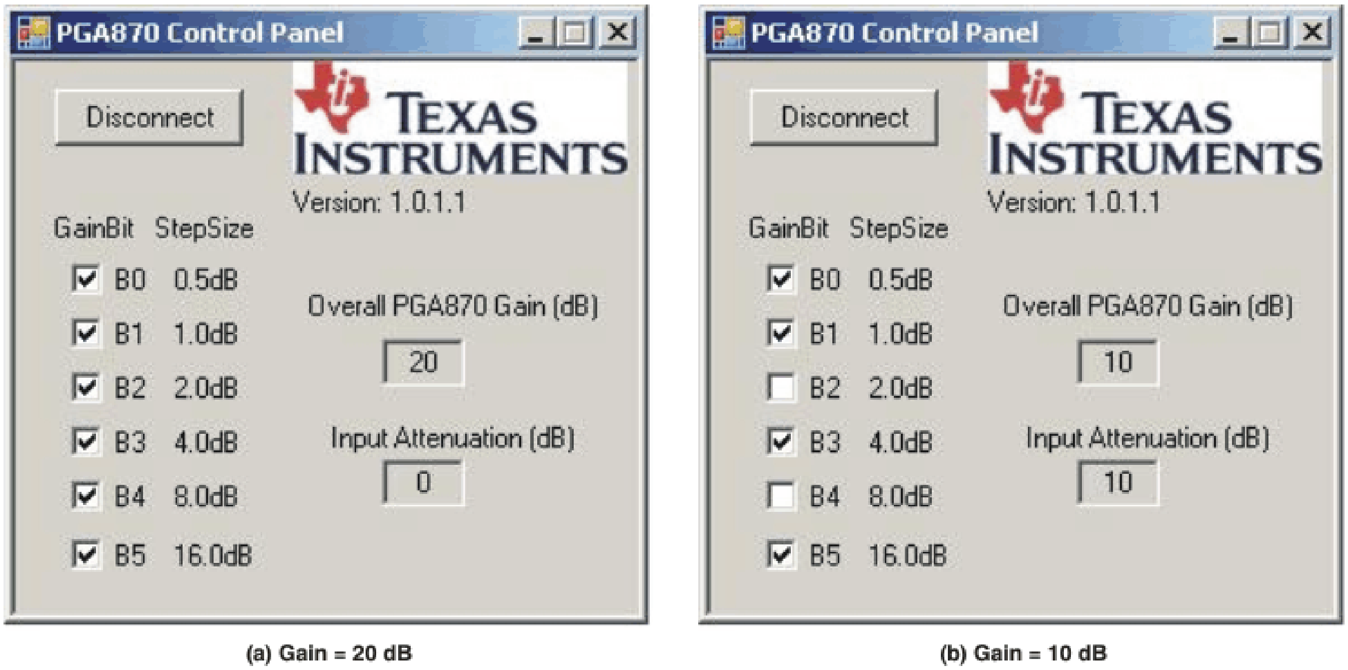


Figure 6. Examples of Control Panel GUI Connected to the PGA870EVM

5 Schematic and Parts List

The EVM schematic is shown in Figure 7.

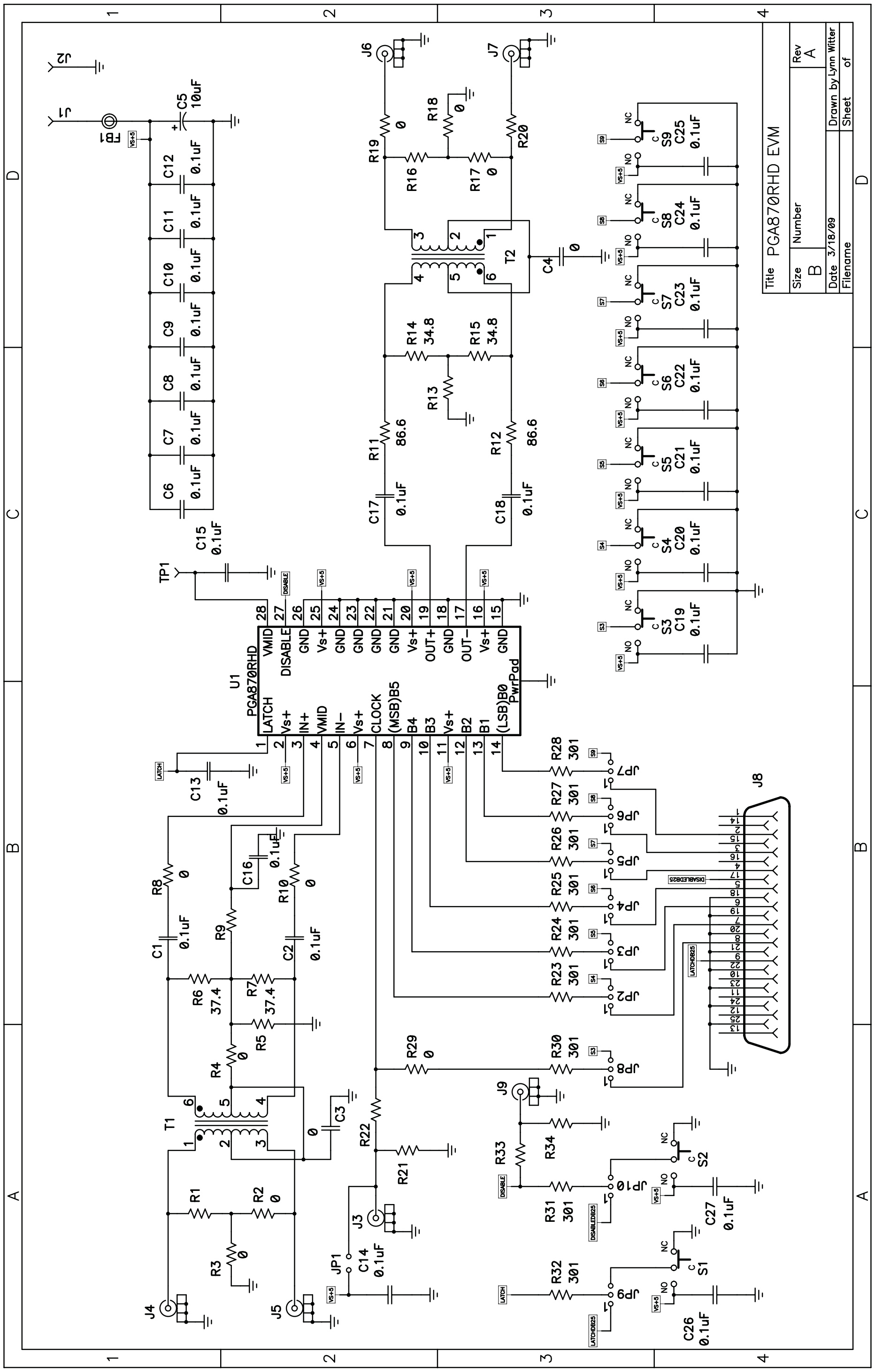


Figure 7. PGA870EVM Schematic

5.1 PCB Layout

The PGA870EVM PCB layers are shown in Figure 8 through Figure 11.

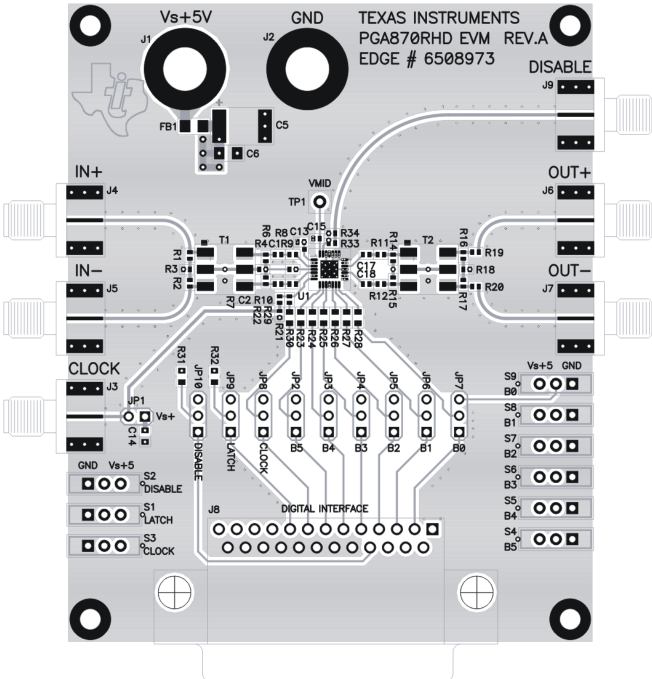


Figure 8. Top Layer (Layer 1)

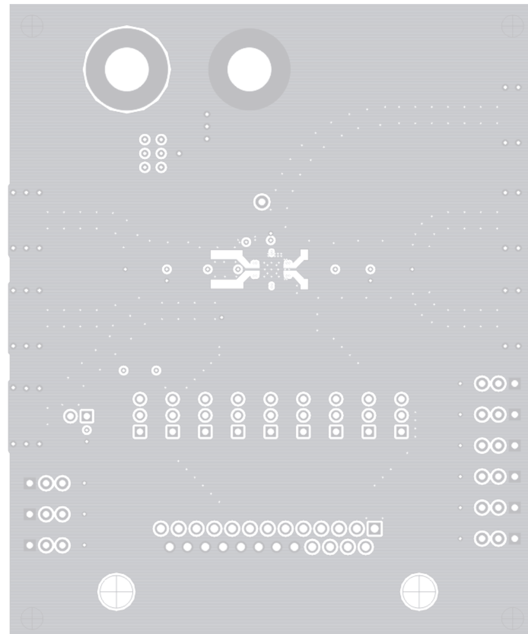


Figure 9. Ground Layer (Layer 2)

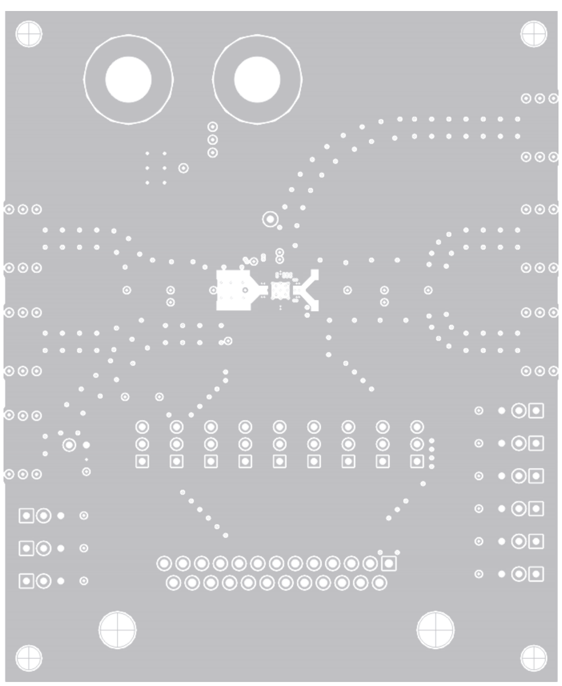


Figure 10. Power Layer (Layer 3)

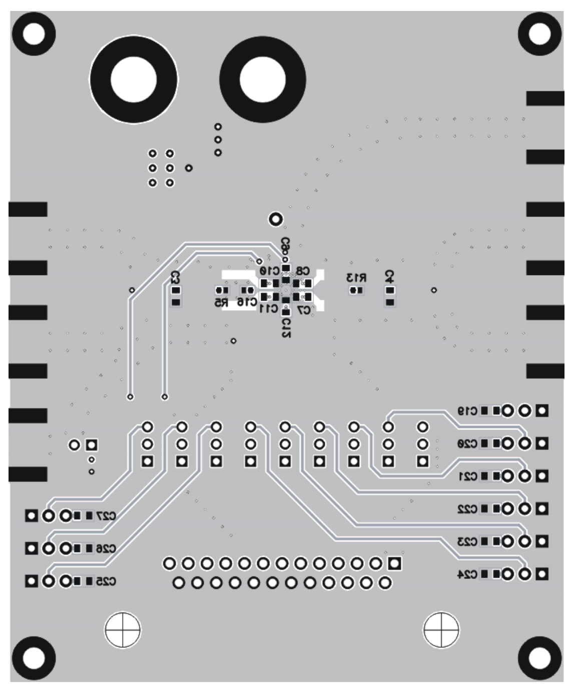


Figure 11. Bottom Layer (Layer 4)

5.2 Bill of Materials

Table 2 lists the bill of materials (BOM) for the PGA870EVM.

Table 2. PGA870EVM Bill of Materials

Item	RefDes	Qty	Description	SMD Size	Manufacturer	Part Number
1	FB1	1	Bead, ferrite, 3 A, 80 Ω	1206	Steward	HI1206N800R-10
2	C5	1	Capacitor, 10 µF, tanatalum, 35 V, 10%	D	AVX	TAJD106K035RNJ
3	C1, C2, C13, C15, C16, C17, C18	7	Capacitor, 0.1 µF, ceramic, X5R, 16 V	0402	AVX	0402YD104KAT2A
4	C7, C8, C9, C10, C11, C12, C14, C19, C20, C21, C22, C23, C24, C25, C26, C27	16	Capacitor, 0.1 µF, ceramic, X7R, 16 V	0603	AVX	06033C104KAT2A
5	C6	1	Capacitor, 0.1 µF, ceramic, X7R, 50 V	1206	AVX	12065C104KAT2A
6	R1, R5, R9, R13, R16, R20, R21, R22, R33, R34	10	Open	0402	—	—
7	R2, R3, R4, R8, R10, R17, R18, R19, R29	9	Resistor, 0 Ω, 1/16W	0402	ROHM	MCR01MZPJ000
8	R14, R15	2	Resistor, 34.8 Ω, 1/16W, 1%	0402	Panasonic	ERJ-2RKF34R8X
9	R6, R7	2	Resistor, 37.4 Ω, 1/16W, 1%	0402	Panasonic	ERJ-2RKF37R4X
10	R11, R12	2	Resistor, 86.6 Ω, 1/16W, 1%	0402	Panasonic	ERJ-2RKF86R6X
11	C3, C4	2	Resistor, 0 Ω, 1/10W	0603	ROHM	MCR03EZPJ000
12	R23, R24, R25, R26, R27, R28, R30, R31, R32	9	Resistor, 301 Ω, 1/10W, 1%	0603	ROHM	MCR03EZPFX3010
13	T1, T2	2	Transformer, RF(1)		Mini-circuits	ADT1-1WT+
14	J1, J2	2	Jack, banana receptance, 0.025-in. dia. hole		SPC	813
15	J3, J4, J5, J6, J7, J9	6	Connector, edge, SMA PCB jack		Johnson	142-0701-801
16	J8	1	Connector, DB25, female		Norcomp	183-025-213R531
17	S1, S2, S3, S4, S5, S6, S7, S8, S9	9	Switch, slide SPDT		E-Switch	EG1218
18	JP1	1	Header, 0.1" CTRS, 0.025-in^2 pins	2 POS.	Sullins	PBC36SAAN
19	JP2, JP3, JP4, JP5, JP6, JP7, JP8, JP9, JP10	9	Header, 0.1" CTRS, 0.025-in^2 pins	3 POS.	Sullins	PBC36SAAN
20	JP1, JP2, JP3, JP4, JP5, JP6, JP7, JP8, JP9, JP10	10	Shunts		Sullins	SSC02SYAN
21	U1	1	IC, PGA870	RHD	TI	PGA870RHD
22		4	Standoff, 4-40 hex, 0.625-in. length		Keystone	1808
23		4	Screw, Phillips, 4-40, .250 in		BF	PMS 440 0031 PH
24			Board, printed circuit		TI	(TI) EDGE# 6508973
25		1	Board, PGA870 USB interface		TI	(TI) EDGE# 6514738

(1) Mount T2 180° from the Pin 1 marking on the board.

Revision History

Changes from Original (December, 2009) to A Revision	Page
• Updated PGA870EVM kit contents list	2
• Revised paragraphs that describe the process of connecting the PGA870EVM to the host computer	5
• Corrected figure captions for Figure 8 through Figure 11	9

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 0 V to +5 V and the output voltage range of 0 V to +5 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than +85° C. The EVM is designed to operate properly with certain components above +85° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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