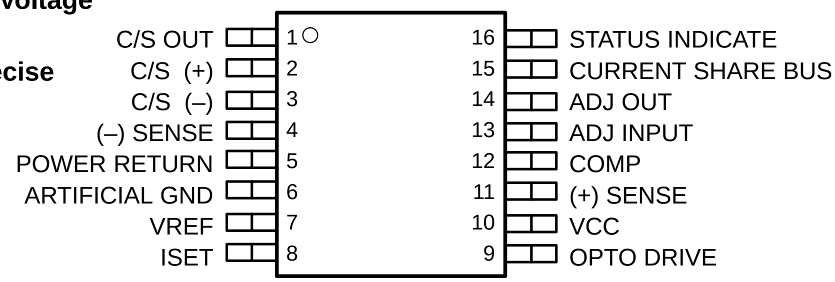
UC1907, UC2907, UC3907 LOAD SHARE CONTROLLER

SLUS165C – MARCH 1999 - REVISED JANUARY 2002

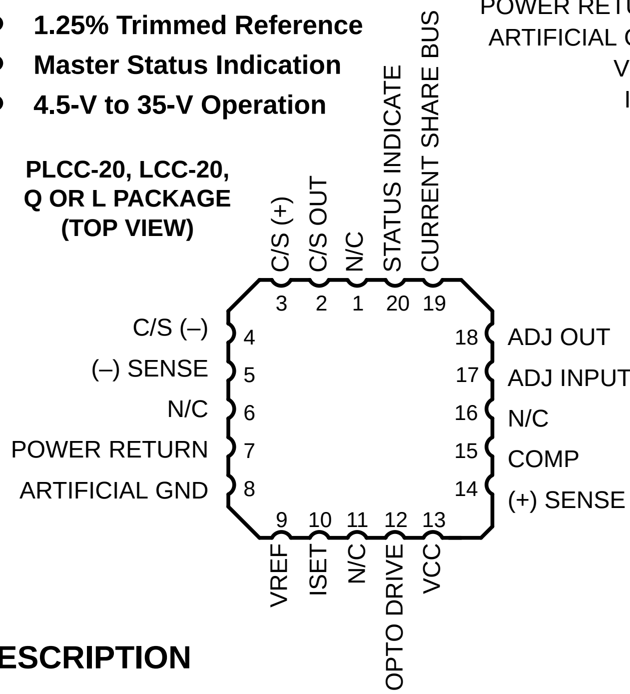
FEATURES

- **Fully Differential High Impedance Voltage Sensing**
- **Accurate Current Amplifier for Precise Current Sharing**
- **Opto Coupler Driving Capability**
- **1.25% Trimmed Reference**
- **Master Status Indication**
- **4.5-V to 35-V Operation**

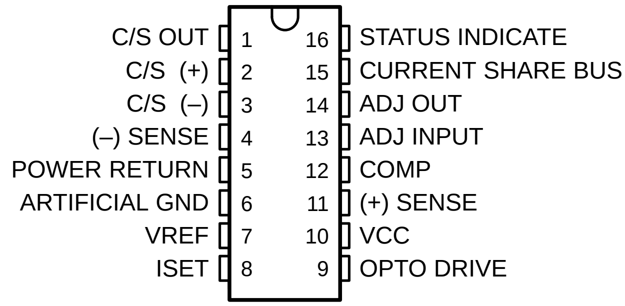
SOIC-16 DW PACKAGE (TOP VIEW)



PLCC-20, LCC-20, Q OR L PACKAGE (TOP VIEW)



DIL-16 J or N PACKAGE (TOP VIEW)



DESCRIPTION

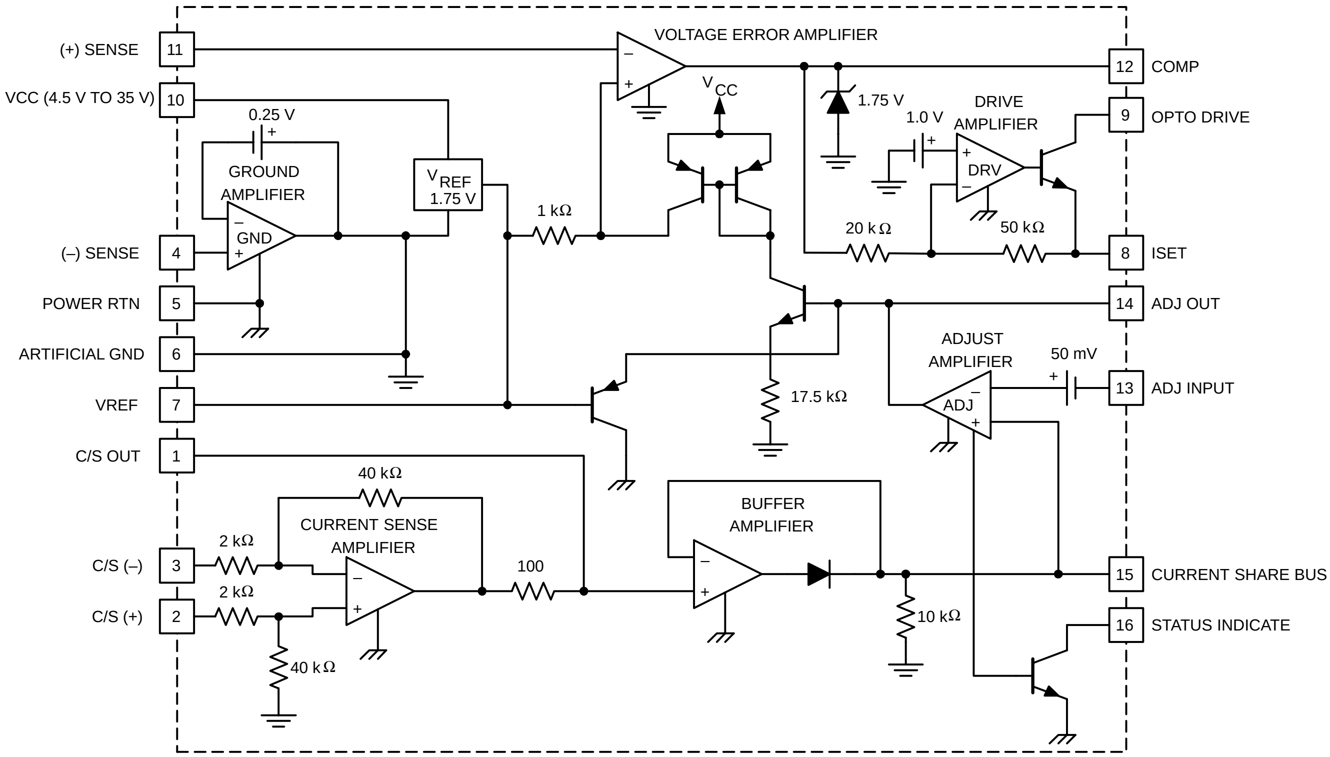
The UCx907 family of load share controller ICs provides all the necessary features to allow multiple-independent-power modules to be paralleled such that each module supplies only its proportionate share to total-load current.

This sharing is accomplished by controlling each module's power stage with a command generated from a voltage-feedback amplifier whose reference can be independently adjusted in response to a common-share-bus voltage. By monitoring the current from each module, the current share bus circuitry determines which paralleled module would normally have the highest output current and, with the designation of this unit as the master, adjusts all the other modules to increase their output current to within 2.5% of that of the master.

The current share bus signal interconnecting all the paralleled modules is a low-impedance, noise-insensitive line which will not interfere with allowing each module to act independently should the bus become open or shorted to ground. The UC3907 controller will reside on the output side of each power module and its overall function is to supply a voltage feedback loop. The specific architecture of the power stage is unimportant. Either switching or linear designs may be utilized and the control signal may be either directly coupled or isolated though the use of an optocoupler or other isolated medium.

Other features of the UC3907 include 1.25% accurate reference: a low-loss, fixed-gain current-sense amplifier, a fully differential, high-impedance voltage sensing capability, and a status indicator to designate which module is performing as master.

block diagram



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage	35 V
Opto out voltage	35 V
Opto out current	20 mA
Status indicate sink current	20 mA
C/S input voltage	35 V
Share bus voltage	–0.3 V to 35 V
Other analog inputs and outputs (zener clamped) maximum forced voltage	–0.3 V to10 V
Other analog inputs and outputs (zener clamped) maximum forced current	±10 mA
Ground amp sink current	50 mA
Pins 1, 9, 12, 15 sink current	20 mA
Storage temperature range, T_{stg}	–65°C to 150°C
Junction temperature, T_J	–55°C to 150°C
Lead temperature (solder 10 seconds)	300°C

† Pin Nos. refer to 16 Pin DIL Package.
‡ Currents are positive into, negative out of the specified terminal. Consult packaging section of databook for thermal limitations and considerations of package.

electrical characteristics, these specifications apply for T_A = –55°C to 125°C for UC1907, –40°C to 85°C for UC2907, and 0°C to 70°C for UC3907, V_{IN} = 15 V, T_A = T_J (unless otherwise stated)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNITS
Voltage Amp Section							
Input voltage	COMP = 1 V,		T_A = 25°C	1.975	2.000	2.025	V
	COMP = 1 V,		over temp	1.960	2.000	2.040	V
Line regulation	V_{IN} = 4.5 V to 35 V					15	mV
Load regulation	I_L reference = 0.0 mA to –10 mA					10	mV
Long term stability	T_A = 125°C,	1000hrs	See Note 2		5	25	mV
Total output variation	Line, load, temp			1.960		2.040	
Input adjust range	ADJ OUT from max high to max low			85	100	115	mV
Input bias current				–1			µA
Open loop gain	COMP = 0.75 V to 1.5 V			65			dB
Unity gain bandwidth	T_A = 25°C		See Note 2	700			kHz
Output sink current	(+) SENSE = 2.2 V,		COMP = 1 V	6	15		mA
Output source current	(+) SENSE = 1.8 V,		COMP = 1 V	400	600		µA
V_{OUT} high	(+) SENSE = 1.8 V,		I_L = –400 µA	1.85	2		V
V_{OUT} low	(+) SENSE = 2.2 V,		I_L = 1 mA		0.15	0.40	V
Reference Section							
Output voltage	T_A = 25°C			1.970	2.000	2.030	V
	Over operating temp			1.955	2.000	2.045	V
Short circuit current	VREF = 0.0 V			–15	–30	–60	mA
Ground Amp Section							
Output voltage				200	250	300	mV
Common mode variation	(–) SENSE from 0.0 V to 2 V					5	mV
Load regulation	I_L = 0.0 mA to 20 mA,		T_A = 25°C			10	mV
	I_L = 0.0 mA to 20 mA,		over temp			15	mV
Adjust Amp Section							
Input offset voltage	ADJ OUT = 1.5 V, V_{CM} = 0.0 V			40	50	60	mV
Input bias current				–2			µA
Open loop gain	1.5 V ≤ ADJ OUT ≤ 2.25 V			65			dB
Unity gain bandwidth	T_A = 25°C,	C_{OUT} =1 µF	See Note 2		500		Hz
Transconductance	I_{OUT} = –10 µA to 10 µA,		V_{OUT} = 1.5 V	1.7	3	4.5	ms
Output sink current	V_{ID} = 0.0 V,		ADJ OUT = 1.5 V	55	135	225	µA
Output source current	V_{ID} = 250 mV,		ADJ OUT = 1.5 V	110	200	350	µA
V_{OUT} high	V_{ID} = 250 mV,		I_{OUT} = – 50 mA	2.20	2.70	2.90	V
V_{OUT} low	V_{ID} = 0.0 V,		I_{OUT} = 50 mA		0.75	1.15	V
Common mode rejection ratio	V_{CM} = 0.0 to 10 V			70			dB
Output gain to V/A	V_{OUT} ADJ OUT = 1.5 V to 2 V, Δ(+) SENSE/ ΔADJ OUT			50	57	64	mV/V

NOTE 1: Unless otherwise specified all voltages are with respect to (–) SENSE. Currents are positive into, negative out of the specified terminal.
NOTE 2: Ensured by design. Not production tested.

electrical characteristics, these specifications apply for T_A = –55°C to 125°C for UC1907, –40°C to 85°C for UC2907, and 0°C to 70°C for UC3907, V_{IN} = 15 V, T_A = T_J (unless otherwise stated)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Current Amp Section						
Gain	V_{CM} = 0.0 V,	V_{ID} = 50 mV to 100 mV	19.2	19.6	20.1	V/V
Output voltage	$V_{C/S}$ (+) = $V_{C/S}$ (–) = 0.0 V,	T_A = 25°C	210	250	290	mV
	$V_{C/S}$ (+) = $V_{C/S}$ (–) = 0.0 V,	over temp	180	250	330	mV
Input offset change with common mode input	V_{CM} = 0 V to 13 V				600	µV/V
V_{OUT} high	V_{ID} = 1 V		10	14.5		V
V_{OUT} low	V_{ID} = – 1 V,	I_L = 1 mA		350	450	mV
Power supply rejection ratio	V_{IN} = 4.5 V to 35 V,	V_{CM} = 0.0 V	60			dB
Slew rate				0.4		V/µs
Drive Amp Section R_{SET} = 500 Ω to Artificial GND, Opto Drive = 15 V						
Voltage gain	COMP = 0.5 V to 1 V		2.3	2.5	2.6	V/V
I_{SET} V_{OUT} high	(+) SENSE = 2.2 V		3.8	4.1	4.4	V
I_{SET} V_{OUT} low	(+) SENSE = 1.8 V			270	300	mV
Opto out voltage range			4		35	V
Zero current input threshold			1.55	1.65	1.75	V
Buffer Amp Section						
Input offset voltage	Input = 1 V				5	mV
Output off impedance	Input = 1 V,	output = 1.5 V to 2 V	5	10	20	kΩ
Output source current	Input = 1 V,	output = 0.5 V	6	15		mA
Common mode rejection ratio	V_{CM} = 0.3 V to 10 V		70			dB
Power supply rejection ratio	V_{IN} = 4.5 V to 35 V		70			dB
Under Voltage Lockout Section						
Startup threshold				3.7	4.4	V
Threshold hysteresis				200		mV
Status Indicate Section						
V_{OUT} low	ADJ OUT = current share bus			0.2	0.5	V
Output leakage	ADJ OUT = 1 V,	V_{OUT} = 35 V		0.1	5	µA
Total Stand by Current Section						
Startup current	V_{IN} = UVLO – 0.2 V			3	5	mA
Operating current	V_{IN} = 35 V			6	10	mA

NOTE 1: Unless otherwise specified all voltages are with respect to (–) SENSE. Currents are positive into, negative out of the specified terminal.
NOTE 2: Ensured by design. Not production tested.

pin assignments

(–) SENSE: (Pin 4) This is a high-impedance pin allowing remote sensing of the system ground, bypassing any voltage drops which might appear in the power return line. This point should be considered as the true ground. Unless otherwise stated, all voltages are with respect to this point.

Artificial Ground: (Pin 6) This is a low-impedance-circuit ground which is exactly 250 mV above the (–) SENSE terminal. This offset allows the ground buffer amplifier negative headroom to return all the control bias and operating currents while maintaining a high impedance at the (–) SENSE input.

Power RTN: (Pin 5) This should be the most negative voltage available and can range from zero to 5 V below the (–) SENSE terminal. It should be connected as close to the power source as possible so that voltage drops across the return line and current-sensing impedances lie between this terminal and the (–) SENSE point.

VREF: (Pin 7) The internal voltage reference is a band-gap circuit set at 2.0 V with respect to the (–) SENSE input (1.75 V above the artificial ground), and an accuracy of ±1.5%. This circuit, as well as all the other chip functions, will work over a supply voltage range of 4.5 V to 35 V allowing operation from unregulated dc, an auxiliary voltage, or the same output voltage that it is controlling. Under-voltage lockout has been included to insure proper startup by disabling internal bias currents until the reference rises into regulation.

Voltage Amplifier: (Pins 11, 12) This circuit is the feedback-control-gain stage for the power module's output-voltage regulation, and overall-loop compensation will normally be applied around this amplifier. Its output will swing from slightly above the ground return to an internal clamp of 2.0 V. The reference trimming is performed closed loop, and measured at pin 11, (+) SENSE. The value is trimmed to 2 V ±1.25%.

Drive Amplifier: (Pins 8, 9, 12) This amplifier is used as an inverting buffer between the voltage amplifier's output and the medium used to couple the feedback signal to the power controller. It has a fixed-voltage gain of 2.5 and is usually configured with a current-setting resistor to ground. This establishes a current-sinking output optimized to drive optical couplers biased at any voltage from 4.5 V to 35 V, with current levels up to 20 mA. The polarity of this stage is such that an increasing voltage at the voltage amplifier's sense input (as, for example, at turnon) will increase the opto's current. In a nonisolated application, a voltage signal ranging from 0.25 V to 4.1 V may be taken from the current-setting output but it should be noted that this voltage will also increase with increasing sense voltage and an external inverter may be required to obtain the correct feedback polarity.

Current Amplifier: (Pins 1, 2, 3) This amplifier has differential-sensing capability for use with an external shunt in the power-return line. The common mode range of its input will accommodate the full range between the power return point and VCC-2 V which will allow undefined-line impedances on either side of the current shunt. The gain is internally set at 20, giving the user the ability to establish the maximum-voltage drop across the current-sense resistor at any value between 50 mV and 500 mV. While the bandwidth of this amplifier may be reduced with the addition of an external-output capacitor to ground, in most cases this is not required as the compensation of the adjust amplifier will typically form the dominant pole in the adjust loop.

Buffer Amplifier: (Pins 1, 15) This amplifier is a unidirectional buffer which drives the current-share bus. The line which will interconnect all power modules paralleled for current sharing. Since the buffer amplifier will only source current, it insures that the module with the highest-output current will be the master and drive the bus with a low-impedance drive capability. All other buffer amplifiers will be inactive with each exhibiting a 10-kΩ load impedance to ground. The share bus terminal is protected against both shorts to ground and accidental voltages in excess of 50 V.

pin assignments

Adjust Amplifier: (Pins 13, 14, 15) This amplifier adjusts the individual module’s reference voltage to maintain equal-current sharing. It is a transconductance type in order that its bandwidth may be limited and noise kept out of the reference-adjust circuitry, with a simple capacitor to ground. The function of this amplifier is to compare its own module-output current to the share-bus signal, which represents the highest output current. This will force an adjust command which is capable of increasing the reference voltage as seen by the voltage amplifier by as much as 100 mV. This number stems from the 17.5:1 internal resistor ratio between the adjust amplifier’s clamped output and the reference, and represents a 5% total range of adjustment. This value should be adequate to compensate for unit-to-unit reference and external-resistor tolerances. The adjust amplifier has a built-in 50-mV offset on its inverting input which will force the unit acting as the master to have a low output, resulting in no change to the reference. While this 50-mV offset represents an error in current sharing, the gain of the current amplifier reduces it to only 2.5 mV across the current-sense resistor. It should also be noted that when the module is acting independently with no connection to the share bus node, or when the share bus node is shorted to ground, its reference voltage will be unchanged. Since only the circuit acting as a master will have a low output from the adjust amplifier, this signal is used to activate a flag output to identify the master, should some corrective action be needed.

Status Indicate: (Pin 16) This pin is an open-collector output intended to indicate the unit which is acting as the master. It achieves this by sensing when the adjust amp is in its low state and pulling the status-indicate pin low.

additional information

Please refer to additional application information.

1. By Mark Jordan, *UC3907 Load Share IC Simplifies Parallel Power Supply Design,* TI Literature Number SLUA147.
2. By Laszlo Balogh, *UC3902 Load Share Controller and its Performance in Distributed Power Systems,* TI Literature Number SLUA128.

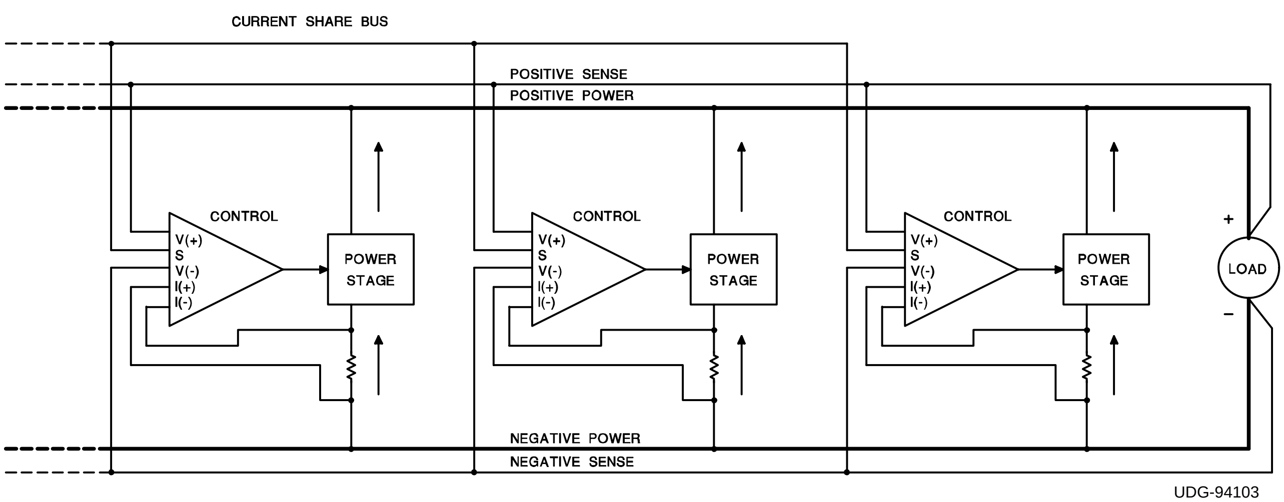


Figure 1. Load System Diagram

additional information (continued)

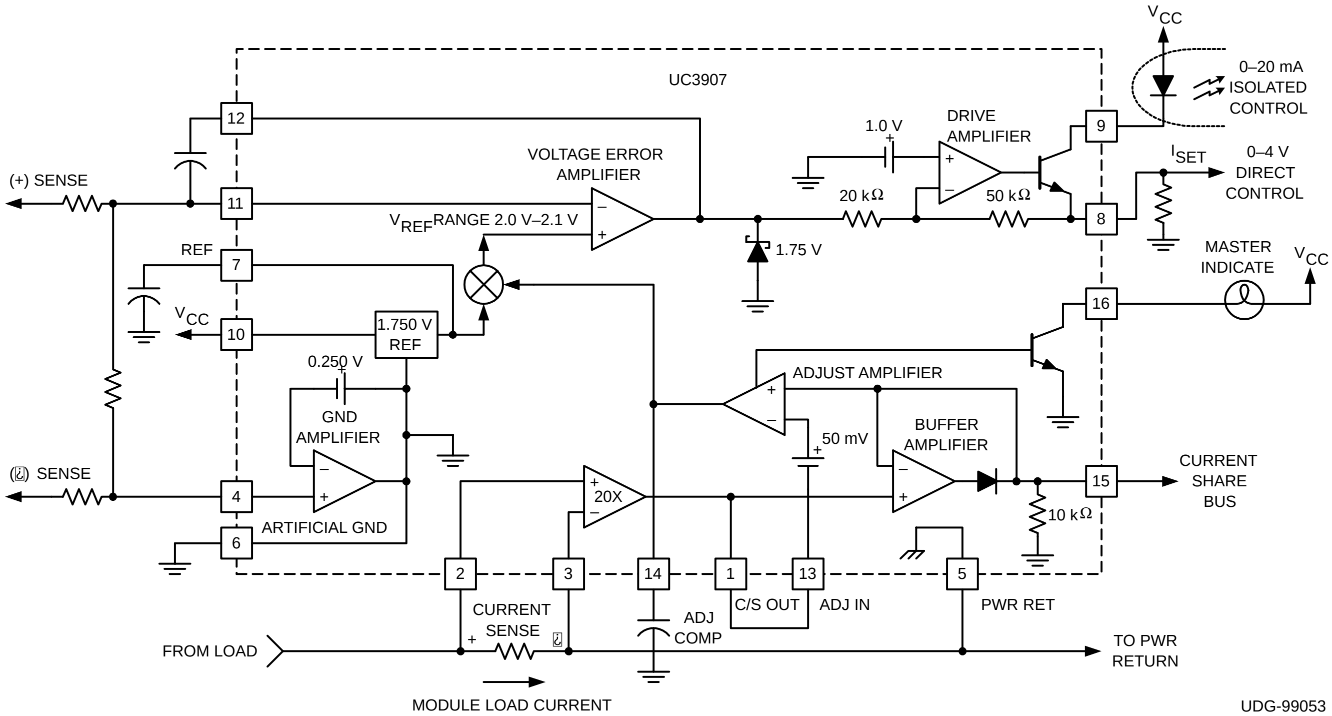


Figure 2. Load System Connection Diagram

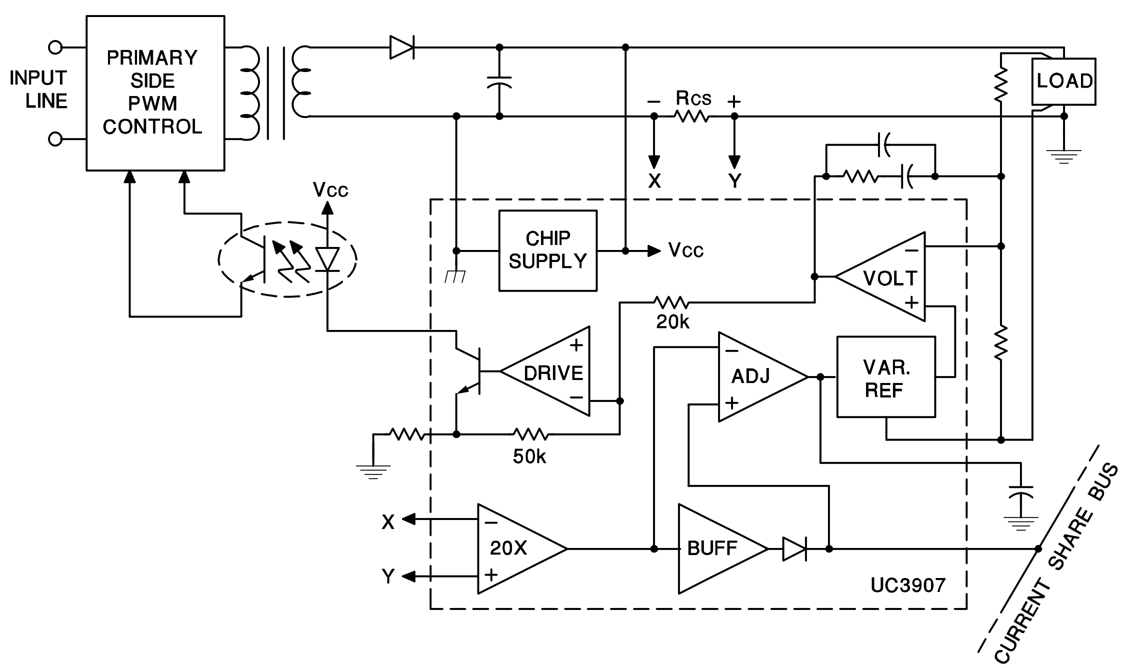


Figure 3. UC3907 In a Load-Sharing Feedback Loop for an Off-Line Isolated Supply

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
UC1907J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
UC1907J883B	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
UC1907L	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI
UC1907L883B	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI
UC2907DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2907DWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2907DWTR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2907DWTRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2907J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
UC2907N	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC2907NG4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC3907DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3907DWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3907DWTR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3907DWTRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3907J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
UC3907N	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC3907NG4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder

temperature.

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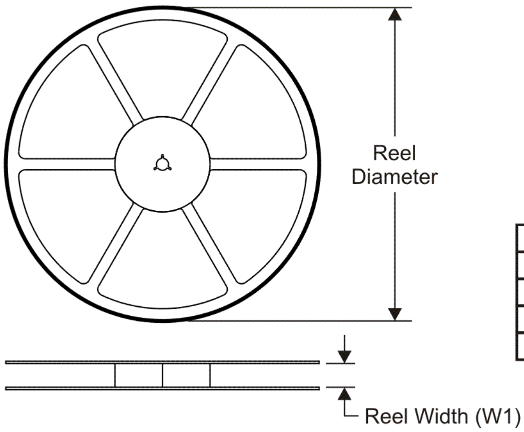
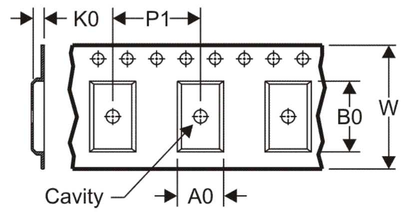
TAPE AND REEL INFORMATION

REEL DIMENSIONS

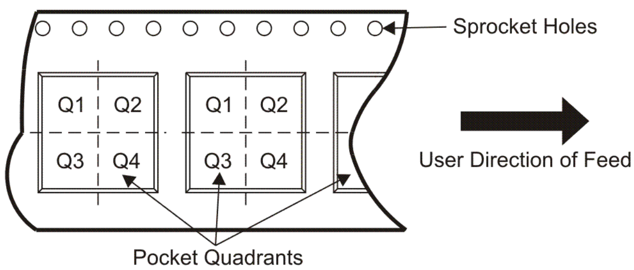


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

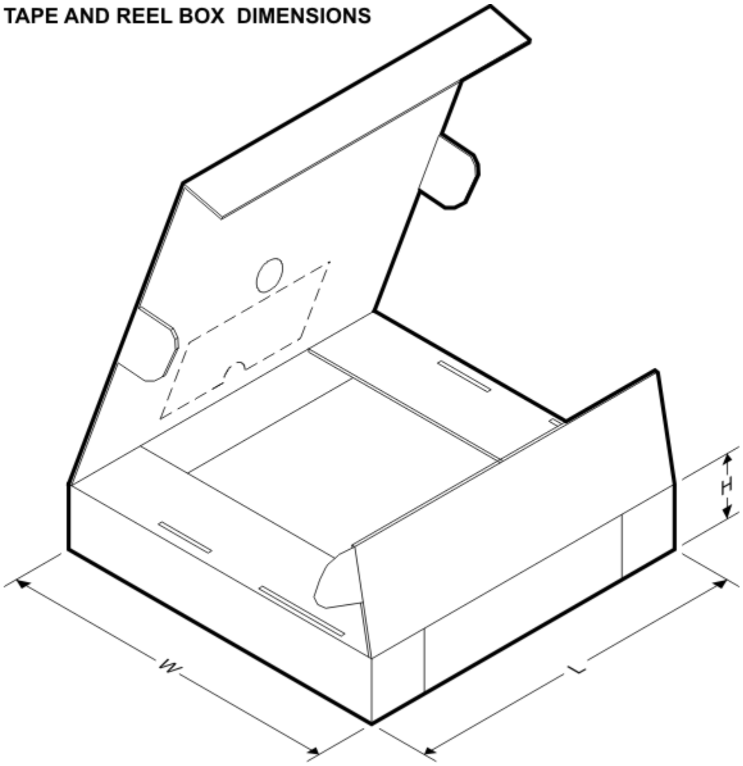
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC2907DWTR	SOIC	DW	16	2000	330.0	16.4	10.85	10.8	2.7	12.0	16.0	Q1
UC3907DWTR	SOIC	DW	16	2000	330.0	16.4	10.85	10.8	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC2907DWTR	SOIC	DW	16	2000	346.0	346.0	33.0
UC3907DWTR	SOIC	DW	16	2000	346.0	346.0	33.0

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

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DSP	dsp.ti.com	Broadband	www.ti.com/broadband
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