TW5864B1

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5D1 H264 Encoder with 4-Channel A/V Decoder and 12 Channel External VD Inputs for Security Applications

The TW5864 is a H.264 encoder solution with integrated 4-channel analog A/V decoders. TW5864 can be used as a low cost single chip solution for 4-channel H.264 hardware compression PC cards, or 16-channel cards by using additional external TW2866 chips. There are 3 versions of TW5864 that can support no external video decoder (TW5864A), 4 channel external video decoders (TW5864B), and 12 channel external video decoders (TW5864C). TW5864 can also be used in embedded DVR applications as an AV front-end chip with H264 encoding capability. It can work with existing H.264 hardcore or DSP based CODECs. In existing H264 CODECs, performance may be limited due to limitation in both memory bandwidth and hardware resources. With the H.264 encoder built in at the front-end, the number of encoding channel supported scales with number of TW5864 chips used. The front-end H264 encoder offloads the processing from the backend CODECs to allow higher port count support and allows DSP resources saved and reserved for product differentiation features such as video analytic intelligence.

The TW5864 features H.264 baseline level 3 compliant encoder capable of performing up to 5 D1 equivalent video encoding (125 fps for PAL and 150 fps for NTSC), 17 channel G.726 ADPCM hardware audio encoder with one channel for two way audio communication. The H.264 video encoder supports dual-bitstream compression for both local storage and network port outputs. It also features a motion JPEG encoder for up to 25 frames per second shared among all video channels.

The TW5864 integrates 4 A/V decoders. It has 4 CVBS analog inputs fed into four internal high quality NTSC/PAL video decoders. In addition, it has 3 digital BT. 656 input, running up to 108 MHz, capable of receiving up to 12 D1 video channels from external multi-channel video decoders such as TW2866 / TW2867. This allows the TW5864 to support a total of 16 video input channels. The video streams from both on-chip/off-chip video decoders are fed into H.264 encoder as well as to external interfaces for preview purpose. The preview stream can go through either four BT. 656 video output interfaces or PCI interfaces. The four BT 656 ports support both multi-channel byte or line interleaved output to interface with various external display solutions.

The TW5864 has built-in de-interlacers and OSDs before encoding is performed. There are also 16 sets of motion detection / night detection / blind detection engine for channel alarm notification. In addition, the hardware encoder generated motion information of each channel is accessible to the external CPU for analytic purpose. TW5864 also integrates many sets of scalers for each of the H264 encoder, MJPEG, and preview paths. Each of these scalers is independently configured.

The TW5864 provides both asynchronous host interface and PCI interface for external CPU control and bitstream upload. The PCI interface can run at 33 or 66 MHz.

Analog Video Decoder

- 4 CVBS analog inputs fed into 4 sets of video decoder accept all NTSC(M/N/4.43) / PAL (B/D/G/H/I/K/L/M/N/60) standards with auto detection
- Integrated video analog anti-aliasing filters and 10 bit CMOS ADCs for each video decoder
- High performance adaptive 4H comb filters for all NTSC/PAL standards
- IF compensation filter for improvement of color demodulation
- Color Transient Improvement (CTI)
- Automatic white peak control
- Programmable hue, saturation, contrast, brightness and sharpness
- Proprietary fast video locking system for non-real-time application
- Noise Reduction to remove impulse noise

Digital Input Ports

- Three BT. 656 ports, each running at 108 MHz, directly interfaced with 3 external TW2866s

- Byte-interleaving supports 4 channels each port
  - Interlaced D1 interface at 60 / 50 fields per second
  - Progressive D1 interface at 30 / 25 frames per second
- **Pre-processing**
- Per channel triple high performance downscalers of each channel scales independently for H264, JPEG and preview output
- Per channel motion detector with 16 X 12 cells
  - Single Box
  - 1-bit per pixel text
  - 12-bit per pixel bitmap
- **Digital Output Ports**
- Preview video for external display chips
- Four BT. 656 ports for preview raw video output
- Byte-Interleaving interlaced D1 for all ports at 27 or 108 MHz
- Line-interleaving for the first 2 ports capable of supporting mix of interlaced D1 and CIF format at 27, 54, 81, or 108 MHz

H.264 Video Encoder
- H.264 baseline profile @ level 3 encoding
- Bit rate from 64 kbps up to 10 mbps each channel
- Maximum 125 fps (PAL) or 150 fps (NTSC)
- Real-time 4 D1 / 16 CIF or non-real-time 16 D1 main stream encoding
- Real-time 4 CIF / 16 QCIF or non-real-time 16 CIF secondary stream encoding
- VBR / CBR controllable
- Configurable GOP interval

Digital Audio CODEC
- Hardware G.726 ADPCM encoder
- Encodes maximum of 17 channels, with 1 channel for two way communication
- Decodes 1 channel of audio for playback
- RTC for AV sync

DDR Interface
- Two 16-bit external DDR SDRAM memories
- Running at 166 MHz
- Total 256 MB up to 1 GB
- Auto refresh

Host Interface
- Configurable 32-bit asynchronous host interface / PCI interface
- PCI Interface runs as both initiator and target at 33 / 66 MHz
- Per channel night / blind detections
- Per channel de-interlacer to convert Interlaced video into progressive before compression
- Per channel OSD for information overlay
- Motion vector granularity at full pel, ½ pel, and ¼ pel
- Motion vector ranges [-256, +255.75]
- In-loop de-blocking filter
- CAVLC entropy coding

Video Analytic Interface
- Per MB type / motion information
- 16x12 cells motion detection information
- Accessible through PCI / Async Host Interface

Motion JPEG Encoder
- Maximum of 25 fps, shared among all channels
- Support picture sizes of D1, CIF, and half-D1

Analog Audio CODEC
- Integrated five audio ADCs and one audio DAC providing multi-channel audio mixed analog output
- Supports a standard I2S interface for record output and playback input
- PCM 8/16 bit and u-Law/A-Law 8bit for audio word length
- Programmable audio sample rate that covers popular frequencies of 8/16/32/44.1/48kHz
- Video through PCI supporting various preview resolution such as
  - 2 D1
  - 1 D1 + 4 CIF
  - 9 CIF
  - 16 QCIF
  - 1 D1 + 15 QCIF
- I2C Interface for external Video Decoder chips configuration
- IRQs and GPIOs

System Clock
- Single 27 MHz external crystal clock input
- 3 built-in PLLs for internal clock generation

Package
- 352 BGA

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Ordering Information

PART NUMBER (NOTE 1)	PART MARKING	PACKAGE (Pb-free)	PKG. DWG. #
TW5864A-BB1-CR	TW5864A BB1-CR	352 BGA (27mmx27mm). Bonding Option A	V352.27x27
TW5864B-BB1-CR	TW5864B BB1-CR	352 BGA (27mmx27mm). Bonding Option B	V352.27x27
TW5864C-BB1-CR	TW5864C BB1-CR	352 BGA (27mmx27mm). Bonding Option C	V352.27x27

NOTE:

1. These Intersil Pb-free BGA packaged products employ special Pb-free material sets; molding compounds/die attach materials and SnAg –e2 solder ball terminals, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free BGA packaged products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Functional Block Diagram

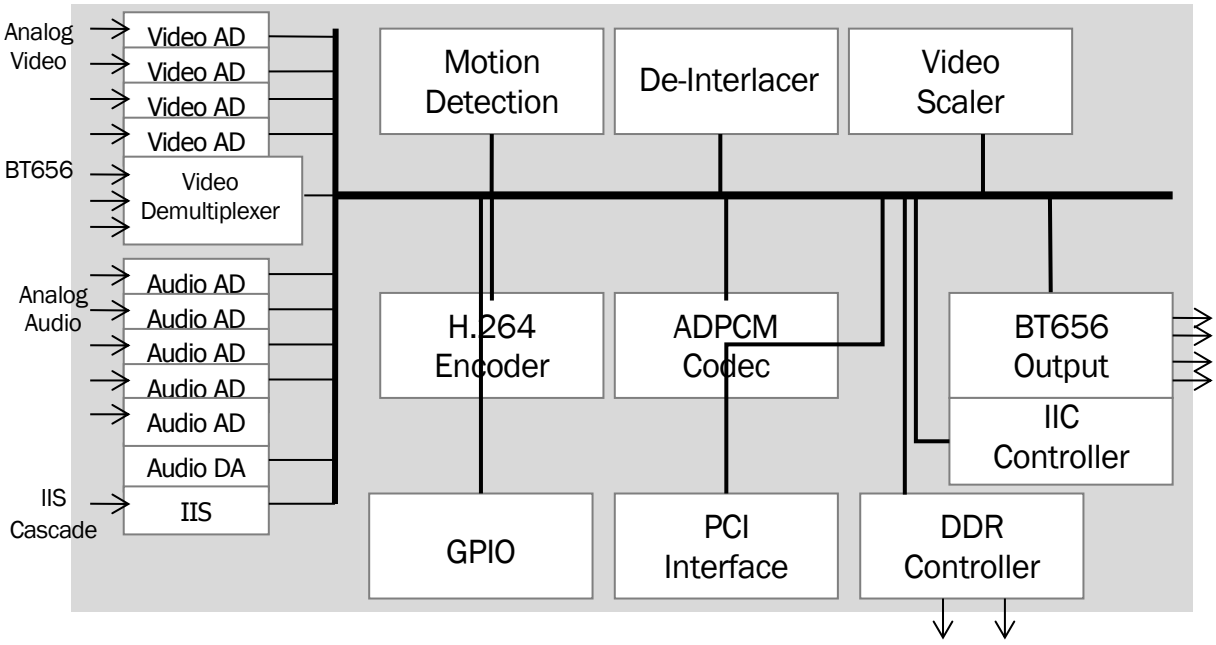


FIGURE 1. TW5864 BLOCK DIAGRAM

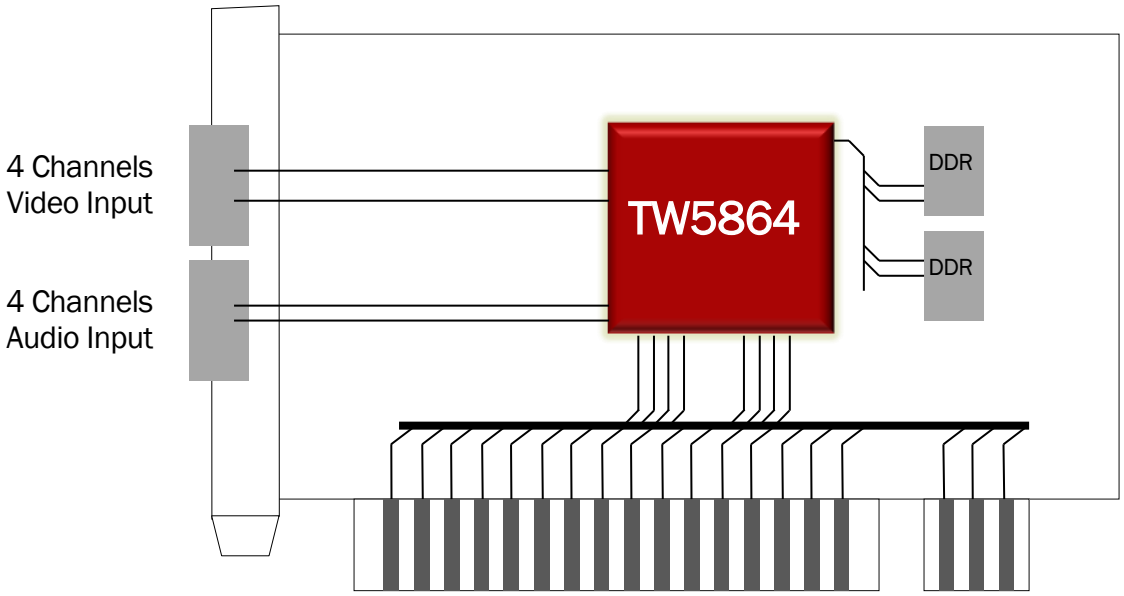


FIGURE 2. TW5864A 4-CHANNEL PC CARD SOLUTION

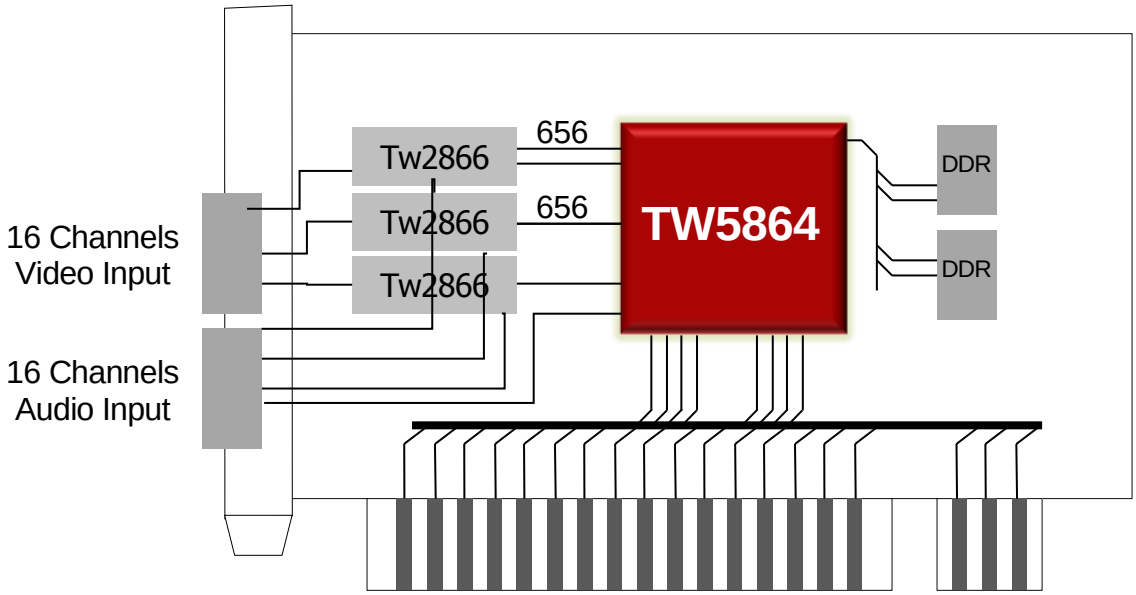


FIGURE 3. TW5864C 16-CHANNEL PC CARD SOLUTION

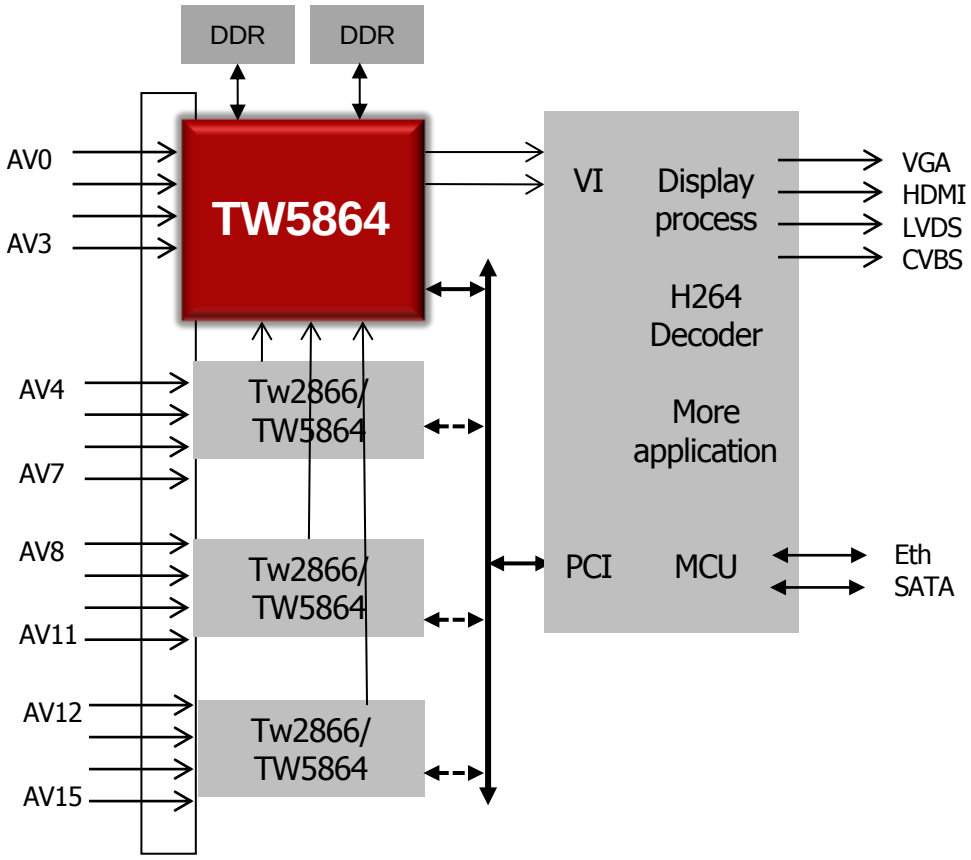


FIGURE 4. TW5864C 16-CHANNEL EMBEDDED DVR SOLUTION

Pin Diagram

TW5864 (352 BGA)

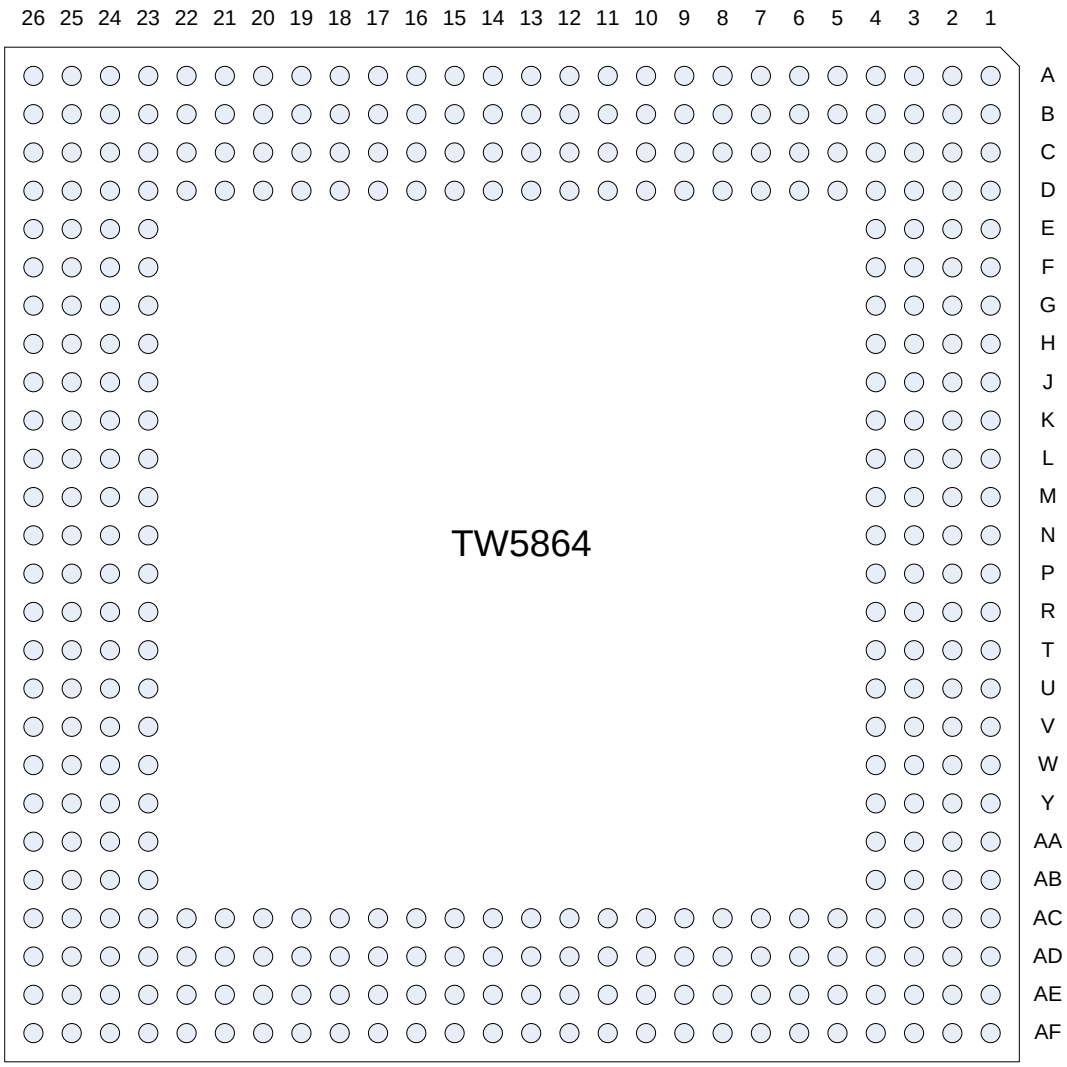


FIGURE 5. TW5864 PIN DIAGRAM (BOTTOM VIEW)

Pin Descriptions

Analog Interface

NAME	PIN #	TYPE	DESCRIPTION
VIN1	B5	A	Composite video input of channel 1.
VIN2	B4	A	Composite video input of channel 2.
VIN3	B3	A	Composite video input of channel 3.
VIN4	B2	A	Composite video input of channel 4.
AIN1	D2	A	Audio input of channel 1.
AIN2	D1	A	Audio input of channel 2.
AIN3	E4	A	Audio input of channel 3.
AIN4	E3	A	Audio input of channel 4.
AIN5	E2	A	Audio input of channel 5.
AINN	D3	A	AINN
AOUT	B1	A	Audio mixing output.

PCI Interface

NAME	PIN#	TYPE	DESCRIPTION
PCI_AD[31:0]	AD14, AE14, AF14, AC15, AD15, AE15, AF15, AD16, AD17, AE17, AF17, AC18, AD18, AE18, AF18, AE19, AE22, AF22, AD23, AE23, AF23, AC24, AD24, AE24, AC25, AD25, AE25, AF25, AC26, AD26, AE26, AF26	I/O	PCI Address / Data Multiplexed Signals
PCI_CBE_N[3:0]	AE16, AF19, AD22, AF24	I/O	PCI Bus Command and Byte Enable Signals
PCI_PAR	AF21	I/O	PCI Parity Signal
PCI_SERR_N	AE21	I/O	PCI System Error Signal
PCI_PERR_N	AD21	I/O	PCI Parity Error Signal
PCI_STOP_N	AC21	I/O	PCI Stop Signal
PCI_DEVSEL_N	AF20	I/O	PCI Device Select Signal
PCI_TRDY_N	AE20	I/O	PCI Target Ready Signal
PCI_IRDY_N	AD20	I/O	PCI Initiator Ready Signal
PCI_FRAME_N	AC20	I/O	PCI Cycle Frame Signal
PCI_IDSEL	AC17	I/O	PCI Initialization Device Select Signal
PCI_CLK	AF16	I	PCI Clock Signal
PCI_REQ_N	AC14	O	PCI Request Signal
PCI_GNT_N	AF13	I/O	PCI Grant Signal
PCI_INTA_N	AE13	O	PCI Interrupt A signal
PCI_RST_N	AB24	I	PCI Reset signal

ASYNC Host Interface

Name	Pin#	Type	Description
AS_ADDR[19:1]	AE7, AD7, AC7, AF6, AE6, AD6, AC6, AF5, AE5, AD5, AF4, AD4, AF3, AE3, AD3, AF2, AE2, AF1, AE1	I	Asynchronous Host Interface Address Bus Note: AS_ADDR[16:1] shared with PV_DATA2 / PV_DATA3
AS_CS	AC8	I	Asynchronous Host Interface Chip Select
SYNC_CS	AE8	I	Sync port chip select
SYNC_CLK	AD8	I	Sync port clock
GPIO[7:0]	AC12, AF11, AE11, AF10, AE10, AD10, AF9, AE9	I/O	General Purpose IO
ENDIAN_TYPE	AD9	I	Endian Type of the Host Interface. This pin is has effect only when the Asynchronous Host Interface mode is used. (MODE_SEL = 0) 1: Big Endian, 0: Little Endian
BUS_WIDTH	AC9	I	Data Bus Width of the Host Interface. This pin has effect only when Asynchronous Host interface is used. (MODE_SEL = 0) 1: 32 bit, 0: 16 bit
MODE_SEL	AF8	I	PCI Mode Select. 1: PCI, 0: Asynchronous Host Interface
I2C_SDA	P2	I/O	I2C Data Signal. The I2C signal is master, and used to control the external TW286x video decoder chips only.
I2C_SCL	P1	I/O	I2C Clock Signal. The I2C signal is master, and used to control the external TW286x video decoder chips only.
IB	R1	I/O	ID Input signal

Video Digital Interface

Name	Pin #	Type	Description
VD1[7:0]	G1, F1, G2, F2, G3, F3, G4, F4	I	Video data of VD1 input in BT. 656 (Tie to ground if TW5864A)
VD_CLK1	H1	I	Clock of VD1 input BT 656 port (Tie to ground if TW5864A)
VD2[7:0]	J1, K2, J2, H2, K3, J3, H3, H4	I	Video data of VD2 input in BT. 656 (Tie to ground if TW5864A and TW5864B)
VD_CLK2	K1	I	Clock of VD2 input BT 656 port (Tie to ground if TW5864A and TW5864B)
VD3[7:0]	M1, L1, N2, M2, L2, N3, M3, L3	I	Video data of VD3 input in BT. 656 (Tie to ground if TW5864A and TW5864B)
VD_CLK3	N1	I	Clock of VD3 input BT 656 port (Tie to ground if TW5864A and TW5864B)
PV_DATA0[7:0]	T1, T2, U1, U2, V1, V2, W1, W2	O	Video data of preview output port 0 in BT. 656
PV_CLK0	Y1	O	Clock of preview output port 0
PV_DATA1[7:0]	Y2, AA1, AA2, AB1, AB2, AC1, AC2, AD2	O	Video data of preview output port 1 in BT. 656
PV_CLK1	AD1	O	Clock of preview output port 1
PV_DATA2[7:0]	AE1, AF1, AE2, AF2, AD3, AE3, AF3, AD4	O	Video data of preview output port 2 in BT. 656 Note: AS_ADDR[8:1] shared with PV_DATA2
PV_CLK2	AE4	O	Clock of preview output port 2
PV_DATA3[7:0]	AF4, AD5, AE5, AF5, AC6, AD6, AE6, AF6	O	Video data of preview output port 3 in BT. 656 Note: AS_ADDR[16:9] shared with PV_DATA3
PV_CLK3	AF7	O	Clock of preview output port 3

Audio Digital Interface

NAME	PIN#	TYPE	DESCRIPTION
ACLKP	AF12	I/O	Audio I2S serial clock input/output of playback.
ASYNP	AE12	I/O	Audio I2S serial sync input/output of playback.
ADATP	AD12	I	Audio I2S serial data input of playback.
ALINKI	P3	I	Link signal for multi-chip connection serial input

DDR SDRAM Interface

NAME	PIN#	TYPE	DESCRIPTION
DDRA_DQ[15:0]	B10, A11, B11, A12, B12, A13, B13, A14, B15, A16, B16, A17, B17, A18, B18, A19	I/O	DDRA DRAM data bus.
DDRA_ADDR[13:0]	A23, B23, C23, D23, A24, B24, C24, D24, B25, C25, D25, B26, C26, D26	O	DDRA DRAM address bus
DDRA_DQS[1:0]	B14, A15	I/O	DDRA DRAM Data Strobe
DDRA_DM[1:0]	A10, B19	O	DDRA Byte Mask
DDRA_BA[1:0]	A26, A25	O	DDRA DRAM bank selection.
DDRA_CS[1:0]	A21, B21	O	DDRA DRAM chip selection.
DDRA_RASB	C22	O	DDRA DRAM row address selection.
DDRA_CASB	B22	O	DDRA DRAM column address selection.
DDRA_WEB	A22	O	DDRA DRAM write enable.
DDRA_CLK	B20	O	DDRA DRAM Clock Output
DDRA_CLKB	A20	O	DDRA DRAM Clock Output
DDRA_CKE	C21	O	DDRA Clock Enable
DDRB_DQ[15:0]	E25, F26, F25, G26, G25, H26, H25, J26, K25, L26,	I/O	DDRB DRAM data bus.

NAME	PIN#	TYPE	DESCRIPTION
	L25, M26, M25, N26, N25, P25		
DDRB_ADDR[13:0]	U24, V26, V25, W26, W25, W24, Y26, Y25, Y24, AA26, AA25, AA24, AB26, AB25	O	DDRB DRAM address bus
DDRB_DQS[1:0]	J25, K26	I/O	DDRB DRAM Data Strobe
DDRB_DM[1:0]	E26, R25	O	DDRB Byte Mask
DDRB_BA[1:0]	U26, U25	O	DDRB DRAM bank selection.
DDRB_CS[1:0]	N24, P24	O	DDRB DRAM chip selection.
DDRB_RASB	T24	O	DDRB DRAM row address selection.
DDRB_CASB	T25	O	DDRB DRAM column address selection.
DDRB_WEB	T26	O	DDRB DRAM write enable.
DDRB_CLK	R26	O	DDRB DRAM Clock Output
DDRB_CLKB	P26	O	DDRB DRAM Clock Output
DDRB_CKE	R24	O	DDRB Clock Enable

Misc Interface

NAME	PIN#	TYPE	DESCRIPTION
EXT_SYSCLK	B6	I/O	EXT_PCLK pin is used for internal testing only. This pin should be left open
EXT_CLK81	A6	I/O	EXT_MCLK pin is used for internal testing only. This pin should be left open
XTI (27 MHz)	D5	I	Crystal (27 MHz) Clock Input
XTO	D6	O	Crystal Clock Output
TP1	C6	I/O	Test Pin 1. For internal testing only. This pin should be left open.
TEST_EN	R2	I	Test mode enable. For internal use only. Normally tied to 0
RSTB	R3	I	System reset. Active low.

Power / Ground Interface

NAME	PIN #	TYPE	DESCRIPTION
VDDO	C7, L4, T4, V3, Y3, AA23, AB3, AC3, AC10, AD19	P	Digital power for output driver 3.3V
VDDI	C8, C10, J4, N4, T3, W3, AA3, AC22, AD11, AD13	P	Digital power for internal logic 1.2V
VSS	D7, D8, K4, M4, P4, R4, U4, V4, Y4, AA4, AB4, AB23, AC4, AC5, AC11, AC13, AC16, AC19, AC23	G	Pad / Core Ground
VDDVADC1	C5	P	Power for Video ADC0 3.3V
VDDVADC2	C4	P	Power for Video ADC1 3.3V
VDDVADC3	C3	P	Power for Video ADC2 3.3V
VDDVADC4	C2	P	Power for Video ADC3 3.3V
VSSVADC1	A5	G	Ground for Video ADC0
VSSVADC2	A4	G	Ground for Video ADC1
VSSVADC3	A3	G	Ground for Video ADC2
VSSVADC4	A2	G	Ground for Video ADC3
VDDAADC	E1	P	Power for Audio ADC 3.3V
VDDADAC	C1	P	Power for Audio DAC 3.3 V
VSSAADC	D4	G	Ground for Audio ADC
VSSADAC	A1	G	Ground for Audio DAC
VDDSYSPLL	B9	P	Power for Memory Clock PLL +3.3V
VSSSYSPLL	A9	G	Ground for Memory Clock PLL
VDDCLK81PLL	B8	P	Power for 81 MHz Clock PLL +3.3V
VSSCLK81PLL	A8	G	Ground for 81 MHz clock PLL
VDDSPLL	B7	P	Power Internal 108 MHz clock PLL +3.3V
VSSSPLL	A7	G	Ground Internal 108 MHz clock PLL
VDDDLL	D14, H24	P	DLL Power +1.2V
VSSDLL	C14, G24	G	DLL Ground
VREFSSTL	C12, C17, E24, J24	P	SSTL Reference Voltage (1.25 V)
VSSRSSTL	D12, D17, F24, K24	G	SSTL Reference Ground
VDDO_SSTL	C9, C11, C13, C16, C18, C19, D21, G23, J23, L23, N23, R23, U23, Y23	P	SSTL I/O Power +2.5V

NAME	PIN #	TYPE	DESCRIPTION
VDD_SSTL	C15, C20, E23, M24, V23	P	SSTL Core Power +1.2V
VSS_SSTL	D9, D10, D11, D13, D15, D16, D18, D19, D20, D22, F23, H23, K23, L24, M23, P23, T23, V24, W23	G	SSTL I/O / Core Ground

Functional Description

The Techwell TW5864 features H264 base-line profile main stream encoding for up to 4 channel of D1 or 16 channels of CIF video content. In addition, TW5864 supports secondary stream encoding of up to ¼ size of each of the main stream channels. TW5864 also supports motion JPEG encoding. The encoded bitstream are available through the PCI / Asynchronous host interface.

There are 4 video decoders embedded in TW5864 to support up to 4 analog video CVBS inputs. In addition, there are 3 ITU-R BT. 656 digital ports to support up to 3 external TW2866 video decoder chips. The digital input interface runs up to 108 MHz to carry up to 4 channels of video streams in byte-interleaved format. In total, there are 16 video channels received by TW5864, with 4 in analog format, and 12 in digital format.

TW5864 supports 4 ITU-R BT. 656 output ports for preview purpose to an external display chip. The preview ports also runs up to 108 MHz also, to support total of 16 D1 channel output. The preview ports support both byte-interleaved and line-interleaved BT. 656 format for flexibility. In addition, the preview video can also be available through the PCI interface for PC-card application.

For each of the input video channel, there is a set of motion detection module generating the motion / blind / night detection alert signal for external CPU. There are also 3 downscalers to downscale D1 video into Half D1 (360x240) / CIF (360x120) and QCIF (180x120) size. Each of these picture sizes can be flexibly selected into the preview output ports, the H264 encoder engine, the motion JPEG engine, or the PCI preview channel.

CVBS Video Input

FORMATS

The TW5864 has build-in automatic standard discrimination circuitry. The circuit uses burst-phase, burst-frequency and frame rate to identify NTSC, PAL or SECAM color signals. The standards that can be identified are NTSC (M), NTSC (4.43), PAL (B, D, G, H, I), PAL (M), PAL (N), PAL (60) and SECAM (M). Each standard can be included or excluded in the standard recognition process by software control. The exceptions are the base standard NTSC and PAL, which are always enabled. The identified standard is indicated by the Standard Selection (SDT) register. Automatic standard detection can be overridden by software controlled standard selection.

TW5864 supports all common video formats as shown in Table 1.

TABLE 1. VIDEO INPUT FORMATS SUPPORTED BY THE TW5864

FORMAT	LINES	FIELDS	FSC	COUNTRY
NTSC-M	525	60	3.579545 MHz	U.S., many others
NTSC-Japan (Note 1)	525	60	3.579545 MHz	Japan
PAL-B, G, N	625	50	4.433619 MHz	Many
PAL-D	625	50	4.433619 MHz	China
PAL-H	625	50	4.433619 MHz	Belgium
PAL-I	625	50	4.433619 MHz	Great Britain, others
PAL-M	525	60	3.575612 MHz	Brazil
PAL-CN	625	50	3.582056 MHz	Argentina
SECAM	625	50	4.406MHz 4.250MHz	France, Eastern Europe, Middle East, Russia
PAL-60	525	60	4.433619 MHz	China
NTSC (4.43)	525	60	4.433619 MHz	Transcoding

NOTE:

1. NTSC-Japan has 0 IRE setup.

The analog front-end converts analog video signals to the required digital format. There are six analog front-end channels. Three channels are dedicated to analog video support. Every channel contains analog anti-aliasing filter, clamping circuit and 10-bit ADCs. It allows the support of CVBS, S-video and YPbPr component input signals for main or sub display. The other three channels are dedicated to YPbPr component video or RGB input support. Every channel contains the analog clamping circuit, variable gain amplifier and high speed ADCs. It allows three separate inputs to be connected simultaneously. A built-in line locked PLL is used to generate the sampling clock for various inputs.

ANALOG FRONT-END

The TW5864 contains four 10-bit ADC (Analog to Digital Converters) to digitize the analog video inputs. The ADC can be put into power-down mode by the V_ADC_PWDN register. The TW5864 also contains an anti-aliasing filter to prevent out-of-band frequency in analog video input signal. So there is no need of external components in analog input pin except ac coupling capacitor and termination resistor. 0 shows the frequency response of the anti-aliasing filter.

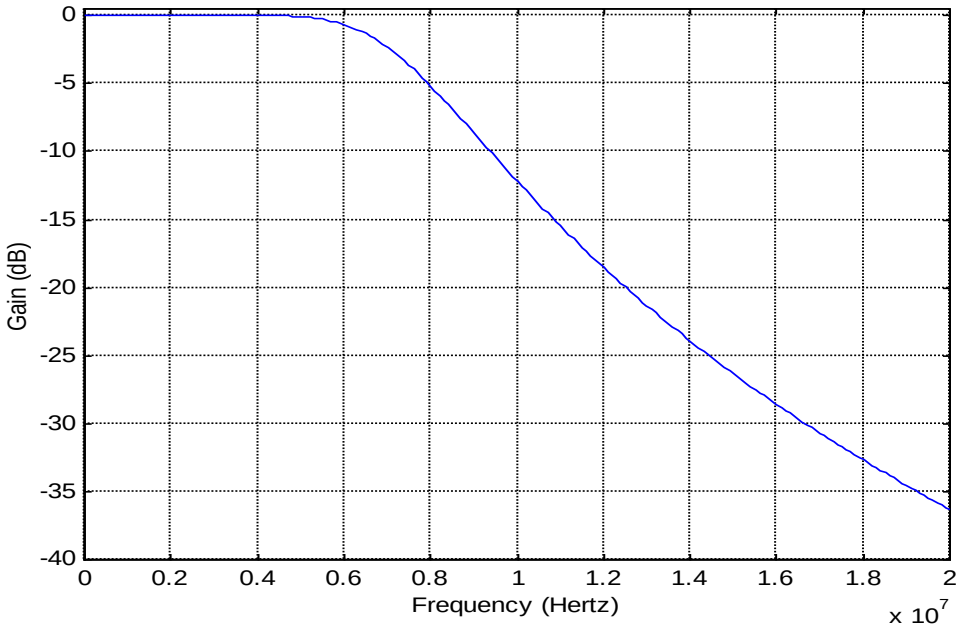


FIGURE 6. THE FREQUENCY RESPONSE OF THE VIDEO INPUT ANTI-ALIASING FILTER

DECIMATION FILTER

The digitized composite video data are over-sampled to simplify the design of analog filter. The decimation filter is required to achieve optimum performance and prevent high frequency components from being aliased back into the video image when down-sampled. 0 shows the characteristic of the decimation filter.

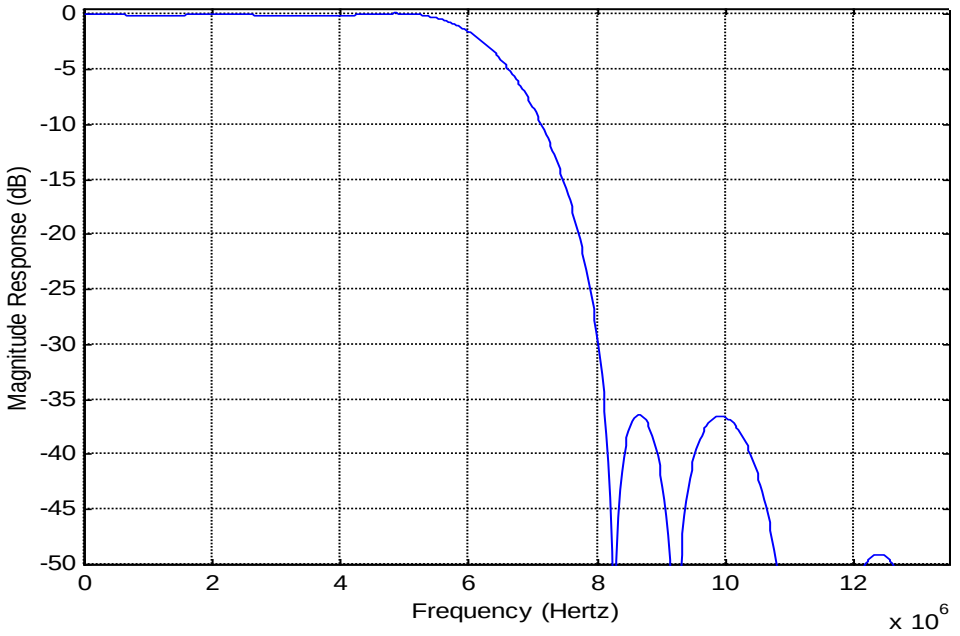


FIGURE 7. THE CHARACTERISTIC OF DECIMATION FILTER

AGC AND CLAMPING

All four analog channels have built-in clamping circuit that restores the signal DC level. The Y channel restores the back porch of the digitized video to a level of 60. This operation is automatic through internal

feedback loop. The Automatic Gain Control (AGC) of the Y channel adjusts input gain so that the sync tip is at a desired level. Programmable white peak protection logic is included to prevent saturation in the case of abnormal signal proportion between sync and white peak level.

SYNC PROCESSING

The sync processor of TW5864 detects horizontal synchronization and vertical synchronization signals in the composite video or in the Y signal of an S-video or component signal. The processor contains a digital phase-locked-loop and decision logic to achieve reliable sync detection in stable signal as well as in unstable signals such as those from VCR fast forward or backward.

The vertical sync separator detects the vertical synchronization pattern in the input video signals. In addition, the actual sync determination is controlled by a detection window to provide more reliable synchronization. An option is available to provide faster responses for certain applications. The field status is determined at vertical synchronization time. The field logic can also be controlled to toggle automatically while tracking the input

Y/C SEPARATION

The color-decoding block contains the luminance/chrominance separation for the composite video signal and multi-standard color demodulation. For NTSC and PAL standard signals, the luminance/chrominance separation can be done either by comb filter or notch/band-pass filter combination. For SECAM standard signals, adaptive notch/band-pass filter is used. The default selection for NTSC/PAL is comb filter.

In the case of comb filter, the TW5864 separates luminance (Y) and chrominance (C) of a NTSC/PAL composite video signal using a proprietary 4H adaptive comb filter. The filter uses a four-line buffer. Adaptive logic combines the upper-comb and the lower-comb results based on the signal changes among the previous, current and next lines. This technique leads to excellent Y/C separation with small cross luminance and cross color at both horizontal and vertical edges

Due to the line buffer used in the comb filter, there are always two lines processing delay at the output except for the component input mode which has only one line delay. The characteristic of the luminance notch filter is shown in Figure 8 for both NTSC and PAL system, when notch/band-pass filter is selected.

COLOR DECODING

CHROMINANCE DEMODULATION

The color demodulation for NTSC and PAL standard is done by first quadrature mixing the chrominance signal to the base band. A low-pass filter is then used to remove carrier signal and yield chrominance components. The low-pass filter characteristic can be selected for optimized transient color performance. For the PAL system, the PAL ID or the burst phase switching is identified to aid the PAL color demodulation.

For SECAM, the color information is FM modulated onto different carrier. The demodulation process therefore consists of FM demodulator and de-emphasis filter. During the FM demodulation, the chrominance carrier frequency is identified and used to control the SECAM color demodulation.

The sub-carrier signal for use in the color demodulator is generated by direct digital synthesis PLL that locks onto the input sub-carrier reference (color burst). This arrangement allows any sub-standard of NTSC and PAL to be demodulated easily with single crystal frequency.

0 and 0 show the frequency response of Chrominance Band-Pass and Low-Pass Filter Curves.

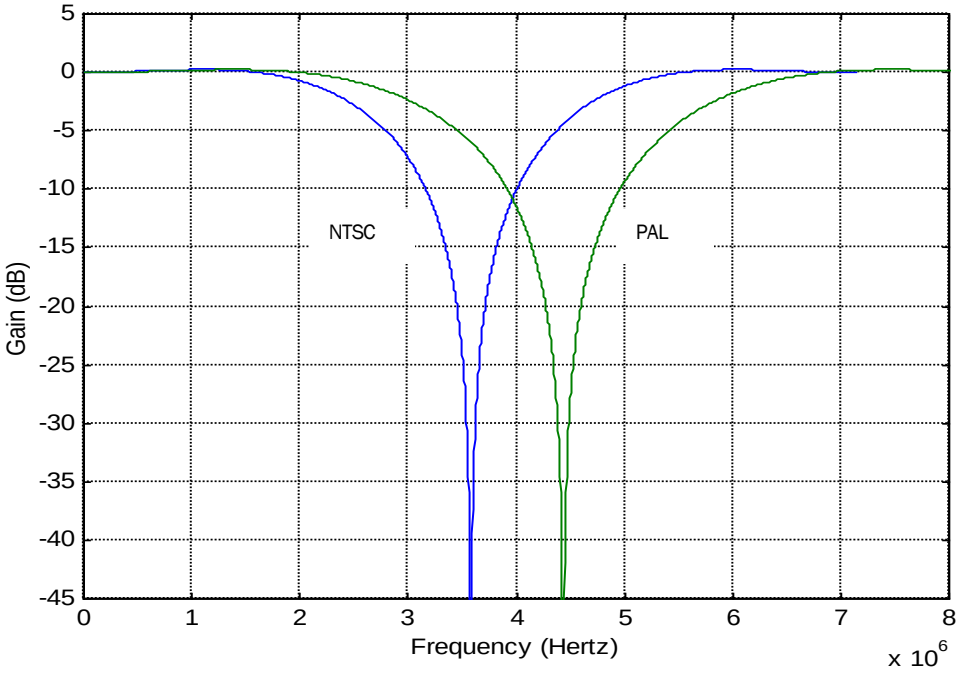


FIGURE 8. THE CHARACTERISTICS OF LUMINANCE NOTCH FILTER FOR NTSC AND PAL

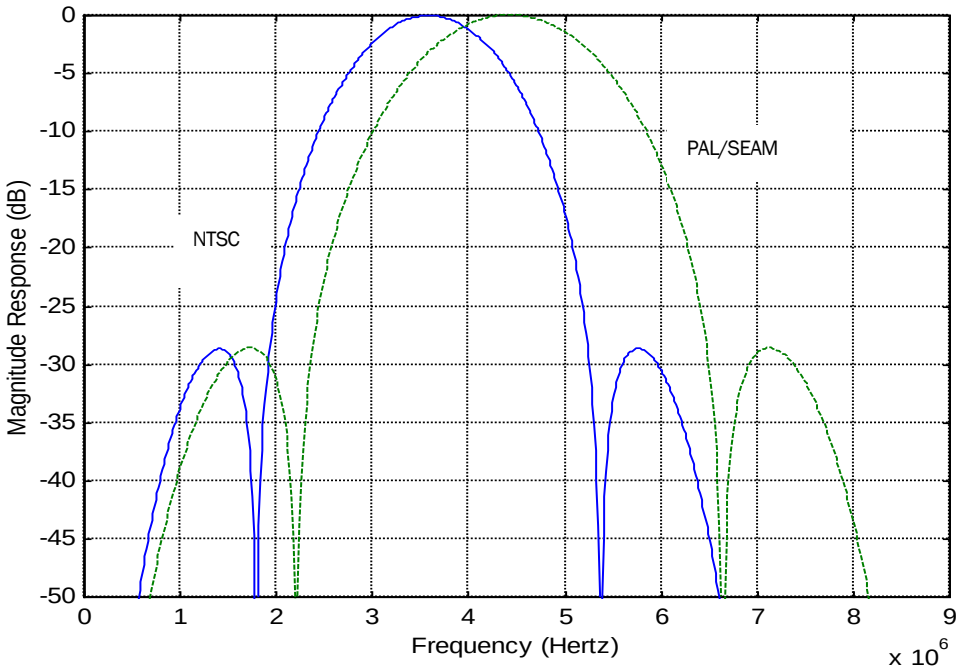


FIGURE 9. THE CHARACTERISTICS OF CHROMINANCE BAND-PASS FILTER FOR NTSC AND PAL

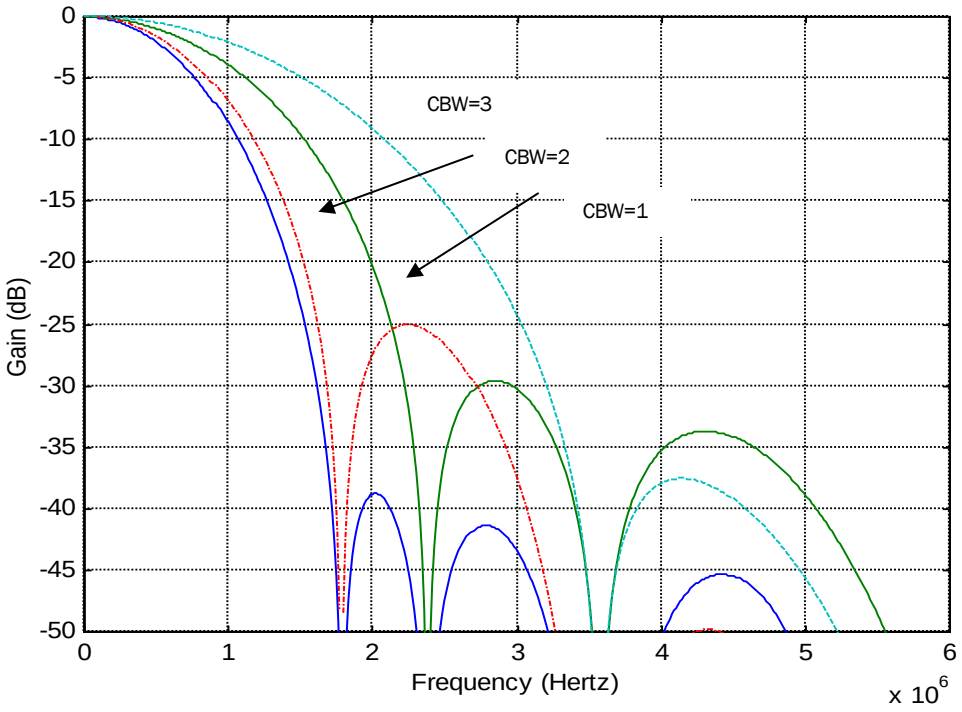


FIGURE 10. THE CHARACTERISTICS OF CHROMINANCE LOW-PASS FILTER CURVES

ACC (AUTOMATIC COLOR GAIN CONTROL)

The Automatic Chrominance Gain Control (ACC) compensates the reduced amplitudes caused by high-frequency loss in video signal. In the NTSC/PAL standard, the color reference signal is the burst on the back porch. It is measured to control the chrominance output gain. The range of ACC control is –6db to +24db.

Chrominance Processing

CHROMINANCE GAIN, OFFSET AND HUE ADJUSTMENT

When decoding NTSC signals, TW5864 can adjust the hue of the chrominance signal. The hue is defined as a phase shift of the subcarrier with respect to the burst. This phase shift of NTSC decoding can be programmed through a control register. For the PAL standard, the PAL delay line is provided to compensate any hue error; therefore, there is no hue adjustment available. The color saturation can be adjusted by changing the gain of Cb and Cr signals for all NTSC, PAL and SECAM formats. The Cb and Cr gain can be adjusted independently for flexibility.

CTI (COLOR TRANSIENT IMPROVEMENT)

The TW5864 provides the Color Transient Improvement function to further enhance the image quality. The CTI enhance the color edge transient without any overshoot or under-shoot.

Luminance Processing

The TW5864 adjusts brightness by adding a programmable value (in register BRIGHTNESS) to the Y signal. It adjusts the picture contrast by changing the gain (in register CONTRAST) of the Y signal.

The TW5864 also provide programmable peaking function to further enhance the video sharpness. The peaking control has built-in coring function to prevent enhancement of noise.

The 0 shows the characteristics of the peaking filter for four different gain modes and different center frequencies.

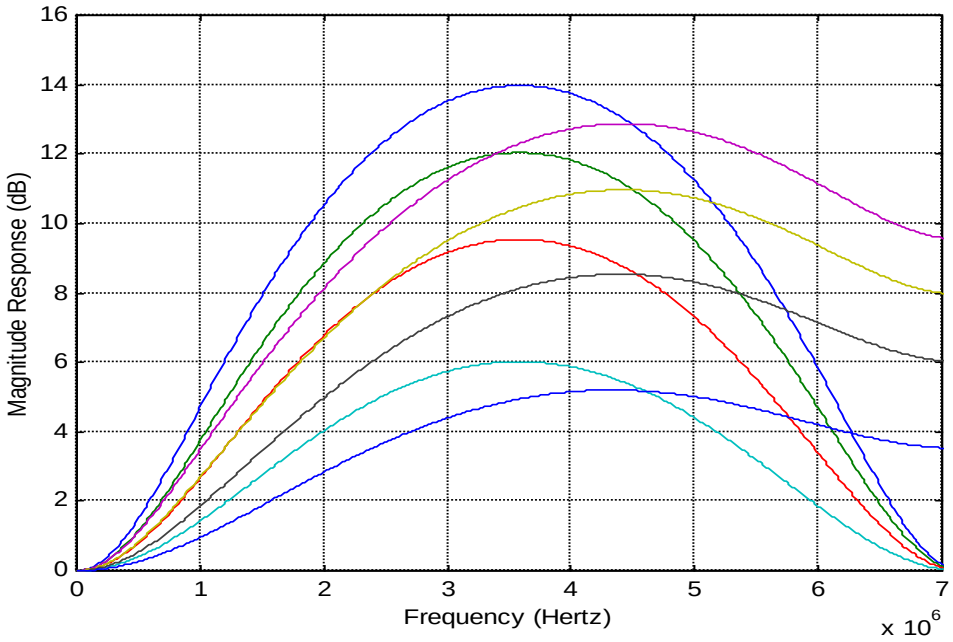


FIGURE 11. THE CHARACTERISTIC OF LUMINANCE PEAKING FILTER

ITU-R BT.656 Digital Input Ports

TW5864 supports 3 BT. 656 ports to connect up to 3 external video decoder chips. Each of the BT. 656 port runs at 108 MHz and supports 4 channels, in byte-interleaved format. In standard single channel ITU-R BT.656 format, SAV and EAV sequences are inserted into the data stream to indicate the active video time. It is noted that the number of active pixels per line is constant in this mode regardless of the actual incoming line length. The output timing is illustrated in Figure 12. The SAV and EAV sequences are shown in

Table 2. An optional set of 656 SAV/EAV code sequence can be enabled to identify no-video status using the NOVID_656 bit.

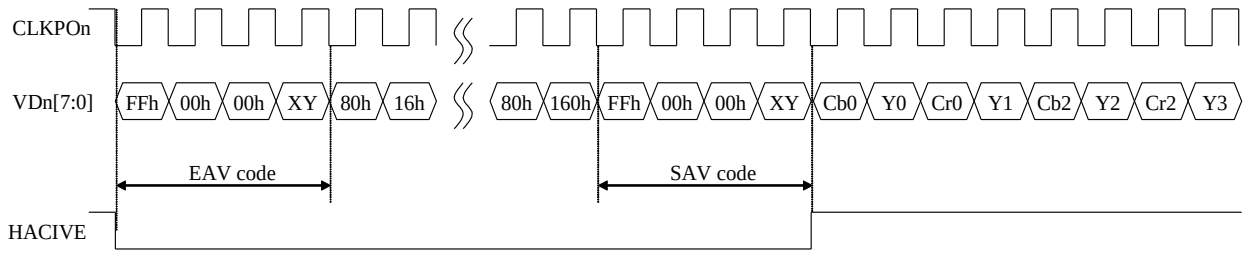


FIGURE 12. TIMING DIAGRAM OF ITU-R BT.656 FORMAT

TABLE 2. ITU-R BT.656 SAV AND EAV CODE SEQUENCE

CONDITION			656 FVH VALUE			SAV/EAV CODE SEQUENCE				
FIELD	V TIME	H TIME	F	V	H	FIRST	SECOND	THIRD	FOURTH	
									NORMAL	OPTION*
EVEN	Blank	EAV	1	1	1	0xFF	0x00	0x00	0xF1	0x71
EVEN	Blank	SAV	1	1	0	0xFF	0x00	0x00	0xEC	0x6C
EVEN	Active	EAV	1	0	1	0xFF	0x00	0x00	0xDA	0x5A
EVEN	Active	SAV	1	0	0	0xFF	0x00	0x00	0xC7	0x47
ODD	Blank	EAV	0	1	1	0xFF	0x00	0x00	0xB6	0x36
ODD	Blank	SAV	0	1	0	0xFF	0x00	0x00	0xAB	0x2B
ODD	Active	EAV	0	0	1	0xFF	0x00	0x00	0x9D	0x1D
ODD	Active	SAV	0	0	0	0xFF	0x00	0x00	0x80	0x00

NOTE: * OPTION INCLUDES VIDEO LOSS INFORMATION IN ITU-R BT.656

In order to reduce pin counts and support more channels, four channel of D1 (720x480) video stream are time-division-multiplexed into a multi-channel data format. With this, TW5864 implements a single 8 bit bus at 4 times the base clock rate of 27MHz while quadrupling the data rate on a single bus to meet the new requirement, individually, each channel data arrangement still retains the base band 27MHz ITU-R BT.656 specification. For interface that can accept the new 108MHz clock bus, only one single clock at 108MHz is required. Embedded timing (SAV-EAV) code and Channel ID are inserted into each channel for de-multiplexing and separation of channel data.

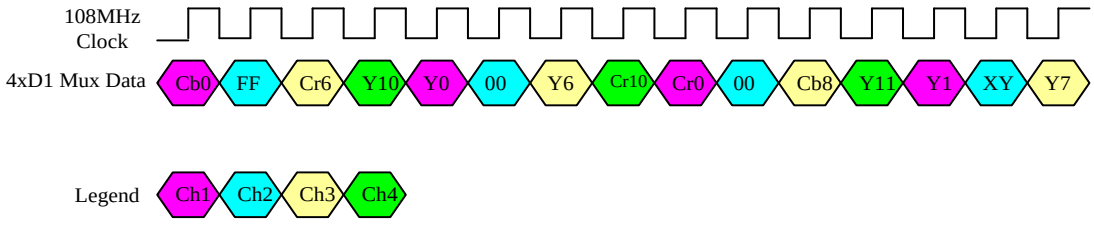


FIGURE 13. TIMING DIAGRAM OF 108MHZ 4 CH D1 TIME-DIVISION-MULTIPLEXED VIDEO DATA

Figure 13 depicts the temporal arrangement of the video data in 108MHz data rate. Each channel is byte level time-division multiplexed (TDM). Main clock is 108MHz clock. This bit stream can be de-multiplexed into 4 individual channels by sampling once in every 4 clock cycle, as show in Figure 14. After de-multiplexing, the channel ID can be identified through the EAV/SAV code from Table 3 and Table 4.

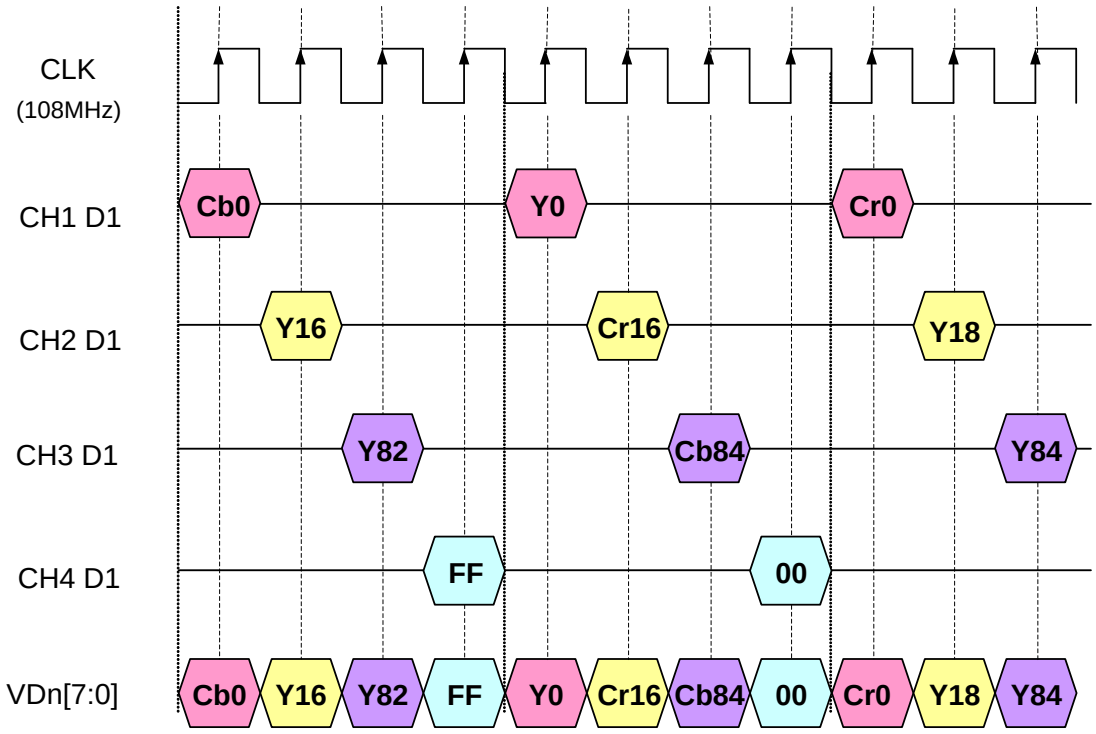


FIGURE 14. PIN OUTPUT TIMING OF 108MHZ 4 CH D1 TIME-DIVISION-MULTIPLEXED VIDEO DATA WITH 108MHZ CLOCK.

TABLE 3. SPECIAL FORMAT OF ITU-R BT. 656 EMBEDDED TIMING CODE AND CHANNEL ID CODE WHEN VIDEO IS ACTIVE

CONDITION			656 FVH VALUE			SAV-EAV CODE						
									FOURTH			
FIELD	V-TIME	H-TIME	F	V	H	FIRST	SECOND	THIRD	CH1	CH2	CH3	CH4
EVEN	BLANK	EAV	1	1	1	0xFF	0x00	0x00	0xF0	0xF1	0xF2	0xF3
EVEN	BLANK	SAV	1	1	0	0xFF	0x00	0x00	0xE0	0xE1	0xE2	0xE3
EVEN	ACTIVE	EAV	1	0	1	0xFF	0x00	0x00	0xD0	0xD1	0xD2	0xD3
EVEN	ACTIVE	SAV	1	0	0	0xFF	0x00	0x00	0xC0	0xC1	0xC2	0xC3
ODD	BLANK	EAV	0	1	1	0xFF	0x00	0x00	0xB0	0xB1	0xB2	0xB3
ODD	BLANK	SAV	0	1	0	0xFF	0x00	0x00	0xA0	0xA1	0xA2	0xA3
ODD	ACTIVE	EAV	0	0	1	0xFF	0x00	0x00	0x90	0x91	0x92	0x93
ODD	ACTIVE	SAV	0	0	0	0xFF	0x00	0x00	0x80	0x81	0x82	0x83

TABLE 4. SPECIAL FORMAT OF ITU-R BT. 656 EMBEDDED TIMING CODE AND CHANNEL ID CODE WHEN VIDEO IS NOT ACTIVE

CONDITION			656 FVH VALUE			SAV-EAV CODE						
									FOURTH			
FIELD	V-TIME	H-TIME	F	V	H	FIRST	SECOND	THIRD	CH1	CH2	CH3	CH4
EVEN	BLANK	EAV	1	1	1	0xFF	0x00	0x00	0x70	0x71	0x72	0x73
EVEN	BLANK	SAV	1	1	0	0xFF	0x00	0x00	0x60	0x61	0x62	0x63
EVEN	ACTIVE	EAV	1	0	1	0xFF	0x00	0x00	0x50	0x51	0x52	0x53
EVEN	ACTIVE	SAV	1	0	0	0xFF	0x00	0x00	0x40	0x41	0x42	0x43
ODD	BLANK	EAV	0	1	1	0xFF	0x00	0x00	0x30	0x31	0x32	0x33
ODD	BLANK	SAV	0	1	0	0xFF	0x00	0x00	0x20	0x21	0x22	0x23
ODD	ACTIVE	EAV	0	0	1	0xFF	0x00	0x00	0x10	0x11	0x12	0x13
ODD	ACTIVE	SAV	0	0	0	0xFF	0x00	0x00	0x00	0x01	0x02	0x03

Pre-processing Modules

Behind the on-chip video decoder and the digital BT656 input ports are several pre-processing modules per channel such as the motion detection, downscalers, and channels selectors. The front-end pre-processing module prepares all the video streams into a format into a correct size that can be used by the backend modules such as line-interleaving preview module, H264 encoding module, motion JPEG encoding modules, and the PCI preview module.

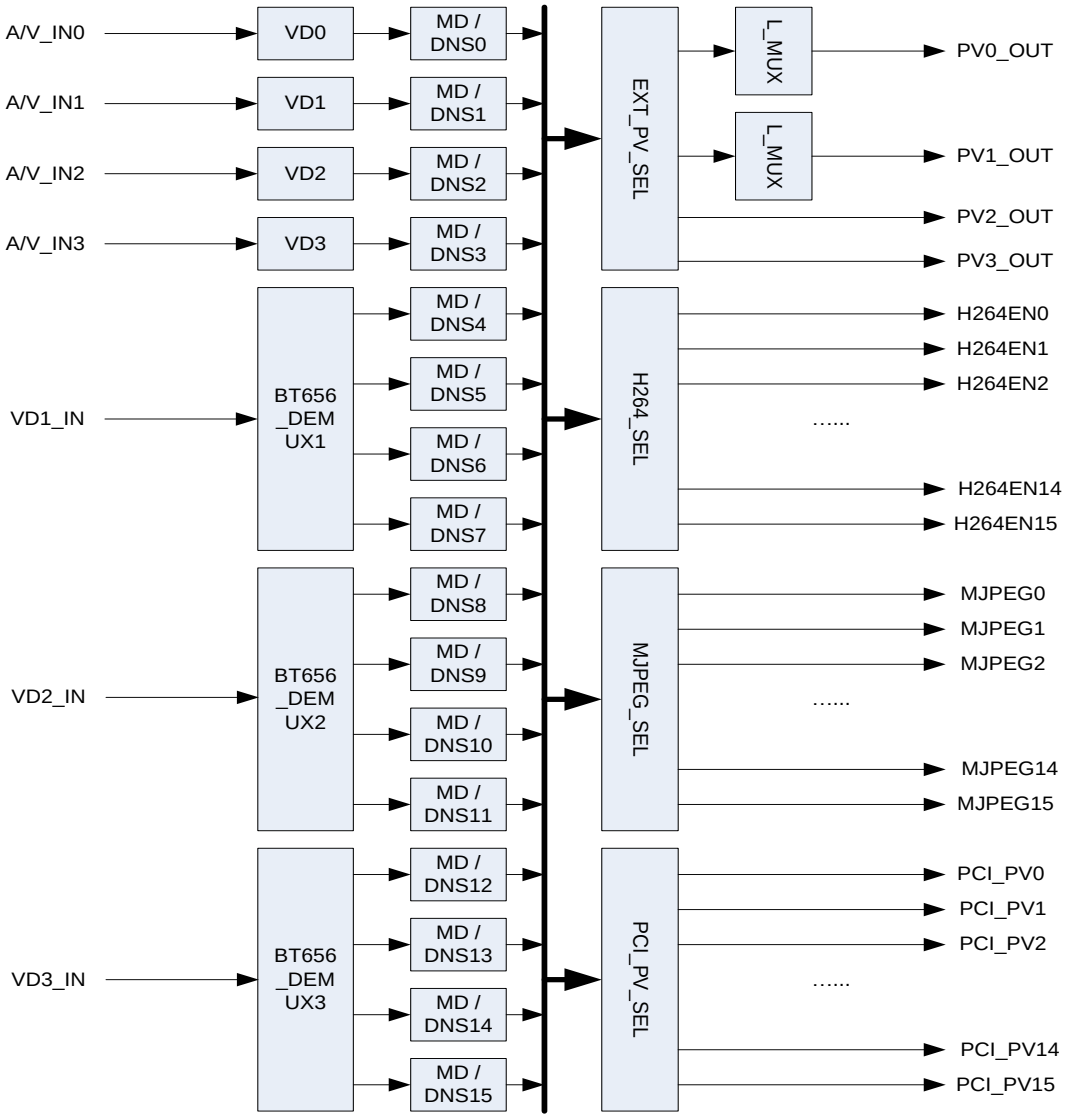


FIGURE 15. THE PRE-PROCESSING MODULE

DOWNSCALERS

The TW5864 has 16 sets of fixed downscalers, one for each incoming channel, to downscale the D1 picture size into one half horizontally (360 pixels), one quarter horizontally (180 pixels), and one half vertically (120 lines NTSC, or 144 lines PAL). With these, the combination of picture size can be 720x240, 360x240, 360x120, 180x120 (NTSC), or 720x288, 360x288, 360x144, 180x144 (PAL). These output pictures can be independently selected for each of the external digital preview port in line interleaved mode, the H264 encoding input, the Motion JPEG encoding input, and the PCI bus preview input.

MOTION DETECTION

The TW5864 supports a motion detector for each of the 16 incoming channels. The built-in motion detection algorithm uses the difference of luminance level between current and the reference field.

To detect motion properly according to situation needed, the TW5864 provides several sensitivity and velocity control parameters for each motion detector. The TW5864 supports manual strobe function to update motion detection so that it is more appropriate for user-defined motion sensitivity control.

When motion is detected in any video inputs, the TW5864 provides the interrupt request to host via the IRQ pin. Through which the host processor can read the motion information by accessing the motion status from register 0x3A0 ~ 0x3B7.

MASK AND DETECTION REGION SELECTION

The motion detection algorithm utilizes the full screen video data and detects individual motion of 16x12 cells. This full screen for motion detection consists of 704 pixels and 240 lines for NTSC and 288 lines for PAL. Starting pixel in horizontal direction can be shifted from 0 to 15 pixels using the MD_PIXEL_OS (0x301 ~ 0x37F) register.

Each cell can be masked via the MD_MASK (0x3E0 ~ 0x3F7) registers as illustrated in 0. If the mask bit in specific cell is set, the related cell is ignored for motion detection. The MD_MASK register has different function for reading and writing mode. For writing mode, setting MD_MASK register to “1” inhibits the specific cell from detecting motion. For reading mode, the MD_MASK register provides the results of the motion detection.

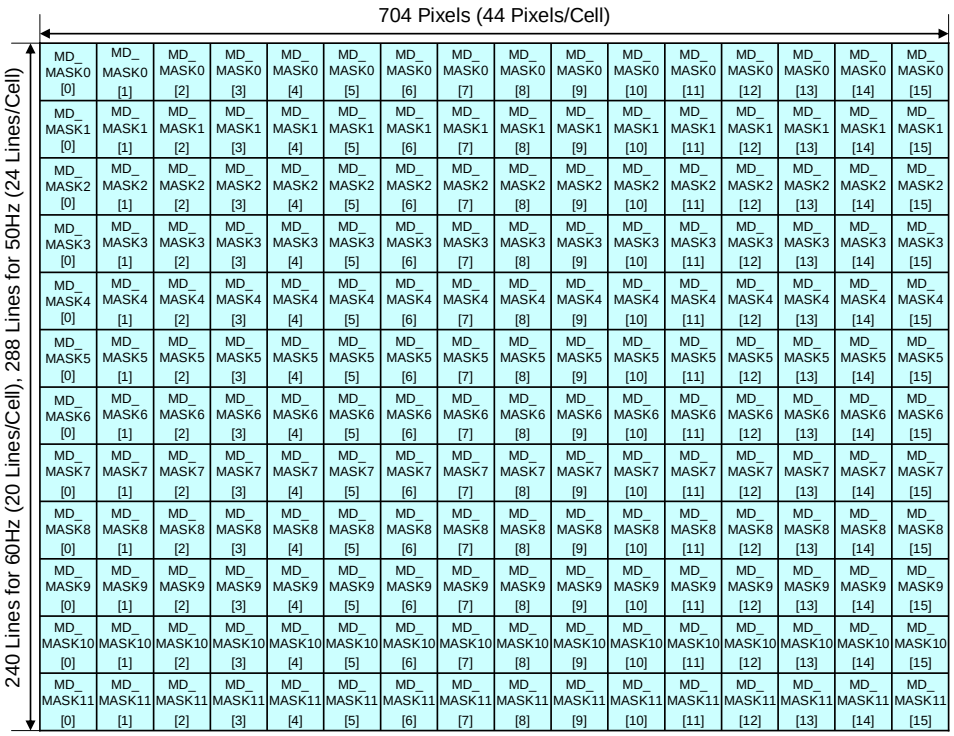


FIGURE 16. MOTION MASK AND DETECTION CELL

SENSITIVITY CONTROL

The motion detector has 4 sensitivity parameters to control threshold of motion detection such as the level sensitivity via the MD_LVSENS register, the spatial sensitivity via the MD_SPSENS and MD_CELSENS register, and the temporal sensitivity parameter via the MD_TMPSENS register.

LEVEL SENSITIVITY

In built-in motion detection algorithm, the motion is detected when luminance level difference between current and reference field is greater than MD_LVSENS value. Motion detector is more sensitive for the smaller MD_LVSENS value and less sensitive for the larger. When the MD_LVSENS is too small, the motion detector may be weak in noise.

SPATIAL SENSITIVITY

The TW5864 uses 192 (16x12) detection cells in full screen for motion detection. Each detection cell is composed of 44 pixels and 20 lines for NTSC and 24 lines for PAL. Motion detection using only luminance level difference between two fields is very weak for pictures with spatial random noise. To remove the fake motion detected from the random noise, the TW5864 supports a spatial filter via the MD_SPSENS register which defines the number of detected cell to decide motion detection in full size image. The large MD_SPSENS value increases the immunity of spatial random noise.

Each detection cell has 4 sub-cells. The actual motion detection result of each cell comes from comparison of 4 sub-cells in it. The MD_CELSENS defines the number of detected sub-cell to decide motion detection in cell. That is, the large MD_CELSENS value increases the immunity of spatial random noise in detection cell.

TEMPORAL SENSITIVITY

Similarly, temporal filter is used to remove the fake motion detection from the temporal random noise. The MD_TMPSENS regulates the number of taps in the temporal filter to control the temporal sensitivity so that the large MD_TMPSENS value increases the immunity of temporal random noise.

VELOCITY CONTROL

A motion has various velocities. That is, in a fast motion an object appears and disappears rapidly between the adjacent fields while in a slow motion it is to the contrary. As the built-in motion detection algorithm uses only the luminance level difference between two adjacent fields, a slow motion is harder to detect than a fast motion. To compensate this weakness, the current field is compared with a previous field up to 64-field time interval before. The MD_SPEED parameter adjusts the field interval in which the luminance level is compared. Thus, for detection of a fast motion a small value is needed and for a slow motion a large value is required. The parameter MD_SPEED value should be greater than MD_TMPSENS value.

Additionally, the TW5864 has 2 more parameters to control the selection of reference field. The MD_FLD register is a field selection parameter such as odd, even, any field or frame.

The MD_REFFLD register is used to control the updating period of reference field. For MD_REFFLD = “0”, the interval from current field to reference field is always same as the MD_SPEED. It means that the reference filed is always updated every field. The 0 shows the relationship between current and reference field for motion detection when the MD_REFFLD is “0”.

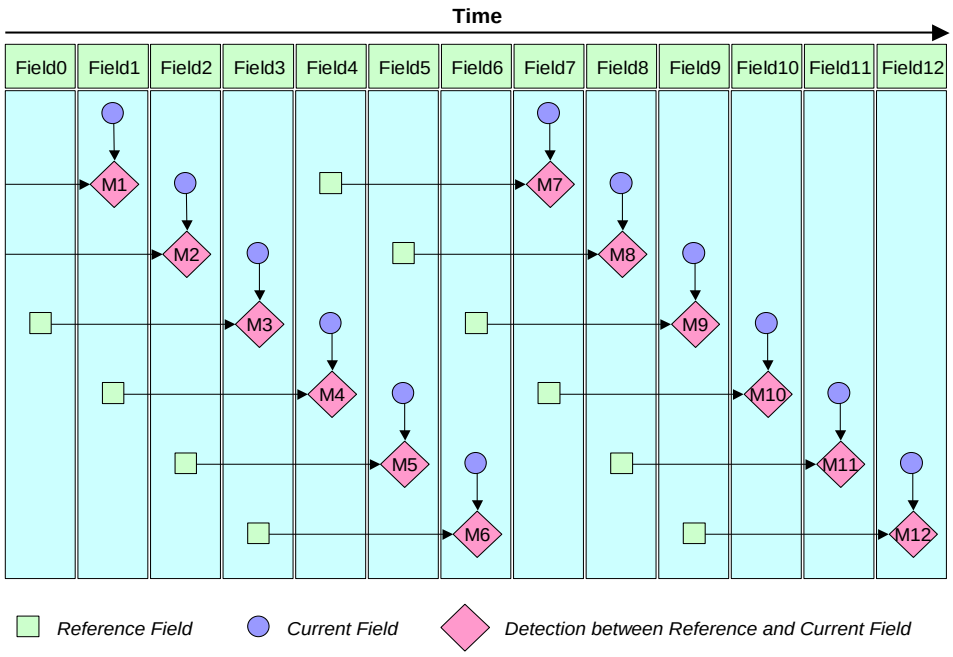


FIGURE 17. THE RELATIONSHIP BETWEEN CURRENT AND REFERENCE FIELD WHEN MD_REFFLD = “0”

The TW5864 can update the reference field only at the period of MD_SPEED when the MD_REFFLD is high. For this case, the TW5864 can detect a motion with sense of a various velocity. The 0 shows the relationship between current and reference field for motion detection when the MD_REFFLD = “1”.

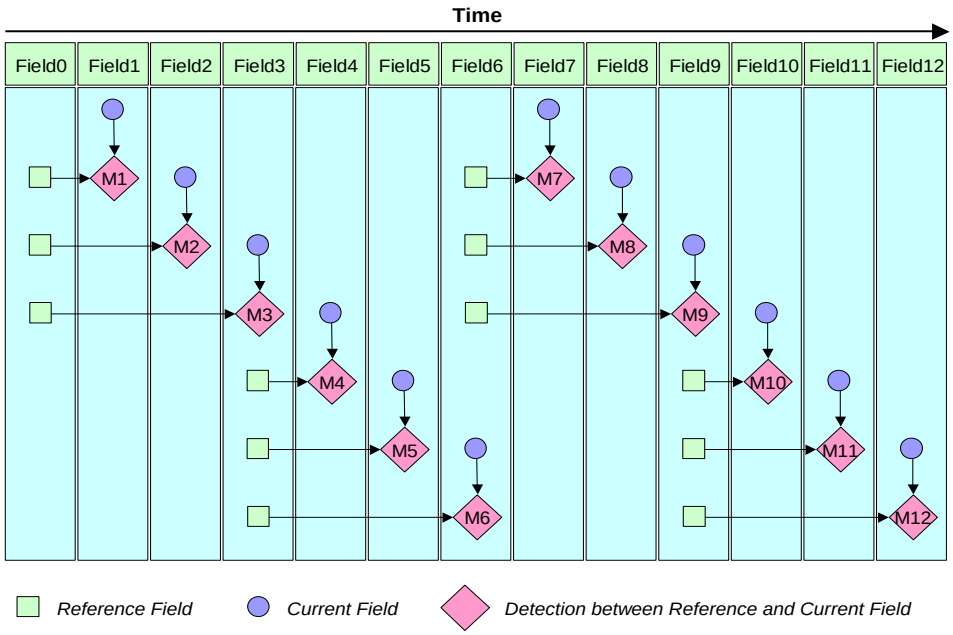


FIGURE 18. THE RELATIONSHIP BETWEEN CURRENT AND REFERENCE FIELD WHEN MD_REFFLD = "1"

The TW5864 also supports the manual detection timing control of the reference field/frame via the MD_STRB_EN and MD_STRB register. For MD_STRB_EN = "0", the reference field/frame is automatically updated and reserved on every reference field/frame. For MD_STRB_EN = "1", the reference field/frame is updated and reserved only when MD_STRB = "1". In this mode, the interval between current and reference field/frame depends on user's strobe timing. This mode is very useful for a specific purpose like non-periodical velocity control and very slow motion detection.

BLIND DETECTION

The TW5864 supports a blind detection for each of the 16 video inputs and generated an interrupt to the host when a blind condition is detected. A blind condition is detected when a camera is shaded / blocked by some unknown object and the video level in wide area of a field is almost equal to average video level of the field.

The TW5864 has two sensitivity parameters to detect blind input such as the level sensitivity via the BD_LVSENS register and spatial sensitivity via the BD_CELSENS register.

The TW5864 uses total 768 (30x224) cells in full screen for blind detection. The BD_LVSENS parameter controls the threshold of level between cell and field average. The BD_CELSENS parameter defines the number of cells to detect blind. For BD_CELSENS = "0", the number of cell whose level is same as average of field should be over than 60% to detect blind, 70% for BD_CELSENS = "1", 80% for BD_CELSENS = "2", and 90% for BD_CELSENS = "3". That is, the large value of BD_LVSENS and BD_CELSENS makes blind detector less sensitive.

The host can read blind detection information via MCU interrupt. When blind input is detected in any video inputs, the host processor can read the information by accessing the INTERRUPT_VECT registers. This status information is updated in the vertical blank period of each input.

NIGHT DETECTION

The TW5864 supports night detection for each of the 16 video inputs and generates an interrupt to the host when a night condition is detected. If an average of a field video level is very low, this input is interpreted as night. Otherwise, the input is treated as day.

The TW5864 has two sensitivity parameters to detect night input such as the level sensitivity via the ND_LVSENS register and the temporal sensitivity via the ND_TMPSENS register. The ND_LVSENS parameter controls threshold level of day and night. The ND_TMPSENS parameter regulates the number of taps in the temporal low pass filter to control the temporal sensitivity. The large value of ND_LVSENS and ND_TMPSENS makes night detector less sensitive.

The host can read night detection information via the MCU interrupt. When night input is detected in any video inputs, the TW5864 provides the interrupt request to host via the IRQ pin. The host processor can read the information of night detection by accessing the INTERRUPT_VECT register. This status information is updated in the vertical blank period of each input.

H264 ENCODING CHANNEL CAPTURE

The TW5864 supports up to 16 channels of real-time / non-real-time video for encoding simultaneously. Each of the 16 channels can be configured to capture picture size of either D1 (720x288 / 720x240) or Half D1 (360x288 / 360x240). The capture module can be configured to capture both fields (odd and even) or just single field. For a D1 compression, both fields should be captured. For CIF compression, however, only a single field needs to be captured in order to support a frame size of 360x288 / 360x240.

There are 4 separate DDR write paths embedded in the H264 capture module. The selection of channels in each path is as shown in Figure 19. In the first stage (CH_0' ~ CH_F'), one channel out of the 16 incoming channels (CH_0 ~ CH_F) is selected. Every 4 channel of the first stage channels are grouped into one DDR write path. In order to encode 4 D1 + 4CIF in H264, the module will only capture up to 4 channels of real-time D1 video streams. Each DDR write path captures 1 channel of real-time D1 video. The secondary stream is automatically generated from the main stream by downscaling ½ in each of the horizontal and vertical direction. In order to support 16 D1 non-real-time encoding, the module captures all 16 channels in D1 resolution while sub-sampling at time domain. The sub-sampling rate is controlled by the external MCU through register settings.

Note that although each video channel can be individually configured with either D1 or Half D1 size, the total peak throughput of each DDR write path should not exceed 2 D1 channel bandwidth, except on the first write path where 1D1+3CIF can be supported. The higher peak bandwidth on the first write path allows TW5864 to support 1D1+15CIF channel configuration. Due to the peak bandwidth limitation on the write path, the selection of channels merged into the same DDR write path has to be carefully selected.

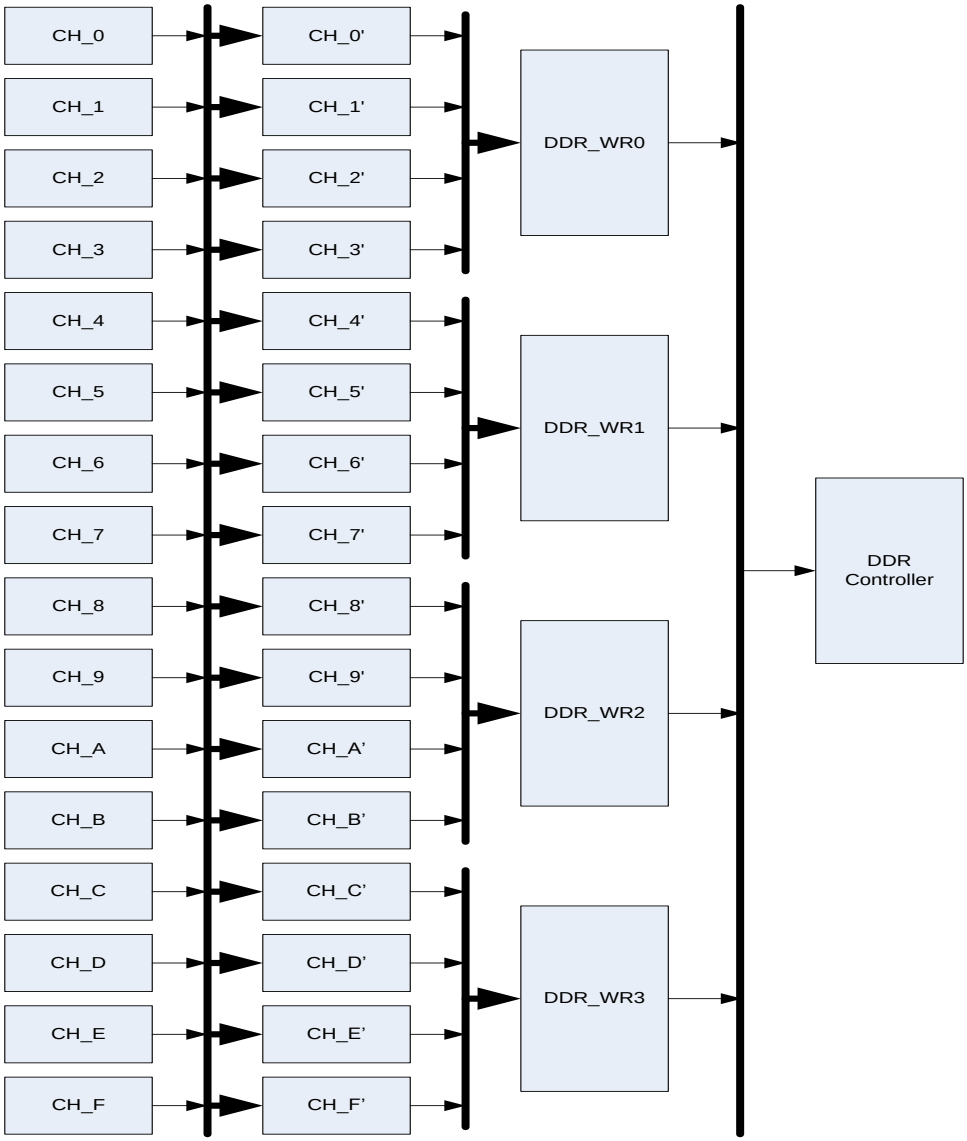


FIGURE 19. H264 ENCODING CAPTURE PATH CHANNEL SELECTION

MJPEG ENCODING CHANNEL CAPTURE

TW5864 MJPEG engine is designed to support a low frame rate encoding operation. When encoding multiple channels, it is time multiplexed between channels.

- At least 1 F/S for each of 16 channels in TW5864
- >= 25 F/S overall encoding capability
- At any time a maximum number of two frames can be captured simultaneously into DDR buffer for JPEG encoding

The TW5864 motion JPEG encoder supports two separate internal capture paths. Each capture path can select one channel out of any of the 16 incoming video channel at any instance of time. With this time sharing mechanism, the MJPEG module can support up to 1 D1 frame per second for each of the 16 channels.

The MJPEG capture modules select various picture sizes independently from channel to channel. The supported sizes are D1 (720x288 / 720x240), Half D1 (360x288 / 360x240), CIF (360x144 / 360x120), and Half CIF (180x144 / 180x120) sizes. The capture module can be configured to capture either both odd and even fields, or only a single field out of a frame.

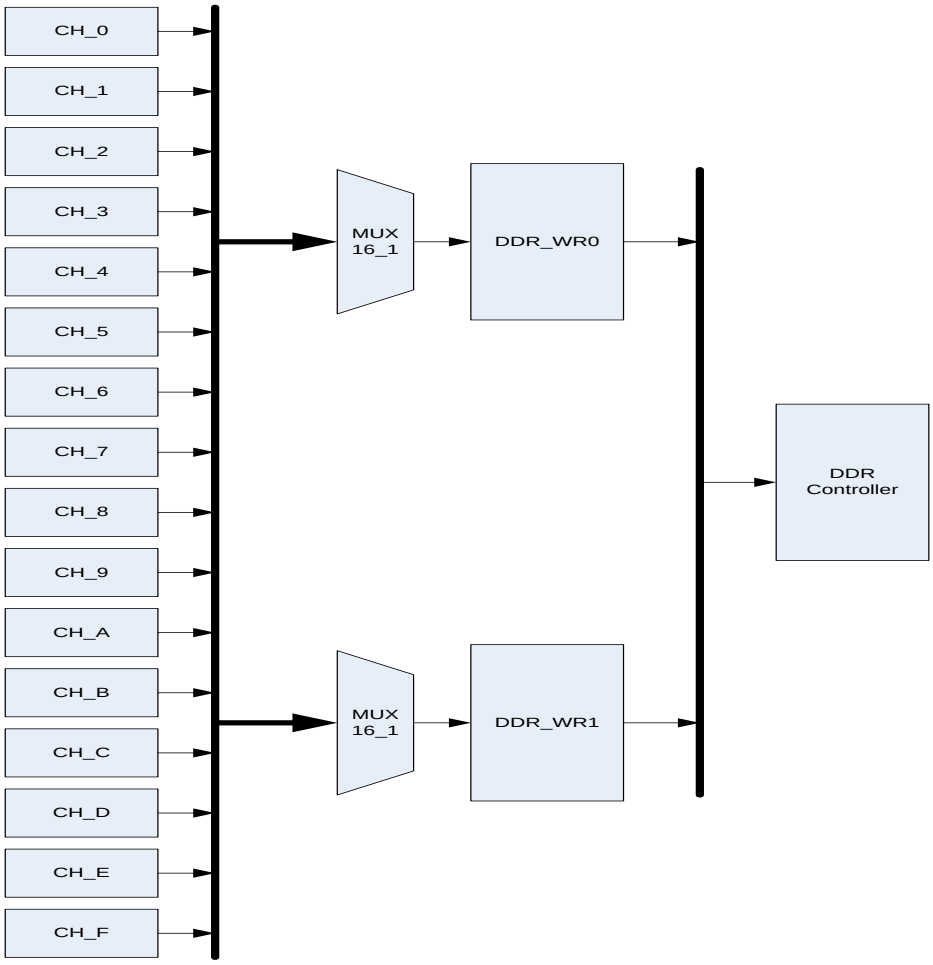


FIGURE 20. MJPEG ENCODING CAPTURE PATH CHANNEL SELECTION

PCI PREVIEW CHANNEL SELECTION

The PCI preview function is designed specifically for PC host application. PCI preview feature in TW5864 supports the following configuration.

- 1D1+1D1
- 4CIF+1D1
- 9CIF (Configurable RT or Non-RT)
- 16QCIF or 15QCIF+1D1 (Configurable RT or Non-RT)

All original video data in preview is sent from TW5864 to PC host in initiator mode. The maximum preview data being sent through PCI bus to PC host is bounded by the PCI bus bandwidth. The TW5864 PCI preview path supports 5 internal buffers BUF_0 ~ BUF_4 for sending the preview pictures onto the PCI bus. Each of the buffers is shared among any 4 channels selected out of 16 video channels except for BUF_4. The BUF_4 only shared among 2 channels. This is shown in Figure 21. At the input, there are total of 16 channels, from CH_0 through CH_F. Each of the first stage channel sections CH_0' through CH_F' can select one channel out of any of the 16 incoming channels. The second stage channel selection for input to BUF_0 selects one channel from of CH_0' ~ CH_0"3. Similarly BUF_1 with input from CH_4' ~ CH_7', BUF_2 with input from CH_8' ~ CH_B', and BUF_3 with input from CH_C' ~ CH_F'. BUF_4 has input from CH_2' and CH_3' only. Each Buffer has a limitation of supporting up to 1 D1 channel, 2 CIF channels, or 4 QCIF channels. In order to support 9 CIF channels, BUF_4 is used to support the addition CIF channel.

The PCI preview path input pictures of D1, Half D1, CIF, and Half CIF for each individual channels. Since there are limitations on sharing the internal buffers, all channels going to the same buffer have to be of the same picture size, either CIF or QCIF.

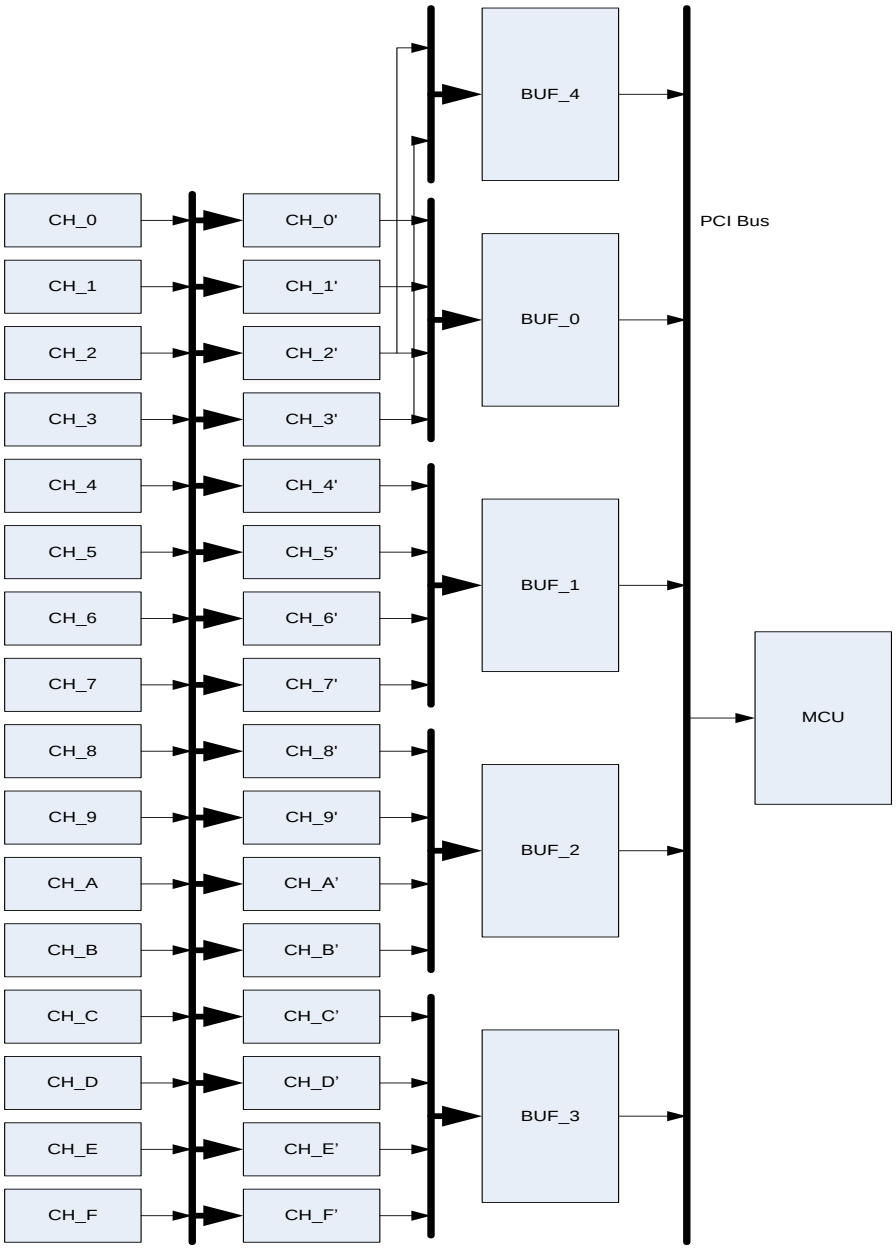


FIGURE 21. PCI PREVIEW PATH CHANNEL SELECTION

Digital Preview Output Port

TW5864 external preview ports support both byte-interleaving and line interleaving mode to put multiple channels into a single port. The following table shows the combination of mux modes supported among the 4 ports. Each port can be set independently, however, with one exception that preview ports 0, 1, 3 need to run at the same output clock rate.

TABLE 5. MUX MODES SUPPORTED IN THE PREVIEW OUTPUT PORTS

PV_SEL	MUX	PORT 0	PORT 1	PORT 2	PORT 3
0	Byte Interleaving	108 MHz D1 from on-chip VD0	108 MHz D1 from VD1	108 MHz D1 BI, from VD2	108 MHz D1 BI, from VD3
1	Byte Interleaving	108 MHz D1 from VD1	108 MHz D1 from VD1	N/A	N/A
2	Byte Interleaving	108 MHz D1 from VD2	108 MHz D1 from VD2	N/A	N/A
3	Byte Interleaving	108 MHz D1 from VD3	108 MHz D1 from VD3	N/A	N/A
4	Single Channel	27 MHz D1 from on-chip VD channel 0	27 MHz D1 from on-chip VD channel 1	27 MHz D1 from on-chip VD channel 2	27 MHz D1 from on-chip VD channel 3
5	Byte Interleaving	54 MHz D1 from on-chip VD channel 0 / 1	54 MHz D1 from on-chip VD channel 2 / 3	54 MHz HD1 from on-chip VD channel 0 / 1 / 2 / 3	N/A
6	Byte Interleaving	108 MHz D1 from on-chip VD channel 0 / 1 / 2 / 3	N/A	N/A	N/A
7	Line Interleaving	Line Mode, various Frequency	Line Mode, various Frequency	N/A	N/A

BYTE-INTERLEAVED FORMAT

The TW5864 has four sets of video output ports, each in BT. 656 interface. The video output sources can be from either the on-chip video decoders (108 MHz, 54 MHz, and 27 MHz) or simply select from the three digital video input ports at 108 MHz. In these cases, the output is in byte-interleaved format, the same as the input BT. 656 ports. The byte-interleaved modes supported in each of the 4 preview ports are the PV_SEL 0 ~ 6 as shown in Table 5.

In single channel standard ITU-R BT.656 format, SAV and EAV sequences are inserted into the data stream to indicate the active video time. It is noted that the number of active pixels per line is constant in this mode regardless of the actual incoming line length. The output timing is illustrated in Figure 22. The SAV and EAV sequences are shown in Table 6. An optional set of 656 SAV/EAV code sequence can be enabled to identify no-video status using the NOVID_656 bit.

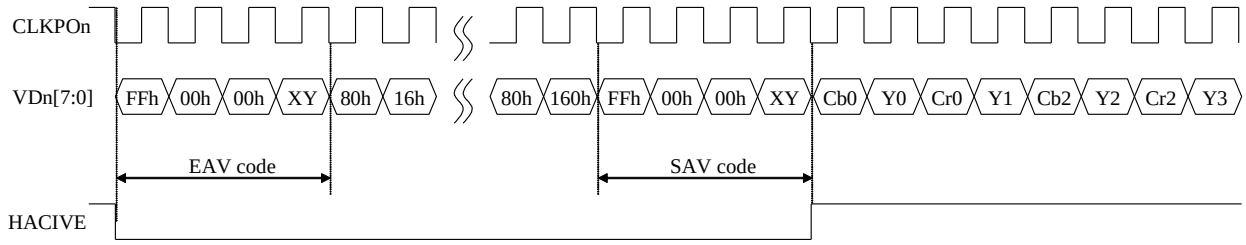


FIGURE 22. TIMING DIAGRAM OF ITU-R BT.656 FORMAT

TABLE 6. SINGLE CHANNEL STANDARD ITU-R BT.656 SAV AND EAV CODE SEQUENCE

CONDITION			656 FVH VALUE			SAV/EAV CODE SEQUENCE				
FIELD	V TIME	H TIME	F	V	H	FIRST	SECOND	THIRD	FOURTH	
									NORMAL	OPTION*
EVEN	Blank	EAV	1	1	1	0xFF	0x00	0x00	0xF1	0x71
EVEN	Blank	SAV	1	1	0	0xFF	0x00	0x00	0xEC	0x6C
EVEN	Active	EAV	1	0	1	0xFF	0x00	0x00	0xDA	0x5A
EVEN	Active	SAV	1	0	0	0xFF	0x00	0x00	0xC7	0x47
ODD	Blank	EAV	0	1	1	0xFF	0x00	0x00	0xB6	0x36
ODD	Blank	SAV	0	1	0	0xFF	0x00	0x00	0xAB	0x2B
ODD	Active	EAV	0	0	1	0xFF	0x00	0x00	0x9D	0x1D
ODD	Active	SAV	0	0	0	0xFF	0x00	0x00	0x80	0x00

NOTE: * OPTION INCLUDES VIDEO LOSS INFORMATION IN ITU-R BT.656

TWO CHANNEL D1 TIME-MULTIPLEXED FORMAT WITH 54MHZ

The TW5864 supports two channels ITU-R BT.656 time-multiplexed format with 54MHz that is useful to security application requiring two channel outputs through one channel video port. To de-multiplex the time-multiplexed data in the display mux chip, the channel ID can be inserted in the data stream using the CHID_MD register. Two kinds of channel ID format can be supported. One is horizontal blanking code with channel ID and the other is ITU-R BT.656 sync code with channel ID. The Figure 23 illustrates the logical timing diagram in the case of CH1 and CH2 time-multiplexed output through one video output port.

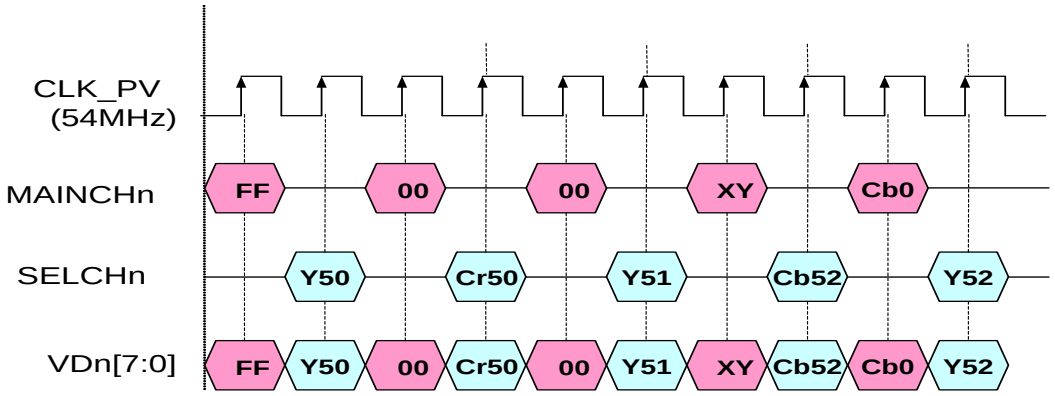


FIGURE 23. TIMING DIAGRAM OF TWO CHANNEL TIME-MULTIPLEXED FORMAT

Four Channel Half D1 Time-multiplexed Format with 54MHz

The four channel Half D1 (360x240x2) time-multiplexed format is supported at second preview port. For this format, each channel ITU-R BT.656 data stream is down-scaled horizontally into a 13.5MHz ITU-R BT.656 data stream except the sync code. Then, the four 13.5MHz ITU-R BT.656 data streams are time-multiplexed into 54MHz data stream. This format requires only one channel video port to transfer whole four channel HD1 data independently. In this mode, TW5864 can support one channel video port to transfer whole four channel D1 data at port 0 (108 MHz) or at both port 0 and port 1 (54 MHz), while using port 2 to ouput 4 channels of Half D1 video bitstreams simultaneously. To de-multiplex the time-multiplexed data in the display mux chip, the channel ID can be decoded from the SAV/EAV sync code. The Figure 24 and Table 7 illustrate the timing diagram and detailed channel ID format for four channel half D1 time-multiplexed format with 54MHz.

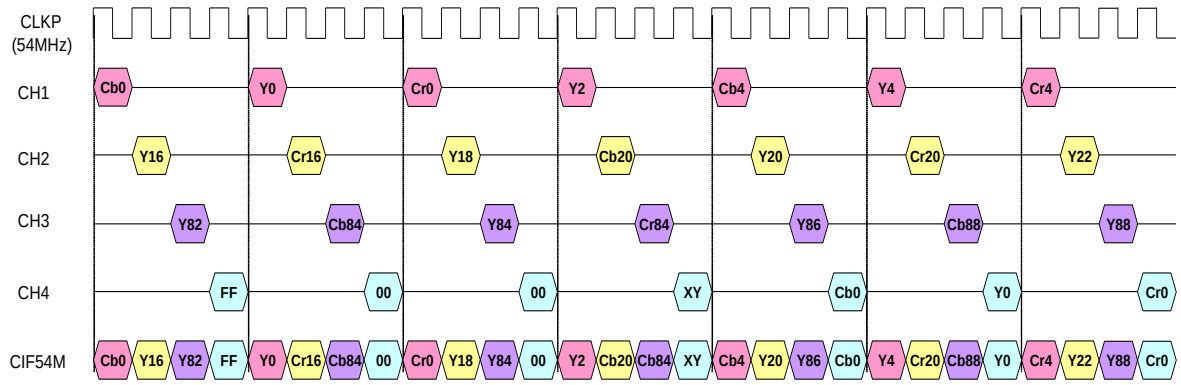


FIGURE 24. LOGICAL TIMING DIAGRAM OF 4 CH HALF D1 TIME-MULTIPLEXED FORMAT

TABLE 7. THE CHANNEL ID FORMAT FOR 4 CH HALF D1 TIME-MULTIPLEXED FORMAT WITH 54MHZ

CONDITION			656 FVH VALUE			SAV/EAV CODE SEQUENCE						
FIELD	VTIME	HTIME	F	V	H	FIRST	SECOND	THIRD	FOURTH			
									CH1	CH2	CH3	CH4
EVEN	Blank	EAV	1	1	1	0xFF	0x00	0x00	0xF0	0xF1	0xF2	0xF3
EVEN	Blank	SAV	1	1	0	0xFF	0x00	0x00	0xE0	0xE1	0xE2	0xE3
EVEN	Active	EAV	1	0	1	0xFF	0x00	0x00	0xD0	0xD1	0xD2	0xD3
EVEN	Active	SAV	1	0	0	0xFF	0x00	0x00	0xC0	0xC1	0xC2	0xC3
ODD	Blank	EAV	0	1	1	0xFF	0x00	0x00	0xB0	0xB1	0xB2	0xB3
ODD	Blank	SAV	0	1	0	0xFF	0x00	0x00	0xA0	0xA1	0xA2	0xA3
ODD	Active	EAV	0	0	1	0xFF	0x00	0x00	0x90	0x91	0x92	0x93
ODD	Active	SAV	0	0	0	0xFF	0x00	0x00	0x80	0x81	0x82	0x83

NOTE:
1. (a) ITU-R BT.656 Sync Code with Channel ID

CHANNEL	H BLANKING CODE WITH CHANNEL ID		
	Y	CB	CR
Ch1	8'h10	8'h80	8'h80
Ch2	8'h11	8'h81	8'h81
Ch3	8'h12	8'h82	8'h82
Ch4	8'h13	8'h83	8'h83

NOTE:
1. (b) Horizontal Blanking Code with Channel ID

Four Channel D1 Time-division-multiplexed Format with 108MHz

Four channel of D1 (720x480) at 27MHz video stream that are time-division-multiplexed at 108MHz data rate format is also implemented in TW5864. In order to reduce pin counts (thus shrink chip size) on both decoder's digital output port and the input port of the backend display mux devices, TW5864 implements single 8 bit bus at 4 times the base band pixel clock rate of 27MHz. While quadrupling the data rate on a single bus to meet the new requirement, individually, each channel data arrangement still retains the base band 27MHz ITU-R BT.656 specification. For interface that can accept the new 108MHz clock bus, only one single clock at 108MHz is required. Embedded timing (SAV-EAV) code and Channel ID are inserted into each channel for de-multiplexing and separation of channel data.

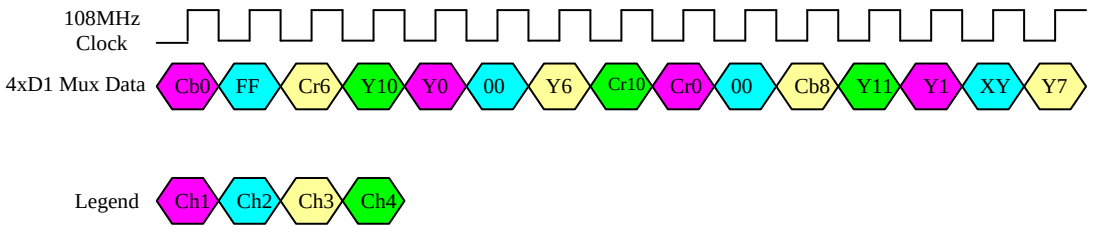


FIGURE 25. TIMING DIAGRAM OF 108MHZ 4 CH D1 TIME-DIVISION-MULTIPLEXED VIDEO DATA

Figure 31 depicts the temporal arrangement of the video data in 108MHz data rate. Each channel is byte level time-division multiplexed (TDM). Main clock is 108MHz clock.

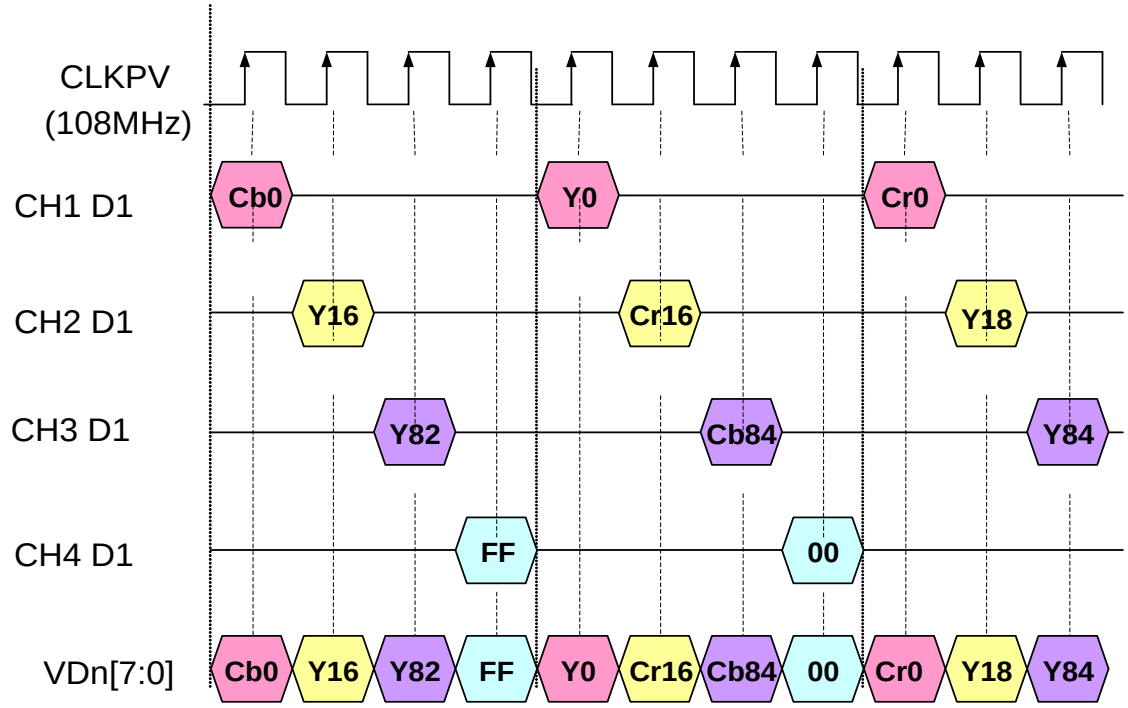


FIGURE 26. OUTPUT TIMING OF 108MHZ 4 CH D1 TIME-DIVISION-MULTIPLEXED VIDEO DATA WITH 108MHZ CLOCK.

TABLE 8. SPECIAL FORMAT OF ITU-R BT. 656 EMBEDDED TIMING CODE AND CHANNEL ID CODE

CONDITION			656 FVH VALUE			SAV-EAV CODE						
									FOURTH			
FIELD	V-TIME	H-TIME	F	V	H	FIRST	SECOND	THIRD	CH1	CH2	CH3	CH4
EVEN	BLANK	EAV	1	1	1	0xFF	0x00	0x00	0xF0	0xF1	0xF2	0xF3
EVEN	BLANK	SAV	1	1	0	0xFF	0x00	0x00	0xE0	0xE1	0xE2	0xE3
EVEN	ACTIVE	EAV	1	0	1	0xFF	0x00	0x00	0xD0	0xD1	0xD2	0xD3
EVEN	ACTIVE	SAV	1	0	0	0xFF	0x00	0x00	0xC0	0xC1	0xC2	0xC3
ODD	BLANK	EAV	0	1	1	0xFF	0x00	0x00	0xB0	0xB1	0xB2	0xB3
ODD	BLANK	SAV	0	1	0	0xFF	0x00	0x00	0xA0	0xA1	0xA2	0xA3
ODD	ACTIVE	EAV	0	0	1	0xFF	0x00	0x00	0x90	0x91	0x92	0x93
ODD	ACTIVE	SAV	0	0	0	0xFF	0x00	0x00	0x80	0x81	0x82	0x83

LINE-INTERLEAVED FORMAT

In addition to the byte-interleaving mode, the first two digital preview ports support line-interleaved format to multiplex up to 9 channel of video content into each BT. 656 port. In this case, the source video can be scaled down into various sizes, and flexibly multiplexed together. The modes supported as shown in Table 9.

TABLE 9. LINE INTERLEAVING MODES SUPPORTED IN THE FIRST TWO PREVIEW OUTPUT PORTS

OUTPUT CHANNEL COMBINATION	CLOCK RATE	PICTURE SIZE
2 D1	54 MHz	720 x 240 (NTSC) / 720 x 288 (PAL)
4 D1	108 MHz	720 x 240 (NTSC) / 720 x 288 (PAL)
4 HD1	54 MHz	360 x 240 (NTSC) / 360 x 288 (PAL)
8 HD1	108 MHz	360 x 240 (NTSC) / 360 x 288 (PAL)
4 CIF	27 MHz	360 x 120 (NTSC) / 360 x 144 (PAL)
8 CIF	54 MHz	360 x 120 (NTSC) / 360 x 144 (PAL)
4 CIF + 1 D1	54 MHz	Combination
8 CIF + 1 D1	81 MHz	Combination

In line-interleaved format, the video data are interleaved based on each line as a unit. The original BT. 656 SAV/EAV codes are maintained. In addition, within the active line, an additional 4 bytes of header are inserted in order to describe the properties of the line of the original video content. The 4 bytes headers are shown in Figure 27. The 4-byte headers codes are shown in Table 10 . The definition of parameters in Table 10 is shown in Table 11.

Since all the video channels are asynchronous to each other, there is no fixed number of spacing among channel lines. Instead, the lines are inserted into the video stream based on the availability of the input source. When there are no lines available from any channel source, a dummy line will be inserted. The dummy line header bytes are 0x01 for all 4 header bytes. In line-interleaved mode, different line sizes can be multiplexed together in either full line (720 pixels) or half line (360 pixels). Because of this, a full line can either maintains a full line, or it can be split into 2 half lines.

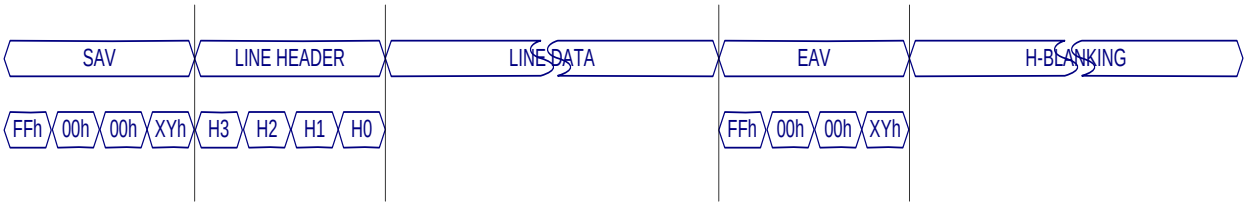


FIGURE 27. THE LINE-INTERLEAVED HEADER FORMAT

TABLE 10. LINE INTERLEAVED MODES HEADER BYTES

HEADER BYTES	7	6	5	4	3	2	1	0
H3	1	RSV	RSV	RSV	RSV	CH_ID		
H2	0	BOL	EOL	VDET	RSV	RSV	LINE_ID[8:7]	
H1	~LINE_ID[6]	LINE_ID[6:0]						
H0	1	F	V	H	P3	P2	P1	P0

TABLE 11. LINE INTERLEAVED HEADER BYTES PARAMETERS DEFINITION

BIT LOCATION	NAME	DESCRIPTION
H3[2:0]	CH_ID	The video channel ID. For preview port 0, CH_ID 0 ~ 7 means channel 0 ~ 7. (On-chip VD and VD1 digital port) For preview port 1, CH_ID 0 ~ 7 means channel 8 ~ 15. (VD2 and VD3 digital ports)
H2[6]	BOL	1: A full line, or the first half line when a full line is split into 2 half lines. 0: The second half line when a full line is split into 2 half lines.
H2[5]	EOL	1: A full line, or the second half of a full line when the line is split. 0: The second first half of a full line when it is split into 2 half lines.
H2[4]	VDET	1: Video detected 0: Video loss
H2[1:0], H1[6:0]	LINE_ID	The active video line number. The LINE_ID of the first line of each field is 0.
H0[6]	F	Field bit as defined in BT. 656
H0[5]	V	V bit as defined in BT. 656
H0[4]	H	H bit as defined in BT. 656
H0[3]	P3	Redundant protection bit 3, P3 = V XOR H
H0[2]	P2	Redundant protection bit 2, P2 = F XOR H
H0[1]	P1	Redundant protection bit 1, P1 = F XOR V
H0[0]	P0	Redundant protection bit 0, P0 = F XOR V XOR H

TABLE 12. LINE INTERLEAVED MODES HEADER BYTES FOR DUMMY LINES

HEADER BYTES	7	6	5	4	3	2	1	0
H3	0	0	0	0	0	0	0	1
H2	0	0	0	0	0	0	0	1
H1	0	0	0	0	0	0	0	1
H0	0	0	0	0	0	0	0	1

H.264 Encoding Module

DE-INTERLACERS

The TW5864 de-interlacer sitting right before H264 encoder is an enhanced cost efficient de-interfacer that performs adaptive field weaving or 2D de-interlacing depending on the content motion. The de-interlacer works on a channel by channel base. Each of the channels can be independently controlled.

OSDS

The TW5864 supports pre-encoding OSD function which overlays fonts/graphics onto the video before H264 encoding is performed. The OSD overlays onto each channel of video independently. For each channel, up to 8 windows are supported. Additionally, in order to support good quality in both main and secondary stream, two different sets of fonts can be overlaid onto the main / secondary streams independently.

H264 ENCODERS

TW5864 has a build-in baseline H264 encoder capable of encoding up to 5D1 in real-time. The H264 encoder performance is summarized as the following:

- H.264 Baseline @ Level 3 encoding, without arbitrary slice ordering (ASO), flexible MB ordering (FMO), and redundant picture
- One slice per frame
- Bitrates from 64 kbps to 10 mbps
- 4 D1 or 16 CIF encoding at 30 frames per second (NTSC) or 25 frame per second (PAL)
- Support VBR / CBR
- Configurable IDR/I Interval
- Support intra-mode (16x16 and 4x4)
- Support variable block size (16x16, 16x8, and 8x8)
- Motion vector granularity at full-pel, ½ pel, and ¼ pel
- Motion vector range [-256, +255.75]
- In-loop deblocking filter
- CAVLC entropy coding
- Collect video analytic information to MPU
- Same channel dual-stream encoding (D1/CIF, D1/QCIF, or CIF/QCIF)

The typical configuration for multichannel encoding is given here as examples:

- 4D1 main streams and 4CIF/QCIF second streams
- 16CIF main streams and 16QCIF second streams
- 16D1 sub-frame rate encoding with aggregated total encoding frames <=125 F/S
- N channel D1 and (16-N) channel CIF.

NOTE: WHEN TW5864 IS ENCODING MORE THAN 4 PHYSICAL CHANNELS, IT NEEDS ADDITIONAL TW2864 EQUIVALENT VIDEO DECODER.

H.264 CODED STREAM

TW5864 generates H.264 standard compliant base-line profile bitstream, decodable by 3rd party standard compliant decoder. TW5864 H.264 bitstream contains progressive I-frame and P-frame information, without arbitrary slice ordering, flexible MB-ordering and redundant picture feature supports.

TW5864 bitstream follows H.264 standard byte stream format by constructed from the NAL (Network Abstraction Layer) unit stream format in decoding order and prefixing each NAL unit with a start code prefix (0x00000001). For each NAL bitstream unit, zero-valued bits or zero-valued bytes are padded in the end of I-frame and P-frame payload data to form an unit of multiple of 4-byte in length.

The NAL unit stream format can be extracted from the byte stream format by searching for the location of the unique start code prefix pattern within this stream of bytes.

In TW5864 bitstream, a SPS (Sequence Parameter Set) and a PPS (Picture Parameter Set) NAL unit are proceeded each IDR (Instantaneous Decoding Refresh)-frame NAL. The following tables describe NAL unit, SPS and PPS syntax in tabular form.

TABLE 13. TW5864 NAL UNIT SYNTAX

NAL UNIT	VALUE(HEX)	BIT NUMBER
NalUnitStartCodePrefix	0x00000001	16
forbiden_zero_bit	0	1
nal_ref_idc	0x02	2
nal_unit_type	nal_unit_type_value	5
NAL payload		Variable
rbsp_trailing_bits( )		Insert zero-valued bit(s) to 32-bit aligned

TABLE 14. TW5864 SPS RBSP SYNTAX

SPS_PARAMETER_SET_RBSP (NAL_UNIT_TYPE=7)	VALUE(HEX)	BIT NUMBER
profile_idc	0x42	8
constraint_set0_flag	0	1
constraint_set1_flag	0	1
constraint_set2_flag	0	1
reserved_zero_5bits	0	5
level_idc	0x1E	8
seq_parameter_set_id	0	ue(v)
log2_max_frame_bun_minus4	0x0B	ue(v)
pic_order_cnt_type	0	ue(v)
log2_max_pic_order_cnt_lsb_minus4	0x0B	ue(v)
num_ref_frames	0x01	ue(v)
gaps_in_frame_num_value_allowed_flag	0	1
pic_width_in_mbs_minus1	(picWidth/16) -1)	ue(v)
pic_heigh_in_map_units_minus1	(picHeight/16) -1)	ue(v)
frame_mbs_only_flag	0x01	1
direct_8x8_inference_flag	0	1
frame_cropping_flag	0	1
vui_parameter_present_flag	0	1
rbsp_trailing_bits		Insert zero-valued bit(s) to 32-bit aligned

TABLE 15. TW5864 PPS RBSP SYNTAX

PIC_PARAMETER_SET_RBSP (NAL_UNIT_TYPE=8)		
pic_parameter_set_id	0	ue(v)
seq_parameter_set_id	0	ue(v)
entropy_coding_mode_flag	0	1
pic_order_present_flag	0	1
num_slice_groups_minus1	0	ue(v)
num_ref_idx_10_active_minus1	0	ue(v)
num_ref_idx_11_active_minus1	0	ue(v)
weighted_pred_flag	0	1
weighted_bipred_idc	0	2
pic_init_qp_minus26	qpbase-26	se(v)
pic_init_qs_minus26	qpbase-26	se(v)
chroma_qp_index_offset	0	se(v)
deblocking_filter_control_present_flag	0	1
constrained_intra_pred_flag	0	1
redundant_pic_cnt_present_flag	0	1
rbsp_trailing_bits		Insert zero-valued bit(s) to 32-bit aligned

Audio A/D Decoder and D/A Encoder

The audio A/D and D/A codec in the TW5864 is composed of five audio Analog-to-Digital converters, 1 Digital-to-Analog converter, audio mixer, digital serial audio interface and audio detector shown as shown in Figure 28. The TW5864 can accept 5 analog audio signals and 1 digital serial audio data and produce 1 mixing analog audio signal and 2 digital serial audio data.

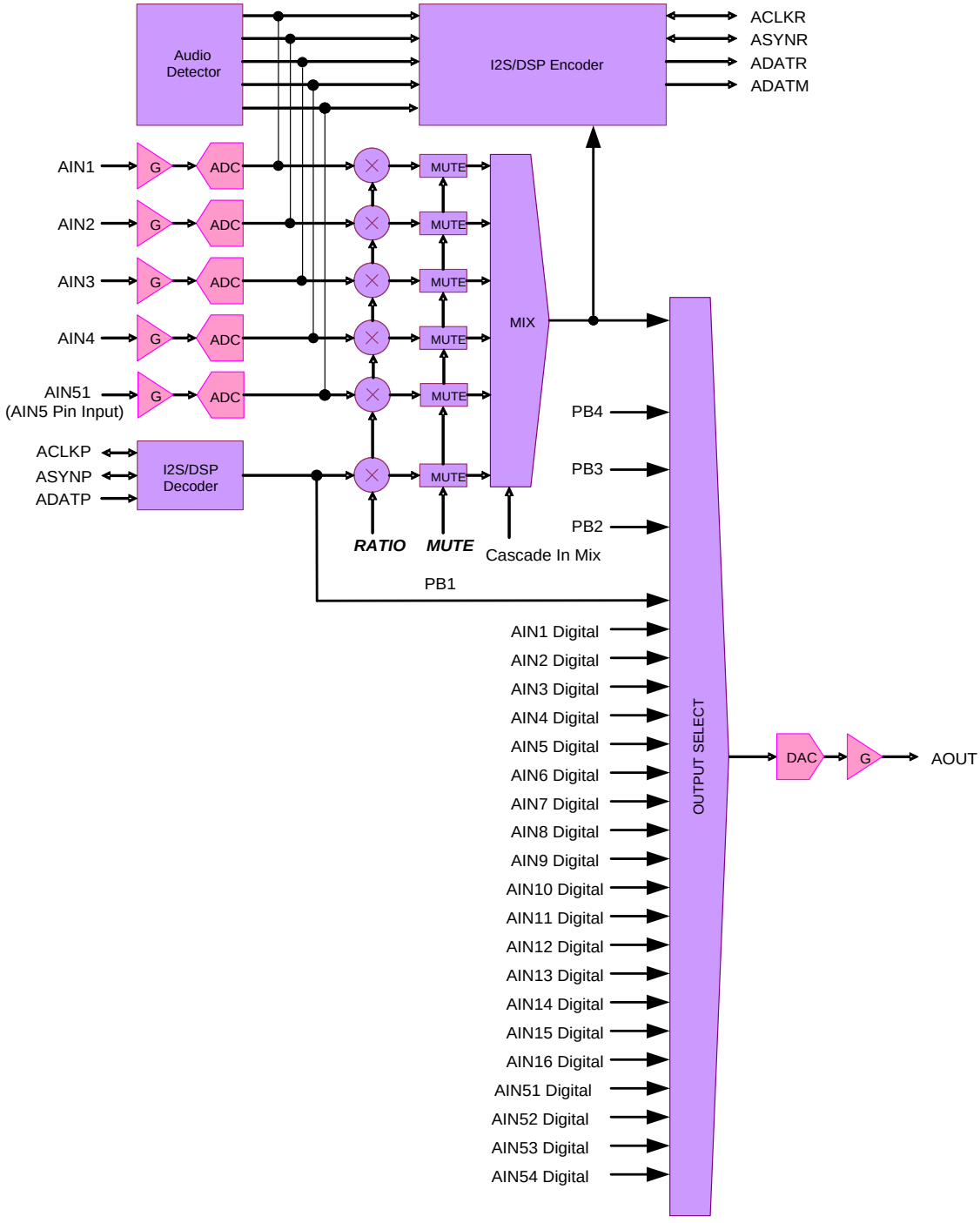
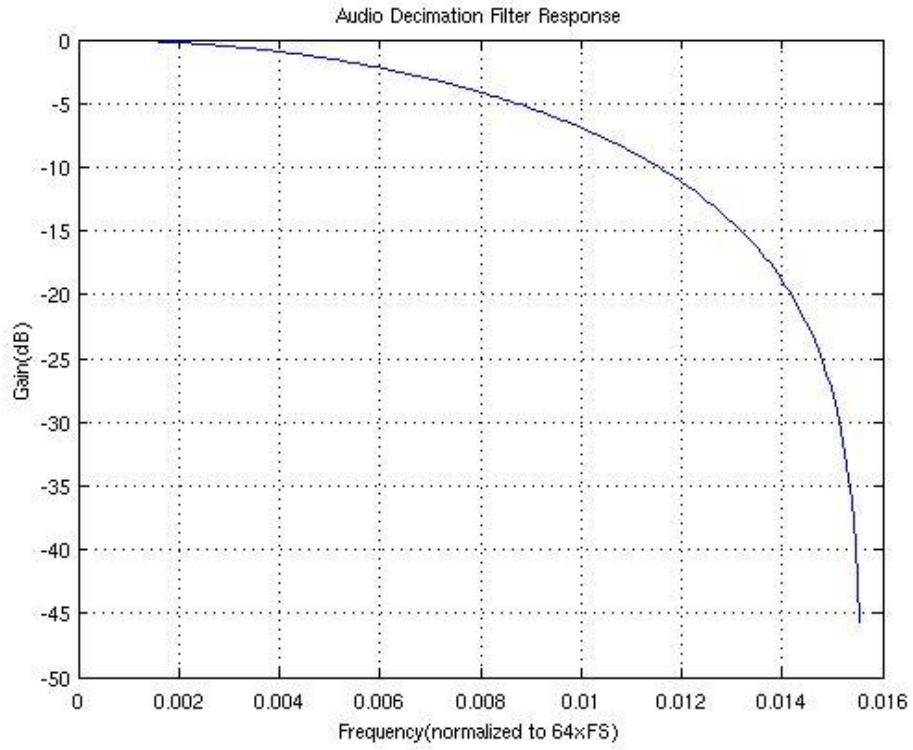


FIGURE 28. BLOCK DIAGRAM OF AUDIO CODEC

The level of analog audio input signal AIN1 ~ AIN5 can be adjusted respectively by internal programmable gain amplifiers that are defined via the AIGAIN1, AIGAIN2, AIGAIN3, AIGAIN4, and AIGAIN5 registers and then sampled by each Analog-to-Digital converters. Figure 29 shows the audio decimation filter response. The digital serial audio input data through the ACLKP, ASYNP and ADATP pin are used for playback function assuming an external audio decoder chip is used to decode the ADPCM audio bitstream. To record audio data, the TW5864 provides the digital serial audio output via the ACLKR, ASYNR and ADATR port, and feed into the back-end ADPCM audio encoding module.

The TW5864 can mix all of audio inputs including analog audio signal and digital audio data according to the predefined mixing ratio for each audio via the MIX_RATIO1 ~ MIX_RATIO5 and MIX_RATIOP registers. This mixing audio output can be provided through the analog and digital interfaces. The embedded audio Digital-to-Analog converter supports the analog mixing audio output whose level can be controlled by programmable gain amplifier via the A_DAC_IBCTL register. The ADATM pin supports the digital mixing audio output and its digital serial audio timings are provided through the ACLKR and ASYNR ports that are shared with the digital serial audio record timing pins.



(*) 0.016 line = 0.016x64xFs

FIGURE 29. AUDIO DECIMATION FILTER RESPONSE

AUDIO DETECTION

The TW5864 has an audio detector for each individual of 5 channels. There are 2 kinds of audio detection method defined by the ADET_MTH. One is the detection of absolute amplitude and the other is of differential amplitude. For both detection methods, the accumulating period is defined by the ADET_FILT register and the detecting threshold value is defined by ADET_TH1 ~ ADET_TH5 registers. The status for audio detection is read by the STATE_AVDET register and it also makes the interrupt request through the IRQ pin with the combination of the status for video loss detection.

SERIAL AUDIO INTERFACE

There are 3 kinds of digital serial audio interfaces in the TW5864, the first is a recording output, the second is a mixing output and the third is a playback input. These 3 digital serial audio interfaces follow a standard I2S or DSP interface as shown in the Figure 30.

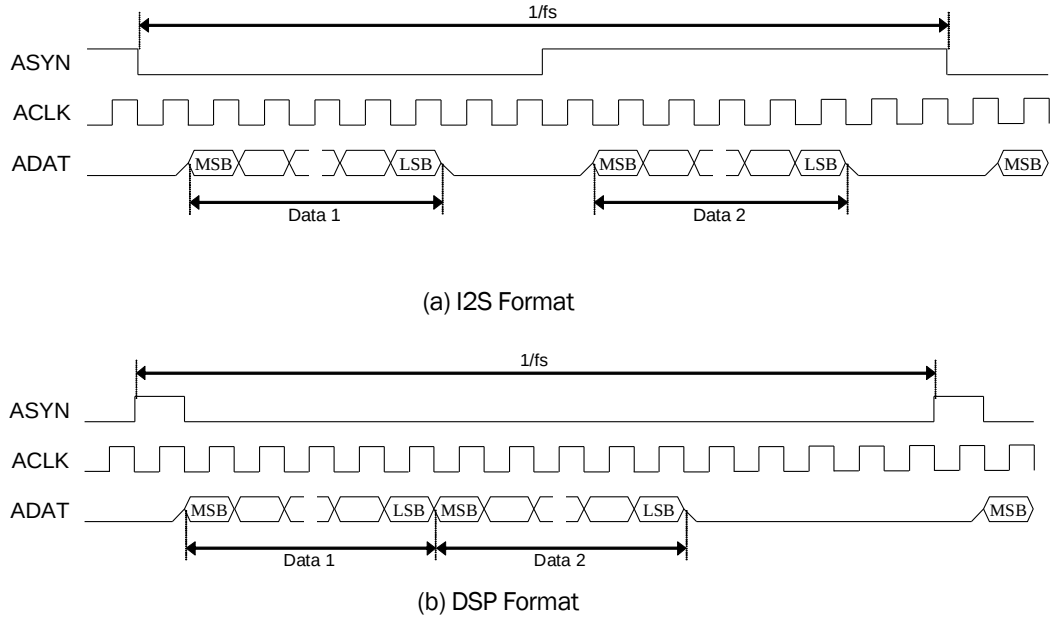


FIGURE 30. TIMING CHART OF SERIAL AUDIO INTERFACE

Playback Input

The serial interface using the ACLKP, ASYNP and ADATP pins accepts the digital serial audio data for the playback purpose. The ACLKP and ASYNP pins can be operated as master or slave mode. For master mode, these pins work as output pin and generate the standard audio clock and synchronizing signal. For slave mode, these pins are input mode and accept the standard audio clock and synchronizing signal. The ADATP pin is always input mode regardless of operating mode. In order to use the on-chip ADPCM decoder, the playback port has to run at the master mode. One of audio data in left or right channel should be selected for playback audio by the PB_LRSEL.

Record Output

To record audio data, the TW5864 provides the digital serial audio data through the ACLKR, ASYNR and ADATR ports. Sampling frequency comes from 256xfs, 320xfs, or 384xfs audio system clock setting. Even though the standard I2S and DSP format can have only 2 audio data on left and right channel, the TW5864 can provide an extended I2S and DSP format which can have 16-channel audio data through ADATR pin. The R_MULTCH defines the number of audio data to be recorded by the ADATR pin. ASYNR signal is always fs frequency rate. One ASYNR period is always equal to 256xACLKR clock length with AIN5MD=0. Figure 31 shows the digital serial audio data organization for multi-channel audio.

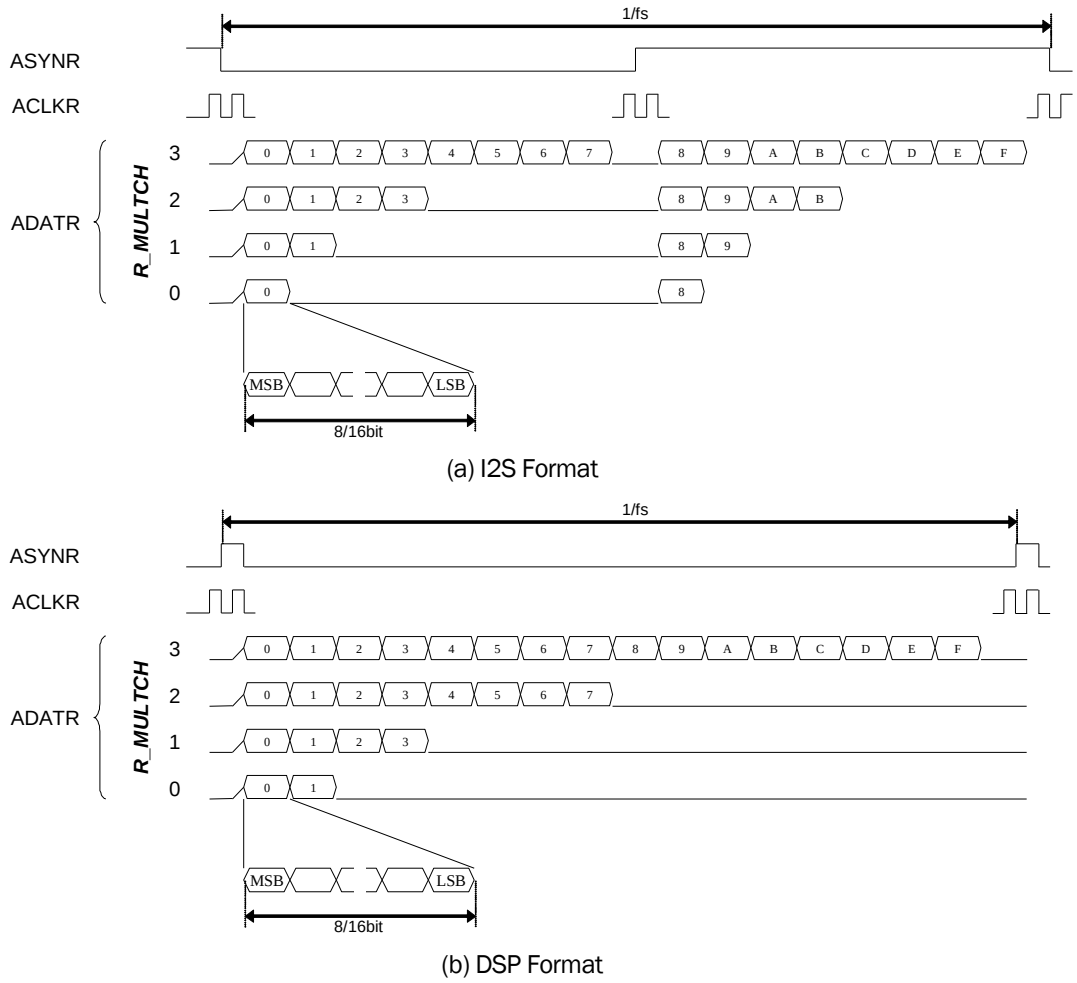


FIGURE 31. TIMING CHART OF MULTI-CHANNEL AUDIO RECORD

The following table shows the sequence of audio data to be recorded for each mode of the R_MULTCH register. The sequences of 0 ~ F do not mean actual audio channel number but represent sequence only. The actual audio channel should be assigned to sequence 0 ~ F by the R_SEQ_0 ~ R_SEQ_F register. When the ADATM pin is used for record via the R_ADATM register, the audio sequence of ADATM is shown also in Table 16.

TABLE 16. SEQUENCE OF MULTI-CHANNEL AUDIO RECORD
(A) I2S FORMAT

R_MULTCH	PIN	LEFT CHANNEL								RIGHT CHANNEL							
0	ADATR	0								8							
	ADATM	F								7							
1	ADATR	0	1							8	9						
	ADATM	F	E							7	6						
2	ADATR	0	1	2	3					8	9	A	B				
	ADATM	F	E	D	C					7	6	5	4				
3	ADATR	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
	ADATM	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0

(B) DSP FORMAT

R_MULTCH	PIN	LEFT/RIGHT CHANNEL															
0	ADATR	0	1														
	ADATM	F	E														
1	ADATR	0	1	2	3												
	ADATM	F	E	D	C												
2	ADATR	0	1	2	3	4	5	6	7								
	ADATM	F	E	D	C	B	A	9	8								
3	ADATR	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
	ADATM	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0

Mix Output

The digital serial audio data on the ADATM pin has 2 different audio data which are mixing audio and playback audio. The mixing digital serial audio data is the same as analog mixing output. The sampling frequency, bit width and number of audio for the ADATM pin are same as the ADATR pin because the ACLKR and ASYNR pins are shared with the ADATR and ADATM pins.

AUDIO MULTI-CHIP CASCADE

TW5864 can output 16 channel audio data on ACLKR/ASYNR/ADATR to the back-end ADPCM module simultaneously. Therefore, up to 3 external TW2866 chips can be connected on most multi-Chip application cases. ALINKI pin is the audio cascade serial input, and ALINKO pin is the audio cascade serial output.

Each stage chip can accept 5 analog audio signals so that four cascaded chips will be 16-channel audio controller as default AIN5MD=0. The first stage chip provides 16ch digital serial audio data for record. Even though the first stage chip has only 1 digital serial audio data pin ADATR for record, the TW5864 can generate 16 channel data simultaneously using multi-channel format. Also, each stage chip can support 4 channel record outputs that are corresponding with analog audio inputs. This first stage chip can also output 16 channels mixing audio data by the digital serial audio data and analog audio signal. The last stage chip accepts the digital serial audio data for playback. The digital playback data can be converted to analog signal by Digital-to-Analog Converter in the last stage chip.

In Multi-Chip Audio operation mode, one same Oscillator clock source (27 MHz) needs to be connected to all TW5864 XTI or TW2866 CLKI pins.

Several Master/Slave mode configurations are available. The Figure 32 shows the most recommended and demanded system with Clock Master Mode (ACLKRMASTER=1).

In each of the following figures, Mix1-16-51-54/Pb1 means Mix output of AIN1-16, AIN51-AIN54, and Playback1. AIN1-16-51-54/Pb1 means one selected Audio output in AIN1-16-51-54/Pb1.

If one TW5864 uses AIN5MD=1, all other cascaded TW2866 chips must set up AIN5MD=1 also. Generally, 4 audio input mode (AIN5MD=0) are most used in this cascade system.

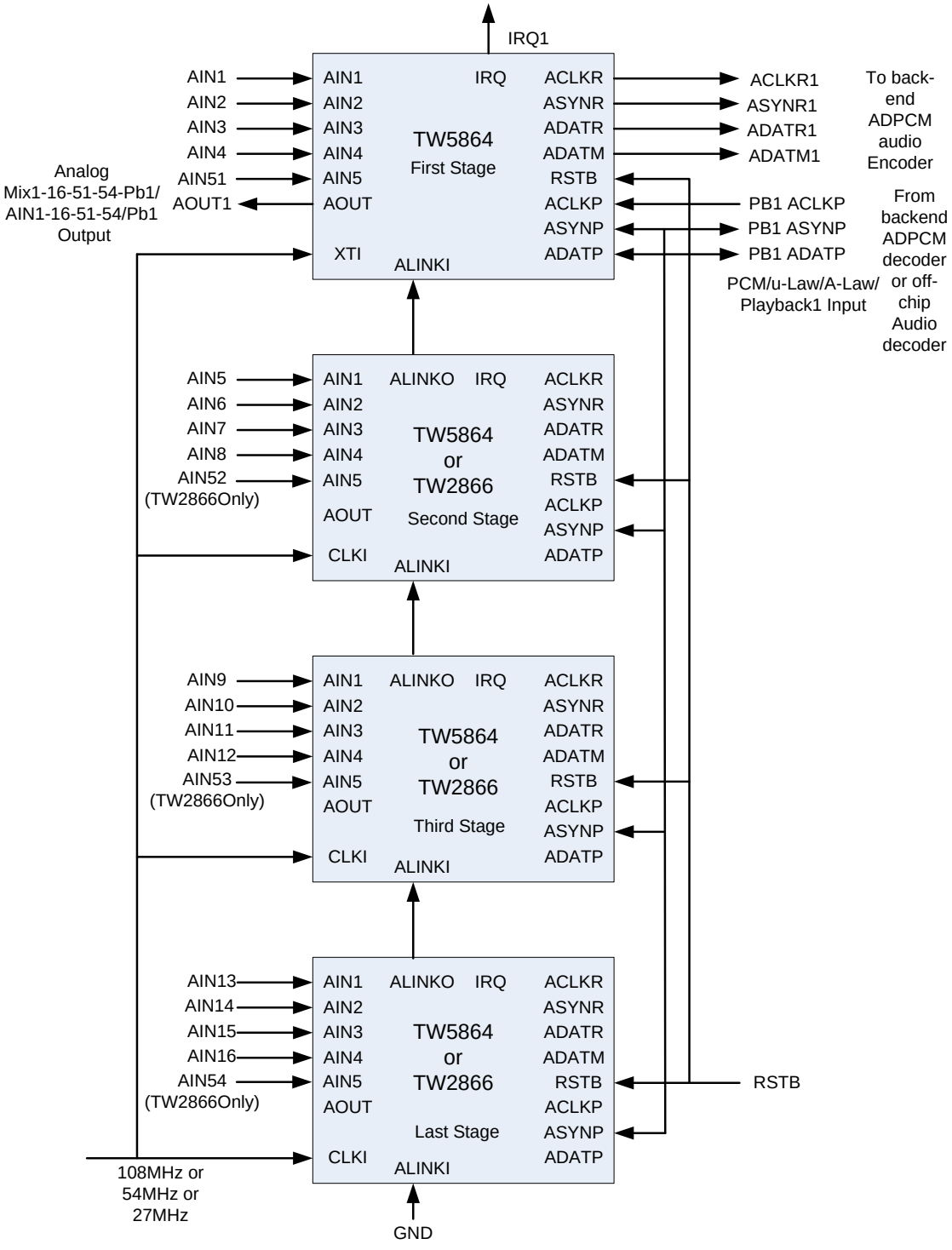


FIGURE 32. RECOMMENDED CLOCK MASTER CASCADE MODE SYSTEM WITH ACLKRMASTER=1

ACLKP/ASYNP SLAVE MODE DATA OUTPUT TIMING

The following 8 data input timing figures are supported. The ADATPDLY register needs to be set up according to the difference of ADATP data input timings. Data1 is only used as default. MSB bit is the first input bit as default PBINSWAP=0. If PBINSWAP=1, LSB bit is the first input bit.

ASYNP is ACLKP Falling Edge Triggered Input

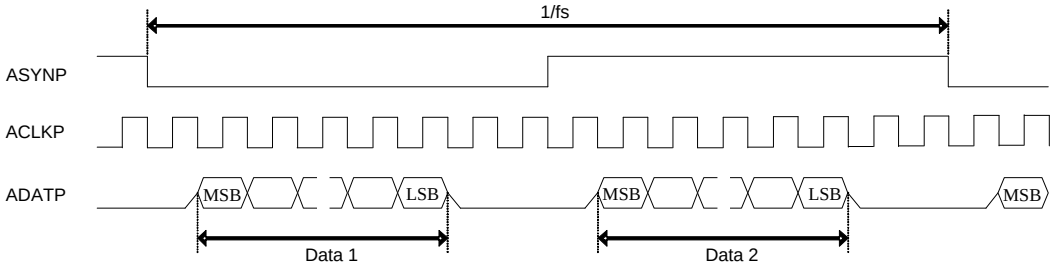


FIGURE 33. AUDIO PLAYBACK FALLING EDGE TRIGGERED INPUT TIMING, RM_SYNC=0, PB_MASTER=0, ADATPDLY=0

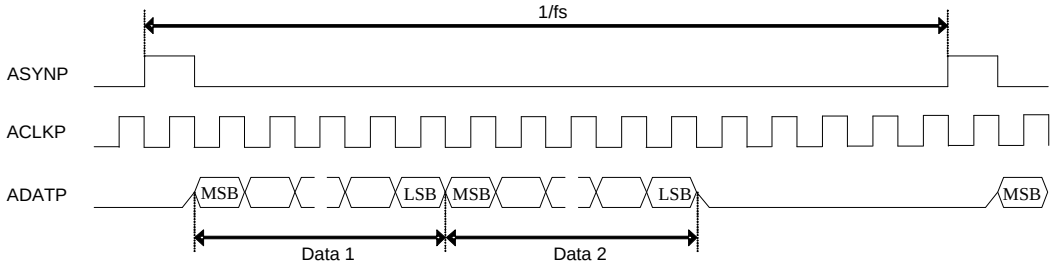


FIGURE 34. AUDIO PLAYBACK FALLING EDGE TRIGGERED INPUT TIMING, RM_SYNC=1, PB_MASTER=0, ADATPDLY=0

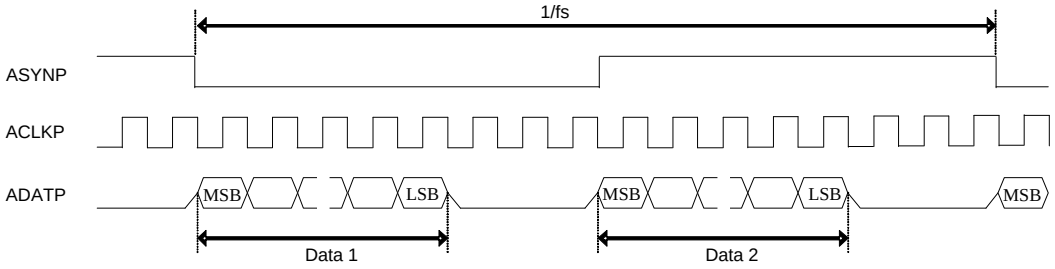


FIGURE 35. AUDIO PLAYBACK FALLING EDGE TRIGGERED INPUT TIMING, RM_SYNC=0, PB_MASTER=0, ADATPDLY=1

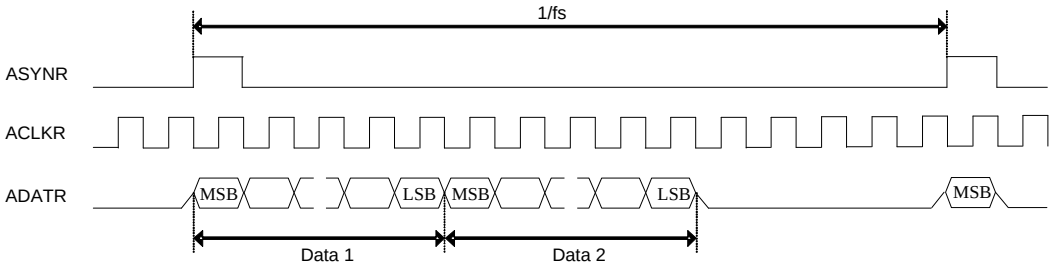


FIGURE 36. AUDIO PLAYBACK FALLING EDGE TRIGGERED INPUT TIMING, RM_SYNC=1, PB_MASTER=0, ADATPDLY=1

ASYNP is ACLKP Rising Edge Triggered Input

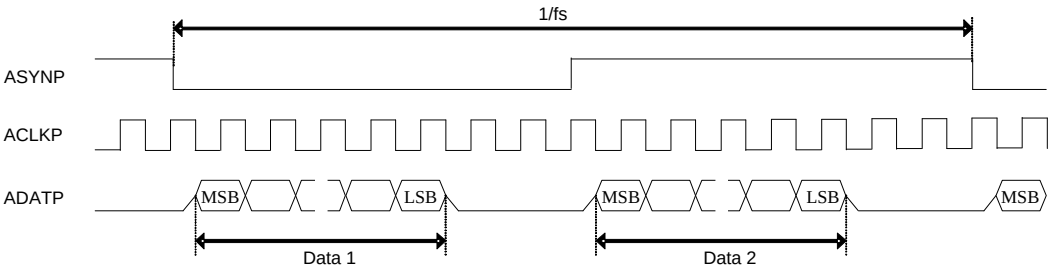


FIGURE 37. AUDIO PLAYBACK RISING EDGE TRIGGERED INPUT TIMING, RM_SYNC=0, PB_MASTER=0, ADATPDLY=1

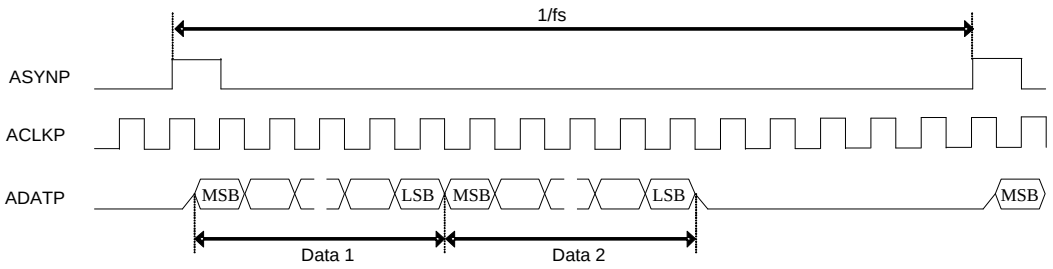


FIGURE 38. AUDIO PLAYBACK RISING EDGE TRIGGERED INPUT TIMING, RM_SYNC=1, PB_MASTER=0, ADATPDLY=1

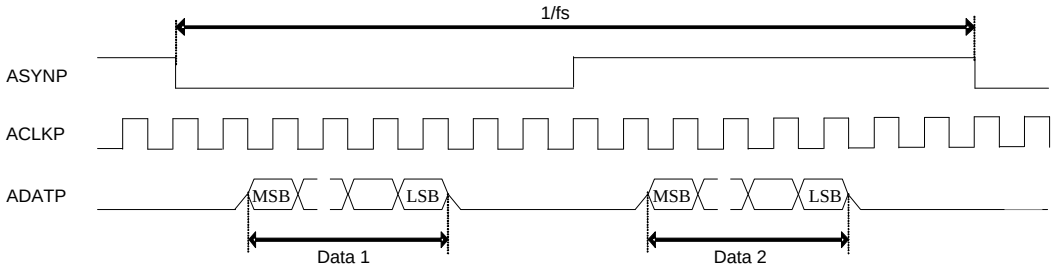


FIGURE 39. AUDIO PLAYBACK RISING EDGE TRIGGERED INPUT TIMING, RM_SYNC=0, PB_MASTER=0, ADATPDLY=0

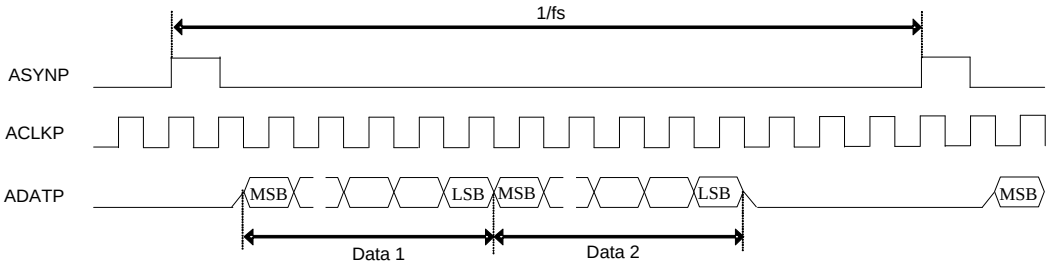


FIGURE 40. AUDIO PLAYBACK RISING EDGE TRIGGERED INPUT TIMING, RM_SYNC=1, PB_MASTER=0, ADATPDLY=0

AUDIO CLOCK GENERATION

TW5864 has built-in field locked audio clock generator for use in video capture applications. The circuitry will generate the same predefined number of audio sample clocks per field to ensure synchronous playback of video and audio after digital recording or compression. The audio clock is digitally synthesized from the crystal clock input. The master audio clock frequency is programmable through ACKN and ACKI register based following two equations.

ACKN = round (F AMCLK / F field), it gives the Audio master Clock per Field.

ACKI = round (F AMCLK / F 27MHz * 2^23), it gives the Audio master Clock Nominal increment.

Following table provides setting example of some common used audio frequency assuming Video Decoder system clock frequency of 27MHz. If ACLKRMASTER register bit is set to 1, following AMCLK is used as audio system clock inside TW5864.

If Slave Playback-in lock mode is required, ACKN=00100hex and PBREFEN=1 needs to be set up. The number of AMCLK clock per one ASYNP input cycle is locked (fixed) to 256 in this mode.

Frequency equation is “AMCLK (Freq) = 256 x ASYNP (Freq)”.

TABLE 17. AUDIO FREQUENCY 256XFS MODE: AIN5MD = 0, AFS384 = 0

AMCLK(MHZ)	FIELD[HZ]	ACKN [DEC]	ACKN [HEX]	ACKI [DEC]	ACKI [HEX]
256 X 48 KHZ					
12.288	50	245760	3-C0-00	3817749	3A-41-15
12.288	59.94	205005	3-20-CD	3817749	3A-41-15
256 X 44.1KHZ					
11.2896	50	225792	3-72-00	3507556	35-85-65
11.2896	59.94	188348	2-DF-BC	3507556	35-85-65
256 X 32 KHZ					
8.192	50	163840	2-80-00	2545166	26-D6-0E
8.192	59.94	136670	2-15-DE	2545166	26-D6-0E
256 X 16 KHZ					
4.096	50	81920	1-40-00	1272583	13-6B-07
4.096	59.94	68335	1-0A-EF	1272583	13-6B-07
256 X 8 KHZ					
2.048	50	40960	A0-00	636291	9-B5-83
2.048	59.94	34168	85-78	636291	9-B5-83

TABLE 18. AUDIO FREQUENCY 320XFS MODE: AIN5MD = 1, AFS384 = 0, 44.1/ 48 KHZ NOT SUPPORTED

AMCLK(MHZ)	FIELD[HZ]	ACKN [DEC]	ACKN [HEX]	ACKI [DEC]	ACKI [HEX]
320 X 32 KHZ					
10.24	50	204800	3-20-00	3181457	30-8B-91
10.24	59.94	170838	2-9B-56	3181457	30-8B-91
320X16 KHZ					
5.12	50	102400	1-90-00	1590729	18-45-C9
5.12	59.94	85419	1-4D-AB	1590729	18-45-C9
320 X 8 KHZ					
2.56	50	51200	C8-00	795364	C-22-E4
2.56	59.94	42709	A6-D5	795364	C-22-E4

TABLE 19. AUDIO FREQUENCY 384XFS MODE: AIN5MD = 0, AFS384 = 1, 44.1/48 KHZ NOT SUPPORTED

AMCLK(MHZ)	FIELD[HZ]	ACKN [DEC]	ACKN [HEX]	ACKI [DEC]	ACKI [HEX]
384 X 32 KHZ					
12.288	50	245760	3-C0-00	3817749	3A-41-15
12.288	59.94	205005	3-20-CD	3817749	3A-41-15
384X16 KHZ					
6.144	50	122880	1-E0-00	1908874	1D-20-8A
6.144	59.94	102503	1-90-67	1908874	1D-20-8A
384 X 8 KHZ					
3.072	50	61440	F0-00	954437	E-90-45
3.072	59.94	51251	C8-33	954437	E-90-45

AUDIO CLOCK AUTO SETUP

If ACLKRMASTER=1 audio clock master mode is selected, and AFAUTO register is set to “1”,TW5864 set up ACKI register by AFMD register value automatically. ACKI control input in ACKG module block is automatically set up to the required value by the condition of AIN5MD and AFS384 register value.

TABLE 20. AUDIO FREQUENCY AUTO SETUP

AFAUTO	AFMD	ACKG MODULE ACKI CONTROL INPUT VALUE
1	0	8kHz mode value by each AIN5MD/AFS384 case.
1	1	16kHz mode value by each AIN5MD/AFS384 case.
1	2	32kHz mode value by each AIN5MD/AFS384 case.
1	3	44.1kHz mode value by each AIN5MD/AFS384 case.
1	4	48kHz mode value by each AIN5MD/AFS384 case.
0	X	ACKI register set up ACKI control input value.

Audio Encoding / Decoding

TW5864 provides a simple ADPCM G.726 hardware CODEC, mainly for speech coding purpose. It is used to map a series of 8-bit u-law (or a-low) PCM samples into a series of 4-bit ADPCM samples.

The ADPCM encoder takes the I2S format audio samples from the on-chip front-end audio analog decoder as well as the off-chip audio input through the I2S input ports. The ADPCM encoder is capable of encoding 17 audio channels simultaneously.

The ADPCM decoder decodes the 4-bit samples back into the I2S format, and drives the on-chip audio DAC to drive the external speaker or pre-amplifier for playback purpose. The decoder can decode only 1 audio channel at a time.

Host Interfaces

TW5864 supports two types of host interfaces, through which external processors control and interact with TW5864 for configuration and data transfer. One is through the standard asynchronous memory bus interface, and the other is through the PCI interface working at either the target or the initiator mode, depending on the operation. While using as a PC card, the PCI interface is always used. In an embedded system, either asynchronous host interface or the PCI interface can be used. TW5864 has the same registers map for these two interfaces so that the firmware on embedded platform does not need to differentiate which interface is in use except the bus control modules in TW5864 driver.

These two interfaces share some common I/O pins, and can only be used exclusively. The interrupt signal is also shared for both PCI and the asynchronous interface.

The host interface supports several modes: single read / write access, burst read / write access, DDR burst read / write, and PCI initiator write access.

PCI INTERFACE

The PCI module in TW5864 will work both as an initiator and target. It is an initiator when it is sending the preview, h264 and audio coded streams to host PC. It is in target mode when PC host is configuring the registers and programming the chip. The PCI interface supports both 33MHz and 66MHz operation.

Single Read/Write Access

Similar to the asynchronous host interface, the TW5864 PCI interface supports the single read/write operation. The address space mapping and the entire indirect access / DDR memory page are used the same way as the asynchronous host interface. Similarly to the asynchronous host interface, the single R/W access runs in the PCI target mode, which makes the TW5864 a slave device to the external MCU.

Target Burst Read

The PCI target burst read of TW5864 allows the external MCU to burst read a whole block of data of a continuous address space from TW5864. This target burst read function is only used to access the TW5864 on-chip double buffer A. The double buffer A is only used for DMA movement between the external DDRs and TW5864.

In order to burst read a space of an external DDR memory, a DMA operation is started to read data from external DDR into the double buffer A. The MCU then issues target burst read operation to read data from the double buffer A into the MCU.

A DMA write operation to the external DDR is supported. However the TW5864 does not support PCI target burst write operation. The MCU has to fill data into the double buffer A through multiple single write operation. Once the double buffer A is filled, a DMA write operation is started to write the data in double buffer A into the external DDR.

Master Burst Write

The TW5864 PCI interface can act as a PCI initiator to burst write a block of data automatically into the memory space of the external MCU. This master burst write function is used by several modules – H264 encoder, the audio ADPCM encoder, and the PCI preview module. When this mode is used, the bitstreams or data sent by each module does not go through the external DDR. They are sent from each module into a buffer for each path, and push into the external MCU memory space.

ASYNCHRONOUS INTERFACE

In addition to the PCI host interface, TW5864 also support commonly used Asynchronous Interface. The most commonly used ARM and PPC processors are supported. The data width can be either 16 bit or 32bit.

Asynchronous host interface only supports single access read and write operation. Using this interface, the TW5864 is always slave to the external MCU. The MCU issue single word read/write operation to access all registers / memory space inside the address map.

The address space of this asynchronous host interface is the same as the PCI interface. It includes all the on-chip registers, a page of space mapped for the external DDR_A and DDR_B, and an indirect access mechanism to read/write the registers at the front-end video / audio decoder registers and external preview multiplexing control registers.

The external DDRs are mapped into a page of address space through a page select register. Each page is 16 Kbytes. The page select register select a page area in either of the external DDRs such that accessing to this address space is equivalent to access the external DDR directly.

Some front-end registers related to embedded video decoder / audio decoder / preview multiplexing previews are accessed through indirect access through the registers 0xB800 ~ 0xB80C.

Although the asynchronous host interfaces only support single word read / writes operation, a block move is possible as long as the external MCU has a DMA controller to access a block of address space continuously though multiple single access automatically.

External DRAM Interface

TW5864 uses two external DDR SDRAMs for various functions. The memory controller of the TW5864 supports 16-bit data width up to 166 MHz clock rate. The memory capacity is 256 Mbytes. The capacity used depends on the feature used on TW5864. If the TW5864 is used for 4 D1 / 16 CIF configuration, and minimum capacity of 256 Mbytes can be used. If, however, a 16 non-real-time D1 configuration is used, a much bigger video frame buffer is needed. At this time DDR of 1 Bytes of memory is needed.

When the chip is powered up, the CPU is responsible for setting all the on-chip configuration registers for DDR memory configuration. Once the registers are set, the CPU releases the software reset signal, then the DDR memory controller initializes the DDR memory configuration using the parameters in the registers. After the initialization is done, the DDR memory is ready for use. After the initialization, the memory controller does the memory refresh automatically.

HW Operation Flow

The key data paths on TW5864 for various encoding and decoding functions are illustrated in Figure 41. The HW operational flow for the four major functions (H.264, JPWG, Audio, Preview) in TW5864 will be described in detail subsequently.

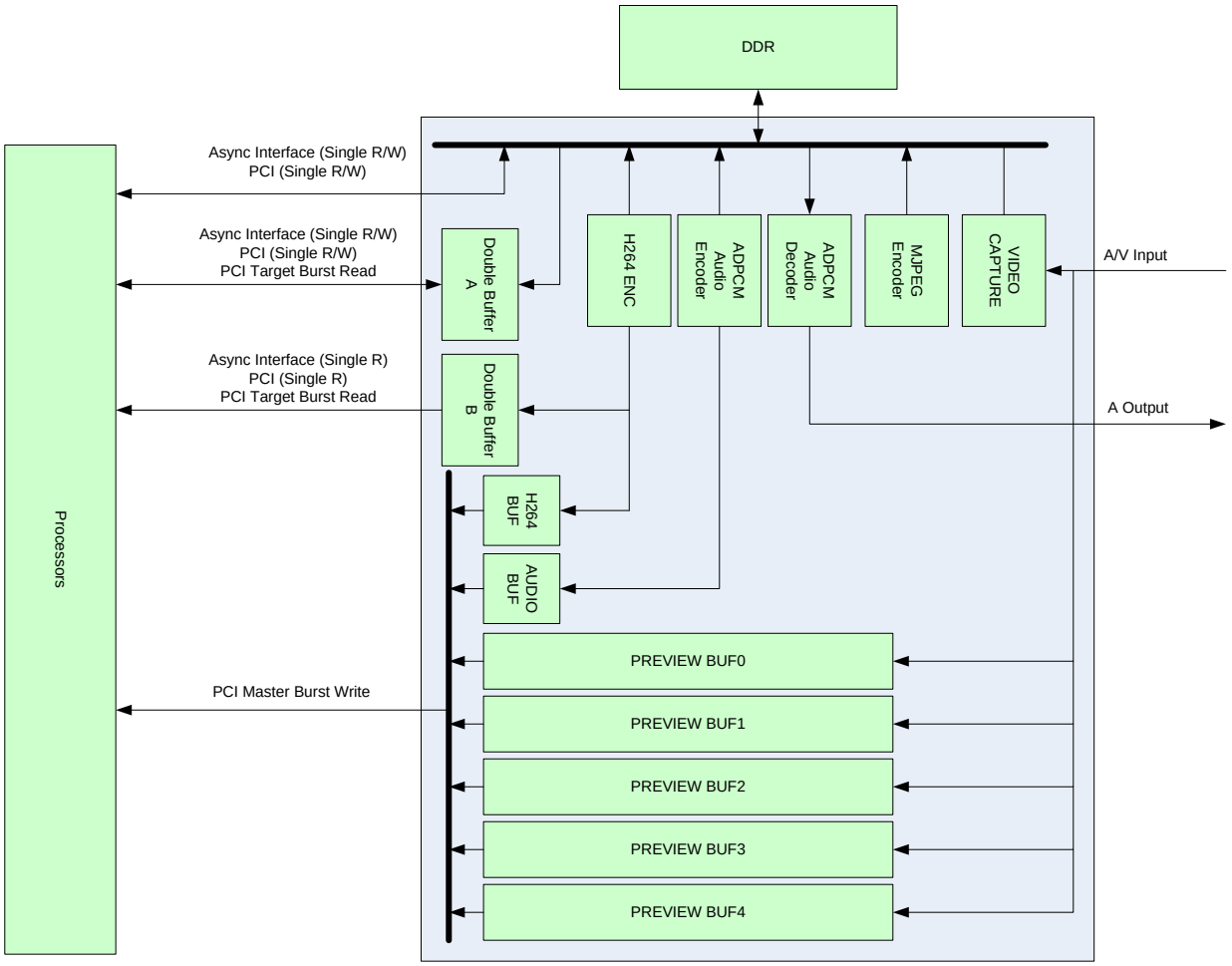


FIGURE 41. TW5864 HW DATA FLOW

H264 Encoding Data Flow

The H264 encoding data flow on TW5864 is shown in the figure below. The video data are captured into the external DDR memory by the video capture module. All the previous encoded reference frames are also stored in the DDR. From there, the H264 encoder generates the reference frame pixels for used for future use into the external DDR. The encoded VLC bitstream is either stored back into DDR, or simply write into the double buffer B.

When the VLC bitstream is stored in the DDR, the external MCU instruct the on-chip DMA module to move the data from external DDR into the double buffer A, from which the external MCU can perform single read or PCI target burst read to move the data from double buffer A into the MCU memory space.

When the VLC bitstream is stored in the double buffer B, the external MCU simply read the bitstream from this data buffer through either single read or PCI target burst read.

With the coded VLC stream in DDR, the MCU has more flexibility in performing the data movement. While if the codec VLC stream is stored in double buffer B, the MCU has to attend to read the data stream quickly to make sure the buffer is not over flown.

When PCI master mode is used, the encoded VLC stream can be pushed into the MCU memory space automatically, as shown in the green arrow below.

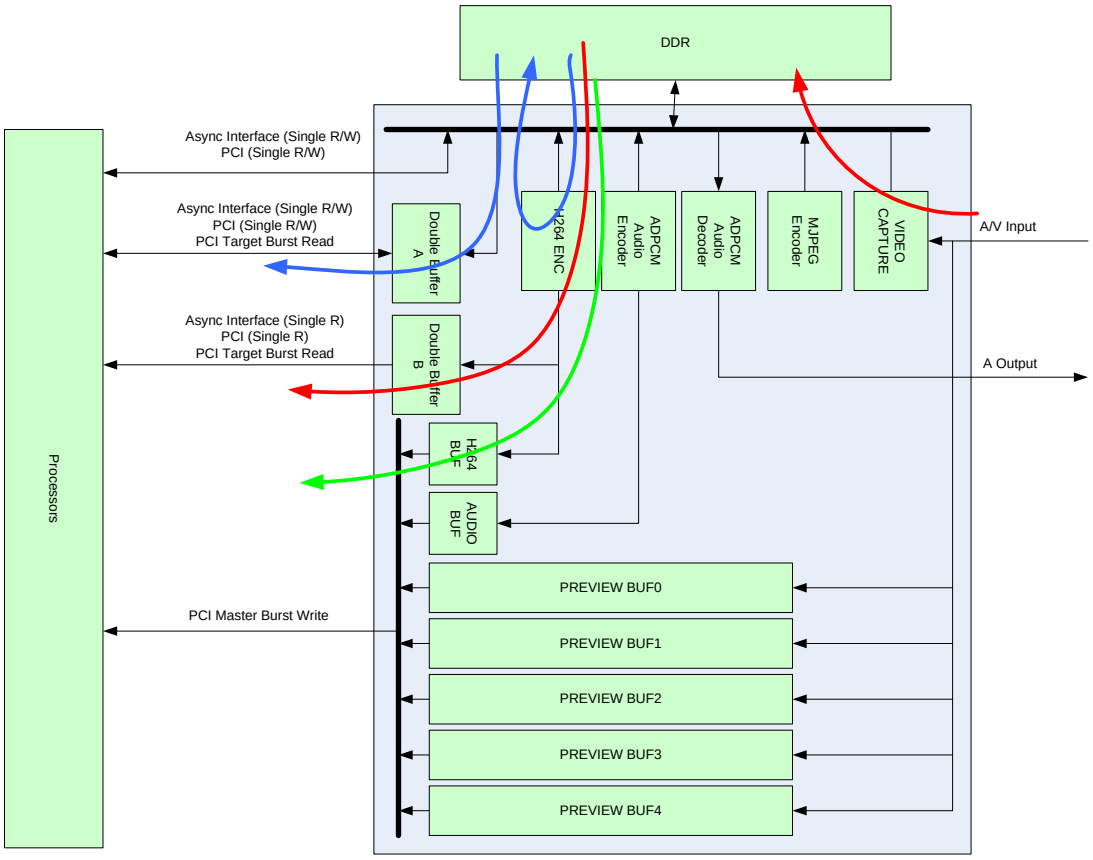


FIGURE 42. H264 ENCODING DATA FLOW

MJPEG Encoding Data Flow

TW5864 MJPEG encoder always encodes the frames/fields back into the DDR memory.

The only way MCU fetch the encoded bitstream is through the double buffer A.

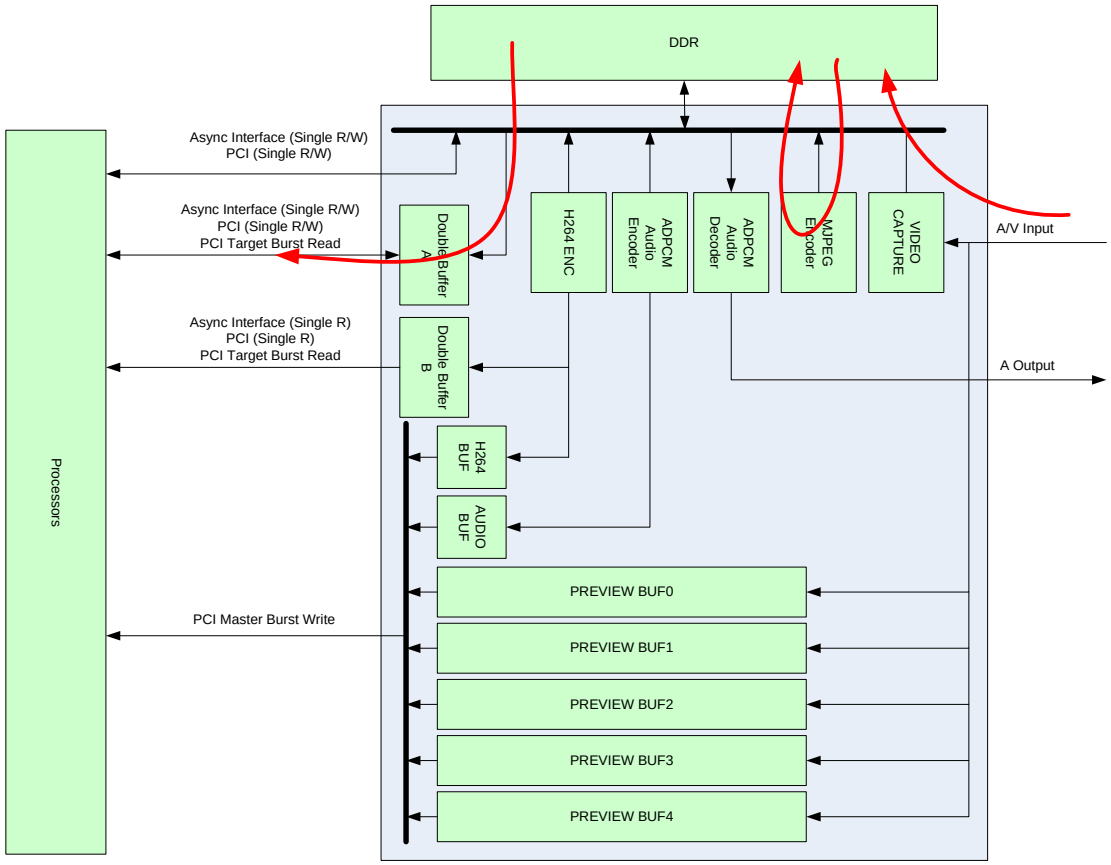


FIGURE 43. MJPEG ENCODING DATA FLOW

ADPCM Encoding Data Flow

Audio ADPCM coded bitstream can be fetched either through the external DDR, or it can be pushed into the audio buffer when PCI master mode is used.

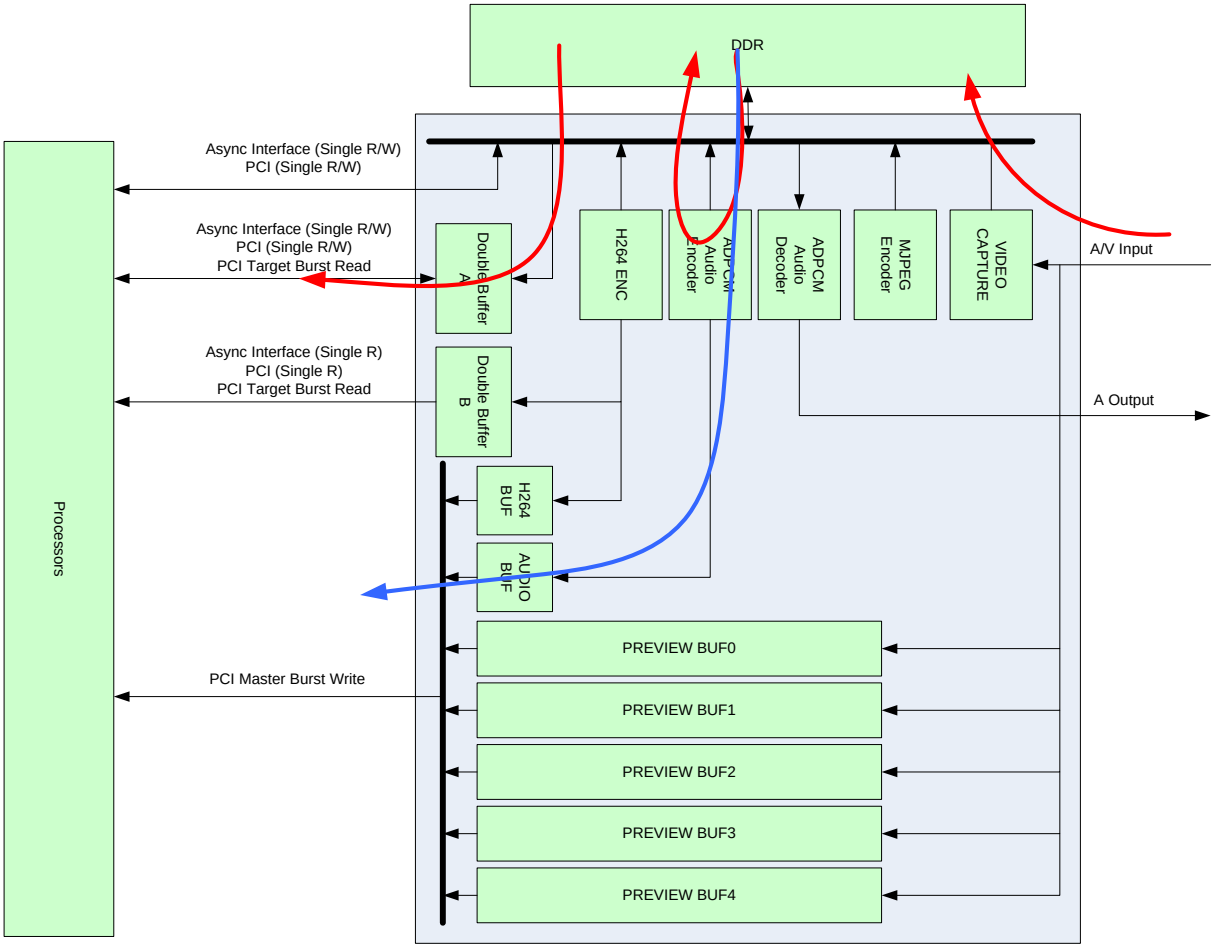


FIGURE 44. ADPCM ENCODING DATA FLOW

ADPCM Decoding Data Flow

Audio ADPCM decoder bitstream can be put into the DDR through either double buffer A, or just through single access read/write of external DDR through page mode mapping. Once the bitstream is in the DDR, the ADPCM decoder can be started to decode and output audio samples through I2S interface.

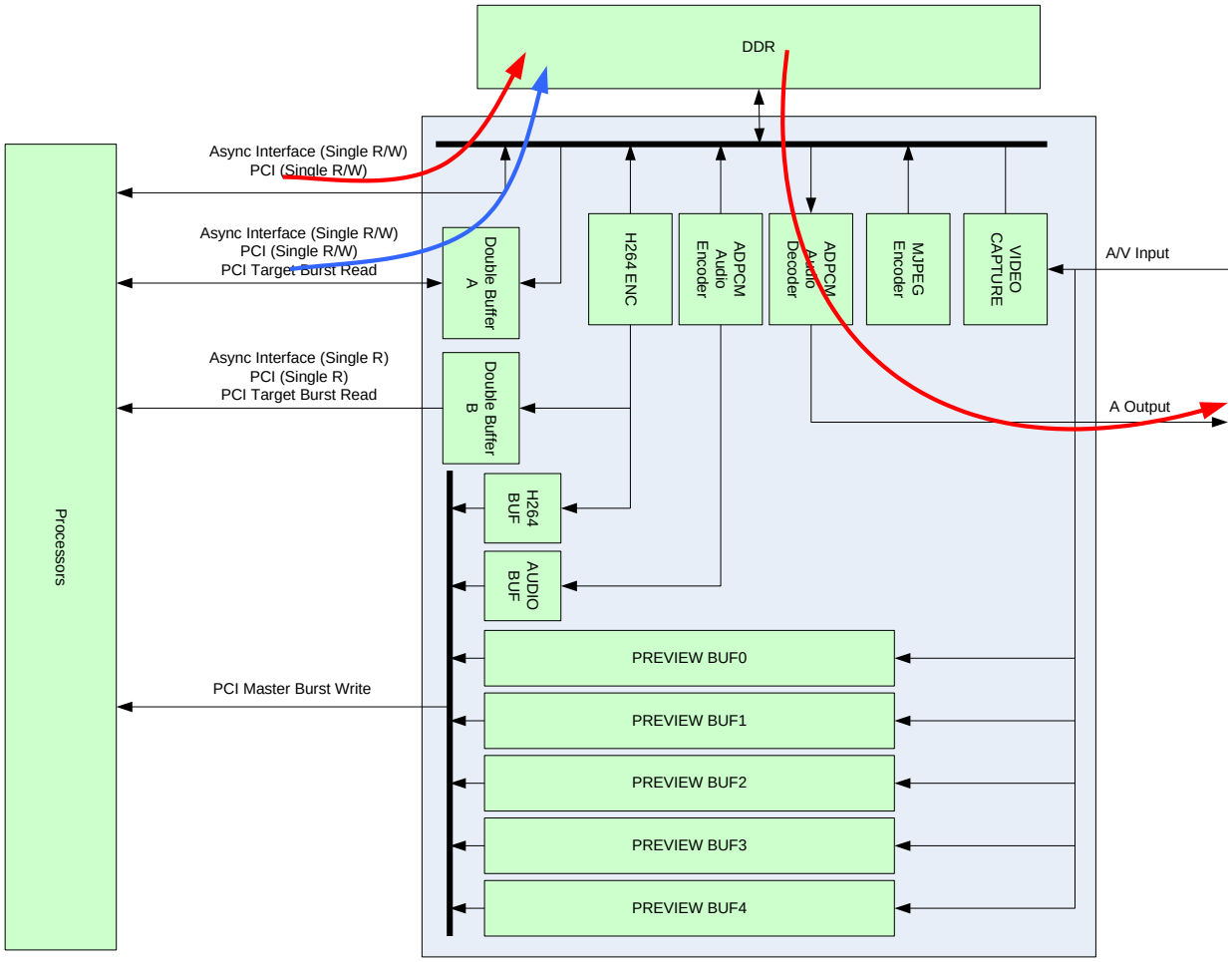


FIGURE 45. ADPCM DECODING DATA FLOW

PCI Preview Data Flow

TW5864 PCI preview path only allows data to push into the external MCU memory space through PCI master mode. The data does not go through the external DDR memory.

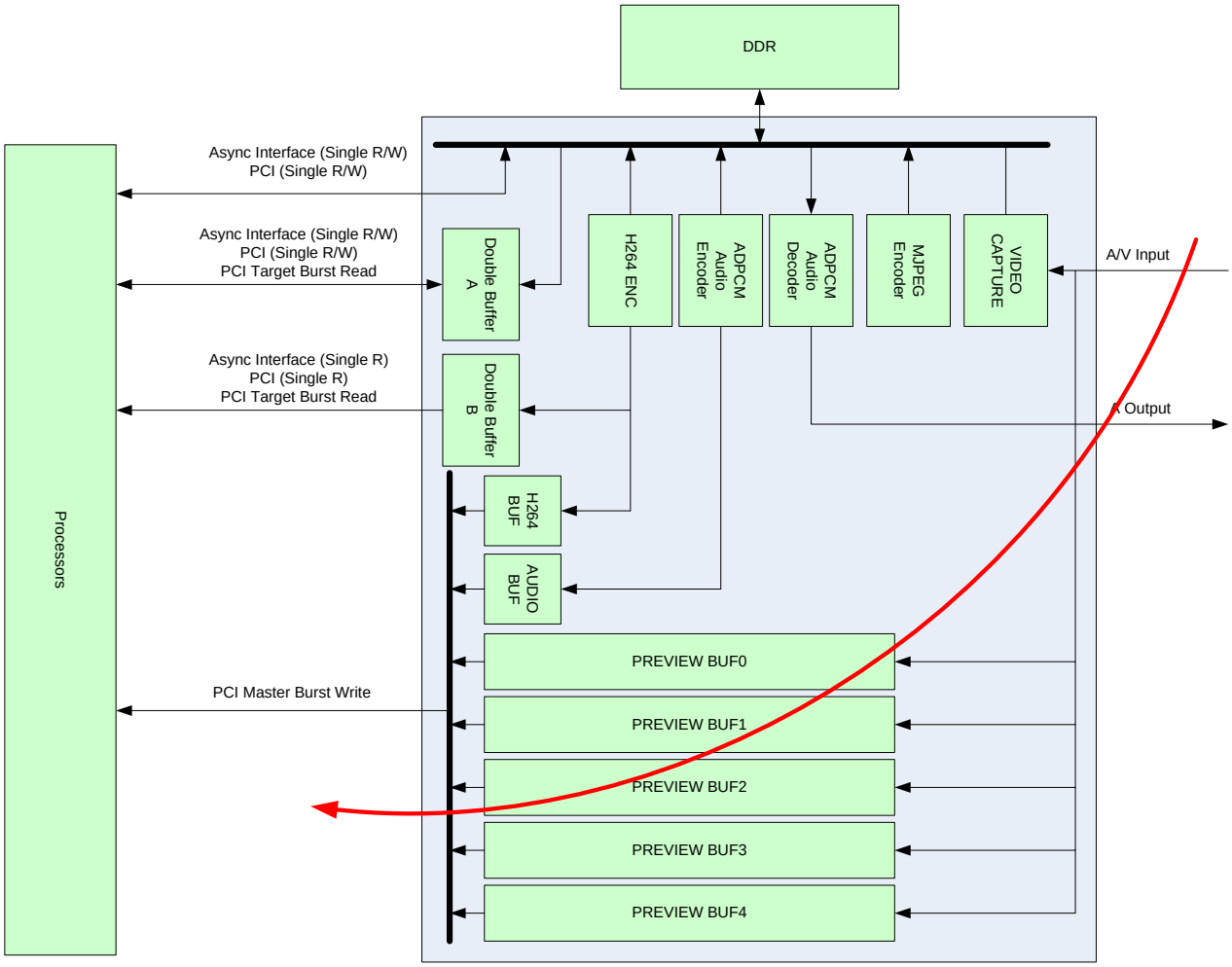


FIGURE 46. PCI PREVIEW PIXEL DATA FLOW

Register Description – Direct Map Space

0x0000 ~ 0x1FFC -- H264 Register Map

Address	[15:0]
0x0000	H264REV

H264REV — The Version register for H264 core (Read Only)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0004	DSP_FRAME_TYPE		EMU_EN_PLBK	EMU_EN_LPF	EMU_EN_BHOST	EMU_EN_SEN	EMU_EN_ME	EMU_EN_DDR

EMU_EN_DDR — DDR controller enabled

EMU_EN_ME — Enable bit for Inter module

EMU_EN_SEN — Enable bit for Sensor Interface module

EMU_EN_BHOST — Enable bit for Host Burst Access

EMU_EN_LPF — Enable bit for Loop Filter module

EMU_EN_PLBK — Enable bit for PLBK module

DSP_FRAME_TYPE — Video Frame mapping in DDR
00 CIF
01 D1
10 Reserved
11 Reserved

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x000C	RESERVED			MAS_SLICE_END	RESERVED			VLC_SLICE_END
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	START_NSLICE	RESERVED						

VLC_SLICE_END — VLC Slice end flag

MAS_SLICE_END — Master Slice End Flag

START_NSLICE — Host to start a new slice

Address	[15:0]
0x0010	ENC_BUF_PTR_REC[15:0]

ENC_BUF_PTR_REC — Two bit for each channel (channel 0 ~ 7). Each two bit is the buffer pointer for the last encoded frame of the corresponding channel.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0018			DSP_MB_QP					
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	DSP_LPF_OFFSET							

DSP_MB_QP H264 QP Value for codec

DSP_LPF_OFFSET H264 LPF_OFFSET (Default 0)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x001C	HD1_MAP_MD	CIF_MAP_MD		VLC_BUF_ID				DSP_CODEC_MODE
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
						MV_FLAG_VLD	MV_VECT_VLD	VLC_VLD

DSP_CODEC_MODE
0 Encode (TW5864B Default)
1 Decode

VLC_BUF_ID
0->3 4 VLC data buffer in DDR (1M each)
0->7 8 VLC data buffer in DDR (512k each)

CIF_MAP_MD
0 4CIF in 1 MB
1 1CIF in 1 MB

HD1_MAP_MD
0 2 half D1 in 1 MB
1 1 half D1 in 1 MB

VLC_VLD
VLC Stream valid
0 Invalid
1 Valid

MV_VECT_VLD
MV Vector Valid
0 Invalid
1 Valid

MV_FLAG_VLD
MV Flag Valid
0 Invalid
1 Valid

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0020	DSP_SEN_PIC_CHM				DSP_SEN_PIC_LU			
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
				DSP_SEN_HFULL		DSP_SEN_PIC_MAX		

DSP_SEN_PIC_LU Org Buffer Base for Luma (default 0)

DSP_SEN_PIC_CHM Org Buffer Base for Chroma (default 4)

DSP_SEN_PIC_MAX Maximum Number of Buffers (default 4)

DSP_SEN_HFULL Original Frame D1 or HD1 switch (Default 0)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0024	DSP_REF_PIC_CHM				DSP_REF_PIC_LU			
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
						DSP_REF_PIC_MAX		

DSP_REF_PIC_LU Ref Buffer Base for Luma (default 0)

DSP_REF_PIC_CHM Ref Buffer Base for Chroma (default 4)

DSP_REF_PIC_MAX Maximum Number of Buffers (default 4)

Address	[15:0]
0x0028	SEN_EN_CH

SEN_EN_CH[n] SENIF original frame capture enable for each channel

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x002C		DSP_FLW_CNTL	DSP_CHROM_SW	DSP_MB_WAIT	DSP_ENC_CHN			
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
					DSP_MB_DELAY			

DSP_ENC_CHN The ID for channel selected for encoding operation

DSP_MB_WAIT Control for MB Delay. See Description below.

DSP_CHROM_SW DSP Chroma Switch
0 DDRB
1 DDRA

DSP_FLW_CNTL VLC Flow Control
0 Disable
1 Enable

DSP_MB_DELAY If DSP_MB_WAIT == 0, the MB delay is

DSP_MB_DELAY * 16

If DSP_MB_DELAY == 1, the MB delay is

DSP_MB_DELAY * 128

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0030	DDR_PAGE_CNT							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	DDR_MODE	DDR_AB_SEL	DDR_BRST_EN					

DDR_PAGE_CNTL DDR Single Access Page Number

DDR_BRST_EN DDR-DPR Burst Read Enable
1 Enable
0 Disable

DDR_AB_SEL DDR A/B Select as HOST access
0 Select DDRA
1 Select DDRB

DDR_MODE DDR Access Mode Select
0 Single R/W Access (Host <-> DDR)
1 Burst R/W Access (Host <-> DPR)

Address	[15:0]
0x0038	SENIF_ORG_FRM_PTR [15:0]
0x003C	SENIF_ORG_FRM_PTR [31:16]

SENIF_ORG_FRM_PTR The original frame capture pointer. Two bits for each channel.

Address	[15:0]
0x004C	ENC_BUF_PTR_REC[31:16]

ENC_BUF_PTR_REC Two bit for each channel (channel 8 ~ 15). Each two bit is the buffer pointer for the last encoded frame of a channel

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0060	CH3_ MV_PTR		CH2_ MV_PTR		CH1_ MV_PTR		CH0_MV_PTR	
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	CH7_ MV_PTR		CH6_ MV_PTR		CH5_ MV_PTR		CH4_ MV_PTR	
0x0064	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
	CHB_ MV_PTR		CHA_ MV_PTR		CH9_ MV_PTR		CH8_MV_PTR	
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	CHF_ MV_PTR		CHE_ MV_PTR		CHD_ MV_PTR		CHC_ MV_PTR	

CHn_MV_PTR Current MV Flag Status Pointer for Channel n. (Read only)

Address	[15:0]
0x0068	RST_MV_PTR

RST_MV_PTR[n] Reset Current MV Flag Status Pointer for Channel n.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0200	DSP_DWN_Y		DSP_DWN_X		DI_MD	DI_EN		
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
								DUAL_STR

DSP_INTER_ST Inter_Mode Start

DI_EN Deinterlacer Enable (1 to enable)

DI_MD De-interlacer Mode
1 Shuffled frame
0 Normal Un-Shuffled Frame

DSP_DWN_X Down scale original frame in X direction
11: Un-used
10: down-sample to ¼
01: down-sample to ½
00: down-sample disabled

DSP_DWN_Y Down scale original frame in Y direction

11: Un-used
10: down-sample to ¼
01: down-sample to ½
00: down-sample disabled

DUAL_STR 1 Dual Stream
0 Single Stream

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0204	DSP_WIN_SIZE[3:0]				DSP_REF_FRM			
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
							DSP_WIN_SIZE[5:4]	

DSP_REF_FRM Number of reference frame (Default 1 for TW5864B)

DSP_WIN_SIZE Window size

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0208	DSP_SKIP_OFEN	DSP_SKIP_OFFSET						
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
		RESERVED						

DSP_SKIP_OFEN Skip Offset Enable bit
0 DSP_SKIP_OFFSET value is not used (default 8)
1 DSP_SKIP_OFFSET value is used in HW

DSP_SKIP_OFFSET Skip mode cost offset (default 8)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x020C		SRCH_OPT		SKIP_EN	INTRA_EN	ME_EN	HPEL_EN	QPEL_EN

QPEL_EN Enable quarter pel search mode

HPEL_EN Enable half pel search mode

ME_EN Enable motion search mode

INTRA_EN Enable Intra mode

SKIP_EN Enable Skip Mode

SRCH_OPT Search Option (Default 2'b01)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0210						DSP_ENC_REF_PTR		
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	DSP_REC_BUF_PTR							

DSP_ENC_REF_PTR Reference Buffer Pointer for encoding

DSP_REC_BUF_PTR Reconstruct Buffer pointer

Address	[15:0]
0x0214	DSP_REF_MVP_LAMBDA

DSP_REF_MVP_LAMBDA Lambda Value for H264

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0218		DSP_PIC_MAX_MB_Y						
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	DSP_PIC_MAX_MB_X							

DSP_PIC_MAX_MB_Y The MB number in Y direction for a frame

DSP_PIC_MAX_MB_X The MB number in X direction for a frame

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x021C								
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	DSP_ENC_ORG_PTR							

DSP_ENC_ORG_PTR The original frame pointer for encoding

Address	[15:0]
0x0220	DSP_OSD_ATTRI_BASE

DSP_OSD_ATTRI_BASE DDR base address of OSD rectangle attribute data

Address	[15:0]
0x0228	DSP_OSD_ENABLE

DSP_ OSD_ENABLE OSD enable bit for each channel

Address	[15:0]
0x0280 -0x02FC	ME_MV_VEC

0x0280 ~ 0x029C – Motion Vector for 1st 4x4 Block, e.g., 80 (X), 84 (Y)
0x02A0 ~ 0x02BC – Motion Vector for 2nd 4x4 Block, e.g., A0 (X), A4 (Y)
0x02C0 ~ 0x02DC – Motion Vector for 3rd 4x4 Block, e.g., C0 (X), C4 (Y)
0x02E0 ~ 0x02FC – Motion Vector for 4th 4x4 Block, e.g., E0 (X), E4 (Y)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x040C			Dsp_i4x4_offset					
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]

DSP_I4x4_OffSET
```
if (intra16x16_cost < (intra4x4_cost+dsp_i4x4_offset))
   Intra_mode = intra16x16_mode
Else
   Intra_mode = intra4x4_mode
```

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0410		DSP_INTRA_MODE						
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]

DSP_INTRA_MODE
0x5 Only 4x4
0x6 Only 16x16
0x7 16x16 & 4x4

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0414			Dsp_i4x4weight					
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]

DSP_I4x4_WEIGHT WEIGHT Factor for I4x4 cost calculation (QP dependent)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0604	DSP_RESID_MODE_OFFSET							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	RESERVED							

DSP_RESID_MODE_OFFSET

Offset used to affect Intra/ME model decision

If (me_cost < intra_cost + dsp_resid_mode_offset)
Pred_Mode = me_mode
Else
Pred_mode = intra_mode

Address	[15:0]
0x0800--x09FF	QUAN_TABLE

QUAN_TAB Quantization TABLE Values

Address	[15:0]
0x0Cn0	RT_CNTR_CHn_FRM0
0x0Cn4	RT_CNTR_CHn_FRM1
0x0Cn8	RT_CNTR_CHn_FRM2
0x0CnC	RT_CNTR_CHn_FRM3

RT_CNTR_CHn_FRM0 RT_CNTR_CHn, channel_n from 0 to f

RT_CNTR_CHn_FRM1

RT_CNTR_CHn_FRM2

RT_CNTR_CHn_FRM3

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0D00				BUS1_D1		FRAME_1	PROG_1B	PROG_1A
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
				BUS2_D1		FRAME_2	PROG_2B	PROG_2A
0x0D04	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
				BUS3_D1		FRAME_3	PROG_3B	PROG_3A
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
				BUS4_D1		FRAME_4	PROG_4B	PROG_4A

PROG_nA	1	Progressive in part A in bus n
	0	Interlaced in part A in bus n
PROG_nB	1	Progressive in part B in bus n
	0	Interlaced in part B in bus n
FRAME_n	1	Frame Mode in bus n
	0	Field Mode in bus n
BUSn_D1	0	4CIF in bus n
	1	1D1 + 4 CIF in bus n
	2	2D1 in bus n

Address	[15:0]
0x0D08	SENIF_HOR_MIR
0x0D0C	SENIF_VER_MIR

SENIF_HOR_MIR[n]	1	Horizontal Mirror for channel n
	0	Normal
SENIF_VER_MIR[n]	1	Vertical Mirror for channel n
	0	Normal

Address	[9:0]
0x0D10	FRAME_WIDTH_BUS0_A
0x0D14	FRAME_WIDTH_BUS0_B
0x0D18	FRAME_HEIGHT_BUS0_A
0x0D1C	FRAME_HEIGHT_BUS0_B
0x0D20	FRAME_WIDTH_BUS1_A
0x0D24	FRAME_WIDTH_BUS1_B
0x0D28	FRAME_HEIGHT_BUS1_A
0x0D2C	FRAME_HEIGHT_BUS1_B
0x0D30	FRAME_WIDTH_BUS2_A
0x0D34	FRAME_WIDTH_BUS2_B
0x0D38	FRAME_HEIGHT_BUS2_A
0x0D3C	FRAME_HEIGHT_BUS2_B
0x0D40	FRAME_WIDTH_BUS3_A
0x0D44	FRAME_WIDTH_BUS3_B
0x0D48	FRAME_HEIGHT_BUS3_A
0x0D4C	FRAME_HEIGHT_BUS3_B

FRAME_WIDTH_BUSn_A

0x15F: 4 CIF
0x2CF: 1 D1 + 3 CIF
0x2CF: 2 D1

FRAME_WIDTH_BUSn_B

0x15F: 4 CIF
0x2CF: 1 D1 + 3 CIF
0x2CF: 2 D1

FRAME_HEIGHT_BUSn_A

0x11F: 4CIF (PAL)
0x23F: 1D1 + 3CIF (PAL)
0x23F: 2 D1 (PAL)

0x0EF: 4CIF (NTSC)
0x1DF: 1D1 + 3CIF (NTSC)
0x1DF: 2 D1 (NTSC)

FRAME_HEIGHT_BUSn_B

0x11F: 4CIF (PAL)
0x23F: 1D1 + 3CIF (PAL)
0x23F: 2 D1 (PAL)

0x0EF: 4CIF (NTSC)
0x1DF: 1D1 + 3CIF (NTSC)
0x1DF: 2 D1 (NTSC)

Address	[15:0]
0x0D50	FULL_HALF_FLAG

FULL_HALF_FLAG 1: the bus mapped Channel n Full D1
0: the bus mapped Channel n Half D1

Address	[15:0]
0x0D54	FULL_HALF_MODE_SEL

FULL_HALF_MODE_SEL
0 The bus mapped Channel select partA Mode
1 The bus mapped Channel select partB Mode

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x1000	VLC_ADD03_EN	VLC_BYTE_SWP	VLC_SLICE_QP					
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	VLC_PCI_SEL	VLC_OVFL_CNTL	VLC_INF_SEL	VLC_BIT_ALIGN				
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
								VLC_A03_DISAB
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	VLC_BUF_RDY							

VLC_SLICE_QP QP Value used by H264 CAVLC

VLC_BYTE_SWP Swap byte order of VLC stream in d-word.
1 Normal (VLC output= [31:0])
0 Swap (VLC output={[23:16],[31:24],[7:0],[15:8]})

VLC_ADD03_EN
0 Bypass Adding 03 circuit for VLC stream
1 Enable Adding 03 circuit for VLC stream

VLC_BIT_ALIGN Number of bit for VLC bit Align

VLC_INF_SEL Synchronous Interface select for VLC Stream
1 CDC_VLCS_MAS read VLC stream
0 CPU read VLC stream

VLC_OVFL_CNTL
1 Enable VLC overflow control
0 Disable VLC overflow control

VLC_PCI_SEL
1 PCI Master Mode
0 Non PCI Master Mode

VLC_A03_DISAB
0 Enable Adding 03 to VLC header and stream
1 Disable Adding 03 to VLC header of “00000001”

VLC_BUF_RDY Status of VLC stream in DDR (one bit for each buffer)
1 VLC is ready in buffer n (HW set)
0 VLC is not ready in buffer n (SW clear)

Address	[15:0]
0x1004	SLICE_TOTAL_BIT

SLICE_TOTAL_BIT Total number of bit in the slice

Address	[15:0]
0x1008	RES_TOTAL_BIT

RES_TOTAL_BIT Total number of bit in the residue

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x100C	VLC_STREAM_LEN[3:0]				DSP_RD_OF	VLC_END_SLICE	VLC_BK1_FULL	VLC_BK0_FULL
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
				VLC_STREAM_LEN[8:4]				

VLC_BK0_FULL VLC BK0 full status, write ‘1’ to clear

VLC_BK1_FULL VLC BK1 full status, write ‘1’ to clear

VLC_END_SLICE VLC end slice status, write ‘1’ to clear

DSP_RD_OF VLC Buffer overflow status, write ‘1’ to clear

VLC_STREAM_LEN VLC string length in either buffer 0 or 1 at end of frame

Address	[15:0]
0x1010	TOTAL_COEF_NO

TOTAL_COEF_NO Total coefficient number in a frame

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x1014								VLC_DSP_INT

VLC_DSP_INTR VLC Encoder Interrupt. Write ‘1’ to clear.

Address	[31:0]
0x1018	VLC_STREAM_CRC

VLC_STREAM_CRC VLC stream CRC checksum

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x101C							VLC_RD_BRST	VLC_RD_MEM

VLC_RD_MEM
1 Read VLC lookup Memory
0 Read VLC Stream Memory

VLC_RD_BRST
1 Read VLC Stream Memory in burst mode
0 Read VLC Stream Memory in single mode

0x2000 ~ 0x2FFC -- H264 Stream Memory Map

A word is 4 bytes. I.e.,

VLC_STREAM_MEM [0] address: 0x2000
VLC_STREAM_MEM [1] address: 0x2004
.....
VLC_STREAM_MEM [3FF]address: 0x2FFC

0x4000 ~ 0x4FFC -- Audio Register Map

Address	[31:0]
0x4000	1ms counter

config 1ms cnt cnt =Realtime clk/1000

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x4004						enc adpcm enb	Org data enb	Dec adpcm enb

Dec_adpcm_enb
ADPCM decoder enable
1 Enable
0 Disable

Org_data_enb
ADPCM input data enable
1 Enable
0 Disable

Enc_data_enb
ADPCM encoder enable
1 Enable
0 Disable

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x4008	AUD_ORG_CH_EN[7:0]							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	AUD_ORG_CH_EN [15:8]							
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
	AUD_SAMPLE_RATE		AUD_TYPE				AD_BIT_MODE	SPK_ORG_EN
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	AUD_MODE	TEST_ADLOOP_EN	TESTLOOP_EN	TESTLOOP_CHID				

AUD_ORG_CH_EN — Record path PCM Audio enable bit for each channel,

SPK_ORG_EN — Speaker path PCM Audio Enable

AD_BIT_MODE
0 16bit
1 8bit

AUD_TYPE
0 PCM
3 ADPCM

AUD_SAMPLE_RATE
0 8K
1 16K

TESTLOOP_CHID — Channel ID used to select audio channel (0 to 16) for loopback

TESTLOOP_EN — Reserved

TEST_ADLOOP_EN
1 Enable AD Loopback Test
0 Disable AD Loopback Test

AUD_MODE
0 Asynchronous Mode or PCI target mode
1 PCI Initiator Mode

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x400C	Aud_ADPCM_CH_EN[7:0]							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	Aud_ADPCM_CH_EN [15:8]							
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
								SPK_ADPCM_EN
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]

AUD_ADPCM_CH_EN — Record path ADPCM audio channel enable, one bit for each.

SPK_ADPCM_EN — Speaker path ADPCM audio channel enable

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x4014			ADPCM_DEC_EN		DA1_BIT_MODE	DA1_MUTE	DA0_BIT_MODE	DA0_MUTE

DAn_Mute — Audio DA mute 1'b1 enable

DAn_BIT_MODE
0 16 bit mode
1 8 bit mode

ADPCM_DEC_EN
ADPCM decoder channel enable
0 Disable
1 Enable

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x4018				PC_BLOCK_ADPCM_RD_NO				

PC_BLOCK_ADPCM_RD_NO — Current channel ID when ADPCM stream moving is finished

Address	[29:0]
0x401C	ADPCM_ENC_WR_PTR[29:0]
0x4020	ADPCM_ENC_WR_PTR[50:30]

ADPCM_ENC_WR_PTR	bit [2:0]	ch0
	Bit [5:3]	ch1
	Bit [8:6]	ch2
	Bit [11:9]	ch3
	Bit [14:12]	ch4
	Bit [17:15]	ch5
	Bit [20:18]	ch6
	Bit [23:21]	ch7
	Bit [26:24]	ch8
	Bit [29:27]	ch9
	Bit [32:30]	ch10
	Bit [35:33]	ch11
	Bit [38:36]	ch12
	Bit [41:39]	ch13
	Bit [44:42]	ch14
	Bit [47:45]	ch15
	Bit [50:48]	ch16

Address	[29:0]
0x4024	ADPCM_ENC_RD_PTR[29:0]
0x4028	ADPCM_ENC_RD_PTR[50:30]

ADPCM_ENC_RD_PTR	bit [2:0]	ch0
	Bit [5:3]	ch1
	Bit [8:6]	ch2
	Bit [11:9]	ch3
	Bit [14:12]	ch4
	Bit [17:15]	ch5
	Bit [20:18]	ch6
	Bit [23:21]	ch7
	Bit [26:24]	ch8
	Bit [29:27]	ch9
	Bit [32:30]	ch10
	Bit [35:33]	ch11
	Bit [38:36]	ch12
	Bit [41:39]	ch13
	Bit [44:42]	ch14
	Bit [47:45]	ch15
	Bit [50:48]	ch16

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x402C	ADPCM_DEC_RD_PTR1				ADPCM_DEC_RD_PTR0			
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	ADPCM_DEC_WR_PTR1				ADPCM_DEC_WR_PTR0			

ADPCM_DEC_RD_PTRn Read pointer of ADPCM decoder

ADPCM_DEC_WR_PTRn Write pointer of ADPCM decoder

Address	[31:0]
0x4030	AD_ORIG_WR_PTR[31:0]
0x4034	AD_ORIG_WR_PTR[63:32]
0x4038	AD_ORIG_WR_PTR[67:64]

AD_ORIG_WR_PTR	bit [3:0]	ch0
	Bit [7:4]	ch1
	Bit [11:8]	ch2
	Bit [15:12]	ch3
	Bit [19:16]	ch4
	Bit [23:20]	ch5
	Bit [27:24]	ch6
	Bit [31:28]	ch7
	Bit [35:32]	ch8
	Bit [39:36]	ch9
	Bit [43:40]	ch10
	Bit [47:44]	ch11
	Bit [51:48]	ch12
	Bit [55:52]	ch13
	Bit [59:56]	ch14
	Bit [63:60]	ch15
	Bit [67:64]	ch16

Address	[31:0]
0x403C	AD_ORIG_RD_PTR[31:0]
0x4040	AD_ORIG_RD_PTR[63:32]
0x4044	AD_ORIG_RD_PTR[67:64]

AD_ORIG_RD_PTR	bit [3:0]	ch0
	Bit [7:4]	ch1
	Bit [11:8]	ch2
	Bit [15:12]	ch3
	Bit [19:16]	ch4
	Bit [23:20]	ch5
	Bit [27:24]	ch6
	Bit [31:28]	ch7
	Bit [35:32]	ch8
	Bit [39:36]	ch9
	Bit [43:40]	ch10
	Bit [47:44]	ch11
	Bit [51:48]	ch12
	Bit [55:52]	ch13
	Bit [59:56]	ch14
	Bit [63:60]	ch15
	Bit [67:64]	ch16

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x4048				PC_BLOCK_ORIG_RD_NO				

PC_BLOCK_ORIG_RD_NO Current channel ID when PCM stream moving is finished

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x404C	PCI_DATA_SEL:[7:0]							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	PCI_DATA_SEL[15:8]							
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
							PCI_AUD_FRM_EN	PCI_FLOW_EN
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]

PCI_DATA_SEL The register is applicable to PCI initiator mode only. Used to select PCM (0) or ADPCM (1) audio data sent to PC. One bit for each channel

PCI_FLOW_EN Audio flow control mode selection bit.
0 Flow control disabled. TW5864B continuously sends audio frame to PC (initiator mode)
1 Flow control enabled

PCI_AUD_FRM_EN When PCI_FLOW_EN is set, PCI need to toggle this bit to send an audio frame to PC. One toggle to send one frame.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x8000							CS2DAT_CNT	

CS2DAT_CNT CS valid to data valid CLK cycles when writing operation

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x8004						DATA_VLD_WIDTH		

DATA_VLD_WIDTH data valid signal width by system clock cycles

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x8008	SYNC_CFG				VLC_OUT_EDGE	VLC_STR_DELAY		SYNC_ADR_EDGE

SYNC_CFG	0	vlc stream to synchronous port
	1	vlc stream to ddr buffers
SYNC_ADR_EDGE	0	SYNC Address sampled on rising edge
	1	SYNC Address sampled on Falling edge
VLC_STR_DELAY	0	No system delay
	1	One system clock delay
	2	Two system clock delay
	3	Three system clock delay
VLC_OUT_EDGE	0	Rising edge output
	1	Falling edge output

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x800C							I2C_PHASE_CFG	

I2C_PHASE_CFG	2'b00	phase set to 180 degree
	2'b01	phase set to 270 degree
	2'b10	phase set to 0 degree
	2'b11	phase set to 90 degree

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x8018	SYSPLL_M[7:0]							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	SYSPLL_N[4:0]					SYSPLL_M[10:8]		

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x8020	SYSPLL_CP_SEL			SYSPLL_IREF	SYSPLL_P		SYSPLL_N[6:5]	
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	SYSPLL_ED_SEL	SYSPLL_LPF_5PF	SYSPLL_ICP_SEL		SYSPLL_LP_X8		SYSPLL_VCO	

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x8024			1	SYSPLL_PD				SYSPLL_RST

The system / DDR clock (166 MHz) is generated with an on-chip system clock PLL (SYSPLL) using input crystal clock of 27 MHz. The system clock PLL frequency is controlled with the following equation.

CLK_OUT = CLK_IN * (M+1) / ((N+1) * P)

SYSPLL_M — M parameter

SYSPLL_N — N parameter

SYSPLL_P — Select P parameter from the following

0	1
1	2
2	4
3	8

SYSPLL_IREF — SYSPLL bias current control

0	Lower current (default)
1	30% higher current

SYSPLL_CP_SEL — SYSPLL charge pump current selection

0	1,5µA
1	4µA
2	9µA
3	19µA
4	39µA
5	79µA

	6	159μA
	7	319μA
SYSPLL_VCO	VCO Range selection	
	00	5 ~ 75 MHz
	01	50 ~ 140 MHz
	10	110 ~ 320 MHz
	11	270 ~ 700 MHz
SYSPLL_LP_X8	Loop resister	
	0	38.5KΩ
	1	6.6KΩ (default)
	2	2.2KΩ
	3	1.1KΩ
SYSPLL_ICP_SEL	PLL charge pump fine tune	
	00	x1 (default)
	01	x1/2
	10	x1/7
	11	x1/8
SYSPLL_LPF_5PF	PLL low pass filter phase margin adjustment	
	0	no 5pF (default)
	1	5pF added
SYSPLL_ED_SEL	PFD select edge for detection	
	0	Falling edge (default)
	1	Rising edge
SYSPLL_RST	Reset SYSPLL	
SYSPLL_PD	Power down SYSPLL	

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x801C				SPLL_CFG	LOAD	SYSPLL_CFG		SRST

SRST — Issue Soft Reset from Async Host Interface / PCI Interface clock domain. Become valid after sync to the xtal clock domain. This bit is set only if LOAD register bit is also set to 1.

SYSPLL_CFG — Issue SYSPLL (166 MHz) configuration latch from Async host interface / PCI Interface clock domain. The configuration setting becomes effective only if LOAD register bit is also set to 1.

SPLL_CFG — Issue SPLL (108 MHz) configuration load from Async host interface / PCI Interface clock domain. The configuration setting becomes effective only if the LOAD register bit is also set to 1.

LOAD — Set this bit to latch the SRST, SYSPLL_CFG, and SPLL_CFG setting into the xtal clock domain to restart the PLL. This bit is self cleared.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x8028		SPLL_IREF	SPLL_LPX4		SPLL_CPX4		SPLL_PD	SPLL_DBG

SPLL_DBG — Internal use only. Set to 0.

SPLL_PD — Power down 108 MHz SPLL.

SPLL_CPX4 — 108 MHz PLL charge pump select

0 1μA
1 5μA (default)
2 10μA
3 15μA

SPLL_LPX4 — 108 MHz PLL loop filter select

0 80KΩ
1 40KΩ (default)
2 30KΩ
3 20KΩ

SPLL_IREF 108 MHz PLL current control

0 Low current (default)

1 Higher current (30% more than setting to 0)

0x8800 ~ 0x88FC -- Interrupt Register Map

Address	[15:0]
0x8800	TRIGER_MODE_L

TRIGER_MODE_L Trigger mode of interrupt source 0 ~ 15

1 Edge trigger mode

0 Level trigger mode

Address	[15:0]
0x8804	TRIGER_MODE_H

TRIGER_MODE_L Trigger mode of interrupt source 16 ~ 31

1 Edge trigger mode

0 Level trigger mode

Address	[15:0]
0x8808	INTR_ENABLE_L

INTR_ENABLE_L Enable of interrupt source 0 ~ 15

1 Enable interrupt

0 Disable interrupt

Address	[15:0]
0x880C	INTR_ENABLE _H

INTR_ENABLE_H Enable of interrupt source 16 ~ 31

1 Enable interrupt

0 Disable interrupt

Address	[15:0]
0x8810	INTR_CLR_L

INTR_CLR_L Clear interrupt command of interrupt source 0 ~ 15

1 Clear interrupt

0 Not clear interrupt

Address	[15:0]
0x8814	INTR_CLR_H

INTR_CLR_H Clear interrupt command of interrupt source 16 ~ 31

1 Clear interrupt

0 Not clear interrupt

Address	[15:0]
0x8818	INTR_ASSERT_L

INTR_ASSERT_L Assertion of interrupt source 0 ~ 15

1 High level or pos-edge is assertion

0 Low level or neg-edge is assertion

Address	[15:0]
0x881C	INTR_ASSERT_H

INTR_ASSERT_H Assertion of interrupt source 16 ~ 31

1 High level or pos-edge is assertion

0 Low level or neg-edge is assertion

Address	[0]
0x8820	INTR_OUT_LEVEL

INTR_OUT_LEVEL Output level of interrupt

1 Interrupt output is high assertion

0 Interrupt output is low assertion

Address	[15:0]
0x8838	INTR_STATUS_L

INTR_STATUS_L Status of interrupt source 0 ~ 15

1 With interrupt

0 No interrupt

Bit [0]: VLC 4k RAM interrupt

Bit [1]: BURST DDR RAM interrupt

Bit [2]: MV DSP interrupt

Bit [3]: video lost interrupt

Bit [4]: gpio 0 interrupt

Bit [5]: gpio 1 interrupt

Bit [6]: gpio 2 interrupt

Bit [7]: gpio 3 interrupt

Bit [8]: gpio 4 interrupt

Bit [9]: gpio 5 interrupt

Bit [10]: gpio 6 interrupt

Bit [11]: gpio 7 interrupt

Bit [12]: JPEG interrupt

Bit [13:15]: Reserved

Address	[15:0]
0x883C	INTR_STATUS_H

INTR_STATUS_H Status of interrupt source 16 ~ 31

1 With interrupt

0 No interrupt

Bit [0]: Reserved

Bit [1]: VLC done interrupt

Bit [2]: Reserved

Bit [3]: AD Vsync interrupt

Bit [4]: Preview eof interrupt

Bit [5]: Preview overflow interrupt

Bit [6]: Timer interrupt

Bit [7]: Reserved

Bit [8]: Audio eof interrupt

Bit [9]: I2C done interrupt

Bit [10]: AD interrupt

Bit [11:15]: Reserved

0x9000 ~ 0x920C -- Video Capture (VIF) Register Map

Address	[15:0]
0x9000	H264EN_CH_STATUS

H264EN_CH_STATUS[n] Status of Vsync synchronized H264EN_CH_EN (Read Only)

1 Channel Enabled

0 Channel Disabled

Address	[15:0]
0x9004	H264EN_CH_EN

H264EN_CH_EN[n] H264 Encoding Path Enable for channel n

1 Channel Enabled

0 Channel Disabled

Address	[15:0]
0x9008	H264EN_CH_DNS

H264EN_CH_DNS[n] H264 Encoding Path Downscale Video Decoder Input for channel n

1 Downscale Y to 1/2

0 Does not downscale

Address	[15:0]
0x900C	H264EN_CH_PROG

H264EN_CH_PROG[n] H264 Encoding Path channel n is progressive

1 Progressive (Not valid for TW5864B)
0 Interlaced (TW5864B default)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x9010					H264EN_BUS_MAX_CH			

H264EN_BUS_MAX_CH[n] H264 Encoding Path maximum number of channel on BUS n

0 Max 4 channels

1 Max 2 channels

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x9014	H264EN_RATE_MAX_LINE_1[2:0]			H264EN_RATE_MAX_LINE_0				
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
							H264EN_RATE_MAX_LINE_1[4:3]	
Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x9018	H264EN_RATE_MAX_LINE_3[2:0]			H264EN_RATE_MAX_LINE_2				
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
							H264EN_RATE_MAX_LINE_3[4:3]	

H264EN_RATE_MAX_LINE_n H264 Encoding path Rate Mapping Maximum Line Number on Bus n

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x9020	H264EN_CH3_FMT		H264EN_CH2_FMT		H264EN_CH1_FMT		H264EN_CH0_FMT	
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	H264EN_CH7_FMT		H264EN_CH6_FMT		H264EN_CH5_FMT		H264EN_CH4_FMT	
Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x9024	H264EN_CH3_FMT		H264EN_CH2_FMT		H264EN_CH1_FMT		H264EN_CH0_FMT	
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	H264EN_CH7_FMT		H264EN_CH6_FMT		H264EN_CH5_FMT		H264EN_CH4_FMT	

H264EN_CHn_FMT H264 Encoding Path Format configuration of Channel n

00 D1 (For D1 and hD1 frame)
01 (Reserved)
10 (Reserved)
11 D1 with ½ size in X (for CIF frame)

NOTE: **TO USED WITH 0X9008 REGISTER TO CONFIGURE THE FRAME SIZE**

Address	[15:0]
0x9100	H264EN_RATE_CNTL_BUS0_CH0[15:0]
0x9104	H264EN_RATE_CNTL_BUS0_CH0[31:16]
0x9108	H264EN_RATE_CNTL_BUS0_CH1[15:0]
0x910C	H264EN_RATE_CNTL_BUS0_CH1[31:16]
0x9110	H264EN_RATE_CNTL_BUS0_CH2[15:0]
0x9114	H264EN_RATE_CNTL_BUS0_CH2[31:16]
0x9118	H264EN_RATE_CNTL_BUS0_CH3[15:0]
0x911C	H264EN_RATE_CNTL_BUS0_CH3[31:16]
0x9120	H264EN_RATE_CNTL_BUS1_CH0[15:0]
0x9124	H264EN_RATE_CNTL_BUS1_CH0[31:16]
0x9128	H264EN_RATE_CNTL_BUS1_CH1[15:0]
0x912C	H264EN_RATE_CNTL_BUS1_CH1[31:16]
0x9130	H264EN_RATE_CNTL_BUS1_CH2[15:0]
0x9134	H264EN_RATE_CNTL_BUS1_CH2[31:16]
0x9138	H264EN_RATE_CNTL_BUS1_CH3[15:0]
0x913C	H264EN_RATE_CNTL_BUS1_CH3[31:16]
0x9140	H264EN_RATE_CNTL_BUS2_CH0[15:0]
0x9144	H264EN_RATE_CNTL_BUS2_CH0[31:16]
0x9148	H264EN_RATE_CNTL_BUS2_CH1[15:0]
0x914C	H264EN_RATE_CNTL_BUS2_CH1[31:16]
0x9150	H264EN_RATE_CNTL_BUS2_CH2[15:0]
0x9154	H264EN_RATE_CNTL_BUS2_CH2[31:16]
0x9158	H264EN_RATE_CNTL_BUS2_CH3[15:0]
0x915C	H264EN_RATE_CNTL_BUS2_CH3[31:16]
0x9160	H264EN_RATE_CNTL_BUS3_CH0[15:0]
0x9164	H264EN_RATE_CNTL_BUS3_CH0[31:16]
0x9168	H264EN_RATE_CNTL_BUS3_CH1[15:0]
0x916C	H264EN_RATE_CNTL_BUS3_CH1[31:16]
0x9170	H264EN_RATE_CNTL_BUS3_CH2[15:0]
0x9174	H264EN_RATE_CNTL_BUS3_CH2[31:16]
0x9178	H264EN_RATE_CNTL_BUS3_CH3[15:0]
0x917C	H264EN_RATE_CNTL_BUS3_CH3[31:16]

H264EN_RATE_CNTL_BUSm_CHn — H264 Encoding Path BUS m Rate Control for Channel n

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x9200	H264EN_BUS0_MAP_CH1				H264EN_BUS0_MAP_CH0			
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	H264EN_BUS0_MAP_CH3				H264EN_BUS0_MAP_CH2			
Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x9204	H264EN_BUS1_MAP_CH1				H264EN_BUS1_MAP_CH0			
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	H264EN_BUS1_MAP_CH3				H264EN_BUS1_MAP_CH2			
Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x9208	H264EN_BUS2_MAP_CH1				H264EN_BUS2_MAP_CH0			
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	H264EN_BUS2_MAP_CH3				H264EN_BUS2_MAP_CH2			
Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x920C	H264EN_BUS3_MAP_CH1				H264EN_BUS3_MAP_CH0			
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	H264EN_BUS3_MAP_CH3				H264EN_BUS3_MAP_CH2			

H264EN_BUSm_MAP_CHn	The16-to-1 MUX configuration register for each encoding channel (total of 16 channels). Four bits for each channel.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x9800	GPIO_DATA_0							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	GPIO_OEN_0							
Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x9804	GPIO_DATA_1							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	GPIO_OEN_1							

GPIO_DATA_n	GPIO DATA of Group n
GPIO_OEN_n	GPIO Output Enable of Group n

0xA000 ~ 0xA8FF – DDR Controller Register Map

DDR Controller A:

Address	[15:3]	[2:0]
0xA000	Reserved	RD_ACK_VLD_MUX

RD_ACK_VLD_MUX Data valid counter after read command to DDR
This is the delay value to show how many cycles the data will be back from DDR after we issue a read command.

Address	[15:12]	[11:8]	[7:4]	[2:0]
0xA004	TRAS_CNT_MAX	RFC_CNT_MAX	TCD_CNT_MAX	TWR_CNT_MAX

TRAS_CNT_MAX Tras value, the minimum cycle of active to precharge command period, default is 7

RFC_CNT_MAX Trfc value, the minimum cycle of refresh to active or refresh command period, default is 4'hf

TCD_CNT_MAX Trcd value, the minimum cycle of active to internal read/write command period, default is 4'h2,

TWR_CNT_MAX Twr value, write recovery time, default is 4'h3

Address	[15:3]	[2:0]
0xA008	Reserved	CAS_LATENCY

CAS_LATENCY CAS latency, the delay cycle between internal read command and the availability of the first bit of output data, default is 3

Address	[15:0]
0xA00C	DDR_REF_CNTR_MAX

DDR_REF_CNTR_MAX Maximum average periodic refresh, the value is based on the current frequency to match 7.8μs.

Address	[15:3]	[2:0]
0xA01C	Reserved	DDR_ON_CHIP_MAP

DDR_ON_CHIP_MAP [1:0]
0x0 256M DDR on board
0x1 512M DDR on board
0x2 1G DDR on board

DDR_ON_CHIP_MAP [2]
0x0 Only one DDR chip
0x1 Two DDR chips

Address	[15:6]	[5:4]	[2]	[1]	[0]

0xA020	Reserved	DATA_MODE	WRITE_FLAG	SINGLE_PROC	MASTER_MODE

MASTER_MODE
0 Common read/write mode
1 DDR self-test mode

SINGLE_PROC
0 DDR self-test single read/write
1 DDR self-test burst read/write

WRITE_FLAG
0 DDR self-test write command
1 DDR self-test read command

DATA_MODE [1:0]
0x0 write 32'haaaa5555 to DDR
0x1 write 32'hffffffff to DDR
0x2 write 32'hha5a55a5a to DDR
0x3 write increasing data to DDR

Address	[15:8]	[7:0]
0xA024	Reserved	BURST_CNTR_MAX

BURST_CNTR_MAX The maximum data of one burst in DDR self-test mode

Address	[15:0]
0xA028	DDR_PROC_CNTR_MAX_L

DDR_PROC_CNTR_MAX_L The maximum burst counter (bit 15~0) in DDR self-test mode

Address	[15:0]
0xA02C	DDR_PROC_CNTR_MAX_H

DDR_PROC_CNTR_MAX_H The maximum burst counter (bit 31~16) in DDR self-test mode

Address	[15:1]	[0]
0xA030	Reserved	DDR_SELF_TEST_CMD

DDR_SELF_TEST_CMD 1 Start one DDR self-test
0 No self-test

Address	[15:0]
0xA034	ERR_CNTR_L

ERR_CNTR_L The maximum error counter (bit15 ~ 0) in DDR self-test

Address	[15]	[14:0]
0xA038	END_FLAG	ERR_CNTR_H

ERR_CNTR_H The maximum error counter (bit30 ~ 16) in DDR self-test

END_FLAG DDR self-test end flag

DDR Controller B:

Address	[15:3]	[2:0]
0xA800	Reserved	RD_ACK_VLD_MUX

RD_ACK_VLD_MUX Data valid counter after read command to DDR

Address	[15:12]	[11:8]	[7:4]	[2:0]
0xA804	TRAS_CNT_MAX	RFC_CNT_MAX	TCD_CNT_MAX	TWR_CNT_MAX

TRAS_CNT_MAX Tras maximum value

RFC_CNT_MAX Trfc maximum value

TCD_CNT_MAX Tcd maximum value

TWR_CNT_MAX Twr maximum value

Address	[15:3]	[2:0]
0xA808	Reserved	CAS_LATENCY

CAS_LATENCY CAS latency

Address	[15:0]
0xA80C	DDR_REF_CNTR_MAX

DDR_REF_CNTR_MAX Maximum value of DDR auto refresh

Address	[15:3]	[2:0]
0xA81C	Reserved	DDR_ON_CHIP_MAP

DDR_ON_CHIP_MAP [1:0]	0x0	256M DDR on board
	0x1	512M DDR on board
	0x2	1G DDR on board
DDR_ON_CHIP_MAP [2]	0x0	Only one DDR chip
	0x1	Two DDR chips

Address	[15:6]	[5:4]	[2]	[1]	[0]
0xA820	Reserved	DATA_MODE	WRITE_FLAG	SINGLE_PROC	MASTER_MODE

MASTER_MODE	0	Common read/write mode
	1	DDR self-test mode
SINGLE_PROC	0	DDR self-test single read/write
	1	DDR self-test burst read/write
WRITE_FLAG	0	DDR self-test write command
	1	DDR self-test read command
DATA_MODE [1:0]	0x0	Write 32'haaaa5555 to DDR
	0x1	Write 32'hffffffff to DDR
	0x2	Write 32'hha5a55a5a to DDR
	0x3	Write increasing data to DDR

Address	[15:8]	[7:0]
0xA824	Reserved	BURST_CNTR_MAX

BURST_CNTR_MAX	The maximum data of one burst in DDR self-test mode

Address	[15:0]
0xA828	DDR_PROC_CNTR_MAX_L

DDR_PROC_CNTR_MAX_L	The maximum burst counter (bit 15~0) in DDR self-test mode

Address	[15:0]
0xA82C	DDR_PROC_CNTR_MAX_H

DDR_PROC_CNTR_MAX_H The maximum burst counter (bit 31~16) in DDR self-test mode

Address	[15:1]	[0]
0xA830	Reserved	DDR_SELF_TEST_CMD

DDR_SELF_TEST_CMD 1 Start one DDR self-test
0 No self-test

Address	[15:0]
0xA834	ERR_CNTR_L

ERR_CNTR_L The maximum error counter (bit15 ~ 0) in DDR self-test

Address	[15]	[14:0]
0xA838	END_FLAG	ERR_CNTR_H

ERR_CNTR_H The maximum error counter (bit30 ~ 16) in DDR self-test

END_FLAG DDR self-test end flag

0xB004 ~ 0xB018 – HW version/ARB12 Register Map

Address	[15:0]
0xB004	TW5864_HW_Version

TW5864_HW_Version Default is C013

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xB010	TWLL_MVD_TMP_REQ_ENB	TWLL_MVD_REQ_ENB	DVM_MV REQ_ENB	VLC_STRM_REQ_ENB	AUD_DEC_REQ1_ENB	AUD_DEC_REQ0_ENB	AUD_ENC_REQ_ENB	AUD_DATA_IN_ENB
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
							MV_FLAG_REQ_ENB	JPEG_REQ_ENB

AUD_DATA_IN_ENB Audio data in to DDR enable (default 1)

AUD_ENC_REQ_ENB Audio encode request to DDR enable (default 1)

AUD_DEC_REQ0_ENB Audio decode request0 to DDR enable (default 1)

AUD_DEC_REQ1_ENB Audio decode request1 to DDR enable (default 1)

VLC_STRM_REQ_ENB VLC stream request to DDR enable (default 1)

DVM_MV _REQ_ENB H264 MV request to DDR enable (default 1)

TWLL_MVD_REQ_ENB mux_core MVD request to DDR enable (default 1)

TWLL_MVD_TMP_REQ_ENB mux_core MVD temp data request to DDR enable (default 1)

JPEG_REQ_ENB JPEG request to DDR enable (default 1)

MV_FLAG_REQ_ENB mv_flag request to DDR enable (default 1)

Address	[15]	[14:0]
0xB018	ARB12_ENB	ARB12_TIME_OUT_CNT

ARB12_ENB ARB12 Enable (default 1)

ARB12_ENB ARB12 maximum value of time out counter (default 15'h1FF)

0xB800 ~ 0xB80C -- Indirect Access Register Map

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xB800	IND_ADDR[7:0]							
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	IND_ADDR15:8]							
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
	Reserved							
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	BUSY						ENABLE	R/W

IND_ADDR	Address used to access indirect register space.
BUSY	Wait until this bit is '0' before using indirect access
ENABLE	Activate the indirect access. This bit is self cleared.
R/W	Read/Write command

Address	[31:0]
0xB804	IND_DATA

IND_DATA	Data used to read/write indirect register space

In order to access the indirect register space, the following procedure is followed.

Write Registers:

(1) Write IND_DATA at 0xB804 ~ 0xB807

(2) Read BUSY flag from 0xB803. Wait until BUSY signal is 0.

(3) Write IND_ADDR at 0xB800 ~ 0xB801. Set R/W to '1', ENABLE to '1'

Read Registers:

(1) Read BUSY flag from 0xB803. Wait until BUSY signal is 0.

(2) Write IND_ADDR at 0xB800 ~ 0xB801. Set R/W to '0', ENABLE to '1'

(3) Read BUSY flag from 0xB803. Wait until BUSY signal is 0.

(4) Read IND_DATA from 0xB804 ~ 0xB807

0xC000 ~ 0xC7FC -- Preview Register Map

Address	[15:0]
0xC000	PCI_PV _CH_STATUS

PCI_PV_CH_STATUS[n] Status of Vsync Synchronized PCI_PV_CH_EN (Read Only)
1 Channel Enabled
0 Channel Disabled

Address	[15:0]
0xC004	PCI_PV _CH_EN

PCI_PV_CH_EN[n] PCI Preview Path Enable for channel n
1 Channel Enable
0 Channel Disable

Address	[15:0]
0xC008	PCI_PV _CH_DNS

PCI_PV_CH_DNS[n] PCI Preview Path Y Direction Downscale Factor for channel n
1 Downscale Y to 1/2
0 Does not downscale

Address	[15:0]
0xC00C	PCI_PV_CH_PROG

PCI_PV_CH_PROG[n] PCI Preview Path channel n is progressive
1 Progressive (Not valid for TW5864B)
0 Interlaced (TW5864B default)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xC010					PCI_PV_BUS_MAX_CH			

PCI_PV_BUS_MAX_CH[n] PCI Preview Path maximum number of channel on BUS n (four bus total, one bit for each channel)
0 Max 4 channels
1 Max 2 channels

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xC014	PCI_PV_RATE_MAX_LINE_1[2:0]			PCI_PV_RATE_MAX_LINE_0				
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
							PCI_PV_RATE_MAX_LINE_1[4:3]	
Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xC018	PCI_PV_RATE_MAX_LINE_3[2:0]			PCI_PV_RATE_MAX_LINE_2				
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
							PCI_PV_RATE_MAX_LINE_3[4:3]	

PCI_PV_RATE_MAX_LINE_n

Maximum of time slot rotation for each bus
PAL (set as 24 for each field)
NTSC (set as 29 for each field)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xC020	PCI_PV_CH3_FMT		PCI_PV_CH2_FMT		PCI_PV_CH1_FMT		PCI_PV_CH0_FMT	
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	PCI_PV_CH7_FMT		PCI_PV_CH6_FMT		PCI_PV_CH5_FMT		PCI_PV_CH4_FMT	
Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xC024	PCI_PV_CH3_FMT		PCI_PV_CH2_FMT		PCI_PV_CH1_FMT		PCI_PV_CH0_FMT	
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	PCI_PV_CH7_FMT		PCI_PV_CH6_FMT		PCI_PV_CH5_FMT		PCI_PV_CH4_FMT	

PCI_PV_CHn_FMT

PCI Preview Path Format configuration of Channel n
00 D1 (For D1 frame)
01 CIF with ½ size in X (for QCIF frame mode)
10 (Reserved)
11 D1 with ½ size in X (for CIF frame)

NOTE: **USED WITH 0XC008 REGISTER TO CONFIGURE THE FRAME SIZE**

Address	[15:0]
0xC028	PCI_PV_FIELD_SEL

PCI_PV_FIELD_SEL[n]

PCI Preview Path Channel n field selection
1 Select Odd field
0 Select Even field

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xC02C								PCIPV_CMD_ST

PCI_PV_CMD_ST

Start command to redistribute Even/Odd filed for preview channel (used when overflow occurs)
This bit is automatically cleared in one cycle.
1 Start command
0 No command

Address	[15:0]
0xC100	PCI_PV_RATE_CNTL_BUS0_CH0[15:0]
0xC104	PCI_PV_RATE_CNTL_BUS0_CH0[31:16]
0xC108	PCI_PV_RATE_CNTL_BUS0_CH1[15:0]
0xC10C	PCI_PV_RATE_CNTL_BUS0_CH1[31:16]
0xC110	PCI_PV_RATE_CNTL_BUS0_CH2[15:0]
0xC114	PCI_PV_RATE_CNTL_BUS0_CH2[31:16]
0xC118	PCI_PV_RATE_CNTL_BUS0_CH3[15:0]
0xC11C	PCI_PV_RATE_CNTL_BUS0_CH3[31:16]
0xC120	PCI_PV_RATE_CNTL_BUS1_CH0[15:0]
0xC124	PCI_PV_RATE_CNTL_BUS1_CH0[31:16]
0xC128	PCI_PV_RATE_CNTL_BUS1_CH1[15:0]
0xC12C	PCI_PV_RATE_CNTL_BUS1_CH1[31:16]
0xC130	PCI_PV_RATE_CNTL_BUS1_CH2[15:0]
0xC134	PCI_PV_RATE_CNTL_BUS1_CH2[31:16]
0xC138	PCI_PV_RATE_CNTL_BUS1_CH3[15:0]
0xC13C	PCI_PV_RATE_CNTL_BUS1_CH3[31:16]
0xC140	PCI_PV_RATE_CNTL_BUS2_CH0[15:0]
0xC144	PCI_PV_RATE_CNTL_BUS2_CH0[31:16]
0xC148	PCI_PV_RATE_CNTL_BUS2_CH1[15:0]
0xC14C	PCI_PV_RATE_CNTL_BUS2_CH1[31:16]
0xC150	PCI_PV_RATE_CNTL_BUS2_CH2[15:0]
0xC154	PCI_PV_RATE_CNTL_BUS2_CH2[31:16]
0xC158	PCI_PV_RATE_CNTL_BUS2_CH3[15:0]
0xC15C	PCI_PV_RATE_CNTL_BUS2_CH3[31:16]
0xC160	PCI_PV_RATE_CNTL_BUS3_CH0[15:0]
0xC164	PCI_PV_RATE_CNTL_BUS3_CH0[31:16]
0xC168	PCI_PV_RATE_CNTL_BUS3_CH1[15:0]
0xC16C	PCI_PV_RATE_CNTL_BUS3_CH1[31:16]
0xC170	PCI_PV_RATE_CNTL_BUS3_CH2[15:0]
0xC174	PCI_PV_RATE_CNTL_BUS3_CH2[31:16]
0xC178	PCI_PV_RATE_CNTL_BUS3_CH3[15:0]
0xC17C	PCI_PV_RATE_CNTL_BUS3_CH3[31:16]

PCI_PV_RATE_CNTL_BUSm_CHn	PCI Preview Path BUS m Rate Control for Channel n

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xC200	PCI_PV_BUS0_MAP_CH1				PCI_PV_BUS0_MAP_CH0			
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	PCI_PV_BUS0_MAP_CH3				PCI_PV_BUS0_MAP_CH2			
Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xC204	PCI_PV_BUS1_MAP_CH1				PCI_PV_BUS1_MAP_CH0			
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	PCI_PV_BUS1_MAP_CH3				PCI_PV_BUS1_MAP_CH2			
Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xC208	PCI_PV_BUS2_MAP_CH1				PCI_PV_BUS2_MAP_CH0			
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	PCI_PV_BUS2_MAP_CH3				PCI_PV_BUS2_MAP_CH2			
Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xC20C	PCI_PV_BUS3_MAP_CH1				PCI_PV_BUS3_MAP_CH0			
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	PCI_PV_BUS3_MAP_CH3				PCI_PV_BUS3_MAP_CH2			

PCI_PV_BUSm_MAP_CHn	The16-to-1 MUX configuration register for each preview channel (total of 16 channels). Four bits for each preview channel.

0xC800 ~ 0xC804 -- JPEG Capture Register Map

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xC800	JPG_CAP_FMT_0		JPG_CAP_CH_0				JPG_BRST_CAP_0	JPG_SING_CAP_0
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
							JPG_DNS_0	JPG_PROG_0
Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xC804	JPG_CAP_FMT_1		JPG_CAP_CH_1				JPG_BRST_CAP_1	JPG_SING_CAP_1
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
							JPG_DNS_1	JPG_PROG_1

JPG_SING_CAP_n — JPEG Path Command for Single capture for bus n

- 1 — Start to capture next frame, de-activated when frame ends
- 0 — No command

JPG_BRST_CAP_n — JPEG Path Command for Burst capture for bus n

- 1 — Start to capture frames until CPU set ENC command
- 0 — No command

JPG_CAP_CH_n — JPEG Path Capture channel Select for bus n

JPG_CAP_FMT_n — JPEG Capture Path Format for bus n

- 00 — D1 (For D1 frame)
- 01 — CIF with ½ size in X (for QCIF frame mode)
- 10 — (Reserved)
- 11 — D1 with ½ size in X (for CIF frame)

JPG_DNS_n — JPEG Capture Path Downscale Input for bus n

- 1 — Downscale in Y to 1/2
- 0 — Does not downscale

JPG_PROG_n — JPEG Path channel n is progressive

- 1 — Progressive (Not valid for TW5864B)
- 0 — Interlaced (TW5864B default)

0xD000 ~ 0xD0FC -- JPEG Control Register Map

Address	[31：0]
0xD000	JPEG_QSCALE

JPEG_QSCALE Jpeg quality scale register. The default value should be 32'h10

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD004			JPG_NEWEST_BUF0		JPG_VLD_FRM0			
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	JPG_VLD_FRM_RES0							
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
	JPG_VLD_FRM_CHID0[7:0]							
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	JPG_VLD_FRM_CHID0[15:0]							

Valid frame indication register, after one frame of path 0 have been stored in the DDR the corresponding bit of this register become valid. Software can acknowledge now it can encode which frame in DDR through this register. This is a read only register

JPG_VLD_FRM0 For every path, there are 4 buffers in DDR and every bit correspond to one buffer, and the order is bit 0 for buffer 0, bit 1 for buffer 1, and so on

JPG_NEWEST_BUF0 Specify the buffer operated recently

JPG_VLD_FRM_RES0 Frame resolution, every buffer use 2 bits

00 D1

01 not used

10 CIF

11 HD1

JPG_VLD_FRM_CHID0Channel ID, every buffer use 4 bits

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD008			JPG_NEWEST_BUF1		JPG_VLD_FRM1			
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	JPG_VLD_FRM_RES1							
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
	JPG_VLD_FRM_CHID1[7:0]							
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	JPG_VLD_FRM_CHID1[15:0]							

Valid frame indication register is used for indicating the path1 buffer status.

JPG_VLD_FRM1 For every path, there are 4 buffers in DDR and every bit correspond to one buffer, and the order is bit 0 for buffer 0, bit 1 for buffer 1, and so on

JPG_NEWEST_BUF1 Specify the buffer operated recently

JPG_VLD_FRM_RES1 Frame resolution, every buffer use 2 bits

00: D1

01: not used

10: CIF

11: HD1

JPG_VLD_FRM_CHID1Channel ID, every buffer use 4 bits

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD00C					BUFFER_SEL			ENCODE_EN

Encode indicate register, through it software can control which buffer is encoded.

ENCODE_EN Encode enable bit

BUFFER_SEL Buffer select. 000-111 indicates all of the eight buffers of two paths. For example, 000 is buffer0 in path0, 001 is buffer1 in path0, 111 is buffer3 in path1, and so on

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD010	ENCODE_COMP							

Encode complete indication register, through rolling this register. Application software can acknowledge which frame has been encoded completely. This register is read only

ENCODE_COMP	Encode complete

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD014								CAP_ENABLE_0

Channel 0 capture enable indication register. Application software should write this bit to 1 after starting to capture one frame using register 0xC800

CAP_ENABLE_0	Channel 0 capture enable indicate

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD018								CAP_ENABLE_1

Channel 1 capture enable indication register. Application software should write this bit to 1 after starting to capture one frame using register 0xC804

CAP_ENABLE_1 Channel 1 capture enable indicate

Address	[31:0]
0xD01C	CAP_TIMEOUT_VALUE

This register is the maximal time interval between capture register is set and one frame has been stored in the DDR. Using this register to enhance system error-tolerance. The default value is 0x80000000. Normally **application software can set this register to 0x01000000, and other value base on DDR load.**

CAP_TIMEOUT_VALUE Capture timeout register

Address	[31:0]
0xD040	JPG_LENGTH0
0xD044	JPG_LENGTH1
0xD048	JPG_LENGTH2
0xD04C	JPG_LENGTH3
0xD050	JPG_LENGTH4
0xD054	JPG_LENGTH5
0xD058	JPG_LENGTH6
0xD05C	JPG_LENGTH7

JPG_LENGTHx Jpeg stream length registers

Address	[31:16]	[15:0]
0xD060	JPG_TIMESTAMP1	JPG_TIMESTAMP1
0xD064	JPG_TIMESTAMP3	JPG_TIMESTAMP2
0xD068	JPG_TIMESTAMP5	JPG_TIMESTAMP4
0xD06C	JPG_TIMESTAMP7	JPG_TIMESTAMP6

JPG_TIMESTAMPx Every channel original video timestamp

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD07C								JPG_NTSC

JPG_NTSC 1: NTSC 0: PAL (default)

Address	[31:0]
0xD0F0	DELAY_NUMBER

DELAY_NUMBER The capture will timeout complete beyond this time. Normally this register should be set to all 1

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD0F8	RESERVE							PCI_MODE

PCI mode The stream will be pushed up to system memory through PCI master

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xD0FC								SOFT_RST

If there are some special situations, like the original source video is not stable and so on, which will make the jpeg encode enter into the incorrect status, the application software can only reset jpeg module and not affect other procession. At first, set 1 to kick off the reset action, and then set 0 to stop it, after this, jpeg core can work again normally.

SOFT_RST	1	start reset
	0	reset complete

0xE000 ~ 0xFC00 – Motion Vector Register Map

Address	[31:0]
0xE000 -0xE7FC	ME_MV_VEC

ME_MV_VEC ME Motion Vector data (Four Byte Each)

ME_MV_VEC [0] address: 0xE000

ME_MV_VEC [1] address: 0XE004

ME_MV_VEC [1FF] address: 0xE7FC

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xFC00	MV_LEN[2:0]			DSP_WR_OF	MV_DSP_INTR	MV_EOF	mv_bk1_ful	MV_BK0_FULL
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
			MPI_DDR_SEL	MV_LEN[7:3]				

MV_BK0_FULL mv bank0 full status , write "1" to clear

MV_BK1_FULL mv bank1 full status , write "1" to clear

MV_EOF slice end status; write "1" to clear

MV_DSP_INTR mv encode interrupt status; write “1” to clear

DSP_WR_OF mv write memory overflow, write "1" to clear

MV_LEN mv stream length

MPI_DDR_SEL The configured status bit written into bit 15 of 0xFC04

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xFC04								
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	MPI_DDR_SEL							

MPI_DDR_SEL SW configure register

0 MV is saved in internal DPR

1 MV is saved in DDR

0x18000 ~ 0x181FC – PCI Master/Slave Control Map

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x18000		TIMER_INTR	PREV_OVERFLOW_INTR	PREV_EOF_INTR	AD_VSYNC_INTR		VLC_DONE_INTR	
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
								AUDIO_EOF_INTR
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
							AD_INTR_REG	IIC_DONE_INTR

VLC_DONE_INTR vlc done

AD_VSYNC_INTR ad vsync

PREV_EOF_INTR preview eof

PREV_OVERFLOW_INTR preview overflow interrupt

TIMER_INTR timer interrupt

AUDIO_EOF_INTR audio eof

IIC_DONE_INTR IIC done

AD_INTR_REG ad interrupt (e.g.: video lost, video format changed)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x18004	JPEG_MAST)_ENB	MCU_TIMER_INTR_ENB	PREV_OVERFLOW_ENB	PREV_MAST_ENB	AD_MAST_ENB	MVD_VLC_MAST_ENB		PCI_MASTER_ENB
	[15:8]							
	AU_MAST_ENB_CHN[7:0]							
	[23:16]							
	AU_MAST_ENB_CHN[15:8]							
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
		PCI_TAR_BURST_ENB[4:0]					AD_INTR_ENB	IIC_INTR_ENB

PCI_MAST_ENB	master enable
MVD_VLC_MAST_ENB	mvd&vlc master enable
AD_MAST_ENB	(Need to set 0 in TW5864A)
PREV_MAST_ENB	preview master enable
PREV_OVERFLOW_ENB	preview overflow enable
MCU_TIMER_INTR_ENB	timer interrupt enable
JPEG_MAST_ENB	JPEG master (push mode) enable
AU_MAST_ENB_CHN	audio master channel enable
IIC_INTR_ENB	IIC interrupt enable
AD_INTR_ENB	ad interrupt enable
PCI_TAR_BURST_ENB [0]	target burst enable
PCI_TAR_BURST_ENB [1]	vlc stream burst enable
PCI_TAR_BURST_ENB [2]	ddr burst enable (1 enable, and must set DDR_BRST_EN)
PCI_TAR_BURST_ENB [3]	(Reserved)
PCI_TAR_BURST_ENB [4]	(Reserved)

Address	[15:0]
0x18008	PREV_INTR_REG
	[31:16]
	AU_INTR_REG

Because preview and audio have 16 channels separately, so using this registers to indicate interrupt status for every channels. This is secondary interrupt status register. OR operating of the PREV_INTR_REG is PREV_EOF_INTR, OR operating of the AU_INTR_REG bits is AUDIO_EOF_INTR

PREV_INTR_REG	preview eof interrupt flag
AU_INTR_REG	audio eof interrupt flag

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x1800C	PCI_JPEG_INTR_ENB		PCI_RREV_OF_INTR_ENB	PCI_PREV_INTR_ENB			PCI_VLC_INTR_ENB	
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
								PCI_AUD_INTR_ENB

PCI_VLC_INTR_ENB	master enable
PCI_PREV_INTR_ENB	mvd and vlc master enable
PCI_PREV_OF_INTR_ENB	ad vsync master enable
PCI_JPEG_INTR_ENB	jpeg interrupt enable
PCI_AUD_INTR_ENB	preview master enable

Address	[15:0]
0x18010	PREV_BUF_FLAG
	[31:16]
	AUDIO_BUF_FLAG

Every channel of preview and audio have ping-pong buffers in system memory, this register is the buffer flag to notify software which buffer is been operated.

PREV_BUF_FLAG	preview buffer A/B flag
AUDIO_BUF_FALG	audio buffer A/B flag

Address	[7:0]							
0x18014	IIC_DATA							
	[15:8]							
	IIC_REG_ADDR							
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
	IIC_DEV_ADDR							IIC_RW
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
								IIC_DONE

IIC_DATA	register data
IIC_REG_ADDR	register address
IIC_RW	rd/wr flag rd=1, wr=0
IIC_DEV_ADDR	device address
IIC_DONE	IIC done, software kick off one time IIC transaction through setting this bit to 1.Then poll this bit, value 1 indicate IIC transaction have completed, if read, valid data have been stored in IIC data

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x18018								APP_SOFT_RST
	[31:16]							
	PCI_INF_VERSION							

APP_SOFT_RST	application software soft reset
PCI_INF_VERSION	PCI interface version, it is read only

Address	[31:0]
0x1801C	VLC_CRC_REG
0x18020	VLC_MAX_LENGTH
0x18024	VLC_LENGTH
0x18028	VLC_INTRA_CRC_I_REG
0x1802C	VLC_INTRA_CRC_O_REG
0x18030	VLC_PAR_CRC_REG
0x18034	VLC_PAR_LENGTH_REG
0x18038	VLC_PARAM_I_REG
0x1803C	VLC_PARAM_O_REG

VLC_CRC_REG	vlc stream CRC value, it is calculated in PCI module
VLC_MAX_LENGTH	vlc max length, it is defined by software based on software assign memory space for vlc
VLC_LENGTH	vlc length of one frame
VLC_INTRA_CRC_I_REG	vlc original CRC value
VLC_INTRA_CRC_O_REG	vlc original CRC value
VLC_PAR_CRC_REG	mv stream CRC value, it is calculated in PCI module
VLC_PAR _LENGTH_REG	mv length
VLC_PAR_I_REG	mv original CRC value
VLC_PAR_O_REG	mv original CRC value

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x18040							PREV_PCI_ENB_CHN	

Configuration register for 9[or 10] CIFs or 1D1+15QCIF Preview mode.

PREV_PCI_ENB_CHN [0]	Enable 9th preview channel (9CIF preview) or 1D1 channel in (1D1+15QCIF preview)
PREV_PCI_ENB_CHN [1]	Enable 10th preview channel

Address	[7:0]
0x18044	PREV_FRAME_FORMAT_IN[7:0]
	[15:8]
	PREV_FRAME_FORMAT_IN[15:8]

PREV_FRAME_FORMAT_IN [1:0]	bus0 frame format
	00: CIF
	01: QCIF
	10: 4CIF
	11: D1
PREV_FRAME_FORMAT_IN [3:2]	bus1 frame format
	00: CIF
	01: QCIF
	10: 4CIF
	11: D1
PREV_FRAME_FORMAT_IN [5:4]	bus2 frame format
	00: CIF
	01: QCIF
	10: 4CIF
	11: D1
PREV_FRAME_FORMAT_IN [7:6]	bus3 frame format
	00: CIF
	01: QCIF
	10: 4CIF
	11: D1
PREV_FRAME_FORMAT_IN [8]	bus0 progressive/interlace flag
	0: interlace
	1: progressive
PREV_FRAME_FORMAT_IN [9]	bus1 progressive/interlace flag
	0: interlace
	1: progressive
PREV_FRAME_FORMAT_IN [10]	bus2 progressive/interlace flag
	0: interlace
	1: progressive
PREV_FRAME_FORMAT_IN [11]	bus3 progressive/interlace flag
	0: interlace
	1: progressive

PREV_FRAME_FORMAT_IN [12]	PAL/NTSC format select, 0: PAL 1: NTSC
PREV_FRAME_FORMAT_IN [14:13]	bus4 frame format 00: CIF 01: QCIF 10: 4CIF 11: D1
PREV_FRAME_FORMAT_IN [15]	bus4 progressive/interlace flag 0: PAL 1: NTSC

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x18048								IIC_EN

IIC_EN	IIC enable

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x1804C							PCI_INTTM_SCALE	

PC I_INTTM_SCALE	PCI Interrupt interval scale 0 1ms INTRRUPT 1 2ms INTRRUPT 2 4ms INTRRUPT 3 8ms INTRRUPT

Address	[31:0]
0x18050	JPEG_MAX_LENGTH

JPEG_MAX_LENGTH	Define the jpeg operation max length, during reset, it will be initialized to default value 100KB

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x18060	JPEG_INTR_REG							

Because JPEG have 8 buffers separately, so using this registers to indicate interrupt status for every buffers. This is secondary interrupt status register.

JPEG_INTR_REG jpeg interrupt register

Address	[31:0]
0x18064	INTR_OUTPUT_ENABLE_REG

This register is used to control which interrupt can be valid in the interrupt line.

INTR_OUTPUT_ENABLE_REG interrupt output enable register

0x18080 ~ 0x180BC – VLC/MC/Audio Burst Base Address

Address	[31:0]
0x18080	VLC stream base address
0x18084	MV stream base address
0x180a0	0x180a0 – 0x180bc: audio burst base address Audio Channel 0 – channel 3 bank A base address
0x180a4	Audio Channel 0 – channel 3 bank B base address
0x180a8	Audio Channel 4 – channel 7 bank A base address
0x180ac	Audio Channel 4 – channel 7 bank B base address
0x180b0	Audio Channel 8 – channel 11 bank A base address
0x180b4	Audio Channel 8 – channel 11 bank B base address
0x180b8	Audio Channel 12 – channel 15 bank A base address
0x180bc	Audio Channel 12 – channel 15 bank B base address

0x180C0 ~ 0x180DC – JPEG Push Mode Buffer Base Address

Address	[31:0]
0x180c0	jpeg buffer0 base address
0x180c4	jpeg buffer1 base address
0x180c8	jpeg buffer2 base address
0x180cc	jpeg buffer3 base address
0x180d0	jpeg buffer4 base address
0x180d4	jpeg buffer5 base address
0x180d8	jpeg buffer6 base address
0x180dc	jpeg buffer7 base address

0x18100 ~ 0x1817C -- Preview Base Address

Address	[31:0]
0x18100	Preview Channel 0 bank A base address
0x18104	Preview Channel 0 bank B base address
0x18108	Preview Channel 1 bank A base address
0x1810c	Preview Channel 1 bank B base address
0x18110	Preview Channel 2 bank A base address
0x18114	Preview Channel 2 bank B base address
0x18118	Preview Channel 3 bank A base address
0x1811c	Preview Channel 3 bank B base address
0x18120	Preview Channel 4 bank A base address
0x18124	Preview Channel 4 bank B base address
0x18128	Preview Channel 5 bank A base address
0x1812c	Preview Channel 5 bank B base address
0x18130	Preview Channel 6 bank A base address
0x18134	Preview Channel 6 bank B base address
0x18138	Preview Channel 7 bank A base address
0x1813c	Preview Channel 7 bank B base address
0x18140	Preview Channel 8 bank A base address
0x18144	Preview Channel 8 bank B base address
0x18148	Preview Channel 9 bank A base address
0x1814c	Preview Channel 9 bank B base address
0x18150	Preview Channel 10 bank A base address
0x18154	Preview Channel 10 bank B base address
0x18158	Preview Channel 11 bank A base address
0x1815c	Preview Channel 11 bank B base address
0x18160	Preview Channel 12 bank A base address
0x18164	Preview Channel 12 bank B base address
0x18168	Preview Channel 13 bank A base address
0x1816c	Preview Channel 13 bank B base address
0x18170	Preview Channel 14 bank A base address
0x18174	Preview Channel 14 bank B base address
0x18178	Preview Channel 15 bank A base address
0x1817c	Preview Channel 15 bank B base address

The above register is PCI base address registers. Application software will initialize them to tell chip where the corresponding stream will be dumped to. Application software will select appropriate base address interval based on the stream length.

0x80000 ~ 0x87FFF -- DDR Burst RW Register Map

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x80000	BRST_LENGTH[5:0]						0	0
	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
	BRST_LENGTH[13:6]							
	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
							NEW_BRST_CMD	BRST_RW
	[31]	[30]	[29]	[28]	[27]	[26]	[25]	[24]
	BRST_BUSY	BRST_ERR	SINGLE_BUSY	SINGLE_ERR	BRST_END_INTR	BRST_ERR_INTR	SING_ERR_INTR	BRST_END

BRST_LENGTH — Length of 32-bit data burst

BRST_RW — Burst Read/Write

0 Read Burst from DDR

1 Write Burst to DDR

NEW_BRST_CMD — Begin a new DDR Burst. This bit is self cleared

BRST_END — DDR Burst End Flag

SING_ERR_INTR — Enable Error Interrupt for Single DDR Access

BRST_ERR_INTR — Enable Error Interrupt for Burst DDR Access

BRST_END_INTR — Enable Interrupt for End of DDR Burst Access

SINGLE_ERR — DDR Single Access Error Flag

SINGLE_BUSY — DDR Single Access Busy Flag

BRST_ERR — DDR Burst Access Error Flag

BRST_BUSY — DDR Burst Access Busy Flag

Address	[27:0]
0x80004	DDR_ADDR

DDR_ADDR DDR Access Address. Bit [1:0] has to be 0

Address	[15:0]
0x80008	DPR_BUF_ADDR

DPR_BUF_ADDR DDR Access Internal Buffer Address. Bit [1:0] has to be 0

Address	[15:0]
0x84000 -0x87FFC	DPR_BUF_ADDR

DPR_BUF_DATA SRAM Buffer MPI Access Space. Totally 16 KB.

Register Description – Indirect Map Space

The indirect space is accessed through 0xB800 ~ 0xB807 registers in direct access space.

Analog Video / Audio Decoder / Encoder

#	Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x000	VDLOSS*	HLOCK*	SLOCK*	FLD*	VLOCK*	NOVIDEO*	MONO*	DET50*
1	0x010								
2	0x020								
3	0x030								

* Read only bits

VDLOSS	1	Video not present. (sync is not detected in number of consecutive line periods specified by MISSCNT register)
	0	Video detected.
HLOCK	1	Horizontal sync PLL is locked to the incoming video source.
	0	Horizontal sync PLL is not locked.
SLOCK	1	Sub-carrier PLL is locked to the incoming video source.
	0	Sub-carrier PLL is not locked.
FLD	1	Even field is being decoded.
	0	Odd field is being decoded.
VLOCK	1	Vertical logic is locked to the incoming video source.
	0	Vertical logic is not locked.
NOVIDEO	Reserved for TEST.	
MONO	1	No color burst signal detected.
	0	Color burst signal detected.
DET50	0	60Hz source detected
	1	50Hz source detected

The actual vertical scanning frequency depends on the current standard invoked.

#	Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x001	VCR*	WKAIR*	WKAIR1*	VSTD*	NINTL*	VSHP		
1	0x011								
2	0x021								
3	0x031								

* Read only bits

VCR — VCR signal indicator

WKAIR — Weak signal indicator 2.

WKAIR1 — Weak signal indicator controlled by WKTH

VSTD
1 = Standard signal
0 = Non-standard signal

NINTL
1 = Non-interlaced signal
0 = interlaced signal

VSHP
Vertical Sharpness Control
0 = None (default)
7 = Highest
**Note: VSHP must be set to '0' if COMB = 0

#	Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x006	0	0	VACTIVE_XY[8]	VDELAY_XY[8]	HACITIVE_XY[9:8]		HDELAY_XY[9:8]	
1	0x016								
2	0x026								
3	0x036								
0	0x002	HDELAY_XY[7:0]							
1	0x012								
2	0x022								
3	0x032								

HDELAY_XY — This 10bit register defines the starting location of horizontal active pixel for display / record path. A unit is 1 pixel. The default value is 0x00F for NTSC and 0x00A for PAL.

#	Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x006	0	0	VACTIVE_XY[8]	VDELAY_XY[8]	HACITIVE_XY[9:8]		HDELAY_XY[9:8]	
1	0x016								
2	0x026								
3	0x036								
0	0x003	HACTIVE_XY[7:0]							
1	0x013								
2	0x023								
3	0x033								

HACTIVE_XY — This 10bit register defines the number of horizontal active pixel for display / record path. A unit is 1 pixel. The default value is decimal 720.

#	Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x006	0	0	VACTIVE_XY[8]	VDELAY_XY[8]	HACITIVE_XY[9:8]		HDELAY_XY[9:8]	
1	0x016								
2	0x026								
3	0x036								
0	0x004	VDELAY_XY[7:0]							
1	0x014								
2	0x024								
3	0x034								

VDELAY_XY — This 9bit register defines the starting location of vertical active for display / record path. A unit is 1 line. The default value is decimal 6.

#	Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x006	0	0	VACTIVE_XY[8]	VDELAY_XY[8]	HACITIVE_XY[9:8]		HDELAY_XY[9:8]	
1	0x016								
2	0x026								
3	0x036								
0	0x005	VACTIVE_XY[7:0]							
1	0x015								
2	0x025								
3	0x035								

VACTIVE_XY — This 9bit register defines the number of vertical active lines for display / record path. A unit is 1 line. The default value is decimal 240.

#	Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x007	HUE							
1	0x017								
2	0x027								
3	0x037								

HUE — These bits control the color hue as 2's complement number. They have value from +36° (7Fh) to -36° (80h) with an increment of 2.8°. The 2 LSB has no effect. The positive value gives greenish tone and negative value gives purplish tone. The default value is 0° (00h). This is effective only on NTSC system. The default is 00h.

#	Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x008	SCURVE	VSF	CTI		SHARPNESS			
1	0x018								
2	0x028								
3	0x038								

SCURVE — This bit controls the center frequency of the peaking filter. The corresponding gain adjustment is HFLT.
0 Low
1 center

VSF — This bit is for internal used. The default is 0.

CTI — CTI level selection. The default is 1.
0 None
3 Highest

SHARPNESS — These bits control the amount of sharpness enhancement on the luminance signals. There are 16 levels of control with '0' having no effect on the output image. 1 through 15 provides sharpness enhancement with 'F' being the strongest. The default is 1.

#	Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x009	CNTRST							
1	0x019								
2	0x029								
3	0x039								

CNTRST — These bits control the luminance contrast gain. A value of 100 (64h) has a gain of 1. The range adjustment is from 0% to 255% at 1% per step. The default is 64h.

VIN	Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x00A	BRIGHT							
1	0x01A								
2	0x02A								
3	0x03A								

BRIGHT — These bits control the brightness. They have value of –128 to 127 in 2's complement form. Positive value increases brightness. A value 0 has no effect on the data. The default is 00h.

#	Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x00B	SAT_U							
1	0x01B								
2	0x02B								
3	0x03B								

SAT_U — These bits control the digital gain adjustment to the U (or Cb) component of the digital video signal. The color saturation can be adjusted by adjusting the U and V color gain components by the same amount in the normal situation. The U and V can also be adjusted independently to provide greater flexibility. The range of adjustment is 0 to 200%. A value of 128 (80h) has gain of 100%. The default is 80h.

#	Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x00C	SAT_V							
1	0x01C								
2	0x02C								
3	0x03C								

SAT_V — These bits control the digital gain adjustment to the V (or Cr) component of the digital video signal. The color saturation can be adjusted by adjusting the U and V color gain components by the same amount in the normal situation. The U and V can also be adjusted independently to provide greater flexibility. The range of adjustment is 0 to 200%. A value of 128 (80h) has gain of 100%. The default is 80h.

#	Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x00D	SF*	PF*	FF*	KF*	CSBAD*	MCVSN*	CSTRIPE*	CTYPE2*
1	0x01D								
2	0x02D								
3	0x03D								

* Read only bits

SF — This bit is for internal use

PF — This bit is for internal use

FF — This bit is for internal use

KF — This bit is for internal use

CSBAD
1 Macrovision color stripe detection may be un-reliable

MCVSN
1 Macrovision AGC pulse detected.
0 Not detected.

CSTRIPE
1 Macrovision color stripe protection burst detected.
0 Not detected.

CTYPE2
This bit is valid only when color stripe protection is detected, i.e. if CSTRIPE=1,
1 Type 2 color stripe protection
0 Type 3 color stripe protection

#	Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x00E	DETSTUS*	STDNOW*			ATREG	STANDARD		
1	0x01E								
2	0x02E								
3	0x03E								

* Read only bits

DETSTUS
- 0 Idle
- 1 Detection in progress

STDNOW

Current standard invoked
- 0 NTSC (M)
- 1 PAL (B, D, G, H, I)
- 2 SECAM
- 3 NTSC4.43
- 4 PAL (M)
- 5 PAL (CN)
- 6 PAL 60
- 7 Not valid

ATREG
- 1 Disable the shadow registers
- 0 Enable VACTIVE and HDELAY shadow registers value depending on STANDARD. (Default)

STANDARD

Standard selection
- 0 NTSC (M)
- 1 PAL (B, D, G, H, I)
- 2 SECAM
- 3 NTSC4.43
- 4 PAL (M)
- 5 PAL (CN)
- 6 PAL 60
- 7 Auto detection (Default)

#	Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x00F	ATSTART	PAL60EN	PALCNEN	PALMEN	NTSC44EN	SECAMEN	PALBEN	NTSCEN
1	0x01F								
2	0x02F								
3	0x03F								

ATSTART	1	Writing 1 to this bit will manually initiate the auto format detection process. This bit is a self-clearing bit
	0	Manual initiation of auto format detection is done. (Default)
PAL60EN	1	Enable recognition of PAL60 (Default)
	0	Disable recognition
PALCNEN	1	Enable recognition of PAL (CN). (Default)
	0	Disable recognition
PALMEN	1	Enable recognition of PAL (M). (Default)
	0	Disable recognition
NTSC44EN	1	Enable recognition of NTSC 4.43. (Default)
	0	Disable recognition
SECAMEN	1	Enable recognition of SECAM. (Default)
	0	Disable recognition
PALBEN	1	Enable recognition of PAL (B, D, G, H, I). (Default)
	0	Disable recognition
NTSCEN	1	Enable recognition of NTSC (M). (Default)
	0	Disable recognition

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x041	0	0	0	0	0	0	vd34_108_pol	vd12_108_pol

VD34_108_POL Use falling edge to sample VD34 from 54 MHz to 108 MHz

VD12_108_POL Use falling edge to sample VD12 from 54 MHz to 108 MHz

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x042	PTRN_CTL							

PTRN_CTL Control setting for internal pattern generator. For testing purpose only.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x045	0	0	VSMODE	FLDPOL	HSPOL	VSPOL	DECVSMODE	DECFLDPOL

VSMODE Control the VS and field flag timing
- 0 VS and field flag is aligned with vertical sync of incoming video (Default)
- 1 VS and field flag is aligned with HS

FLDPOL Select the FLD polarity
- 0 Odd field is high
- 1 Even field is high (Default)

HSPOL Select the HS polarity
- 0 Low for sync duration (Default)
- 1 High for sync duration

VSPOL Select the VS polarity
- 0 Low for sync duration (Default)
- 1 High for sync duration

DECVSMODE 0 Default

DECFLDPOL 0 Default

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x046	AGCEN4	AGCEN3	AGCEN2	AGCEN1	AGCGAIN4[8]	AGCGAIN3[8]	AGCGAIN2[8]	AGCGAIN1[8]
0x047	AGCGAIN1[7:0]							
0x048	AGCGAIN2[7:0]							
0x049	AGCGAIN3[7:0]							
0x04A	AGCGAIN4[7:0]							

AGCENn — Select Video AGC loop function on VIN of channel n
- 0 AGC loop function enabled (recommended for most application cases) (default).
- 1 AGC loop function disabled. Gain is set by AGCGAINn

AGCGAINn — These registers control the AGC gain of channel n when AGC loop is disabled. Default value is 0F0h.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x04B	PD_BIAS	V_ADC_SAVE			0	0	0	YFLEN

PD_BIAS
- 1 Power down the bias of all 4 VADC
- 0 Do not power down the bias

V_ADC_SAVE — Power Saving Mode Selection.
- 0 Most Power Consuming
- 7 Most Power Saving

IREF
- 0 Internal current reference 1 for Video ADC (default)
- 1 Internal current reference increase 30% for Video ADC.

VREF
- 0 Internal voltage reference for Video ADC (default)
- 1 Internal voltage reference shut down for Video ADC

YFLEN — Analog Video CH1/CH2/CH3/CH4 anti-alias filter control
- 1 Enable (default)
- 0 Disable

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x04D	TST_ADC_VD1	ADC_SEL1			0	0	0	0

TST_ADC_VD1 0 Default

ADC_SEL1 0 Default

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x04E	TST_ADC_VD2	ADC_SEL2			0	0	0	0

TST_ADC_VD2 0 Default

ADC_SEL2 0 Default

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x04F	FRM		YNR		CLMD		PSP	

FRM Free run mode control
0 Auto (default)
2 Default to 60Hz
3 Default to 50Hz

YNR Y HF noise reduction
0 None(default)
1 Smallest
2 Small
3 Medium

CLMD Clamping mode control
0 Sync top
1 Auto (default)
2 Pedestal
3 N/A

PSP Slice level control
0 Low
1 Medium (default)
2 High

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x050	HFLT2				HFLT1			
0x051	HFLT4				HFLT3			

HFLTn — HFLTn controls the peaking function of channel n. Reserved for test purpose.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x052	CTEST	YCLEN	0	AFLTEN	GTEST	VLPF	CKLY	CKLC

CTEST — Clamping control for debugging use. (Test purpose only) (default 0)

YCLEN
- 1 Y channel clamp disabled (Test purpose only)
- 0 Enabled (default)

AFLTEN
- 1 Analog Audio input Anti-Aliasing Filter enabled (default)
- 0 Disabled

GTEST
- 1 Test (Test purpose only)
- 0 Normal operations (default)

VLPF — Clamping filter control (default 0)

CKLY — Clamping current control 1 (default 0)

CKLC — Clamping current control 2 (default 0)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x053	NT502	NT501						

NT501
- 1 Force the Video Decoder 1 to a special NTSC 50 Hz format
- 0 Do not force to NTSC 50 Hz format

NT502
- 1 Force the Video Decoder 2 to a special NTSC 50 Hz format
- 0 Do not force to NTSC 50 Hz format

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x054	NT504	NT503	DIV_RST	DOUT_RST	ACALEN	AADC_SAVE		

NT503 1 Force the Video Decoder 4 to a special NTSC 50 Hz format
0 Do not force to NTSC 50 Hz format

NT504 1 Force the Video Decoder 4 to a special NTSC 50 Hz format
0 Do not force to NTSC 50 Hz format

DIV_RST Audio ADC divider reset. This bit must be set to 0 again after reset.

DOUT_RST Audio ADC digital output reset for all channel. This bit must be setup up to 0 again after reset.

ACALEN Audio ADC Calibration control. This be must be set up to 0 again after enabled.

AADC_SAVE Audio ADC Power Saving Mode. 7 is most power saving.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x055	FLD*				VAV*			

FLD Status of the field flag for corresponding channel (*Read only)*
FLD [3:0] are FIELD ID for VIN3 to VIN0.
0 Odd field when FLDPOL (0x045) = 1
1 Even field when FLDPOL (0x045) = 1

VAV Status of the vertical active video signal for corresponding channel (*Read only).* VAV [3:0] is Vertical Active Video Signal for VIN3 to VIN0.
0 Vertical blanking time
1 Vertical active time

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x057	SHCOR				ANA_SW4	ANA_SW3	ANA_SW2	ANA_SW1

SHCOR These bits provide coring function for the sharpness control (default 3h)

ANA_SWn Control the analog input channel switch for VIN1 to VIN4 input
0 VIN_A channel is selected (default)
1 VIN_B channel is selected

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x058	PBW	DEM	PALSW	SET7	COMB	HCOMP	YCOMB	PDLY

PBW
1 Wide Chroma BPF BW (Default)
0 Normal Chroma BPF BW

DEM
Reserved (Default 1)

PALSW
1 PAL switch sensitivity low.
0 PAL switch sensitivity normal (Default)

SET7
1 The black level is 7.5 IRE above the blank level.
0 The black level is the same as the blank level (Default)

COMB
1 Adaptive comb filter for NTSC and PAL (Recommended). This setting is not for SECAM (Default)
0 Notch filter. For SECAM, always set to 0.

HCOMP
1 Operation mode 1 (Recommended) (Default)
0 Mode 0

YCOMB
1 Bypass Comb filter when no burst presence
0 No bypass (Default)

PDLY
0 Enable PAL delay line (default)
1 Disable PAL delay line

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x059	GMEN	CKHY		HSDLY				

GMEN
Reserved (Default 0)

CKHY
Color killer hysteresis.
0 Fastest (Default)
1 Fast
2 Medium
3 Slow

HSDLY
Reserved for test

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x05A	CTCOR		CCOR		VCOR		CIF	

CTCOR — These bits control the coring for CTI (Default 1h)

CCOR — These bits control the low level coring function for the Cb/Cr output (Default 0h)

VCOR — These bits control the coring function of vertical peaking (Default 1h)

CIF — These bits control the IF compensation level.
0 None (default)
1 1.5dB
2 3dB
3 6dB

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x05B	CLPEND				CLPST			

CLPEND — These 4 bits set the end time of the clamping pulse. Its value should be larger than the value of CLPST (Default 5h)

CLPST — These 4 bits set the start time of the clamping. It is referenced to PCLAMP position. (Default 0h)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x05C	NMGAIN				WPGAIN			FC27

NMGAIN — These bits control the normal AGC loop maximum correction value (Default 4h)

WPGAIN — Peak AGC loop gain control (Default 1h)

FC27
1 Normal ITU-R656 operation (Default)
0 Squared Pixel mode for test purpose only

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x05D	PEAKWT							

PEAKWT — These bits control the white peak detection threshold. Setting ‘FF’ can disable this function (Default D8h)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x05E	CLMPLD	CLMPL						

CLMPLD
0 Clamping level is set by CLMPL
1 Clamping level preset at 60d (Default)

CLMPL
These bits determine the clamping level of the Y channel (Default 3Ch)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x05F	SYNCTD	SYNCT						

SYNCTD
0 Reference sync amplitude is set by SYNCT
1 Reference sync amplitude is preset to 38h (Default)

SYNCT
These bits determine the standard sync pulse amplitude for AGC reference (Default 38h)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x060	AIGAIN2				AIGAIN1			
0x061	AIGAIN4				AIGAIN3			

AIGAINx
Audio Input ADC gain control

0 0.25
1 0.31
2 0.38
3 0.44
4 0.50
5 0.63
6 0.75
7 0.88
8 1.00 (default)
9 1.25
10 1.50
11 1.75
12 2.00
13 2.25
14 2.50
15 2.75

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x062	M_RLSWAP	RM_SYNC	RM_PBSEL		R_ADATM		R_MULTCH	

M_RLSWAP — Define the sequence of mixing and playback audio data on the ADATM pin

If RM_SYNC=0: I2S format

0 Mixing audio on position 0 and playback audio on position 8 (Default)

1 Playback audio on position 0 and mixing audio on position 8

If RM_SYNC=1: DSP format

0 Mixing audio on position 0 and playback audio on position 1 (Default)

1 Playback audio on position 0 and mixing audio on position 1

RM_SYNC — Define the digital serial audio data format for record and mixing audio on the ACLKR, ASYNR, ADATR and ADATM pin

0 I2S format (Default)

1 DSP format

RM_PBSEL — Select the output PlayBackIn data for the ADATM pin

0 First Stage PalyBackIn audio (Default)

1 Second Stage PalyBackIn audio

2 Third Stage PalyBackIn audio

3 Last Stage PalyBackIn audio

R_ADATM — Select the output mode for the ADATM pin

0 Digital serial data of mixing audio (Default)

1 Digital serial data of ADATR format record audio

2 Digital serial data of ADATM format record audio

R_MULTCH — Define the number of audio for record on the ADATR pin

0 2 audios (Default)

1 4 audios

2 8 audios

3 16 audios

Number of output data is limited as shown on Sequence of Multi-channel Audio Record table. Also, each output position data are selected by R_SEQ_0/R_SEQ_1/.../R_SEQ_F registers.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x063	AAUTO_MUTE	PBREFEN	VRSTSEL		FIRSTCNUM			

AAUTO_MUTE
1 When input Analog data is less than ADET_TH level, output PCM data will be set to 0. Audio DAC data input is 0x200.
0 No effect

PBREFEN
Audio ACKG Reference (refin) input select
0 ACKG has video VRST refin input selected by VRSTSEL register (Default)
1 ACKG has audio ASYNP refin input

VRSTSEL
Select VRST (V reset) signal on ACKG (Audio Clock Generator) refin input.
0 VIN0 Video Decoder Path VRST (default)
1 VIN1 Video Decoder Path VRST
2 VIN2 Video Decoder Path VRST
3 VIN3 Video Decoder Path VRST

FIRSTCNUM
Set up First Stage number on audio cascade mode connection.
Set up the value of (Cascade chip number-1). In 4 chips cascade case, this value is 3h for ALINK mode. In single chip application case, this doesn't need to be set up.
0 (default)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x064	R_SEQ_1				R_SEQ_0			
0x065	R_SEQ_3				R_SEQ_2			
0x066	R_SEQ_5				R_SEQ_4			
0x067	R_SEQ_7				R_SEQ_6			
0x068	R_SEQ_9				R_SEQ_8			
0x069	R_SEQ_B				R_SEQ_A			
0x06A	R_SEQ_D				R_SEQ_C			
0x06B	R_SEQ_F				R_SEQ_E			

R_SEQ
Define the sequence of record audio on the ADATR pin.
Refer to Table 16 for the detail of the R_SEQ_0 ~ R_SEQ_F.
The default value of R_SEQ_0 is "0", R_SEQ_1 is "1", and R_SEQ_F is "F".
0 AIN1
1 AIN2
: :
: :
14 AIN15
15 AIN16

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x06C	ADACEN	AADCEN	PB_ MASTER	PB_LRSEL	PB_SYNC	RM_8BIT	ASYNROEN	ACLKRMASTER

ADACEN — Audio DAC Function mode
- 0 Audio DAC function disable (test purpose only)
- 1 Audio DAC function enable (Default)

AADCEN — Audio ADC Function mode
- 0 Audio ADC function disable (test purpose only)
- 1 Audio ADC function enable (Default)

PB_MASTER — Define the operation mode of the ACLKP and ASYNP pin for playback.
- 0 All type I2S/DSP Slave mode (ACLKP and ASYNP is input) (Default)
- 1 TW5864 type I2S/DSP Master mode (ACLKP and ASYNP is output)

PB_LRSEL — Select the channel for playback.
- 0 Left channel audio is used for playback input (Default)
- 1 Right channel audio is used for playback input

PB_SYNC — Define the digital serial audio data format for playback audio on the ACLKP, ASYNP and ADATP pin.
- 0 I2S format (Default)
- 1 DSP format

RM_8BIT — Define output data format per one word unit on ADATR pin.
- 0 16bit one word unit output (Default)
- 1 8bit one word unit packed output

ASYNROEN — Define input/output mode on the ASYNR pin.
- 1 ASYNR pin is input
- 0 ASYNR pin is output (Default)

ACLKRMASTER — Define input/output mode on the ACLKR pin and set up audio 256xfs system processing
- 0 ACLKR pin is input. External 256xfs clock should be connected to ACLKR pin. This function is single chip Audio slave mode only.
- 1 ACLKR pin is output. Internal ACKG generates 256xfs clock (Default)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x06D	LAWMD		MIX_ DERATIO	MIX_MUTE				

LAWMD — Select u-Law/A-Law/PCM/SB data output format on ADATR and ADATM pin.
0 PCM output (default)
1 SB (Signed MSB bit in PCM data is inverted) output
2 u-Law output
3 A-Law output

MIX_DERATIO — Disable the mixing ratio value for all audio.
0 Apply individual mixing ratio value for each audio (default)
1 Apply nominal value for all audio commonly

MIX_MUTE[n] — Enable the mute function for audio channel AINn when n is 0 to 3. It effects only for mixing. When n = 4, it enable the mute function of the playback audio input. It effects only for single chip or the last stage chip
0 Normal
1 Muted (default)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x06E	MIX_RATIO2				MIX_RATIO1			
0x06F	MIX_RATIO4				MIX_RATIO3			
0x070	0	0	0	0	MIX_RATIOP			

MIX_RATIOn — Define the ratio values for audio mixing of channel AINn
MIX_RATIOP — Define the ratio values for audio mixing of playback audio input
If MRATIOMD = 0 (default)
0 0.25
1 0.31
2 0.38
3 0.44
4 0.50
5 0.63
6 0.75
7 0.88
8 1.00 (default)
9 1.25
10 1.50
11 1.75
12 2.00
13 2.25
14 2.50
15 2.75

If MRATIONMD = 1, Mixing ratio is MIX_RATIOn / 64

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x071	V_ADC_CKPOL	A_ADC_CKPOL	A_DAC_CKPOL	MIX_OUTSEL				

V_ADC_CKPOL Test purpose only (Default 0)

A_ADC_CKPOL Test purpose only (Default 0)

A_DAC_CKPOL Test purpose only (Default 0)

MIX_OUTSEL Define the final audio output for analog and digital mixing out.

0 Select record audio of channel 1
1 Select record audio of channel 2
2 Select record audio of channel 3
3 Select record audio of channel 4
4 Select record audio of channel 5
5 Select record audio of channel 6
6 Select record audio of channel 7
7 Select record audio of channel 8
8 Select record audio of channel 9
9 Select record audio of channel 10
10 Select record audio of channel 11
11 Select record audio of channel 12
12 Select record audio of channel 13
13 Select record audio of channel 14
14 Select record audio of channel 15
15 Select record audio of channel 16
16 Select playback audio of the first stage chip
17 Select playback audio of the second stage chip
18 Select playback audio of the third stage chip
19 Select playback audio of the last stage chip
20 Select mixed audio (default)
21 Select record audio of channel AIN51
22 Select record audio of channel AIN52
23 Select record audio of channel AIN53
24 Select record audio of channel AIN54

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x072	AAMPMD	ADET_FILT			ADET_TH4[4]	ADET_TH3[4]	ADET_TH2[4]	ADET_TH1[4]
0x073	ADET_TH2[3:0]				ADET_TH1[3:0]			
0x074	ADET_TH4[3:0]				ADET_TH3[3:0]			

AAMPMD — Define the audio detection method.
0 Detect audio if absolute amplitude is greater than threshold
1 Detect audio if differential amplitude is greater than Threshold (default)

ADET_FILT — Select the filter for audio detection (default 4h)
0 Wide LPF
: :
7 Narrow LPF

ADET_THn — Define the threshold value for audio detection of AINn (Default Ah)
0 Low value
: :
31 High value

If fs = 8kHz Audio Clock setting mode, Registers
0x072 = 0xC0
0x073 = 0xAA
0x074 = 0xAA
are typical setting.

If fs=16kHz/32kHz/44.1kHz/48kHz Audio Clock setting mode, Registers
0x072 = 0xE0
0x073 = 0xBB
0x074 = 0xBB
are typical setting.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x075	ACKI[7:0]							
0x076	ACKI[15:8]							
0x077	0	0	ACKI[21:16]					

ACKI — These bits control ACKI Clock Increment in ACKG block.
09B583h for fs = 8kHz is default

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x078	ACKN[7:0]							
0x079	ACKN[15:8]							
0x07A	0	0	0	0	0	0	ACKN[17:16]	

ACKN — These bits control ACKN Clock Number in ACKG block.
000100h for Playback Slave-in lock is default.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x07B	0	0	SDIV					

SDIV — These bits control SDIV Serial Clock Divider in ACKG block (Default 01h)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x07C	0	0	LRDIV					

LRDIV — These bits control LRDIV Left/Right Clock Divider in ACKG block (Default 20h)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x07D	APZ	APG			0	ACPL	SRPH	LRPH

APZ — These bits control Loop in ACKG block (Default 1)

APG — These bits control Loop in ACKG block (Default 4h)

ACPL — These bits control Loop closed/open in ACKG block

0 Loop closed

1 Loop open (recommended on typical application case) (Default)

SRPH — Reserved. These bits are not used in TW5864 chip.

LRPH — Reserved. These bits are not used in TW5864 chip.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x07E					AIGAIN5			

AIGAIN5 — Audio Input ADC gain control

16	0.25
17	0.31
18	0.38
19	0.44
20	0.50
21	0.63
22	0.75
23	0.88
24	1.00 (default)
25	1.25
26	1.50
27	1.75
28	2.00
29	2.25
30	2.50
31	2.75

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0C0	BGNDEN				BGNDCOL	AUTO_BGND	LIM_656	0

BGNDEN[n] Enable the background color for channel n for byte-interleave video decoder output.
0 Background color is disabled (Default)
1 Background color is enabled

BGNDCOL Select the background color when BGNDEN = "1" or when AUTO_BGND = "1" and Video Loss is detected
0 Blue color (Default)
1 Black color

AUTO_BGND Select the decoder background mode.
0 Manual background mode (Default)
1 Automatic background mode when No-video is detected

LIM_656 Clamp the Y and C value in the video stream
0 Maximum of Y is 254, Minimum of Y is 1
Maximum of C is 254, Minimum of Y is 1
1 Maximum of Y is 235, Minimum of Y is 16
Maximum of Y is 240, Minimum of Y is 16

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0C1	0	OUT_CHID	0	TST_EHAV_BLK	0	0	0	0

TST_EHAV_BLK Testing purpose only
1 Force the Y value to be 0 when HAV is high.
0 Normal Operation

OUT_CHID Enable the channel ID format in the horizontal blanking period
0 Disable the channel ID format (default)
1 Enable the channel ID format
The lowest 4 bits of Y and C pixel value during horizontal blanking is
Bit 3 Video Loss
Bit 2 Analog Mux A/B
Bit 1-0 Port ID

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0D0	AADC3OFS[9:8]		AADC2OFS[9:8]		AADC1OFS[9:8]		AADC0OFS[9:8]	
0x0D1	AADC0OFS[7:0]							
0x0D2	AADC1OFS[7:0]							
0x0D3	AADC2OFS[7:0]							
0X0D4	AADC3OFS[7:0]							
0x0D5	0	0	0	0	0	0	AADC4OFS[9:8]	
0x0D6	AADC4OFS[7:0]							

Digital ADC input data offset control. Digital ADC input data is adjusted by

ADJAADCn = AUDADCn + AADCnOFS

Where AUDADCn is 2's formatted Analog Audio ADC output, and AADCnOFS is adjusted offset value by 2's format. All default 10bit data value is 3EFh.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0D7	0	ADCISEL			AUDADCn[9:8]*		ADJAADCn[9:8]*	
0x0D8	AUDADCn[7:0]*							
0x0D9	ADJAADCn[7:0]*							

AUDADCn
`

Current Analog Audio n ADC Digital Output Value by 2's format
These value show the first input data value in front of Digital Audio Decimation Filtering process.

ADJAADCn

Current adjusted Audio ADC Digital input data value by 2's format. These value show the first input data value in front of Digital Audio Decimation Filtering process.

ADCISEL

Select AUDADCn, ADJAADCn Audio input number. AUDADCn and ADJAADCn read value shows following selected Audio input data.

0 AIN1
1 AIN2
2 AIN3
3 AIN4

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0DA	0	0	0	I2SO_RSEL				
0x0DB	0	0	0	I2SO_LSEL				
0x0DC	I2SRECSEL53		I2SRECSEL52		I2SRECSEL51		I2SRECSEL50	
0x0DD	A5OUT_OFF	ADATM_ I2SOEN	MIX_MUTE _A5	ADET_TH5				

A5OUT_OFF — AIN5 data output control on ADATR record signal.
- 0 Output AIN51/AIN52/AIN53/AIN54 record data on DATR
- 1 Not output AIN51/AIN52/AIN53/AIN54 record data on ADATR

ADATM_I2SOEN — Define ADATM pin output 2 word data to make standard I2S output.
- 0 Output Mixing or Playback data only on ADATM pin as specified by M_RLSWAP register (Default)
- 1 L/R data on ADATM pin is selected by I2SO_RSEL/I2SO_LSEL registers

MIX_MUTE_A5 — Audio input AIN5 mute function control
- 0 Normal
- 1 Muted

ADET_TH5 — AIN5 threshold value for audio detection

I2SO_RSEL/ I2SO_LSEL — Select L/R output data on ADATM pin when ADATM_I2SOEN=1. Both I2SO_RSEL and I2SO_LSEL select output data by following order.
- 0 Select record audio of channel 1(AIN0)
- 1 Select record audio of channel 2(AIN1)
- 2 Select record audio of channel 3(AIN2)
- 3 Select record audio of channel 4(AIN3)
- 4 Select record audio of channel 5(AIN4)
- 5 Select record audio of channel 6(AIN5)
- 6 Select record audio of channel 7(AIN6)
- 7 Select record audio of channel 8(AIN7)
- 8 Select record audio of channel 9(AIN8)
- 9 Select record audio of channel 10(AIN9)
- 10(Ah) Select record audio of channel 11(AIN10)
- 11(Bh) Select record audio of channel 12(AIN11)
- 12(Ch) Select record audio of channel 13(AIN12)
- 13(Dh) Select record audio of channel 14(AIN13)
- 14(Eh) Select record audio of channel 15(AIN14)
- 15(Fh) Select record audio of channel 16(AIN15)
- 16(10h) Select playback audio of the first stage chip (PB1)
- 17(11h) Select playback audio of the second stage chip (PB2)
- 18(12h) Select playback audio of the third stage chip (PB3)
- 19(13h) Select playback audio of the last stage chip (PB4)
- 20(14h) Select mixed audio
- 21(15h) Select record audio of channel 51(AIN51) (default)
- 22(16h) Select record audio of channel 52(AIN52)
- 23(17h) Select record audio of channel 53(AIN53)
- 24(18h) Select record audio of channel 54(AIN54)
- Others No audio output

I2SRECSEL5n Select output data of port n in the position below
0 AIN51
1 AIN52
2 AIN53
3 AIN54

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0DE					MIX_RATIO5			

MIX_RATIO5 Define the ratio values for audio mixing of channel AIN4 using MIX_RATIO4 to the ratio values for audio mixing of playback audio input

If MRATIOMD = 0 (default)
0 0.25
1 0.31
2 0.38
3 0.44
4 0.50
5 0.63
6 0.75
7 0.88
8 1.00 (default)
9 1.25
10 1.50
11 1.75
12 2.00
13 2.25
14 2.50
15 2.75

If MRATIONMD = 1, Mixing ratio is MIX_RATIO4 / 64

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0DF	ATHROUGH	ASYNSERIAL	ACLKR128	ACLKR64	AFS384	AIN5MD	0	0

ATHROUGH Default 0

ASYNSERIAL Default 0

ACLKR128 ACLKR clock output mode for special 16x8bit (total 128bit) data interface.
0 ACLKR output is normal (Default).
1 the number of ACLKR clock per fs is 128.This function is effective with RM_8BIT=1 8bit mode (special purpose).

ACLKR64 ACLKR clock output mode for special 4 word output interface. ACLKRMASTER=1 mode only.
0 ACLKR output is normal (Default)
1 the number of ACLKR clock per fs is 64.

AFS384 Special Audio fs Sampling mode.
0 Audio fs Sampling mode is normal 256xfs if AIN5 = 0. (Default)
1 Audio fs Sampling mode is 384xfs mode. In this mode, AIMANU=1, A1NUM=0, A2NUM=1, A3NUM=2, A4NUM = 3, A5NUM=4 setting are needed.

AIN5MD Audio Input process mode
0 AIN1/AIN2/AIN3/AIN4 4 audio input mode. This mode is 256xfs if AFS384 = 0. In this mode, AIN5 is not used.
1 AIN1/AIN2/AIN3/AIN4/AIN5 5 audio input mode. This mode is 320xfs mode if AFS384 = 0.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0E0	MRATIOMD	ADACTEST	0	0	0	0	0	0

MRATIOMD
1 Use a more exponential way to interpret the MRATIO. Perform the following transformation before using the ratio
0 ~ 3 => 4 ~ 7
4 ~ 7 => 8 ~ 14
8 ~ 11 => 16 ~ 28
12 ~ 15 => 32 ~ 44
0 Use the MRATIO as the ratio

ADACTEST Test feature for ADAC. Set to 0.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0E3	EXT_ADATP	ACLKPPOLO	ACLKRPOL	ACLKPPOLI	AFAUTO	AFMD		

EXT_ADATP — ADATP signal is coming from external ADPCM decoder, instead of on-chip ADPCM decoder.

ACLKPPOLO — ACLKP output signal polarity inverse

ACLKRPOL — ACLKR input signal polarity inverse.
0 Not inversed (Default)
1 Inversed

ACLKPPOLI — ACLKP input signal polarity inverse.
0 Not inversed (Default)
1 Inversed

AFAUTO — ACKI [21:0] control automatic set up with AFMD registers
This mode is only effective when ACLKRMASTER=1
0 ACKI [21:0] registers set up ACKI control
1 ACKI control is automatically set up by AFMD register values

AFMD — AFAUTO control mode
0 8kHz setting (Default)
1 16kHz setting
2 32kHz setting
3 44.1kHz setting
4 48kHz setting

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0E4	I2S8MODE	MASCKMD	PBINSWAP	ASYNRDLY	ASYNPDLY	ADATPDLY	INLAWMD	

I2S8MODE — 8bit I2S Record output mode.
0 L/R half length separated output (Default).
1 One continuous packed output equal to DSP output format.

MASCKMD — Audio Clock Master ACLKR output wave format.
0 High periods is one 27MHz clock period (default).
1 Almost duty 50-50% clock output on ACLKR pin. If this mode is selected, two times bigger number value need to be set up on the ACKI register. If AFAUTO=1, ACKI control is automatically set up even if MASCKMD=1.

PBINSWAP — Playback ACLKP/ASYNP/ADATP input data MSB-LSB swapping.
0 Not swapping
1 Swapping.

ASYNRDLY — ASYNR input signal delay.
0 No delay
1 Add one 27MHz period delay in ASYNR signal input

ASYNPDLY — ASYNP input signal delay.
0 no delay
1 add one 27MHz period delay in ASYNP signal input

ADATPDLY — ADATP input data delay by one ACLKP clock.
0 No delay (Default).This is for I2S type 1T delay input interface.
1 Add 1 ACLKP clock delay in ADATP input data. This is for left-justified type 0T delay input interface.

INLAWMD — Select u-Law/A-Law/PCM/SB data input format on ADATP pin.
0 PCM input (Default)
1 SB (Signed MSB bit in PCM data is inverted) input
2 u-Law input
3 A-Law input

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0E5	0	0	0	0	0	0	AINTPOFF	A5DETENA

AINTPOFF — Test feature for ADAC. Set to 0.

A5DETENA — Enable state register updating and interrupt request of audio AIN5 detection for each input
0 Disable state register updating and interrupt request
1 Enable state register updating and interrupt request

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0E7	HASYNC	OFDLY			DECOUTMD	0	0	0

HASYNC
1 The length of EAV to SAV is set up and fixed by HBLEN register
0 The length of SAV to EAV is setup and fixed by HACTIVE registers

OFDLY
FIELD output delay
0h 0H line delay FIELD output (601 mode only)
1h~6h 1H ~ 6H line delay FIELD output
7h Reserved

DECOUTMD
Default 1

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0E8	HBLEN							

HBLEN
These bits are effective when HASYNC bit is set to 1. These bits setup the length of EAV to SAV code when HASYNC bit is 1. Normal value is (Total pixel per line – HACTIVE) value.

NTSC/PAL-M (60Hz) 8Ah = 858 – 720
PAL/SECAM (50Hz) 90h = 864 – 720

If register 0x0E[3] (ATREG for CH1) is set to 0, this value changes into 8Ah or 90h at audio video format detection initial time automatically according to CH1 video detection status.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0E9	CKLM	YDLY			0	0	0	0

CKLM
Color Killer mode.
0 Normal (Default)
1 Fast (For special application)

TDLY
Luma delay fine adjustment. This 2's complement number provides –4 to +3 unit delay control (Default 3h)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0EA	0	0	ADECRST	0	VDEC4RST	VDEC3RST	VDEC2RST	VDEC1RST

ADECRST
A 1 written to this bit resets the audio portion to its default state but all register content remains unchanged. This bit is self-cleared.

VDECnRST
A 1 written to this bit resets the VINn path Video Decoder portion to its default state but all register content remain unchanged. This bit is self cleared.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0EB	MISSCNT				HSWIN			

MISSCNT — These bits set the threshold for horizontal sync miss count threshold (Default 4h)

HSWIN — These bits determine the VCR mode detection threshold (Default 4h)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0EC	PCLAMP							

PCLAMP — These bits set the clamping position from the PLL sync edge (Default 2Ah)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0ED	VLCKI		VLCKO		VMODE	DETV	AFLD	VINT

VLCKI — Vertical lock in time
0 Fastest (Default)
:
3 Slowest.

VLCKO — Vertical lock out time
0 Fastest (Default)
:
3 Slowest

VMODE — This bit controls the vertical detection window
1 Search mode
0 Vertical countdown mode (Default)

DETV
1 Recommended for special application only
0 Normal Vsync logic (Default)

AFLD — Auto field generation control
0 Off (Default)
1 On

VINT — Vertical integration time control
1 Short
0 Normal (Default)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0EE	BSHT			VSHT				

BSHT — Burst PLL center frequency control (Default 0h)

VSHT — Vsync output delay control in the increment of half line length (Default 0h)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0EF	CKILLMAX		CKILLMIN					

CKILLMAX — These bits control the amount of color killer hysteresis. The hysteresis amount is proportional to the value (Default 1h)

CKILLMIN — These bits control the color killer threshold. Larger value gives lower killer level (Default 28h)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0F0	COMBMD	HTL			VTL			

COMBMD
0 Adaptive mode (Default)
1 Fixed comb

HTL — Adaptive Comb filter threshold control 1 (Default 4h)

VTL — Adaptive Comb filter threshold control 2 (Default Ch)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0F1	HPLC	EVCNT	PALC	SDET	0	BYPASS	0	0

HPLC — Reserved for internal use (Default 0)

EVCNT
1 Even field counter in special mode
0 Normal operation (Default)

PALC — Reserved for future use (Default 0)

SDET — ID detection sensitivity. A '1' is recommended (Default 1)

BYPASS — It controls the standard detection and should be set to ‘1’ in normal use (Default 1)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0F2	HPM		ACCT		SPM		CBW	

HPM — Horizontal PLL acquisition time.
- 3 Fast
- 2 Auto1 (Default)
- 1 Auto2
- 0 Normal

ACCT — ACC time constant
- 0 No ACC
- 1 Slow
- 2 Medium (Default)
- 3 Fast

SPM — Burst PLL control
- 0 Slowest
- 1 Slow (Default)
- 2 Fast
- 3 Fastest

CBW — Chroma low pass filter bandwidth control. Refer to filter curves (Default 1)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0F3	NKILL	PKILL	SKILL	CBAL	FCS	LCS	CCS	BST

NKILL
1 Enable noisy signal color killer function in NTSC mode (Default)
0 Disabled

PKILL
1 Enable automatic noisy color killer function in PAL mode (Default)
0 Disabled

SKILL
1 Enable automatic noisy color killer function in SECAM Mode (Default)
0 Disabled

CBAL
0 Normal output (Default)
1 Special output mode.

FCS
1 Force decoder output value determined by CCS
0 Disabled (Default)

LCS
1 Enable pre-determined output value indicated by CCS when video loss is detected
0 Disabled (Default)

CCS
When FCS is set high or video loss condition is detected when LCS is set high, one of two colors display can be selected.
1 Blue color
0 Black (Default)

BST
1 Enable blue stretch
0 Disabled (Default)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0F4	0	0	MONITOR					
0x0F5	HREF*							

These registers are for test purpose only. The MONITOR is used to select the HREF status of a certain video decoder port in Reg0x0F5 HREF

MONITOR Value
Select video decoder port for register 0x0F5
00h VIN0 Video Decoder Path HREF [9:2] value
10h VIN1 Video Decoder Path HREF [9:2] value
20h VIN2 Video Decoder Path HREF [9:2] value
30h VIN3 Video Decoder Path HREF [9:2] value

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0F6	0	CVSTD1*			CVFMT1			
0x0F7	0	CVSTD2*			CVFMT2			
0x0F8	0	CVSTD3*			CVFMT3			
0x0F9	0	CVSTD4*			CVFMT4			

CVSTDn
CVFMTn

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0FA	IDX1		NSEN1/SSEN1/PSEN1/WKTH1					
0x0FB	IDX2		NSEN2/SSEN2/PSEN2/WKTH2					
0x0FC	IDX3		NSEN3/SSEN3/PSEN3/WKTH3					
0x0FD	IDX4		NSEN4/SSEN4/PSEN4/WKTH4					

NSENn/SSENn/PSENn/WKTHn shared the same 6 bits in the register. IDXn is used to select which of the four parameters is being controlled. The write sequence is a two steps process unless the same register is written. A write of {ID, 000000} selects one of the four registers to be written. A subsequent write will actually write into the register. (Default 0h)

IDXn
- 0 Controls the NTSC color carrier detection sensitivity (NSENn) (Default 1Ah)
- 1 Controls the SECAM ID detection sensitivity (SSENn) (Default 20h)
- 2 Controls the PAL ID detection sensitivity (PSENn) (Default 1Ch)
- 3 Controls the weak signal detection sensitivity (WKTHn) (Default 2Ah)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x0FE	DEV_ID *					REV_ID *		

* Read only

DEV_ID The TW5864 product ID code is 01000

REV_ID The revision number is 0h

Front-End Scalers / Multiplexers

#	Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x200	IN_PIC_WIDTH							
1	0x204								
2	0x208								
3	0x20C								
4	0x210								
5	0x214								
6	0x218								
7	0x21C								
8	0x220								
9	0x224								
10	0x228								
11	0x22C								
12	0x230								
13	0x234								
14	0x238								
15	0x23C								

IN_PIC_WIDTH	Input picture width setting for scalers. The value is the line width / 4. (Default 720 / 4)

#	Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x201		IN_PIC_HEIGHT						
1	0x205								
2	0x209								
3	0x20D								
4	0x211								
5	0x215								
6	0x219								
7	0x21D								
8	0x221								
9	0x225								
10	0x229								
11	0x22D								
12	0x231								
13	0x235								
14	0x239								
15	0x23D								

IN_PIC_HEIGHT	Input picture height setting for scalers. The value is the height / 4. (Default 240 / 4)

#	Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x202	OUT_PIC_WIDTH							
1	0x206								
2	0x20A								
3	0x20E								
4	0x212								
5	0x216								
6	0x21A								
7	0x21E								
8	0x222								
9	0x226								
10	0x22A								
11	0x22E								
12	0x232								
13	0x236								
14	0x23A								
15	0x23E								

OUT_PIC_WIDTH Output picture width setting for scalers. This value is used to decide the width of HD1 / CIF. The QCIF width will be derived from this setting. The setting value is the CIF width / 4. (Default 360 / 4)

#	Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x203	FLD_POL	OUT_PIC_HEIGHT						
1	0x207								
2	0x20B								
3	0x20F								
4	0x213								
5	0x217								
6	0x21B								
7	0x21F								
8	0x223								
9	0x227								
10	0x22B								
11	0x22F								
12	0x233								
13	0x237								
14	0x23B								
15	0x23F								

OUT_PIC_HEIGHT Output picture height setting for scalers. This value is used to decide The height of CIF. The QCIF height will be derived from this setting. The value for is CIF height / 4. (default 120 / 4)

FLD_POL Reverse the field ID used by the scaler.

#	Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x240		PV0_LM_RES		PV0_LM_EN		PV0_LM_CHID		
1	0x241								
2	0x242								
3	0x243								
4	0x244								
5	0x245								
6	0x246								
7	0x247								
8	0x248								

PV0_LM_CHID — Select the channels included in PV0 port line interleaving mode
The PV0 port supports up to 9 channels (0x240 ~ 0x248) of video selected from on-chip video decoders VIN1 ~ VIN4 and off-chip video decoders through VD1.

000 VIN1
001 VIN2
010 VIN3
011 VIN4
100 VD1, channel 1
101 VD1, channel 2
110 VD1, channel 3
111 VD1, channel 4

PV0_LM_RES — Specify the picture size (resolution of line mode pictures)

00 D1
01 CIF
10 Half D1

PV0_LM_EN — Enable the entry specified in 0x240 ~ 0x248 to insert a channel into PV0

1 Enable
0 Disable

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x24C	LM_SUPERFRAME_SIZE[15:8]							
0x24D	LM_SUPERFRAME_SIZE[7:0]							
0x24E							PV0__HBI_SIZE[9:8]	
0x24F	PV0_LM_HBI_SIZE[7:0]							

LM_SUPERFRAME_SIZE — Specify the superframe size in line interleaving mode

PV0_LM_HBI_SIZE — Specify the horizontal blanking size of each line in line interleaving mode of port PV0

#	Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x250		PV1_LM_RES		PV1_LM_EN		PV1_LM_CHID		
1	0x251								
2	0x252								
3	0x253								
4	0x254								
5	0x255								
6	0x256								
7	0x257								
8	0x258								

PV1_LM_CHID — Select the channels included in PV1 port line interleaving mode
The PV1 port supports up to 9 channels (0x250 ~ 0x258) of video selected from off-chip video decoders through VD2 and VD3.

000 VD2, channel 1
001 VD2, channel 2
010 VD2, channel 3
011 VD2, channel 4
100 VD3, channel 1
101 VD3, channel 2
110 VD3, channel 3
111 VD3, channel 4

PV1_LM_RES — Specify the picture size (resolution of line mode pictures)

00 D1
01 CIF
10 Half D1

PV0_LM_EN — Enable the entry specified in 0x250 ~ 0x258 to insert a channel into PV1

1 Enable
0 Disable

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x25E							PV1_LM_HBI_SIZE[9:8]	
0x25F	PV1_LM_HBI_SIZE[7:0]							

PV1_LM_HBI_SIZE — Specify the horizontal blanking size of each line in line interleaving mode of port PV1

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x260					CLR_EN	CROP_EN	SMALL_FR	PAL

PAL NTSC/PAL control for mode detection
0 NTSC
1 PAL

SMALL_FR Small frame size setting for simulation
0 Normal frame size
1 Small frame size

CROP_EN Enable cropping from 720 to 704

CLR_EN Enable reset at every field. For internal testing only.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x263	LM_FRM_HEIGHT[7:0]							
0x264				LM_FIFO_VRES[8]			LM_FRM_HEIGHT[9:8]	
0x265	LM_FIFO_VRES[7:0]							

LM_FRM_HEIGHT Internal testing only

LM_FIFO_VRES Internal testing only

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x268	PV0_LM_OV [7:0]							
0x269	PV0_LM_UN [7:0]							
0x26A				PV0_LM_UN[8]				PV0_LM_OV [8]

PV0_LM_OV [8:0] Internal testing only

PV0_LM_UN [8:0] Internal testing only

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x26B	PV1_LM_OV [7:0]							
0x26C	PV1_LM_UN [7:0]							
0x26D				PV1_LM_UN[8]				PV1_LM_OV [8]

PV1_LM_OV [8:0] Internal testing only

PV1_LM_UN [8:0] Internal testing only

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x2D0	INTERRUPT[7:0]							
0x2D1	INTERRUPT[15:8]							
0x2D2	INTERRUPT[23:16]							
0x2D3	INTERRUPT[31:24]							
0x2D4	INTERRUPT[39:32]							
0x2D5	INTERRUPT[47:40]							
0x2D6	INTERRUPT[55:48]							
0x2D7	INTERRUPT[63:56]							
0x2E0	INTERRUPT[71:64]							
0x2E1	INTERRUPT[79:72]							
0x2E2	INTERRUPT[87:80]							
0x2E3	INTERRUPT[95:88]							

INTERRUPT Interrupt status register from the front-end. Write "1" to each bit to clear the interrupt

15:0 Motion detection interrupt for channel 0 ~ 15
31:16 Night detection interrupt for channel 0 ~ 15
47:32 Blind detection interrupt for channel 0 ~ 15
63:48 No video interrupt for channel 0 ~ 15
79:64 Line mode underflow interrupt for channel 0 ~ 15
95:80 Line mode overflow interrupt for channel 0 ~ 15

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x2D8	INTERRUPT_MASK[7:0]							
0x2D9	INTERRUPT[_MASK 15:8]							
0x2DA	INTERRUPT_MASK [23:16]							
0x2DB	INTERRUPT_MASK [31:24]							
0x2DC	INTERRUPT_MASK [39:32]							
0x2DD	INTERRUPT_MASK [47:40]							
0x2DE	INTERRUPT_MASK [55:48]							
0x2DF	INTERRUPT_MASK [63:56]							
0x2E8	INTERRUPT_MASK[71:64]							
0x2E9	INTERRUPT_MASK[79:72]							
0x2EA	INTERRUPT_MASK[87:80]							
0x2EB	INTERRUPT_MASK[95:88]							

INTERRUPT_MASK Interrupt mask register for interrupts in 0x2D0 ~ 0x2D7

15:0 Motion detection interrupt for channel 0 ~ 15
31:16 Night detection interrupt for channel 0 ~ 15
47:32 Blind detection interrupt for channel 0 ~ 15
63:48 No video interrupt for channel 0 ~ 15
79:64 Line mode underflow interrupt for channel 0 ~ 15
95:80 Line mode overflow interrupt for channel 0 ~ 15

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x2F0	INTERRUPT_SUMMARY[7:0]							
0x2F1					INTERRUPT_SUMMARY[11:8]			

INTERRUPT_SUMMARY Interrupt summary register for interrupts & interrupt mask from in 0x2D0 ~ 0x2D7 and 0x2D8 ~ 0x2DF

bit 0: interrupt occurs in 0x2D0 & 0x2D8
bit 1: interrupt occurs in 0x2D1 & 0x2D9
bit 2: interrupt occurs in 0x2D2 & 0x2DA
bit 3: interrupt occurs in 0x2D3 & 0x2DB
bit 4: interrupt occurs in 0x2D4 & 0x2DC
bit 5: interrupt occurs in 0x2D5 & 0x2DD
bit 6: interrupt occurs in 0x2D6 & 0x2DE
bit 7: interrupt occurs in 0x2D7 & 0x2DF
bit 8: interrupt occurs in 0x2E0 & 0x2E8
bit 9: interrupt occurs in 0x2E1 & 0x2E9
bit 10: interrupt occurs in 0x2E2 & 0x2EA
bit 11: interrupt occurs in 0x2E3 & 0x2EB

Motion / Blind / Night Detection

#	Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x300								
1	0x308								
2	0x310								
3	0x318								
4	0x320								
5	0x328								
6	0x330								
7	0x338			MD_DIS		MD_STRB	MD_STRB_E N	BD_CELLSENS	
8	0x340								
9	0x348								
10	0x350								
11	0x358								
12	0x360								
13	0x368								
14	0x370								
15	0x378								

MD_DIS — Disable the motion and blind detection.
0 Enable motion and blind detection (default)
1 Disable motion and blind detection

MD_STRB — Request to start motion detection on manual trigger mode
0 None Operation (default)
1 Request to start motion detection

MD_STRB_EN — Select the trigger mode of motion detection
0 Automatic trigger mode of motion detection (default)
1 Manual trigger mode for motion detection

BD_CELSENS — Define the threshold of cell for blind detection.
0 Low threshold (More sensitive) (default)
: :
3 High threshold (Less sensitive)

#	Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x301	MD_TMPSENS				MD_PIXEL_OS			
1	0x309								
2	0x311								
3	0x319								
4	0x321								
5	0x329								
6	0x331								
7	0x339								
8	0x341								
9	0x349								
10	0x351								
11	0x359								
12	0x361								
13	0x369								
14	0x371								
15	0x379								

MD_TMPSENS Control the temporal sensitivity of motion detector.
0 More Sensitive (default)
: :
15 Less Sensitive

MD_PIXEL_OS Adjust the horizontal starting position for motion detection
0 0 pixel (default)
: :
15 15 pixels

#	Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x302	MD_REFFLD	MD_FIELD		MD_LVSENS				
1	0x30A								
2	0x312								
3	0x31A								
4	0x322								
5	0x32A								
6	0x332								
7	0x33A								
8	0x342								
9	0x34A								
10	0x352								
11	0x35A								
12	0x362								
13	0x36A								
14	0x372								
15	0x37A								

MD_REFFLD — Control the updating time of reference field for motion detection.
0 Update reference field every field (default)
1 Update reference field according to MD_SPEED

MD_FIELD — Select the field for motion detection.
0 Detecting motion for only odd field (default)
1 Detecting motion for only even field
2 Detecting motion for any field
3 Detecting motion for both odd and even field

MD_LVSENS — Control the level sensitivity of motion detector.
0 More sensitive (default)
: :
15 Less sensitive

#	Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x303	MD_SELSENS		MD_SPEED					
1	0x30B								
2	0x313								
3	0x31B								
4	0x323								
5	0x32B								
6	0x333								
7	0x33B								
8	0x343								
9	0x34B								
10	0x353								
11	0x35B								
12	0x363								
13	0x36B								
14	0x373								
15	0x37B								

MD_CELSENS — Define the threshold of sub-cell number for motion detection.

0 Motion is detected if 1 sub-cell has motion (More sensitive) (default)
1 Motion is detected if 2 sub-cells have motion
2 Motion is detected if 3 sub-cells have motion
3 Motion is detected if 4 sub-cells have motion (Less sensitive)

MD_SPEED — Control the velocity of motion detector.
Large value is suitable for slow motion detection.
In MD_DUAL_EN = 1, MD_SPEED should be limited to 0 ~ 31.

0 1 field intervals (default)
1 2 field intervals
: :
61 62 field intervals
62 63 field intervals
63 Not supported

#	Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x304	MD_SPSENS				BD_LVSENS			
1	0x30C								
2	0x314								
3	0x31C								
4	0x324								
5	0x32C								
6	0x334								
7	0x33C								
8	0x344								
9	0x34C								
10	0x354								
11	0x35C								
12	0x364								
13	0x36C								
14	0x374								
15	0x37C								

MD_SPSENS Control the spatial sensitivity of motion detector.
0 More Sensitive (default)
: :
15 Less Sensitive

BD_LVSENS Define the threshold of level for blind detection.
0 Low threshold (More sensitive) (default)
: :
15 High threshold (Less sensitive)

#	Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0	0x305	ND_TMPSENS				ND_LVSENS			
1	0x30D								
2	0x315								
3	0x31D								
4	0x325								
5	0x32D								
6	0x335								
7	0x33D								
8	0x345								
9	0x34D								
10	0x355								
11	0x35D								
12	0x365								
13	0x36D								
14	0x375								
15	0x37D								

ND_TMPSENS Define the threshold of temporal sensitivity for night detection.
0 Low threshold (More sensitive) (default)
: :
15 High threshold (Less sensitive)

ND_LVSENS Define the threshold of level for night detection.
0 Low threshold (More sensitive) (default)
: :
3 High threshold (Less sensitive)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x380	MD_BASE_ADDR[7:0[							
0x381					MD_BASE_ADDR[11:8]			

MD_BASE_ADDR — The base address of the motion detection buffer. This address is in unit of 64K bytes. The generated DDR address will be {MD_BASE_ADDR, 16'h0000}. The default value should be 12'h000

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x382					RGR_MOTION_SEL			

RGR_MOTION_SEL — This controls the channel of the motion detection result shown in register 0x3A0 ~ 0x3B7. Before reading back motion result, always set this first.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x386	MD_STRB [7:0]*							
0x387	MD_STRB [15:8]*							
0x388	NOVID_DET[7:0]*							
0x389	NOVID_DET[15:8]*							
0x38A	MD_DET[7:0]*							
0x38B	MD_DET[15:8]*							
0x38C	BD_DET[7:0]*							
0x38D	BD_DET[15:8]*							
0x38E	ND_DET[7:0]*							
0x38F	ND_DET[15:8]*							

* Read Only

MD_STRB[n] — MD strobe has been performed at channel n (read only)

NOVID_DET[n] — NO_VIDEO Detected from channel n (read only)

MD_DET[n] — Motion Detected from channel n (read only)

BD_DET[n] — Blind Detected from channel n (read only)

ND_DET[n] — Night Detected from channel n (read only)

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x3A0	MOTION_FLAG[7:0]							
0x3A1	MOTION_FLAG[15:8]							
0x3A2	MOTION_FLAG[23:16]							
0x3A3	MOTION_FLAG[31:24]							
0x3A4	MOTION_FLAG[39:32]							
0x3A5	MOTION_FLAG[47:40]							
0x3A6	MOTION_FLAG[55:48]							
0x3A7	MOTION_FLAG[63:56]							
0x3A8	MOTION_FLAG[71:64]							
0x3A9	MOTION_FLAG[79:72]							
0x3AA	MOTION_FLAG[87:80]							
0x3AB	MOTION_FLAG[95:88]							
0x3AC	MOTION_FLAG[103:96]							
0x3AD	MOTION_FLAG[111:104]							
0x3AE	MOTION_FLAG[119:112]							
0x3AF	MOTION_FLAG[127:120]							
0x3B0	MOTION_FLAG[135:128]							
0x3B1	MOTION_FLAG[143:136]							
0x3B2	MOTION_FLAG[151:144]							
0x3B3	MOTION_FLAG[159:152]							
0x3B4	MOTION_FLAG[167:160]							
0x3B5	MOTION_FLAG[175:168]							
0x3B6	MOTION_FLAG[183:176]							
0x3B7	MOTION_FLAG[191:184]							

MOTION_FLAG — 192 bit motion flag of the channel specified by RGR_MOTION_SEL in 0x382

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x3B8	MD_DI_CNT[7:0]*							
0x3B9							MD_DI_CNT[9:8]*	

* Read only

MD_DI_CNT — The motion cell count of a specific channel selected by 0x382. This is for DI purpose.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x3BA	MD_DI_CELLSENS							
0x3BB	MD_DI_LVSENS							

MD_DI_CELLSENS — The motion detection cell sensitivity for DI purpose

MD_DI_LVSENS — The motion detection threshold level for DI purpose

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x3E0	MOTION_MASK[7:0]							
0x3E1	MOTION_ MASK [15:8]							
0x3E2	MOTION_ MASK [23:16]							
0x3E3	MOTION_ MASK [31:24]							
0x3E4	MOTION_ MASK [39:32]							
0x3E5	MOTION_ MASK [47:40]							
0x3E6	MOTION_ MASK [55:48]							
0x3E7	MOTION_ MASK [63:56]							
0x3E8	MOTION_ MASK [71:64]							
0x3E9	MOTION_ MASK [79:72]							
0x3EA	MOTION_ MASK [87:80]							
0x3EB	MOTION_ MASK [95:88]							
0x3EC	MOTION_ MASK [103:96]							
0x3ED	MOTION_ MASK [111:104]							
0x3EE	MOTION_ MASK [119:112]							
0x3EF	MOTION_ MASK [127:120]							
0x3F0	MOTION_ MASK [135:128]							
0x3F1	MOTION_ MASK [143:136]							
0x3F2	MOTION_ MASK [151:144]							
0x3F3	MOTION_ MASK [159:152]							
0x3F4	MOTION_ MASK [167:160]							
0x3F5	MOTION_ MASK [175:168]							
0x3F6	MOTION_ MASK [183:176]							
0x3F7	MOTION_ MASK [191:184]							

MOTION_MASK 192 bit motion mask of the channel specified by MASK_CH_SEL in 0x3FE

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x3FE				MASK_CH_SEL				

MASK_CH_SEL The channel selection to access masks in 0x3E0 ~ 0x3F7

Clock PLL / Analog IP Control

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xEB0	CLK81_LOCK	CLK81_PD	EXT_CLK81_SEL	CLK81_IREF	CLK81_CPX4		CLK81_LPX4	

CLK81_LPX4 — 81 MHz clock PLL loop filter select
- 0 80K Ohms
- 1 40K Ohms (default)
- 2 30K Ohms
- 3 20K Ohms

CLK81_CPX4 — 81 MHz clock PLL charge pump select
- 0 1μA
- 1 5μA (default)
- 2 10μA
- 3 15μA

CLK81_IREF — 81 MHz clock PLL current control
- 0 Low current (default)
- 1 Higher current (30% more)

EXT_CLK81_SEL
- 0 Select 81 MHz clock from internal PLL (default)
- 1 Select 81 MHz clock from EXT_CLK81 pin

CLK81_PD
- 0 Do not power down 81 MHz PLL (default)
- 1 Power down 81 MHz PLL

CLK81_LOCK — PLL Lock signal. Used for FPGA mode only. Read only.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xEB8	CLK108_LOCK	CLK108_PD		CLK108_IREF	CLK108_CPX4		CLK108_LPX4	

CLK108_LPX4 — 108 MHz clock PLL loop filter select
- 0 80K Ohms
- 1 40K Ohms (default)
- 2 30K Ohms
- 3 20K Ohms

CLK108_CPX4 — 108 MHz clock PLL charge pump select
- 0 1μA
- 1 5μA (default)
- 2 10μA
- 3 15μA

CLK108_IREF — 108 MHz clock PLL current control
- 0 Low current (default)
- 1 Higher current (30% more)

CLK108_PD
- 0 Do not power down 108 MHz PLL
- 1 Power down 108 MHz PLL

CLK108_LOCK — The 108 MHz clock PLL is locked. Used for FPGA mode only. Read Only.

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xEB9		DBG_CODEC		DBG_CLK108	DBG_DLL_SEL	DBG_DLL	DBG_SYSPLL	DBG_CLK81

DBG_CLK81	0	Don't 81 MHz PLL output to EXT_CLK81
	1	Send CLK81 PLL output to EXT_CLK81 pin
DBG_SYSPLL	0	Don't send SYSPLL output to EXT_SYSCLK pin
	1	Send SYSPLL output to EXT_SYSCLK pin
DBG_DLL	0	When DBG_CLK108 = 1, the TP1 output 108 MHz clock from 108 MHz PLL
	1	The TP1 output DLL0 or DLL1 test output
DBG_DLL_SEL	0	When DBG_DLL is 1, TP1 output DLL0 test signal
	1	When DBG_DLL is 1, TP1 output DLL1 test signal
DBG_CLK108	0	Do not output 108 MHz PLL output to TP1 pin
	1	Output 108 MHz PLL output to TP1 pin when DBG_DLL is 0
DBG_CODEC	0	Disable CODEC test signal output
	1	Enable CODEC test signal output

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xEC4	EXT_VADC	EXT_AADC	A_DAC_PD	A_ADC_PD	V_ADC_PD			

V_ADC_PD[n]	1	Power down channel n video ADC
	0	Do not power down video ADC
A_ADC_PD	1	Power down audio ADC
	0	Do not power down audio ADC
A_DAC_PD	1	Power down audio DAC
	0	Do not power down audio DAC
EXT_AADC	1	Use external digital input to bypass audio ADC
	0	Use audio ADC output
EXT_VADC	1	Use external digital input to bypass video ADC
	0	Use video ADC output

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xEC5	EXT_ADAC	VADC_CKPOL	ADAC_CKPOL	AADC_CKPOL				

EXT_ADAC	1	ADPCM decoder output ADATP to external audio DAC or I2S receiver (ADATP pin is output)
	0	ADATP is pin is input
VADC_CKPOL		Reverse the clock polarity for video ADC
ADAC_CKPOL		Reverse the clock polarity for audio DAC
AADC_CKPOL		Reverse the clock polarity for audio ADC

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xEC6			ADAC_IBCTL					
0xEC7	ADAC_LPFBIAS							
0xEC8	ADAC_LPF_SEL			ADAC_IB_OTA			ADAC_BIAS	
0xEC9						ADAC_TEST		

ADAC_IBCTL	Internal Testing Features
ADAC_LPFBIAS	Internal Testing Features
ADAC_BIAS	Internal Testing Features
ADAC_IB_OTA	Internal Testing Features
ADAC_LPF_SEL	Internal Testing Features
ADAC_TEST	Internal Testing Features

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xEE6					DDRA_DLL_DQS_SEL0			
0xEE7					DDRA_DLL_DQS_SEL1			
0xEE8					DDRA_DLL_CLK90_SEL			
0xEE9	DDRA_DLL_TEST_SEL						DDRA_DLL_TAP_S	

DDRA_DLL_DQS_SEL0 Select input DQS0 delay phase

4'h0: delay 1/32 clock phase
4'h1: delay 2/32 clock phase
....
4'hE: delay 15/32 clock phase
4'hF: by pass DLL

DDRA_DLL_DQS_SEL1 input DQS1 delay phase

4'h0: delay 1/32 clock phase
4'h1: delay 2/32 clock phase
....
4'hE: delay 15/32 clock phase
4'hF: by pass DLL

DDRA_DLL_CLK90_SEL Select the phase of 90 degree CLK generated from DLL. (for write data DQ)

4'h0: delay 1/32 clock phase
4'h1: delay 2/32 clock phase
....
4'hE: delay 15/32 clock phase
4'hF: by pass DLL

DDRA_DLL_TAP_S DLL internal charge pump setting, set to 2'b01;

DDRA_DLL_TEST_SEL DLL test output signal select (For internal testing only)

00xx DLL debug output (see DLL IP for details)
01xx DQS0 output
10xx DQS1 output
11xx Clock 90 DLL output

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xEEB					DDRB_DLL_DQS_SEL0			
0xEEC					DDRB_DLL_DQS_SEL1			
0xEED					DDRB_DLL_CLK90_SEL			
0xEEE	DDRB_DLL_TEST_SEL						DDRB_DLL_TAP_S	

DDRB_DLL_DQS_SEL0 Select input DQS0 delay phase

4'h0: delay 1/32 clock phase
4'h1: delay 2/32 clock phase
....
4'hE: delay 15/32 clock phase
4'hF: by pass DLL

DDRB_DLL_DQS_SEL1 input DQS1 delay phase
4'h0: delay 1/32 clock phase
4'h1: delay 2/32 clock phase
....
4'hE: delay 15/32 clock phase
4'hF: by pass DLL

DDRB_DLL_CLK90_SEL Select the phase of 90 degree CLK generated from DLL. (for write data DQ)
4'h0: delay 1/32 clock phase
4'h1: delay 2/32 clock phase
....
4'hE: delay 15/32 clock phase
4'hF: by pass DLL

DDRB_DLL_TAP_S DLL internal charge pump setting, set to 2'b01;

DDRB_DLL_TEST_SEL DLL test output signal select (For internal testing only)
00xx DLL debug output (see DLL IP for details)
01xx DQS0 output
10xx DQS1 output
11xx Clock 90 DLL output

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xEF0	int_resetn	dll_resetn	mux_resetn					

int_resetn Software reset for VD front-end

dll_resetn Software reset for DLL

mux_resetn Software reset for mux_core

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xEF8	PV_CLK_DLY1				PV_CLK_DLY0			
0xEF9	PV_CLK_DLY3				PV_CLK_DLY2			

PV_CLK_DLYn PV output clock delay control

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xEFA	PV1_MD	PV1_SEL			PV0_MD	PV0_SEL		
0xEFB	PV3_MD	PV3_SEL			PV2_MD	PV2_SEL		

PVn_MD 1 Insert motion detection flag into the video stream for preview port n.

0 Do not insert motion detection flag into the video stream for preview port n

PV0_ SEL Preview port 0 selection

001 Output external TW2866 through VD1 port in 108 MHz byte-interleaved format

010 Output external TW2866 through VD2 port in 108 MHz byte-interleaved format

011 Output external TW2866 through VD3 port in 108 MHz byte-interleaved format

100 Output on-chip VIN1 in 27 MHz single channel format

101 Output on-chip VIN1/VIN2 in 54 MHz byte-interleaved format

110 Output on-chip VIN1/VIN2/VIN3/VIN4 in 108 MHz byte-interleaved format

111 Output on-chip VIN1~VIN4 and off-chip VD1 video stream in line-interleaved format from

PV1_ SEL Preview port 1 selection

00X Output external TW2866 through VD1 port in 108 MHz byte-interleaved format

010 Output external TW2866 through VD2 port in 108 MHz byte-interleaved format

011 Output external TW2866 through VD3 port in 108 MHz byte-interleaved format

100 Output on-chip VIN2 in 27 MHz single channel format

101 Output on-chip VIN3/VIN4 in 54 MHz byte-interleaved format

111 Output off-chip TW2866 video stream through VD2/ VD3 video stream in line-interleaved format from

PV2_ SEL Preview port 2 selection

0XX Output external TW2866 through VD2 port in 108 MHz

byte-interleaved format

1XX Output on-chip VIN3 in 27 MHz single channel format

PV3_ SEL Preview port 3 selection

0XX Output external TW2866 through VD3 port in 108 MHz byte-interleaved format

1XX Output on-chip VIN4 in 27 MHz single channel format

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xEFC	PV_CLK_SEL2		PV_CLK_SEL					PV_CLK_POL

PV_CLK_POL Reverse the preview module clock polarity

PV_CLK_SEL Select the preview on-chip module clock rate for PV port 0, 1, and 3

00 27 MHz

01 54 MHz

10 81 MHz

11 108 MHz

PV_CLK_SEL2 Select the preview on-chip module clock rate for PV port 2

00 27 MHz

01 54 MHz

10 Reserved

11 108 MHz

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xEFD	VD3_CK_POL	VD2_CK_POL	VD1_CK_POL		PV3_CK_POL	PV2_CK_POL	PV1_CK_POL	PV0_CK_POL

PVn_CK_POL Reverse the preview port n clock polarity

VDn_CK_POL Reverse the VD port n input clock polarity

Address	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0xEFE			PV_CLKO_SEL2		PV_CLKO_SEL		VD_CLKO_SEL	

VD_CLKO_SEL Select the output clock for external video decoder. This is used for FPGA mode only

00 27 MHz

01 54 MHz

1X 108 MHz

PV_CLKO_SEL Select the output clock for preview ports

00 27 MHz

01 54 MHz

10 81 MHz

11 108 MHz

PV_CLKO_SEL2 Select the output clock for preview ports

00 27 MHz

01 54 MHz

10 Reserved

11 108 MHz

Parametric Information

AC/DC Electrical Parameters

TABLE 21. CHARACTERISTICS

PARAMETER	SYMBOL	MIN (NOTE 1)	TYPICAL	MAX (NOTE 1)	UNITS
POWER SUPPLY					
Power Supply — Digital I/O	V_{DDO}	2.97	3.3	3.63	V
Power Supply — SSTL I/O	$V_{DDOSSTL}$	2.3	2.5	2.7	V
Power Supply — SYSPLL	$V_{DDSYSPLL}$	2.97	3.3	3.63	V
Power Supply — C108PLL	V_{DDSPLL}	2.97	3.3	3.63	V
Power Supply — C81PLL	$V_{DDCLK81PLL}$	2.97	3.3	3.63	V
Power Supply — Video Decoder A/D	$V_{DDVADC1}$, $V_{DDVADC2}$, $V_{DDVADC3}$, $V_{DDVADC4}$,	2.97	3.3	3.63	V
Power Supply — Audio Decoder A/D, D/A	V_{DDAADC}, V_{DDADAC},	2.97	3.3	3.63	V
Power Supply — DLL	V_{DDDLL}	1.08	1.2	1.32	V
Power Supply — SSTL Core	V_{DDSSTL}	1.08	1.2	1.32	V
Power Supply — Digital Core	V_{DDI}	1.08	1.2	1.32	V
Voltage Reference for SSTL PAD	$V_{REFSSTL}$	-	$V_{DDOSSTL}/2$	-	V
Analog CVBS Video ADC Supply current	$I_{VDDVADC}$	-	60	-	mA
Analog Audio ADC/DAC	$I_{VDDAADC}$, $I_{VDDADAC}$,		40		mA
Digital I/O Supply Current	I_{VDDO}	-	110	-	mA
Digital I/O SSTL Supply Current	$I_{VDDOSSTL}$		160		mA
PLL Supply Current	$I_{VDDSYSPLL}$, $I_{VDDSPLL}$, $I_{VDDCLK81PLL}$	-	10	-	mA
Internal Core Supply Current	I_{VDDI},	-	275	-	mA
SSTL Core Supply Current	$I_{VDDSSTL}$	-	180	-	mA
DLL Supply Current	$I_{IVDDDLL}$	-	10	-	mA
SSTL Reference Supply Current	$I_{VREFSSTL}$	-	10	-	mA
Ambient Operating Temperature	T_A	0		+70	°C
DIGITAL INPUTS					
Input High Voltage (TTL)	V_{IH}	2.0	-	3.6	V
Input Low Voltage (TTL)	V_{IL}	-0.3	-	0.8	V

PARAMETER	SYMBOL	MIN (NOTE 1)	TYPICAL	MAX (NOTE 1)	UNITS
Input High Current (V_{IN} = V_{DD})	I_{IH}	-	-	10	µA
Input Low Current (V_{IN} = VSS)	I_{IL}	-	-	–10	µA
Input Capacitance (f =1MHz, V_{IN} = 2.4V)	C_{IN}	-	6	-	pF
DIGITAL OUTPUTS					
Output High Voltage (I_{OH} = –4mA)	V_{OH}	2.4	-	V DD33	V
Output Low Voltage (I_{OL} = 4mA)	V_{OL}	-	-	0.4	V
3-State Current	I_{OZ}	-	-	10	µA
Output Capacitance	C_O	-	6	-	pF
ANALOG INPUT					
Analog Pin Input voltage at VIN1A, VIN1B, VIN2A, VIN2B, VIN3, VIN3B, VIN4A, VIN4B, AIN1, AIN2, AIN3, AIN4, AIN5 Input Range (AC Coupling Required)	Vi	0	1.0	2.0	Vpp
Analog Pin Input Capacitance	C_A	-	6	-	pF
ADCS					
ADC Resolution	ADCR	-	10	-	bits
ADC Integral Non-linearity	AINL	-	±1	-	LSB
ADC Differential non-linearity	ADNL	-	±1	-	LSB
ADC Clock Rate	f_{ADC}	24	27	30	MHz
HORIZONTAL PLL					
Line Frequency (50Hz)	f_{LN}	-	15.625	-	KHz
Line Frequency (60Hz)	f_{LN}	-	15.734	-	KHz
Static Deviation	Δf_H	-	-	6.2	%
SUBCARRIER PLL					
Subcarrier Frequency (NTSC-M)	f_{SC}	-	3579545	-	Hz
Subcarrier Frequency (PAL-BDGHI)	f_{SC}	-	4433619	-	Hz
Subcarrier Frequency (PAL-M)	f_{SC}	-	3575612	-	Hz
Subcarrier Frequency (PAL-N)	f_{SC}	-	3582056	-	Hz
Lock In Range	Δf_H	±450	-	-	Hz
CRYSTAL SPEC					
Nominal Frequency (Fundamental)		-	27	-	MHz
Deviation		-	-	±50	ppm
Temperature Range	Ta	0	-	70	°C
Load Capacitance	CL	-	20	-	pF

PARAMETER	SYMBOL	MIN (NOTE 1)	TYPICAL	MAX (NOTE 1)	UNITS
Series Resistor	RS	-	80	-	Ω

NOTE:

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

DDR Interface AC Characteristics

TABLE 22. DDR INTERFACE AC CHARACTERISTICS

SYMBOL	PARAMETER	MIN (NOTE 1)	TYPICAL	MAX (NOTE 1)
$SLEW_R$	Input Signal Minimum Rising Slew Rate	1.0 V/ns		
$SLEW_F$	Input Signal Minimum Falling Slew Rate	1.0 V/ns		
$V_{IH}(ac)$	Maximum AC Input Logic High	$V_{REFSSTL}$ + 0.31V		
$V_{IH}(dc)$	Minimum DC Input Logic High	$V_{REFSSTL}$ + 0.15V		$V_{DDOSSTL}$ + 0.3V
$V_{IL}(ac)$	Minimum AC Input Logic Low			$V_{REFSSTL}$ – 0.31V
$V_{IL}(dc)$	Maximum DC Input Logic Low	-0.3V		$V_{REFSSTL}$ – 0.15V
V_{SWING}	Input Maximum Swing			1.5V

DDR Interface AC Timing

TABLE 23. DDR INTERFACE AC TIMING

SYMBOL	PARAMETER	MIN (ns) (NOTE 1)	TYP (NS)	MAX (ns) (NOTE 1)
t_{AC}	Access Window of DQ Input from CK/CK#	-0.7		0.7
t_{DQSCK}	Access Window of DQS Input from CK/CK#	-0.6		0.6
$t_{CK(avg)}$ CL = 3.0	Clock Cycle Time Measured at either Rising or Falling Edge	5		7.5
t_{CH}	Average Clock High Level Width	0.45CK		0.55CK
t_{CL}	Average Clock Low Level Width	0.45CK		0.55CK
$t_{PER_JIT\ (PK-PK)}$	DDR Clock Period Jitter (Peak to Peak)		0.93	1.15
t_{HP}	Half Clock Period	min(tCH,tCL)		max(t_{CH},t_{CL})
t_{DQSQ}	DQS – DQ Skew, DQS to Last DQ Valid, Per Group	0		0.6
t_{QH}	DQS – DQ Hold, DQS to First DQ to go Non-valid, per Group			$t_{HP\ (min)}$ – 0.5
t_{DQSS}	Write Command to DQS First Latching Transition	0.72CK		1.28CK
t_{DSS}	DQS Falling Edge to CK Rising Setup Time	0.25CK		
t_{DSH}	DQS Falling Edge from CK Rising Hold Time	0.25CK		
t_{HZ}	Data Hi-Z Windows from CK/CK#			0.7

SYMBOL	PARAMETER	MIN (ns) (NOTE 1)	TYP (NS)	MAX (ns) (NOTE 1)
t_{LZ}	Data Low-Z windows from CK/CK#	-0.7		
t_{WPRE}	DQS Write Preamble	0.25CK		
t_{WPST}	DQS Write Postamble	0.4CK		0.6CK
t_{RPRE} CL = 3.0	DQS Read Preamble	0.9CK		1.1CK
t_{RPST}	DQS Read Postamble	0.4CK		0.6CK
t_{DQSH}	DQS High Pulse Width	0.35CK		
t_{DQSL}	DQS Low Pulse Width	0.35CK		
t_{DS}	DQ and DM Output Setup Time Relative to DQS	0.6		
t_{DH}	DQ and DM Output Hold Time Relative to DQS	0.6		
t_{IS}	Address and Control Output Setup Time	0.8		
t_{IH}	Address and Control Output Hold Time	0.8		

NOTE:

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
2. The Vref on the evaluation is 1.25v. VDDQ is 2.5v.
3. CK: clock period
4. For all the timing, please refer to the figures below.

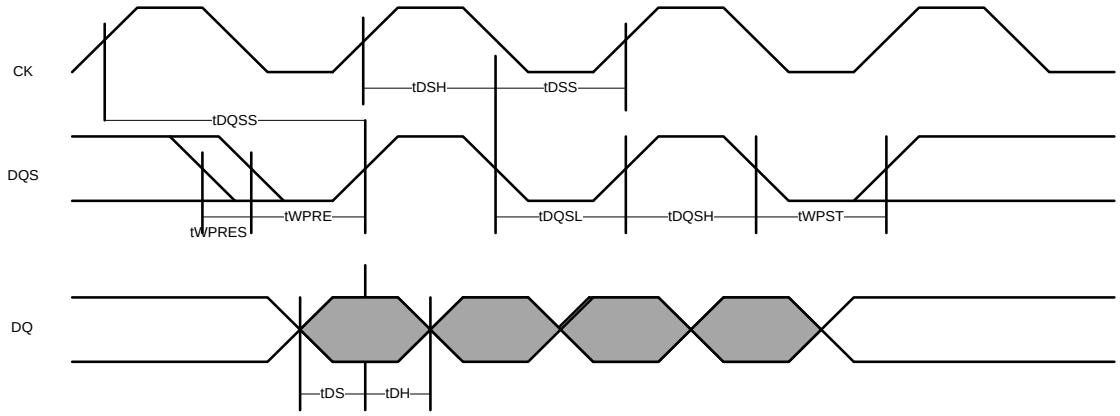


FIGURE 47. DDR INTERFACE OUTPUT TIMING

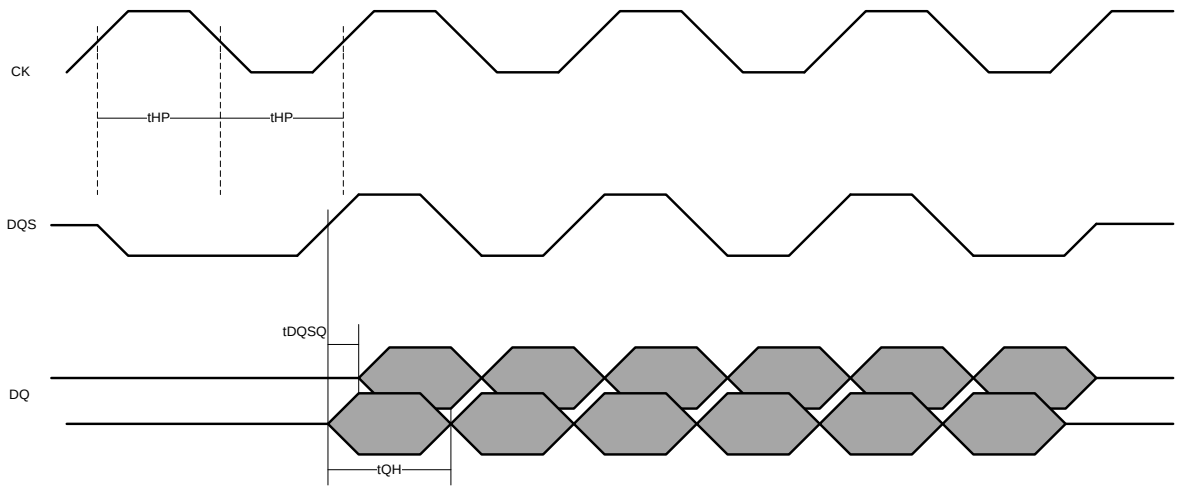


FIGURE 48. DDR INTERFACE INPUT TIMING (I)

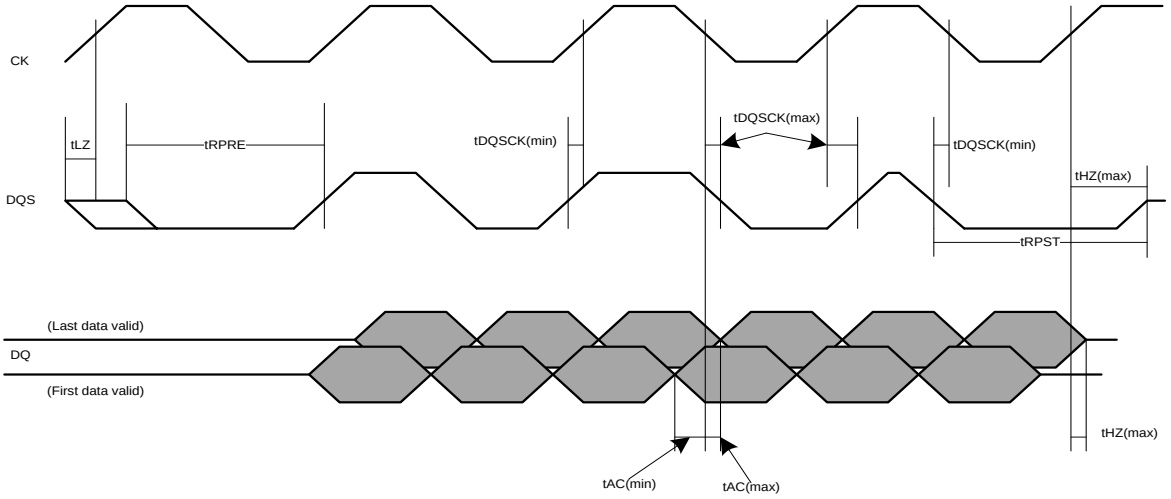


FIGURE 49. DDR INTERFACE INPUT TIMING (II)

PCI Interface AC Timing

TABLE 24. PCI INTERFACE AC TIMING

SYMBOL	PARAMETER	66 MHZ		33 MHZ		
		MIN (NOTE 1)	MAX (NOTE 1)	MIN (NOTE 1)	MAX (NOTE 1)	UNITS
t_{SU}	Input Setup Time to PCI_CLK – Bused Signals	3	-	7	-	ns
$t_{SU(PTP)}$	Input Setup Time to PCI_CLK – Point-to-Point	5	-	10, 12(4)	-	
t_H	Input Hold Time from PCI_CLK	0	-	0	-	
t_{VAL}	PCI_CLK to Signal Valid Delay – Bused Signals	2	6	2	11	
$t_{VAL(PTP)}$	PCI_CLK to Signal Valid Delay – Point-to-Point	2	6	2	12	
t_{ON}	Float to Active Delay	2	-	2	-	
t_{OFF}	Active to Float Delay	-	14	-	28	
t_{CYCLE}	PCI_CLK Cycle Time	15	30	30		
t_{HIGH}	PCI_CLK High Time	6	-	11		
t_{LOW}	PCI_CLK Low Time	6	-	11		
t_{RST}	Reset Active Time After Power Stable	1		1		ms
$t_{RST-CLK}$	Reset Active Time After PCI_CLK Stable	100		100		µs
$t_{RST-OFF}$	Reset Active to Output Float		40		40	ns

NOTE:

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
2. See PCI Signal Timing Measurement Conditions.
3. All interface signals are synchronized to PCI_CLK.
4. Point-to-point signals are PCI_REQ_N, PCI_GNT_N. Bused signals are PCI_AD, PCI_CBE_N, PCI_PAR, PCI_PERR_N, PCI_SERR_N, PCI_STOP_N, PCI_FRAME_N, PCI_IRDY_N, PCI_TRDY_N, PCI_DEVSEL_N, and PCI_IDSEL.
5. REQ_N signals have a setup of 10 and GNT_N signals have a setup of 12.

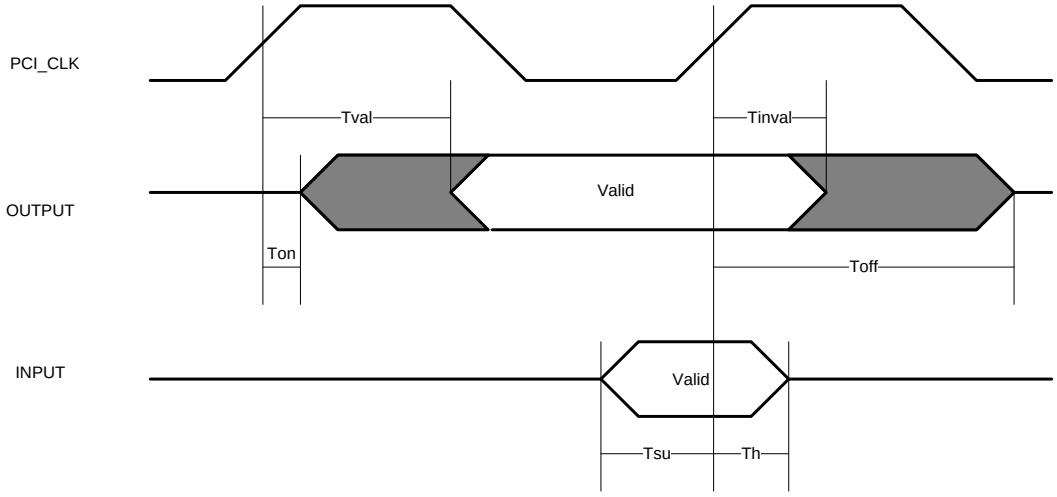


FIGURE 50. PCI INTERFACE TIMING CONDITION

Video Interface AC Timing

TABLE 25. VIDEO INTERFACE AC TIMING

SYMBOL	PARAMETER	MIN (NOTE 5)	MAX (NOTE 5)	UNITS
t_{SU}	VDx Input Setup Time to VD_CLKx	3	-	ns
t_H	VDx Input Hold Time from VD_CLKx	0	-	
t_{DELAY}	Delay from PV_CLKx to PV_DATAx	2	7	

NOTE:

1. VD_CLKx – VD_CLK1, VD_CLK2, VD_CLK3
2. VDx – VD1 [7:0], VD2 [7:0], VD3 [7:0]
3. PV_CLKx – PV_CLK0, PV_CLK1, PV_CLK2, PV_CLK3
4. PV_DATAx – PV_DATA0 [7:0], PV_DATA1 [7:0], PV_DATA2 [7:0], PV_DATA [7:0]
5. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

I2C Interface AC Timing

TABLE 26. I2C INTERFACE AC TIMING

SYMBOL	PARAMETER	MIN (NOTE 1)	MAX (NOTE 1)	UNITS
t_{BF}	Bus Free Time Between STOP and START	1.3		µs
t_{S_SDAT}	SDAT Setup Time	100		
t_{H_SDAT}	SDAT Hold Time		0.9	
t_{S_STA}	Setup Time for START Condition	0.6		
t_{H_STA}	Hold Time for START Condition	0.6		
t_{S_STO}	Setup Time for STOP Condition	0.6		
t_R	Rising Time for SDAT and SCLK		300	
t_F	Falling Time for SDAT and SCLK		300	
C_{BUS}	Capacity Load for Each Bus Line		400	pF
F_{SCLK}	SCLK Clock Frequency		400	KHz

NOTE:

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

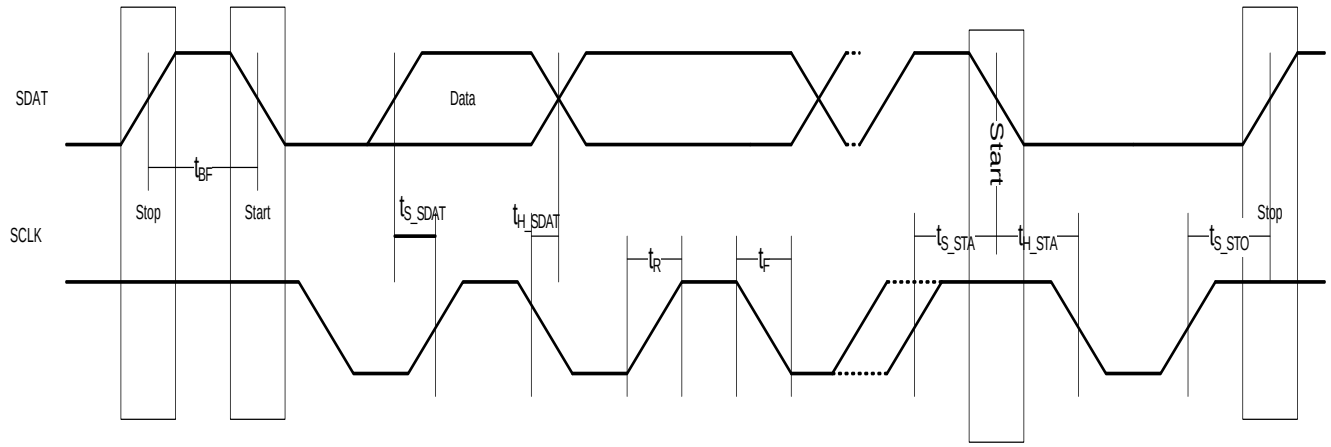


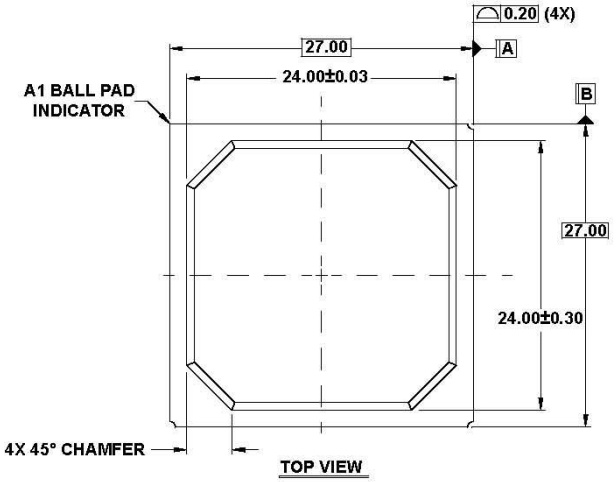
FIGURE 51. I2C INTERFACE TIMING CONDITION

Package Outline Drawing

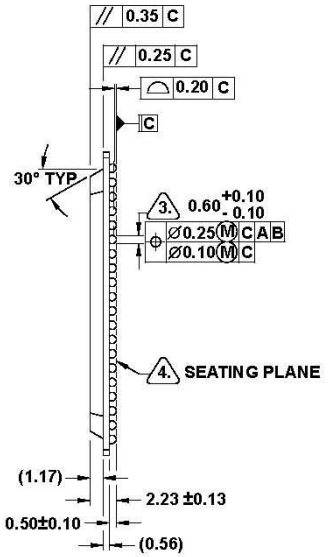
V352.27x27

352 PLASTIC BALL GRID ARRAY PACKAGE

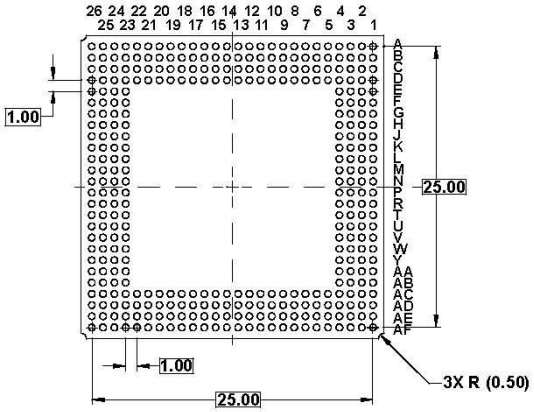
Rev 0, 3/11



TOP VIEW



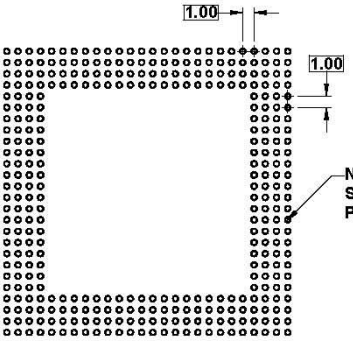
SIDE VIEW



BOTTOM VIEW

NOTES:

1. All dimensions and tolerances conform to ASME Y14.5-1994.
2. Dimensions are in millimeters.
3. Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
4. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
5. This drawing confirms to the JEDEC registered outline MS-034 variation AAL-1.
6. Dimensions in ( ) are for reference only



TYPICAL RECOMMENDED LAND PATTERN

Life Support Policy

These products are not authorized for use as critical components in life support devices or systems.

Revision History

DATE	REVISION	CHANGES NOTE
January 10, 2012	FN7961.1	Corrected lead finish note in “Ordering Information” on page 6 to reflect e2 classification instead of e1. Changed from: “These Intersil Pb-free WLCSP and BGA packaged products employ special Pb-free material sets; molding compounds/die attach materials and SnAgCu - e1 solder ball terminals, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free WLCSP and BGA packaged products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.” to: “These Intersil Pb-free BGA packaged products employ special Pb-free material sets; molding compounds/die attach materials and SnAg –e2 solder ball terminals, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free BGA packaged products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.”
December 1, 2011	FN7961.0	Revised datasheet from rev A1 chip into rev B1 (1) Added 0xD0F0, 0xD0F8 register (2) Added bit 7 of 0x18004 register (3) Added bit 7 of 0x1800C register (4) Added 0x18050, 0x18060, 0x18064 registers (5) Added 0x180C0 ~ 0x180DC registers (6) Remove unused 0x0040 register (7) Added 0xB004 ~ 0xB018 registers (8) Added missing description of 0x4018, 0x402C, x4048 (9) Revise register description of 0xA000 ~ 0xA00C, 0xEE6 ~0xEEE (10) Added AC timing for various digital interfaces (11) Fixed cross reference errors Modified the ordering info from TW5864-BA1-GR to TW5864-BB1-CR. This datasheet is for bonding option A/B/C.

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