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December 2011

# FDS6911

# Dual N-Channel Logic Level PowerTrench<sup>®</sup> MOSFET 20V, 7.5A, $13m\Omega$

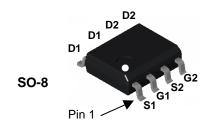
## **General Description**

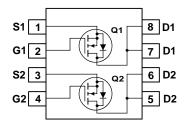
These N-Channel Logic Level MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.

### **Features**

- $r_{DS(on)} = 13 \text{ m}\Omega$  @ V<sub>GS</sub> = 10 V  $r_{DS(on)} = 17 \text{ m}\Omega$  @ V<sub>GS</sub> = 4.5 V
- Fast switching speed
- Low gate charge
- High performance trench technology for extremely low R<sub>DS(ON)</sub>
- High power and current handling capability





# Absolute Maximum Ratings T<sub>A</sub>=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V <sub>DSS</sub>	Drain-Source Voltage		20	V
V <sub>GSS</sub>	Gate-Source Voltage		± 20	V
I <sub>D</sub>	Drain Current - Continuous	(Note 1a)	7.5	Α
	– Pulsed		20	
P <sub>D</sub>	Power Dissipation for Single Operation	(Note 1a)	1.6	W
		(Note 1b)	1.0	
		(Note 1c)	0.9	
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperat	ture Range	-55 to +150	°C

## **Thermal Characteristics**

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78	°C/W
R <sub>eJC</sub>	Thermal Resistance, Junction-to-Case	(Note 1)	40	°C/W

**Package Marking and Ordering Information** 

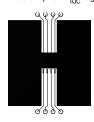
Device Marking	Device	Reel Size	Tape width	Quantity
FDS6911	FDS6911	13"	12mm	2500 units

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Char	acteristics		1			
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, \qquad I_{D} = 250 \mu\text{A}$	20			V
$\Delta BV_{DSS} \over \Delta T_{J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu A$ , Referenced to 25°C		28		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	$V_{DS} = 20 \text{ V},  V_{GS} = 0 \text{ V}$ $V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55^{\circ}\text{C}$			1 10	μА
$I_{GSS}$	Gate-Source Leakage	$V_{GS} = \pm 20 \text{ V},  V_{DS} = 0 \text{ V}$			±100	nA
On Chara	acteristics (Note 2)					
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \ \mu A$	1	1.8	3	V
$\Delta V_{GS(th)} \over \Delta T_J$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250 \mu A$ , Referenced to 25°C		-4.7		mV/°C
r <sub>DS(on)</sub>	Static Drain–Source On–Resistance	$V_{GS} = 10 \text{ V},  I_D = 7.5 \text{ A}$ $V_{GS} = 4.5 \text{ V},  I_D = 6.5 \text{ A}$ $V_{GS} = 10 \text{ V},  I_D = 7.5 \text{ A},  T_J = 125 ^{\circ}\text{C}$		10.6 13 14.5	13 17 20	mΩ
I <sub>D(on)</sub>	On-State Drain Current	$V_{GS} = 10 \text{ V},  V_{DS} = 5 \text{ V}$	20			Α
<b>g</b> FS	Forward Transconductance	$V_{DS} = 5 \text{ V}, \qquad I_{D} = 7.5 \text{ A}$		36		S
Dynamic	Characteristics					
C <sub>iss</sub>	Input Capacitance	$V_{DS} = 15 \text{ V},  V_{GS} = 0 \text{ V},$		1130		pF
C <sub>oss</sub>	Output Capacitance	f = 1.0 MHz		300		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			100		pF
R <sub>G</sub>	Gate Resistance	$V_{GS} = 15 \text{ mV}, f = 1.0 \text{ MHz}$		2.4		Ω
Switchin	g Characteristics (Note 2)					
t <sub>d(on)</sub>	Turn-On Delay Time	$V_{DD} = 15 \text{ V},  I_D = 1 \text{ A},$		9	18	ns
t <sub>r</sub>	Turn-On Rise Time	$V_{GS} = 10 \text{ V},  R_{GEN} = 6 \Omega$		5	10	ns
t <sub>d(off)</sub>	Turn-Off Delay Time			26	42	ns
t <sub>f</sub>	Turn-Off Fall Time			7	14	ns
$Q_{g(TOT)}$	Total Gate Charge at Vgs=10V			17	24	nC
Q <sub>g</sub>	Total Gate Charge at Vgs=5V	$V_{DD} = 15 \text{ V},  I_D = 7.5 \text{ A},$		9	13	nC
$Q_{gs}$	Gate-Source Charge			3.1		nC
$Q_{gd}$	Gate-Drain Charge			2.7		nC

Electrical Characteristics TA = 25°C unless otherwise noted						
Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Drain-Sou	Drain-Source Diode Characteristics and Maximum Ratings					
Is	Maximum Continuous Drain-Source D	ain-Source Diode Forward Current 1.3 A			Α	
V <sub>SD</sub>	Drain–Source Diode Forward Voltage	$V_{GS} = 0 \text{ V},  I_{S} = 1.3 \text{ A}  \text{(Note 2)}$			1.2	V
t <sub>rr</sub>	Diode Reverse Recovery Time	$I_F = 7.5 \text{ A},  d_{iF}/d_t = 100 \text{ A/}\mu\text{s}$		24		nS
Q <sub>rr</sub>	Diode Reverse Recovery Charge			13		nC

#### Notes

1. R<sub>0JA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>0JC</sub> is guaranteed by design while R<sub>0CA</sub> is determined by the user's board design.



a) 78°C/W when mounted on a 0.5 in² pad of 2 oz copper



b) 125°C/W when mounted on a .02 in<sup>2</sup> pad of 2 oz copper

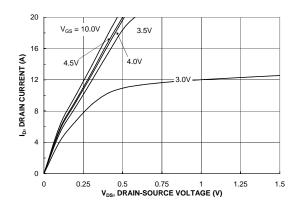


c) 135°C/W when mounted on a minimum pad.

Scale 1:1 on letter size paper

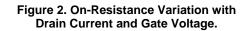
2. Pulse Test: Pulse Width <  $300\mu s,$  Duty Cycle < 2.0%

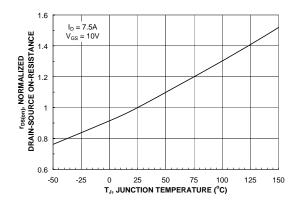
# **Typical Characteristics**



2.6 V<sub>GS</sub> = 3.0V V

Figure 1. On-Region Characteristics.





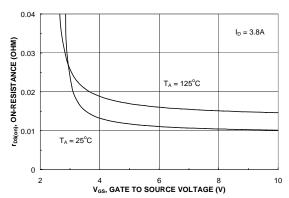
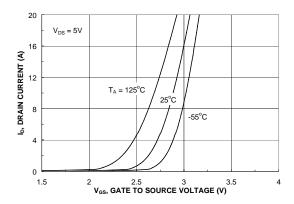


Figure 3. On-Resistance Variation with Temperature.

Figure 4. On-Resistance Variation with Gate-to-Source Voltage.



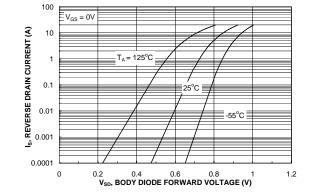
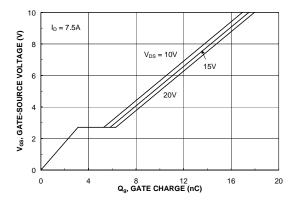


Figure 5. Transfer Characteristics.

Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

# **Typical Characteristics**



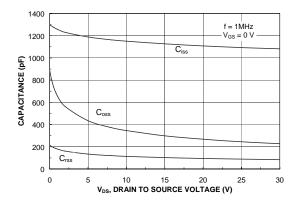
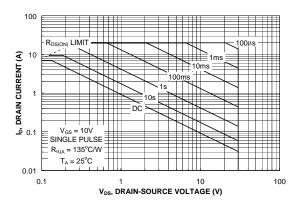


Figure 7. Gate Charge Characteristics.





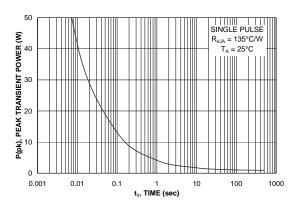


Figure 9. Maximum Safe Operating Area.

Figure 10. Single Pulse Maximum Power Dissipation.

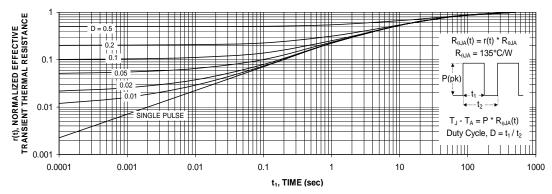


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.





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