

# 2N6387, 2N6388

## Plastic Medium-Power Silicon Transistors

These devices are designed for general-purpose amplifier and low-speed switching applications.

### Features

- High DC Current Gain –  $h_{FE} = 2500$  (Typ) @  $I_C = 4.0$  Adc
- Collector–Emitter Sustaining Voltage – @ 100 mA dc  
 $V_{CE(sus)} = 60$  Vdc (Min) – 2N6387  
 $= 80$  Vdc (Min) – 2N6388
- Low Collector–Emitter Saturation Voltage –  
 $V_{CE(sat)} = 2.0$  Vdc (Max) @  $I_C$   
 $= 5.0$  Adc – 2N6387, 2N6388
- Monolithic Construction with Built–In Base–Emitter Shunt Resistors
- TO–220AB Compact Package
- Pb–Free Packages are Available\*

### MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CEO}$	60 80	Vdc
Collector–Base Voltage	$V_{CB}$	60 80	Vdc
Emitter–Base Voltage	$V_{EB}$	5.0	Vdc
Collector Current – Continuous – Peak	$I_C$	10 15	A dc
Base Current	$I_B$	250	mA dc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	65 0.52	W W/ $^\circ\text{C}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	2.0 0.016	W W/ $^\circ\text{C}$
Operating and Storage Junction, Temperature Range	$T_J, T_{stg}$	–65 to +150	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	1.92	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C}/\text{W}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Indicates JEDEC Registered Data.

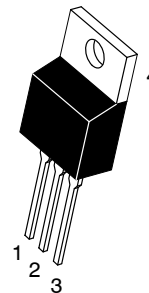


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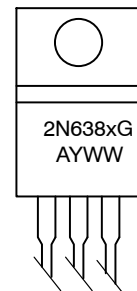
<http://onsemi.com>

## DARLINGTON NPN SILICON POWER TRANSISTORS 8 AND 10 AMPERES 65 WATTS, 60 – 80 VOLTS

### MARKING DIAGRAM



TO–220AB  
CASE 221A  
STYLE 1



2N638x = Device Code  
x = 7 or 8

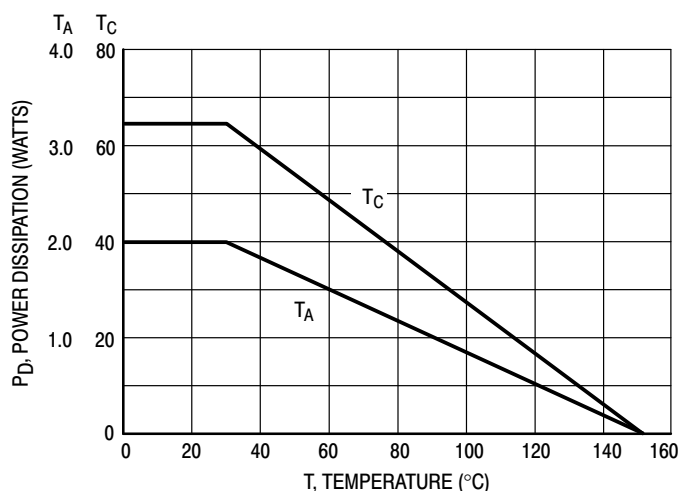
G = Pb–Free Package  
A = Assembly Location  
Y = Year  
WW = Work Week

### ORDERING INFORMATION

Device	Package	Shipping
2N6387	TO–220AB	50 Units / Rail
2N6387G	TO–220AB (Pb–Free)	50 Units / Rail
2N6388	TO–220AB	50 Units / Rail
2N6388G	TO–220AB (Pb–Free)	50 Units / Rail

\*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## 2N6387, 2N6388



**Figure 1. Power Derating**

### ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted) (Note 2)

Characteristic	Symbol	Min	Max	Unit	
<b>OFF CHARACTERISTICS</b>					
Collector-Emitter Sustaining Voltage (Note 3) ( $I_C = 200\text{ mAdc}$ , $I_B = 0$ )	2N6387 2N6388	$V_{CEO(sus)}$	60 80	– –	Vdc
Collector Cutoff Current ( $V_{CE} = 60\text{ Vdc}$ , $I_B = 0$ ) ( $V_{CE} = 80\text{ Vdc}$ , $I_B = 0$ )	2N6387 2N6388	$I_{CEO}$	– –	1.0 1.0	mAdc
Collector Cutoff Current ( $V_{CE} = 60\text{ Vdc}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ ) ( $V_{CE} = 80\text{ Vdc}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ ) ( $V_{CE} = 60\text{ Vdc}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ , $T_C = 125^\circ\text{C}$ ) ( $V_{CE} = 80\text{ Vdc}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ , $T_C = 125^\circ\text{C}$ )	2N6387 2N6388 2N6387 2N6388	$I_{CEX}$	– – – –	300 300 3.0 3.0	$\mu\text{Adc}$ mAdc
Emitter Cutoff Current ( $V_{BE} = 5.0\text{ Vdc}$ , $I_C = 0$ )		$I_{EBO}$	–	5.0	mAdc
<b>ON CHARACTERISTICS (Note 3)</b>					
DC Current Gain ( $I_C = 5.0\text{ Adc}$ , $V_{CE} = 3.0\text{ Vdc}$ ) ( $I_C = 1.0\text{ Adc}$ , $V_{CE} = 3.0\text{ Vdc}$ )	2N6387, 2N6388 2N6387, 2N6388	$h_{FE}$	1000 100	20,000 –	–
Collector-Emitter Saturation Voltage ( $I_C = 5.0\text{ Adc}$ , $I_B = 0.01\text{ Adc}$ ) ( $I_C = 10\text{ Adc}$ , $I_B = 0.1\text{ Adc}$ )	2N6387, 2N6388 2N6387, 2N6388	$V_{CE(sat)}$	– –	2.0 3.0	Vdc
Base-Emitter On Voltage ( $I_C = 5.0\text{ Adc}$ , $V_{CE} = 3.0\text{ Vdc}$ ) ( $I_C = 10\text{ Adc}$ , $V_{CE} = 3.0\text{ Vdc}$ )	2N6387, 2N6388 2N6387, 2N6388	$V_{BE(on)}$	– –	2.8 4.5	Vdc
<b>DYNAMIC CHARACTERISTICS</b>					
Small-Signal Current Gain ( $I_C = 1.0\text{ Adc}$ , $V_{CE} = 5.0\text{ Vdc}$ , $f_{test} = 1.0\text{ MHz}$ )		$ h_{fe} $	20	–	–
Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f = 1.0\text{ MHz}$ )		$C_{ob}$	–	200	pF
Small-Signal Current Gain ( $I_C = 1.0\text{ Adc}$ , $V_{CE} = 5.0\text{ Vdc}$ , $f = 1.0\text{ kHz}$ )		$h_{fe}$	1000	–	–

2. Indicates JEDEC Registered Data.

3. Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

# 2N6387, 2N6388

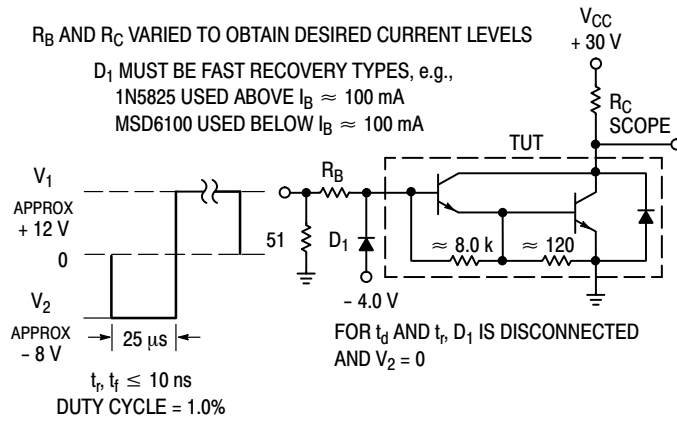


Figure 2. Switching Times Test Circuit

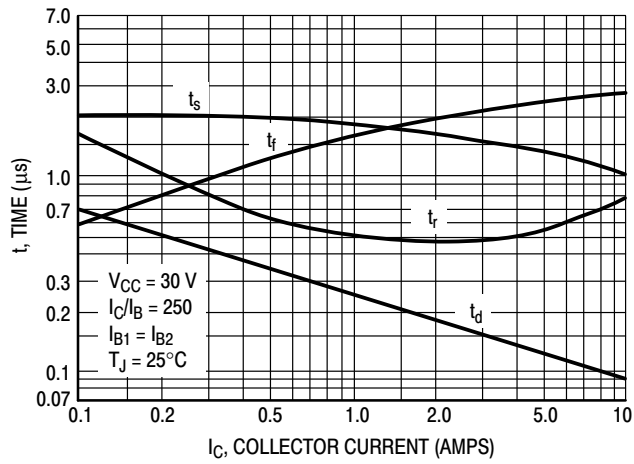


Figure 3. Switching Times

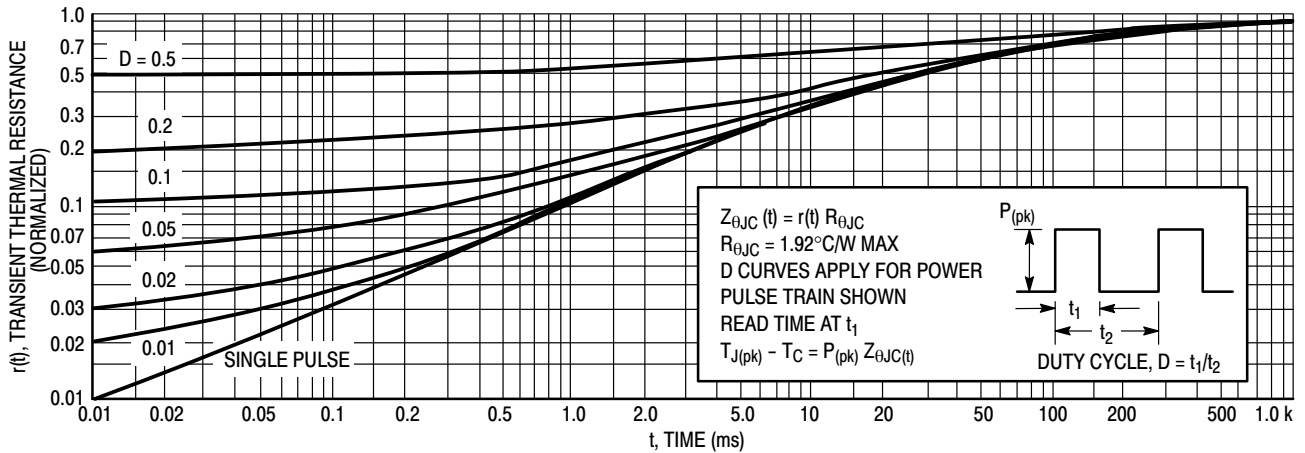
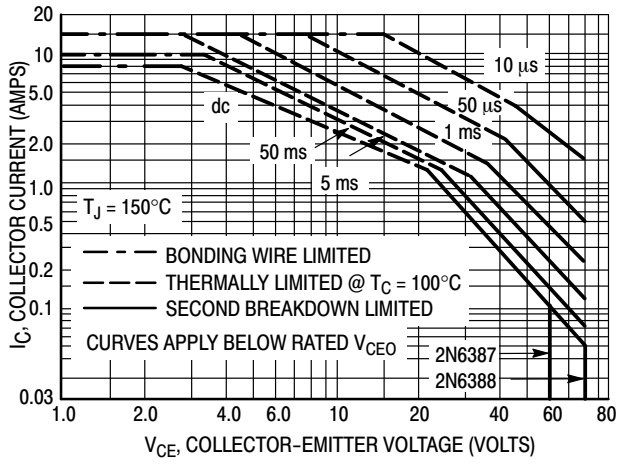


Figure 4. Thermal Response

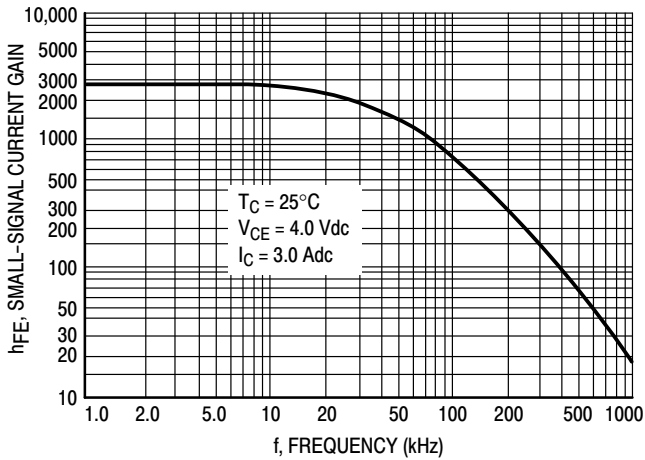
## 2N6387, 2N6388



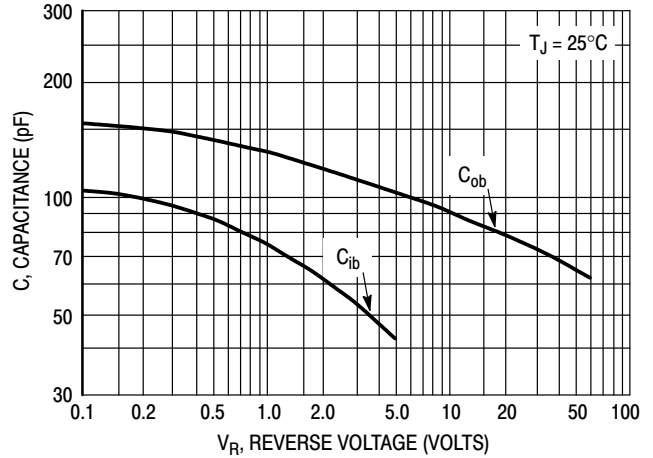
**Figure 5. Active-Region Safe Operating Area**

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

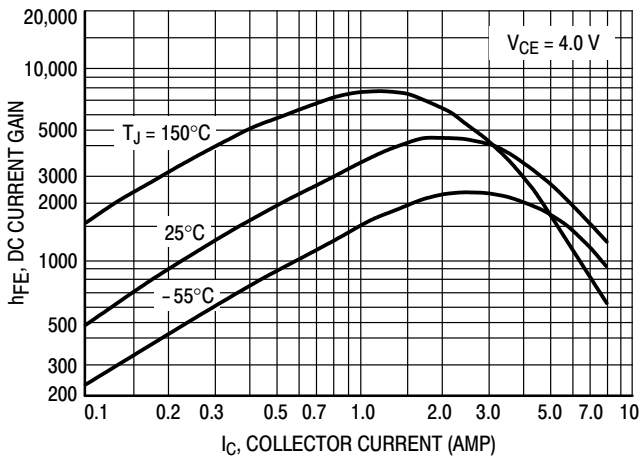
The data of Figure 5 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} < 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown



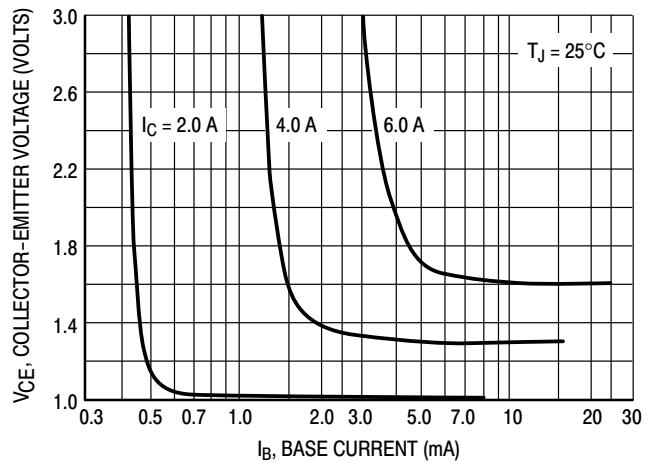
**Figure 6. Small-Signal Current Gain**



**Figure 7. Capacitance**



**Figure 8. DC Current Gain**



**Figure 9. Collector Saturation Region**

2N6387, 2N6388

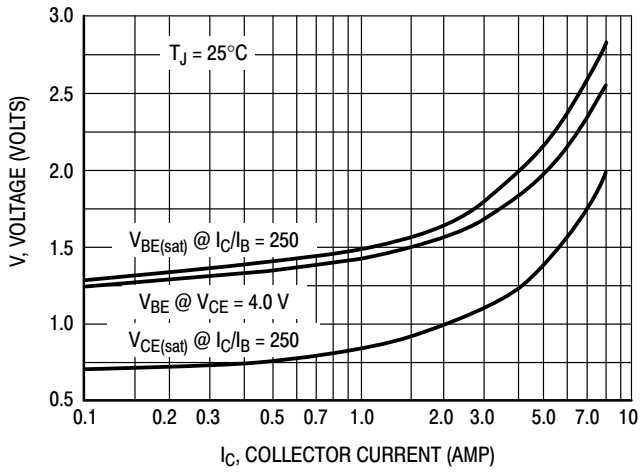


Figure 10. "On" Voltages

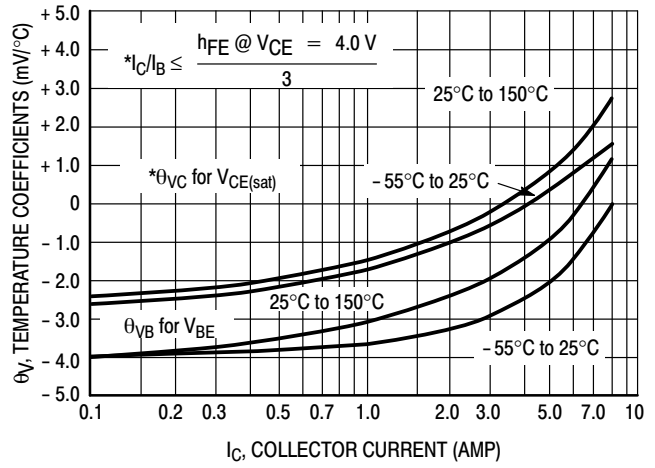


Figure 11. Temperature Coefficients

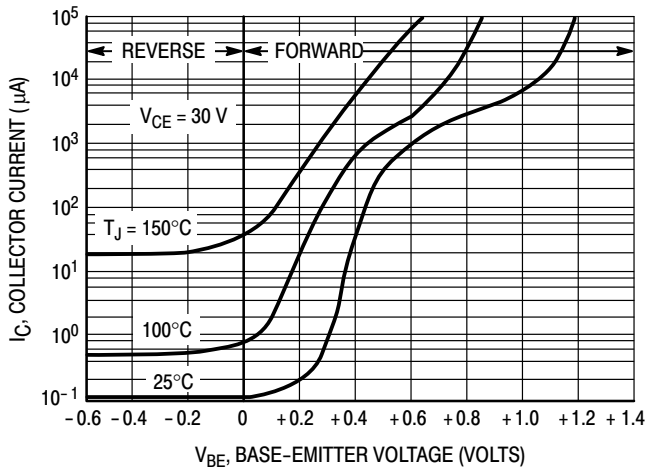


Figure 12. Collector Cut-Off Region

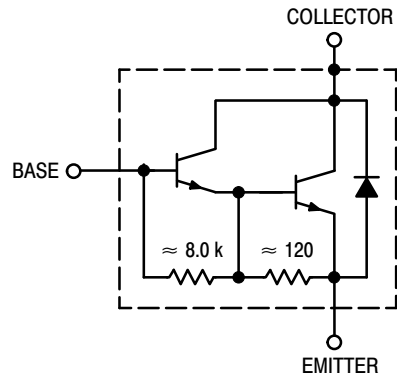
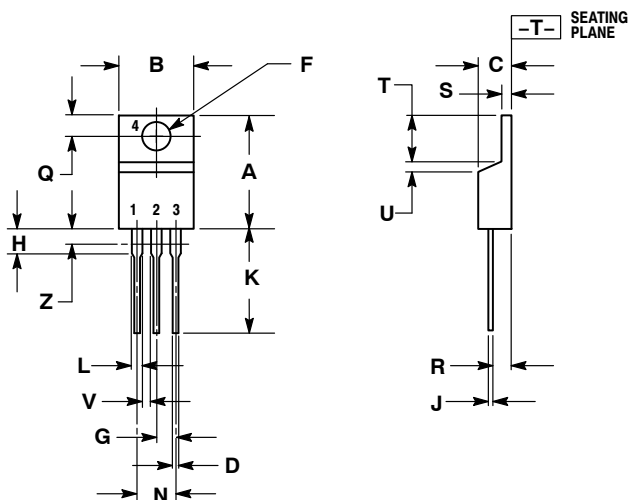


Figure 13. Darlington Schematic

# 2N6387, 2N6388

## PACKAGE DIMENSIONS

### TO-220 CASE 221A-09 ISSUE AG



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.036	0.64	0.91
F	0.142	0.161	3.61	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.161	2.80	4.10
J	0.014	0.025	0.36	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

- STYLE 1:  
PIN 1. BASE  
2. COLLECTOR  
3. EMITTER  
4. COLLECTOR

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