Advanced PMU with 3 Bucks, 2 LDOs and Load Bypass Switch

BENEFITS and FEATURES

- **Wide input voltage range**
  - **Vin = 2.7V to 5.5V**
- **Complete integrated power solution**
  - **One 4A DC/DC Step-Down with Bypass Mode**
  - **Two 3A DC/DC Step-Down Regulators**
  - **Two 300mA LDOs**
  - **High Power Load Switch Gate Driver with Slew Rate Control**
- **Space Savings**
  - **Fully integrated**
  - **High Fsw = 2.25MHz or 1.125MHz**
  - **Integrated sequencing**
  - **Standard PTH PCB Compatible Footprint**
- **Easy system level design**
  - **Configurable sequencing**
  - **Seamless sequencing with external supplies**
  - **Programmable Reset and Power Good GPIO's**
- **Buck 1 Bypass Mode for 3.3V system level compliance**
- **Highly configurable**
  - **µP interface for status reporting and controllability**
  - **Flexible Sequencing Options**
  - **I²C Interface – 1MHz**
  - **Multiple Sleep Modes**
  - **See ACT88326 for Pushbutton Startup**

APPLICATIONS

- Solid-State Drives
- Microcontroller Applications
- FPGA
- Personal Navigation Devices

GENERAL DESCRIPTION

The ACT88325 PMIC is an integrated ActivePMU™ power management unit. It is highly flexible and can be reconfigured via I²C for multiple applications without the need for PCB changes. The low external component count and high configurability significantly speeds time to market. Examples of configurable options include output voltage, startup time, system level sequencing, switching frequency, sleep modes, operating modes etc. The core of the device includes 3 DC/DC step down converters using integrated power FETs, and 2 low-dropout regulators (LDOs). Each regulator can be configured for a wide range of output voltages through the I²C interface.

ACT88325 is programmed at the factory with a default configuration. The default settings can be optimized for a specific design through the I²C interface. Contact the factory for specific default configurations.

The ACT88325 includes features that allow flexibility for all system level configurations. The buck converter can be reconfigured as a bypass switch. It also contains a high power load switch controller. It's external power supply enable and power good interface allows seamless sequencing with external power supplies.

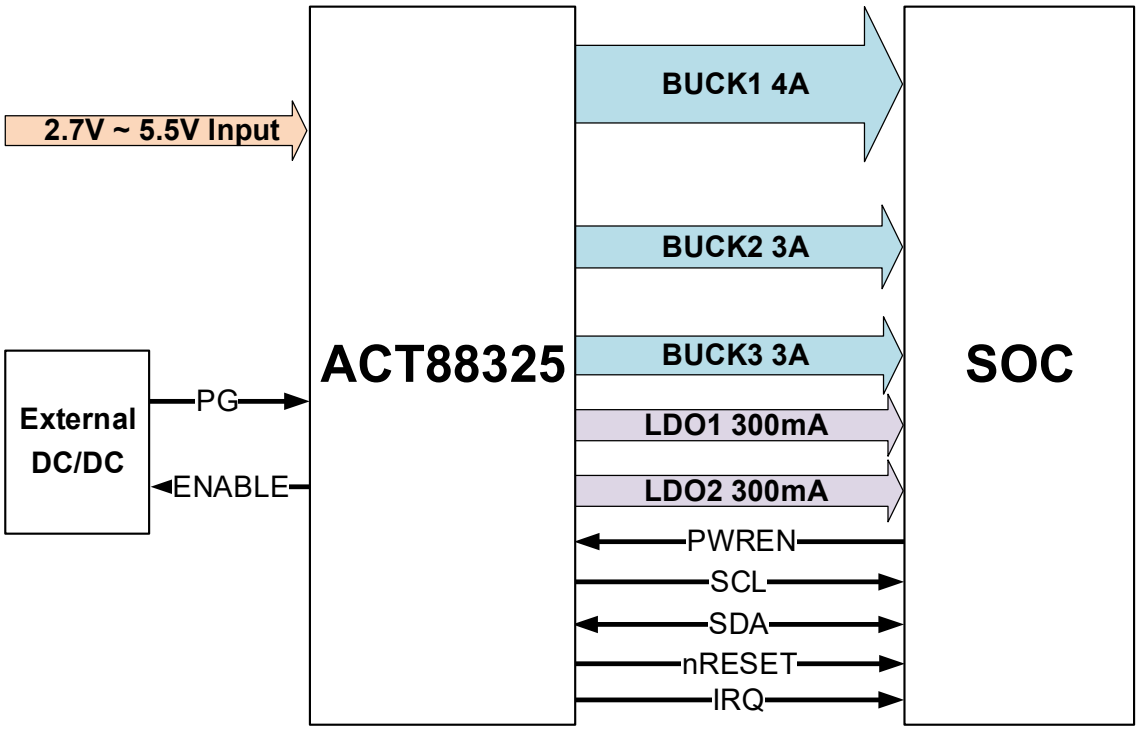
The ACT88325 PMIC is available in a 2.7 x 3 mm 36 pin WLCSP package. The IC pinout is optimized to allow standard, low-cost PTH PCB layouts.

The ACT88325 is optimized for compatible with many different Solid State Disk Drive (SSD) controllers. This includes, but is not limited to the following.

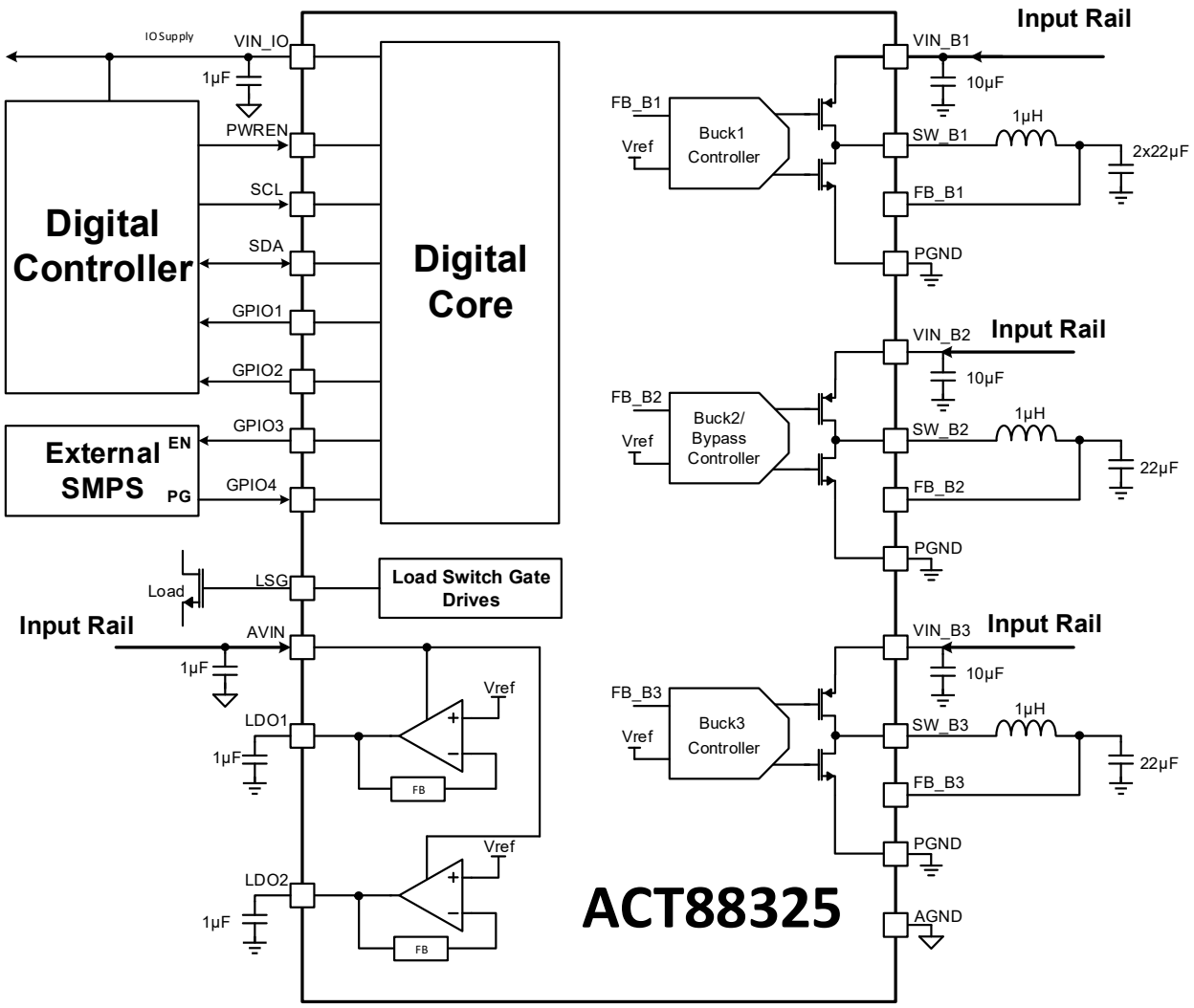
SSD Controller Compatibility

SSD Controller Vendor	SSD Controller
SMI	SM2258
SMI	SM2258H
SMI	SM2258XT
SMI	SM2259
SMI	SM2262
SMI	SM2263
SMI	SM2263XT
Marvell	Dean
Marvell	Eldora

Typical Application Diagram

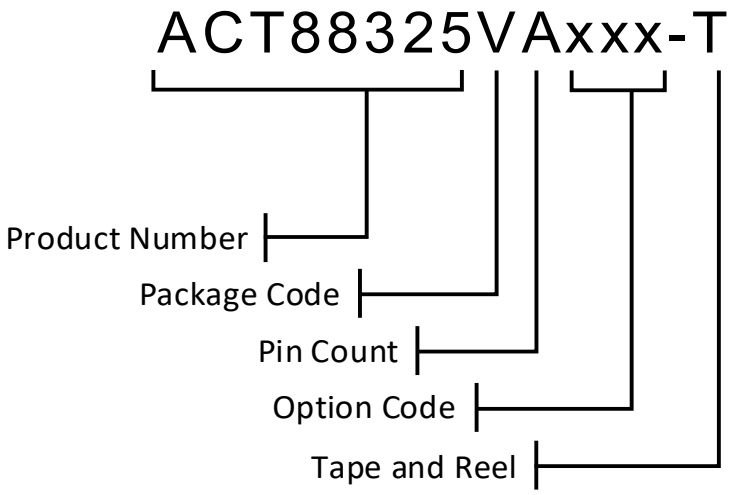


FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

PART NUMBER	Input Voltage	V_{BUCK1}	V_{BUCK2}	V_{BUCK3}	V_{LDO1}	V_{LDO2}	V_{LSG}
ACT88325VA101-T	3.3V	Bypass	0.9V	1.2V/1.8V	1.8V	3.3V	OFF
ACT88325VA105-T	3.3V	Bypass	0.9V	1.2V/1.8V	1.8V	3.3V	OFF



Note 1: Standard product options are identified in this table. Contact factory for custom options, minimum order quantity required.

Note 2: All Active-Semi components are RoHS Compliant and with Pb-free plating unless specified differently. The term Pb-free means semiconductor products that are in compliance with current RoHS (Restriction of Hazardous Substances) standards.

Note 3: Package Code designator "V" represents CSP

Note 4: Pin Count designator "A" represents 36 pins

Note 5: "xxx" represents the CMI (Code Matrix Index) option. The CMI identifies the IC's default register settings

PIN CONFIGURATION

	A	B	C	D	E	F
1	FB_B3	LDO1	AVIN	LDO2	PWREN	FB_B2
2	VIN_B3	VIN_B3	LSG	VIN_B2	VIN_B2	VIN_B2
3	SW_B3			SW_B2	SW_B2	SW_B2
4	SW_B3			PGND12	PGND12	PGND12
5	PGND3			SW_B1	SW_B1	SW_B1
6	AGND	GPIO3	GPIO2	VIN_B1	VIN_B1	VIN_B1
7	SDA	SCL	GPIO1	GPIO4	VIN_IO	FB_B1

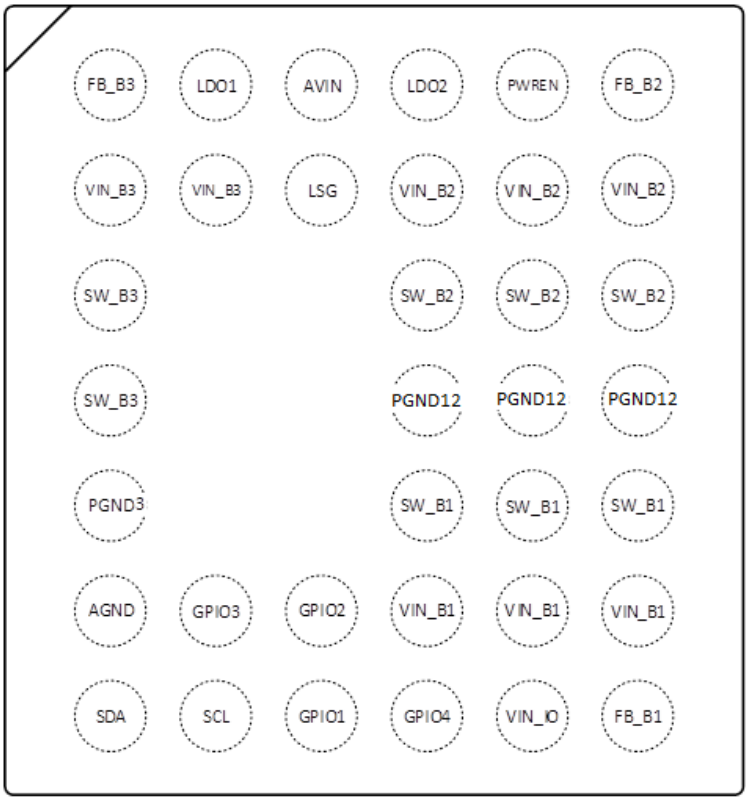


Figure 1: Pin Configuration – Top View (bumps down) CSP 36 Balls 2.7mm x 3mm

PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
A1	FB_B3	Feedback for Buck3 Regulator. Connect directly to the Buck3 output capacitor.
B1	LDO1	Output for LDO1 Regulator
C1	AVIN	Dedicated VIN Power Input for LDO1 & LDO2 Regulators and Analog VIN Input
D1	LDO2	Output for LDO2 Regulator
E1	PWREN	Power Enable Digital Input
F1	FB_B2	Feedback for Buck2 Regulator. Connect directly to the Buck2 output capacitor.
A2, B2	VIN_B3	Dedicated Buck3 VIN Power Input. Connect the Buck3 input caps directly to these pins
C2	LSG	Load Switch Gate Driver Output
D2, E2, F2	VIN_B2	Dedicated Buck2 VIN Power Input. Connect the Buck2 input caps directly to these pins.
A3, A4	SW_B3	Switch Pin for Buck3 Regulator
D3, E3, F3	SW_B2	Switch Pin for Buck2 Regulator
D4, E4, F4	PGND12	Power Ground for Buck1 and Buck2. Connect the Buck1 and Buck2 input caps directly to these pins.
A5	PGND3	Power Ground for Buck3. Connect the Buck3 input caps directly to these pins.
D5, E5, F5	SW_B1	Switch Pin for Buck1 Regulator
A6	AGND	Analog Ground
B6	GPIO3 / nIRQ	General Purpose I/O Port 3. Typically configured as an interrupt (IRQ) open drain output.
C6	GPIO2	General Purpose I/O Port 2. Can be configured for several different functions.
D6, E6, F6	VIN_B1	Dedicated Buck1 VIN Power Input. Connect the Buck1 input caps directly to these pins.
A7	SDA	I^2C Data Input and Output
B7	SCL	I^2C Clock Input
C7	GPIO1 / DVS	General Purpose I/O Port 1. Typically configured as a dynamic voltage scaling input or voltage select input.
D7	GPIO4 / nRESET	General Purpose I/O Port 4. Typically configured as an nRESET open drain output
E7	VIN_IO	Digital Input Reference Voltage Input
F7	FB_B1	Feedback for Buck1 Regulator. Connect directly to the Buck1 output capacitor.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	VALUE	UNIT
All Pins to PGND12 unless stated otherwise below	-0.3 to 6	V
VIN_xx to PGND12	-0.3 to 6	V
SW_Bx to PGND12	-0.3 to VIN_xx + 1	V
PWREN to AGND	-0.3 to AVIN + 0.3	V
GPIOx to AGND	-0.3V to VIN_IO + 0.3	V
FB_Bx to PGND	-0.3 to VIN_xx + 0.3	V
LDOx to PGND	-0.3 to VIN_xx + 0.3	V
AGND to PGND12	-0.3 to + 0.3	V
Junction to Ambient Thermal Resistance (Note 2)	39	°C/W
Junction to Case Thermal Resistance (Note 2)	6.5	°C/W
Operating Junction Temperature	-40 to 150	°C
Storage Temperature	-55 to 150	°C

Note1: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.

Note2: Measured on Active-Semi Evaluation Kit

DIGITAL I/O ELECTRICAL CHARACTERISTICS

(VIN_IO = 5V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PWREN Input Low	AVIN = 3.3V			0.9	V
PWREN Input High	AVIN = 3.3V	2.25			V
PWREN Input Low	AVIN = 5.0V			1.0	V
PWREN Input High	AVIN = 5.0V	3.3			V
GPIO1, GPIO2, GPIO4 Input Low	VIN_IO = 1.8V			0.40	V
GPIO3 Input Low	VIN_IO = 1.8V			0.25	V
GPIO1, GPIO2, GPIO3, GPIO4 Input High	VIN_IO = 1.8V	1.25			V
GPIO1, GPIO2, GPIO4 Input Low	VIN_IO = 3.3V			1.0	V
GPIO3 Input Low	VIN_IO = 3.3V			0.40	V
GPIO1, GPIO2, GPIO3, GPIO4 Input High	VIN_IO = 3.3V	2.3			V
GPIO1, GPIO2, GPIO3, GPIO4 Leakage Current	Output = 5V			1	µA
GPIO1, GPIO2, GPIO4 Output Low	I_{OL} = 10mA			0.35	V
GPIO3 Output Low	I_{OL} = 1mA			0.35	V
GPIO1, GPIO2 Output High	I_{OH} = 1mA	VIN_IO-0.35			V
PWREN, GPIO4 Deglitch Time (falling)			15		µs
PWREN, GPIO4 Deglitch Time (rising)			10		µs
VIN_IO Operating Range		1.5		VIN	V

SYSTEM CONTROL ELECTRICAL CHARACTERISTICS

(VIN_IO = 5V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Supply Voltage Range: AVIN referenced to AGND		2.7		5.5	V
UVLO Threshold Falling		2.5	2.6	2.7	V
UVLO Hysteresis		100			mV
System Monitor (SYSMON) Programmable Range		2.7		4.2	V
OV Threshold Rising		5.4	5.75	6.0	V
OV Hysteresis		80	200	320	mV
Operating Supply Current	All Regulators Disabled		10		µA
Operating Supply Current	All Regulators Enabled but no load		250		µA
Thermal Shutdown	Temperature rising	140	160	180	°C
Thermal Shutdown Hysteresis			30		°C
Power Up Delay after initial VIN	Time from VIN > UVLO threshold to Internal Power-On Clear (POR)		120	200	µs
Startup Delay after initial VIN	Time from VIN > UVLO threshold to start of first regulator turning On. (zero delay)		1500	2000	µs
Oscillator Frequency		2.13	2.25	2.37	MHz
VIN UV Interrupt Threshold Falling	Referenced to rising threshold		200		mV
VIN UV Threshold Rising Programming Range	Rising edge threshold can power up device. Configurable in 100mV steps.	2.7	3.6	4.2	V
VIN UV Shutdown Threshold Falling			2.6		V
VIN OV Shutdown Threshold Rising			5.75		V
VIN OV Shutdown Threshold Falling			5.5		V
VIN Deglitch Time UV			100		µs
VIN Deglitch Time OV			200		µs
Transition time from Deep Sleep (DPSLP) State to Active State	Time from PWREN pin low to high transition to time when the first regulator turns ON with minimum turn on delay configuration.			1	ms
Transition time from Sleep State (SLEEP) to Active State	Time from I^2C command to clear sleep mode to time when the first regulator turns ON with minimum turn on delay configuration.		100		µs
Time to first power rail turn off	Time from turn Off event to when the first power rail turns off with minimum turn off delay configuration		120		µs
Startup Delay Programmable Range	ONDLY=00 ONDLY=01 ONDLY=10 ONDLY=11		0 0.25 0.5 1.0		ms
Turn Off Delay Programmable Range	Configurable in 0.25ms steps	0		7.75	ms
nRESET Programmable Range	Configurable to 20, 40, 60 or 100ms.	20		100	ms

Note 1: All Under-voltage Lockout, Overvoltage measurements are referenced to the AVIN Input and AGND Pins.
Note 2: All POK Under-voltage and Overvoltage measurements are referenced to the VIN Input and PGNDx Pins.

INTERNAL STEP-DOWN DC/DC ELECTRICAL CHARACTERISTICS REGULATOR: (BUCK1)

(VIN = 5V, T_A = 25°C, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Input Operating Voltage Range		2.7		5.5	V
Output Voltage Programming Range 1	See CMI section for programming details	0.6		3.0	V
Output Voltage Programming Range 2	See CMI section for programming details	0.8		4.0	V
Standby Supply Current, Low Power Mode Enabled	V_{OUT_B1} = 103% setpoint, Enabled, V_{OUT_B1} setpoint = 1.0V, No Load		40	60	µA
Shutdown Current	Regulator Disabled			1	µA
Output Voltage Accuracy	V_{OUT_B1} = default CMI voltage, continuous PWM mode	-1	V_{NOM}	1	%
Output Voltage Accuracy	V_{OUT_B1} = default CMI voltage, PFM mode	-2	V_{NOM}	2	%
Line Regulation	V_{OUT_B1} = default CMI voltage, PWM Regulation		0.1		%/V
Load Regulation	V_{OUT_B1} = at default CM, PWM Regulation		0.1		%/A
Power Good Threshold	V_{OUT_B1} Rising	90	92.5	95	$\%V_{NOM}$
Power Good Hysteresis	V_{OUT_B1} Falling		3		$\%V_{NOM}$
Overvoltage Fault Threshold	V_{OUT_B1} Rising	107.5	110	112.5	$\%V_{NOM}$
Overvoltage Fault Hysteresis	V_{OUT_B1} Falling		3		$\%V_{NOM}$
Switching Frequency	V_{OUT_B1} ≥ 20% of V_{NOM}, Configurable	-5%	1.125 / 2.25	+5%	MHz
Soft-Start Period T_{set}	10% to 90% V_{NOM}		480	750	µs
Current Limit, Cycle-by-Cycle (accuracy is only valid for the specific CMI's default setting)	ILIM[1:0] = 00 ILIM[1:0] = 01 ILIM[1:0] = 10 ILIM[1:0] = 11	4.2 3.6 3.0 2.4	5.4 4.7 3.8 3.1	6.6 5.7 4.6 3.7	A
Current Limit, Shutdown	% compared to Current Limit, cycle-by-cycle	112.5	122.5	132.5	%
Current Limit, Warning	% compared to Current Limit, cycle-by-cycle	67.5	75	82.5	%
PMOS On-Resistance	I_{SW} = -1A, VIN = 5.0V		40	50	mΩ
NMOS On-Resistance	I_{SW} = 1A, VIN = 5.0V		16	25	mΩ
SW Leakage Current	VIN = 5.5V, V_{SW} = 0V			1	µA
	VIN = 5.5V, V_{SW} = 5.5V			1	µA
Dynamic Voltage Scaling Rate			3.50		mV/µs
Output Pull Down Resistance	Enabled when regulator disabled		4.4	8.75	Ohms

INTERNAL STEP-DOWN DC/DC ELECTRICAL CHARACTERISTICS REGULATOR: (BUCK1) – BYPASS MODE

(VIN = 3.3V, T_A = 25°C, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage for By-Pass Mode		2.7	3.3	5.5	V
PMOS On-Resistance	I_{SW} = -1A, VIN = 3.3V, Max=125°C at $T_{Junction}$		0.04	0.06	Ω
Internal PMOS Current Detection	Triggers Interrupt on IRQ Pin	2.8	4.2	5.4	A
Internal PMOS Current Detection Deglitch Time			10		µs
Internal PMOS Current Shutdown	Shuts down after deglitch time and stays off for Off-Time	4.7	6.5	8.7	A
Internal PMOS Current Shutdown Deglitch Time			5		µs
Internal PMOS Current Shutdown Off-Time (Retry time)			14		ms
Internal PMOS Soft start	VIN = 3.3V Input, C_{out} = 47uF, Default setting ISS[1:0]=00		500		µs

INTERNAL STEP-DOWN DC/DC ELECTRICAL CHARACTERISTICS REGULATOR: (BUCK2/3)

(AVIN = VIN = 5V, T_A = 25°C, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Input Operating Voltage Range		2.7		5.5	V
Buck2 Output Voltage Programming Range 1	See CMI section for programming details	0.6		3.0	V
Buck2 Output Voltage Programming Range 2	See CMI section for programming details	0.8		4.0	V
Buck3 Output Voltage Programming Range	See CMI section for programming details	0.8		4.0	V
Standby Supply Current, Low Power Mode Enabled	V_{OUTx} = 103%, Regulator Enabled, No load, V_{OUTx} = default CMI voltage		40		µA
Shutdown Current	VIN = 5.0V, Regulator Disabled		0.1	1	µA
Output Voltage Accuracy	V_{OUTx} = default CMI voltage, I_{OUTx} = 1A (continuous PWM mode)	-1%	V_{NOM}	1%	V
Line Regulation	V_{OUTx} = default CMI voltage, PWM Regulation		0.1		%
Load Regulation	V_{OUTx} = default CMI voltage, PWM Regulation		0.1		%
Power Good Threshold	V_{OUTx} Rising	90	92.5	95	$\%V_{NOM}$
Power Good Hysteresis	V_{OUTx} Falling		3		$\%V_{NOM}$
Overvoltage Fault Threshold	V_{OUTx} Rising	107.5	110	112.5	$\%V_{NOM}$
Overvoltage Fault Hysteresis	V_{OUTx} Falling		3		$\%V_{NOM}$
Switching Frequency	V_{OUTx} ≥ 20% of VNOM	-5%	1.125 / 2.25	+5%	MHz
Soft-Start Period T_{set}	10% to 90% VNOM		480	750	µs
Startup Time	Time from Enable to PG		700		µs
Current Limit, Cycle-by-Cycle (accuracy is only valid for the specific CMI's default setting)	ILIM[1:0] = 00 ILIM[1:0] = 01 ILIM[1:0] = 10 ILIM[1:0] = 11	3.7 3.1 2.6 2.2	4.6 3.9 3.2 2.6	5.4 4.5 3.8 3.1	A
Current Limit, Shutdown	% compared to Current Limit, cycle-by-cycle	112.5	122.5	132.5	%
Current Limit, Warning	% compared to Current Limit, cycle-by-cycle	67.5	75	82.5	%
PMOS On-Resistance	I_{SW_Bx} = -500mA, V_{IN} = 5V		80		mΩ
NMOS On-Resistance	I_{SW_Bx} = 500mA, V_{IN} = 5V		50		mΩ
SW Leakage Current	V_{IN} = 5.5V, V_{SW_Bx} = 0 or 0V			1	µA
	V_{IN} = 5.5V, V_{SW_Bx} = 0 or 5.5V			1	µA
Dynamic Voltage Scaling Rate			3.50		mV/us
Output Pull Down Resistance	Enabled when regulator disabled		9.4	20	Ω

LDO1-2 ELECTRICAL CHARACTERISTICS

(AVIN = VIN = 5V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range LDO1	AVIN (Input Voltage) to the LDO1	2.7		5.5	V
Output Voltage Range	Option 1 Configurable in 9.375mV steps	0.6		2.991	V
	Option 2 Configurable in 12.5mV steps	0.8		3.9875	V
Output Current		270	300		mA
Output Voltage Accuracy	AVIN - V_{LDOx_OUT} > 0.4V	-1	V_{NOM}	1	%
Line Regulation	AVIN - V_{LDOx_OUT} > 0.4V I_{LDOx_OUT} = 1mA		0.03	0.2	%
Load Regulation	I_{LDOx_OUT} = 1mA to 100mA, V_{LDOx_OUT} = default CMI			0.5	%
Power Supply Rejection Ratio	f = 1kHz, I_{LDOx_OUT} = 20mA, V_{LDOx_OUT} = 1.8V, Note 1		40.8		dB
	f = 10kHz, I_{LDOx_OUT} = 20mA, V_{LDOx_OUT} = 1.8V, Note 1		31.2		dB
	f = 2.25MHz, I_{LDOx_OUT} = 20mA, V_{LDOx_OUT} = 1.8V, Note 1		53.6		dB
Supply Current per Output	Regulator Disabled			1	µA
Supply Current	Regulator Enabled, No load		15	20	µA
Soft-Start Period	Time from soft start “ON” to PGOOD. V_{LDOx} = 1.8V	140	225	350	µs
	Time from soft start “ON” to PGOOD. V_{LDOx} = 3.3V	140	300	430	µs
Power Good Threshold	V_{LDOx_OUT} Rising	90	92.5	95	% V_{NOM}
Power Good Hysteresis	V_{LDOx_OUT} Falling		3		% V_{NOM}
Overvoltage Fault Threshold	V_{LDOx_OUT} Rising	105	110	115	% V_{NOM}
Overvoltage Fault Hysteresis	V_{LDOx_OUT} Falling		3		% V_{NOM}
Discharge Resistance			50	125	Ω
Dropout Voltage	I_{LDOx_OUT} = 220mA, V_{LDOx_OUT} = 2.7V			150	mV
Output Current Limit	ILIM [1:0] = 00 ILIM [1:0] = 01 ILIM [1:0] = 10 ILIM [1:0] = 11	-35%	190 250 330 465	+35%	mA
Startup Time	Time from Enable to PG		300	400	µs

Note 1: AVIN - V_{LDOx_OUT} > 0.4V

LDO2 LOAD SWITCH MODE ELECTRICAL CHARACTERISTICS – BYPASS MODE

(AVIN = VIN = 5V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range LDO2	AVIN (Input Voltage) to the LDO2	2.7		5.5	V
PMOS On-Resistance			0.3	0.5	mΩ
Internal PMOS Current Detection	Triggers Interrupt on IRQ Pin	330	500		mA
Internal PMOS Current Detection De-glitch Time			10		µs
Supply Current	Load Switch Enabled, No load		25	55	µA
Internal PMOS Current Shutdown	Shuts down after deglitch time and stays off for Off-Time	330	500		mA
Internal PMOS Current Shutdown Deglitch Time			5		µs
Internal PMOS Current Shutdown Off time (Retry time)			14		ms
Internal PMOS Soft start	Only used with 3.3V Input, C_{out} = 1uF, Default Setting ISS [1:0] = 00.		10		mV/ µs

LOAD SWITCH GATE DRIVER ELECTRICAL CHARACTERISTICS

(VIN = 5V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range		2.7		5.5	V
Maximum Output - Gate Voltage	Gate fully on			2*VIN	V
Soft-Start Slew Rate	Gate Node rising from 0 to 2V with 1nF output capacitor. (Configurable)		800 400 260 200		us
Gate Pull-up Current	GATE1 SLEW = 00		2.5		µA
	GATE1 SLEW = 01		5		µA
	GATE1 SLEW = 10		7.5		µA
	GATE1 SLEW = 11		10		µA
Fault Deglitch Time			10		µs
Gate Discharge Resistance				75	Ω
Startup Delay				75	µs

I²C INTERFACE ELECTRICAL CHARACTERISTICS

(VIN_IO = 1.8V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SCL, SDA Input Low	VIN_IO = 1.8V			0.4	V
SCL, SDA Input High	VIN_IO = 1.8V	1.25			V
SCL, SDA Input Low	VIN_IO = 3.3V			1.0	V
SCL, SDA Input High	VIN_IO = 3.3V	2.3			V
SDA Leakage Current	SDA=5V			1	µA
SDA Output Low	I_{OL} = 5mA			0.35	V
SCL Clock Frequency, f_{SCL}		0		1000	kHz
SCL Low Period, t_{LOW}		0.5			µs
SCL High Period, t_{HIGH}		0.26			µs
SDA Data Setup Time, t_{SU}		50			ns
SDA Data Hold Time, t_{HD}	(Note1)	0			ns
Start Setup Time, t_{ST}	For Start Condition	260			ns
Stop Setup Time, t_{SP}	For Stop Condition	260			ns
Capacitance on SCL or SDA Pin				10	pF
SDA Fall Time SDA, T_{of}	Device requirement			120	ns
Pulse Width of spikes must be suppressed on SCL and SDA		0		50	ns

Note1: Comply with I²C timings for 1MHz operation - “Fast Mode Plus”.

Note2: No internal timeout for I²C operations, however, I²C communication state machine will be reset when entering Deep Sleep, Sleep, OVUVFLT, and THERMAL states to clear any transactions that may have been occurring when entering the above states.

Note3: This is an I²C system specification only. Rise and fall time of SCL & SDA not controlled by the device.

Note4: Device Address is factory configurable to 7’h25, 7’h27, 7’h67, 7’h6B.

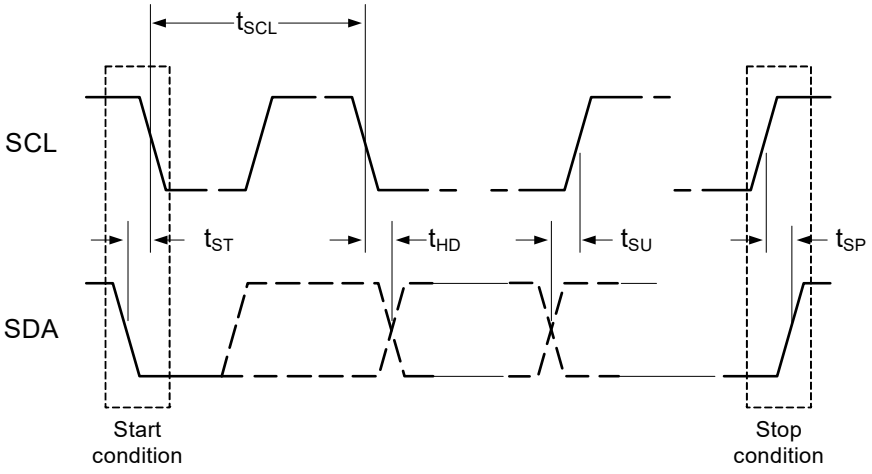


Figure 2: I²C Data Transfer

SYSTEM CONTROL INFORMATION

General

The ACT88325 is a single-chip integrated power management solution designed to power many processors such as the Silicon Motion SM2258/59/62/63/63XT solid state drive controllers and the Atmel SAMA5D processors. It integrates three highly efficient buck regulators, two LDOs, and an integrated load bypass switch. Its high integration and high switching frequency result in an extremely small footprint and low cost power solution. It contains a master controller that manages startup sequencing, timing, voltages, slew rates, sleep states, and fault conditions. I²C configurability allows system level changes without the need for costly PCB changes. The built-in load bypass switch enables full sequencing configurability in 3.3V systems.

The ACT88325 master controller monitors all outputs and reports faults via I²C and hardwired status signals. Faults can be masked and fault levels and responses are configurable via I²C.

Many of the ACT88325 pins and functions are configurable. The IC's default functionality is defined by the default CMI (Code Matrix Index), but much of this functionality can be changed via I²C. Several GPIOs can be configured as enable inputs, reset outputs, dynamic voltage (DVS) inputs, LED drivers, etc. The GPIO configuration is specifically defined for each ACT88325 orderable part number. The first part of the datasheet describes basic IC functionality and default pin functions. The end of the datasheet provides the configuration and functionality specific to each CMI version. Contact sales@active-semi.com for additional information about other configurations.

I²C Serial Interface

To ensure compatibility with a wide range of systems, the ACT88325 uses standard I²C commands. The ACT88325 operates as a slave device, and can be factory configured to one of four 7-bit slave addresses. The 7-bit slave address is followed by an eighth bit, which indicates whether the transaction is a read-operation or a write-operation. Refer to each specific CMI for the IC's slave address

7-Bit Slave Address		8-Bit Write Address	8-Bit Read Address
0x25h	010 0101b	0x4Ah	0x4Bh
0x27h	010 0111b	0x4Eh	0x4Fh
0x67h	110 0111b	0xCEh	0xCFh
0x6Bh	110 1011b	0xD6h	0xD7h

There is no timeout function in the I²C packet processing state machine, however, any time the I²C state machine receives a start bit command, it immediately resets the packet processing, even if it is in the middle of a valid packet. The I²C functionality is operational in all states except RESET.

I²C commands are communicated using the SCL and SDA pins. SCL is the I²C serial clock input. SDA is the data input and output. SDA is open drain and must have a pull-up resistor. Signals on these pins must meet timing requirements in the Electrical Characteristics Table.

I²C Registers

The ACT88325 contains an array of internal registers that contain the IC's basic instructions for setting up the IC configuration, output voltages, sequencing, fault thresholds, fault masks, etc. These registers are what give the IC its operating flexibility. The two types of registers are described below.

Basic Volatile – These are R/W (Read and Write) and RO (Read only). After the IC is powered, the user can modify the R/W register values to change IC functionality. Changes in functionality include things like masking certain faults. The RO registers communicate IC status such as fault conditions. Any changes to these registers are lost when power is recycled. The default values are fixed and cannot be changed by the factory or the end user.

Basic Non-Volatile – These are R/W and RO. After the IC is powered, the user can modify the R/W register values to change IC functionality. Changes in functionality include things like output voltage settings, startup delay time, and current limit thresholds. Any changes to these registers are lost when power is recycled. The default values can be modified at the factory to optimize IC functionality for specific applications. Please consult sales@active-semi.com for custom options and minimum order quantities.

When modifying only certain bits within a register, take care to not inadvertently change other bits. Inadvertently changing register contents can lead to unexpected device behavior.

State Machine

Figure 3 shows the ACT88325 internal state machine.

RESET State

In the RESET, or “cold” state, the ACT88325 is waiting for the input voltage on VIN to be within a valid range defined by the VIN_UV and VIN_OV thresholds. All regulators are off in RESET. All reset outputs are asserted low. All volatile registers are reset to defaults and Non-Volatile registers are reset to programmed defaults. The IC transitions from RESET to POWER SEQUENCE START when the input voltage enters the valid range. The IC transitions from any other state to RESET if the input voltage drops below the VIN_UV threshold voltage. It is important to note any transition to RESET returns all volatile and non-volatile registers to their default states.

POWER SEQUENCE START State

The POWER SEQUENCE START state is a transitional state while the regulators are starting. The IC does not operate in this state.

ACTIVE State

The ACTIVE state is the normal operating state when the input voltage is within the allowable range, all outputs are turned on, and no faults are present.

SLEEP State

The SLEEP state is a low power mode for the operating system. Each output can be programmed to be on or off in the SLEEP state. The outputs follow their programmed sequencing delay times when turning on or off as they enter or exit the SLEEP state. Buck1/2/3 can be programmed to regulate to their VSET0 voltage, VSET1 voltage, or be turned off in the SLEEP state. LDO1/2 can be programmed to regulate to their VSET0 voltage or can be programmed to be turned off. Note that LDO1/2 do not have a VSET1 voltage.

The IC can enter SLEEP state via I²C registers SLEEP and SLEEP EN. Table 1 shows the conditions to enter SLEEP state. ACT88325 I²C stays enabled in SLEEP state. The IC exits the SLEEP state when the conditions to enter SLEEP state are no longer present.

SLEEP Mode				
SLEEP MODE (Register)	PWREN Pin	SLEEP_EN (Register)	SLEEP (Register)	Enter SLEEP State
x	x	0	0	NO
x	x	0	1	NO
x	x	1	0	NO
x	x	1	1	YES
x	x	0	0	NO
x	x	0	1	NO
x	x	1	0	NO
x	x	1	1	YES

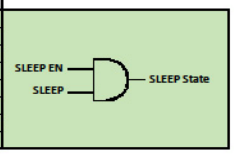


Table 1. SLEEP Mode Truth Table

DPSLP State

The DPSLP state is another low power operating mode for the operating system. It is intended to be used in a lower power configuration than the SLEEP mode. It is similar to the SLEEP state, but DPSLP uses slightly different configurations to enter and exit this mode. Each output can be programmed to be on or off in the DPSLP state. This programming can be different from the SLEEP state. The outputs follow their programmed sequencing delay times when turning on or off as they enter or exit the DPSLP state.

The IC can enter DPSLP state via I²C registers DPSLP and DPSLP EN and/or a GPIO input pin. Table 2 shows the conditions to enter DPSLP state. ACT88325 I²C stays enabled in DPSLP state. The IC exits the DPSLP state when the conditions to enter DPSLP state are no longer present.

If OV, UV, or THERMAL faults occur when in DPSLP state, the IC resets to the POWER ON/Active state.

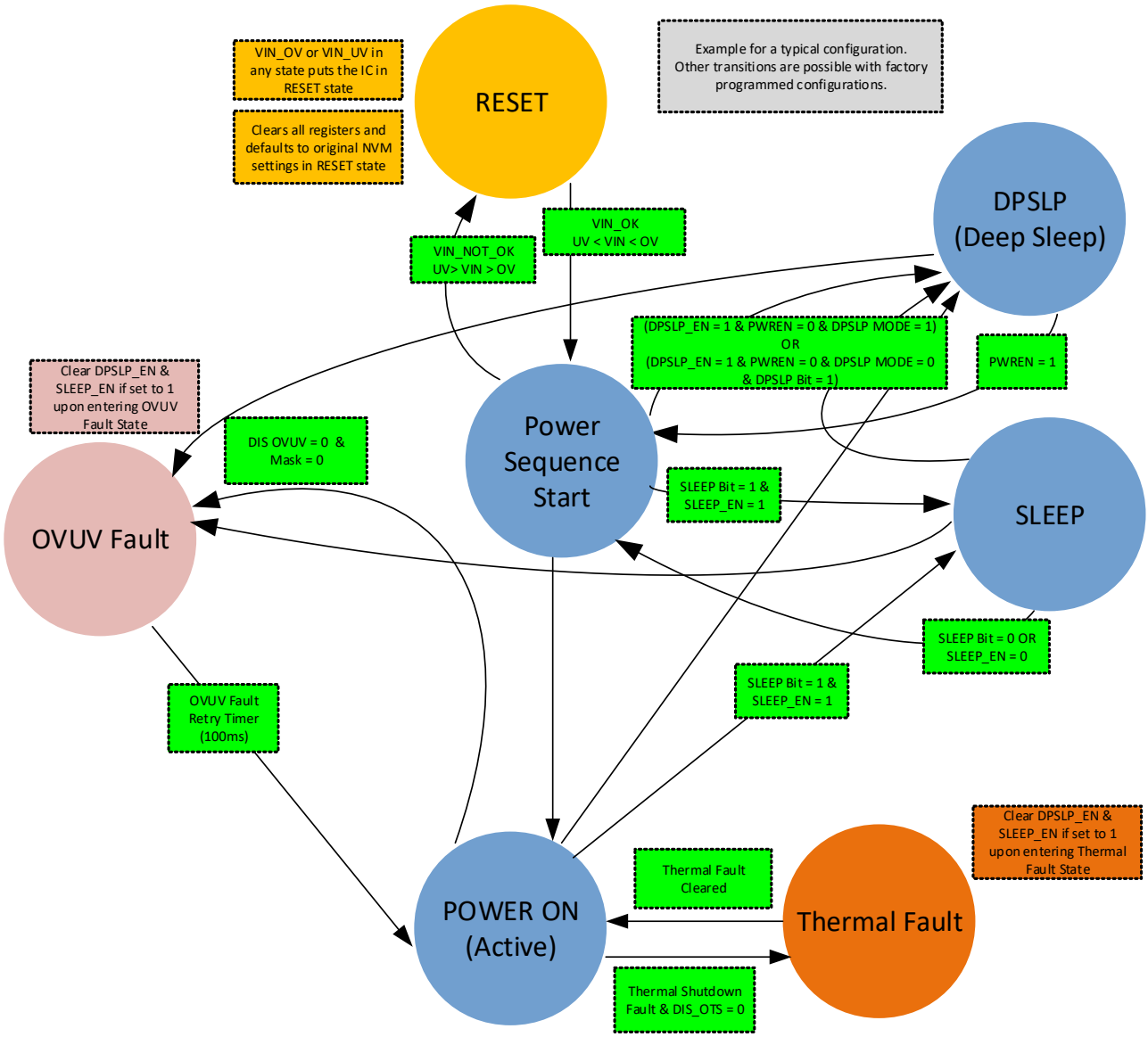


Figure 3: PWREN State Machine

Special consideration is needed for DPSLP state in with a non-I2C system. When PWREN is first toggled high after power up, the ACT88325 detects the first rising transition of PWREN from 0 to 1 and sets the DPSLP_EN register bit to 1. On the falling transition of PWREN from 1 to 0, DPSLP state is entered. In a condition when the system is powered up when PWREN = 1, PWREN must be toggled to 0 and back to 1 to set the DPSLP_EN bit. The next falling PWREN transition puts the IC into the DPSLP state. While in DPSLP mode, if there is a fault condition such as system UV or OV or a thermal fault, the IC resets the DPSLP_EN bit back to 0 when it exits DPSLP mode. This requires PWREN to be toggled high to set the DPSLP_EN to 1 again and then toggled back low to enter DPSLP state again. The IC does not automatically go back into DPSLP state after exiting the DPSLP state due to fault conditions.

DPSLP Mode				
DPSLP MODE (Register)	PWREN pin	DPSLP_EN (Register)	DPSLP (Register)	Enter DPSLP State
0	0	0	0	No
0	0	0	1	No
0	0	1	0	No
0	0	1	1	Yes
0	1	0	0	No
0	1	0	1	No
0	1	1	0	No
0	1	1	1	No
1	0	0	0	No
1	0	0	1	No
1	0	1	0	Yes
1	0	1	1	Yes
1	1	0	0	No
1	1	0	1	No
1	1	1	0	No
1	1	1	1	No

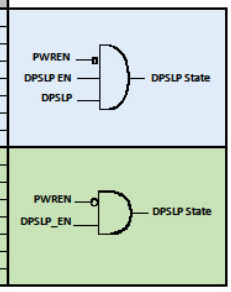


Table 2. DPSLP Mode with Truth Table

THERMAL State

In the THERMAL state the chip has exceeded the thermal shutdown temperature. To protect the device, all the regulators are shut down and the reset pins are asserted low. This state can be disabled by setting register 0x01h bit5 (TMSK) = 1. TMSK prevents the interrupt from going active, but does not prevent the IC from entering the THERMAL State.

OVUV FAULT State

In the OVUV FAULT state one of the regulators has exceed an OV level at any time or UV level after the soft start ramp has completed. All regulators shutdown and all three reset outputs are asserted low when the IC enters OVUVFLT state. The OVUVFLT state is timed to retry after 100ms and enter the ACTIVE state. If the OV or UV condition still exists in the ACTIVE state the IC returns back to the OVUVFLT state. The cycle continues until the OV or UV fault is removed or the input power is removed. This state can be disabled by setting the DIS_OVUV_SHUTDOWN bit high. The IC does not directly enter OVUVFLT in an overcurrent condition, but does enter this state due to the resulting UV condition.

Each regulator has an undervoltage fault mask and an overvoltage fault mask. If the UV or OV fault mask is active, nIRQ is not asserted in the fault condition. Even though the fault is masked, the system can still read each regulators UV and OV. Even though the fault is masked, the IC still enters the OVUV Fault state.

Startup/Shutdown

The IC automatically transitions from the RESET state to the POWER SEQUENCE START state when input power is applied. The IC then transitions to either the POWER ON, SLEEP, or DPSLP state depending on the status of the inputs in Tables 1 and 2. A typical startup profile is for the system to automatically transition from RESET to POWER ON when input power is applied. The typical shutdown sequence is for the system to pull PWREN low to enter DPSLP.

Sequencing

The ACT88325 provides the end user with extremely versatile sequencing capability that can be optimized for many different applications. Each of the five outputs has four basic sequencing parameters: input trigger, turn-on delay, turn-off delay, and output voltage. The buck converters also have softstart time control. Each of these parameters is controlled via the ICs internal registers. As an example, the ACT88325QI101-T sequencing and output voltages are optimized for the Silicon Motion SM2258 and SM2259 processors. The specifics for this IC as well as others are detailed at the end of the datasheet. Contact sales@active-semi.com for custom sequencing configurations. Refer to the Active-Semi Application Note AN112, ACT88325VA101 Register Definitions, for full details on the I²C register map functionality and programming ranges.

Input trigger. The input trigger for a regulator is the event that turns that regulator on. Each output can have a separate input trigger. The input trigger can be the internal power ok (POK) signal from one of the other regulators, the internal VIN POK signal, or an external signal applied to an input pin such as EXT_PG or GPIO. This flexibility allows a wide range of sequencing possibilities, including having some of the outputs be sequenced with an external power supply or a control signal from the host. As an example, if the LDO1 input trigger is Buck1, LDO1 will not turn on until Buck1 is in regulation. Input triggers are defined at the factory and can only be changed with a custom CMI configuration. The GPIOx outputs can be connected to an internal power supply's POK signal and used to trigger external supplies in the overall sequencing scheme. The GPIOx inputs can also be connected to an external power supply's power good output and used as an input trigger for an ACT88325 supply.

Turn-on Delay. The turn-on delay is the time between an input trigger going active and the output starting to turn on. Each output's turn-on delay is configured via its I²C bit ON DELAY. Turn-on delays can be changed after the IC is powered on, but they are volatile and reset to the factory defaults when power is recycled.

Turn-off Delay. The turn-off delay is the time between an input trigger going inactive and the output starting to turn off. Each output's turn-off delay is configured via its I²C bit OFF DELAY. Turn-off delays can be changed

after the IC is powered on, but they are volatile and reset to the factory defaults when power is recycled.

Softstart Time. The softstart time is the time it takes an output to ramp from 10% to 90% of its programmed voltage. All buck converter softstart times are controlled by a single I²C bit ALL_BUCKS_FASTER_SS. When set to 0, the softstart times are 600µs. When set to 1, the softstart times are 250µs. The default softstart time can be changed after the IC is powered on, but it is volatile and resets to the factory defaults when power is recycled.

Output Voltage. The output voltage is each regulator's desired voltage. Each buck's output voltage is programmed via its I²C bits VSET0 and VSET1. The output regulates to VSET0 in ACTIVE mode. They can be programmed to regulate to VSET1 in DVS, SLEEP, and DSPSLP modes. Each LDO has a single register, VSET, to set its output voltage. Each output's voltage can be changed after the IC is powered on, but the new setting is volatile and is reset to the factory defaults when power is recycled. Output voltages can be changed on the fly. If a large output voltage change is required, it is best to make multiple smaller changes. This prevents the IC from detecting an instantaneous over or under voltage condition because the fault thresholds are immediately changed, but the output takes time to respond.

Dynamic Voltage Scaling

On-the-fly dynamic voltage scaling (DVS) for the three buck converters is available via either the I²C interface or a GPIO. DVS allows systems to save power by quickly adjusting the microprocessor performance level when the workload changes. Note that DVS is not a different operating state. The IC operates in the ACTIVE state, but just regulates the outputs to a different voltage. Each buck converter operates at its VOUT0 voltage in normal operation and operates at its VOUT1 voltage when the DVS input trigger is active. DVS can be implemented two ways.

DVS can be implemented for all buck converters at one time via a single GPIO input. The IC's specific CMI determines the specific GPIO used for DVS. This setting can be modified with a custom CMI.

DVS can be implemented for all buck converters at one time via I²C. The user can select from two different configurations to enter DVS via I²C. Note that DVS is disabled when EN_DVS_I2C = 0.

1. **Enable DVS via a single I²C write to I2C_DVS_ON bit:** With EN_DVS_I2C = 1 and SEL_DVS_IN = 0, the IC outputs enter DVS when I2C_DVS_ON = 1 and exit DVS when it equals 0.

2. **Enable DVS whenever the IC enters SLEEP state:** With EN_DVS_I2C = 1 and SEL_DVS_IN = 1, any condition that puts the IC into SLEEP state also puts the IC into DVS mode. Note that I2C_DVS_ON bit does not affect this configuration.

Note that the IC cannot be configured to enter DVS in DPSLP state. Table 3 summarizes I²C DVS functionality.

EN_DVS_I2C	SEL_DVS_IN	I2C_DVS_ON	DVS MODE
0	x	x	Off
1	0	0	Off
1	0	1	On
1	1	x	On in SLEEP state

Table 3. I²C DVS Control

For fault free operation, the user must ensure output load conditions plus the current required to charge the output capacitance during a DVS rising voltage condition does not exceed the current limit setting of the regulator. As with any power supply, changing an output voltage too fast can require a current higher than the current limit setting. The user must ensure that the voltage step, slew rate, and load current conditions do not result in an instantaneous loading that results in a current limit condition.

Input Voltage Monitoring (SYSMON)

The ACT88325 monitors the input voltage on the VINx pins to ensure it is within specified limits for system level operation. The IC "wakes up" and allows I²C communication when VINx rises above UVLO (~2.7V). However, the outputs do not turn on until VINx rises above the SYSMON threshold. SYSMON is programmable between 2.7V and 4.2V. The IC then asserts the nIRQ pin if VINx drops below SYSMON, but the outputs continue to operate normally. The IC turns off all outputs if the input voltage drops below UVLO. I²C bit VSYSSTAT = 1 when VINx < SYSMON and 0 when VINx > SYSMON. This fault can be masked with I²C bit VSYSMSK.

Fault Protection

The ACT88325 contains several levels of fault protection, including the following:

Output Overvoltage

Output Undervoltage

Output Current Limit and short circuit

Thermal Warning

Thermal Shutdown

There are three types of I²C register bits associated with each fault condition: fault flag bits, fault bits, and mask bits. The fault flag bits display the real-time fault status. Their status is valid regardless of whether or not that fault is masked. The mask bits either block or allow the fault to affect the fault bit. Each potential fault condition can be masked via I²C if desired. Any unmasked fault condition results in the fault bit going high, which asserts the nIRQ pin. nIRQ is typically active low. The nIRQ pin only de-asserts after the fault condition is no longer present and the corresponding fault bit is read via I²C. Note that masked faults can still be read in the fault flag bit. Refer to Active-Semi Application Note describing the Register Map for full details on I²C functionality and programming ranges.

nIRQ (Interrupt)

The interrupt function is typically used to drive the interrupt input of the system processor. Many of the ACT88325's functions support interrupt-generation as a result of various conditions. These are typically masked by default, but may be unmasked via the I²C interface. For more information about the available fault conditions, refer to the appropriate sections of this datasheet. nIRQ can be triggered from:

1. Die temperature warning generated
2. Any buck regulator exceeding peak current limit for 16 cycles after soft start or a UV/OV condition.
3. Any LDO regulator exceeding current limit for more than 16uS after soft start or a UV/OV condition.
4. Input goes above OVP threshold or falls below the UV threshold.

If any of these faults occur the nIRQ output is asserted active low. After nIRQ pin is asserted, an I²C reading operation of the interrupt status registers clears the interrupt provided the interrupting condition is removed. If the interrupting condition is still present, nIRQ stays asserted and the interrupt status bit stays set. The interrupt status registers are 0x00h, 0x01h, 0x03h, 0x04h, 0x05h, 0xA0h, 0xA6h, and 0xE5h.

The ICs specific CMI determines which GPIOx is used for the nIRQ pin. nIRQ is an open-drain output and should be pulled up to an appropriate supply voltage with a 10kΩ or greater pull-up resistor.

nRESET

The ACT88325 provides a reset function to issue a master reset to the system CPU/controller. nRESET is immediately asserted low when either the VIN voltage is above or below the UV or OV thresholds or any power supply that is connected to the nRESET functionality goes below its Power Good threshold. The IC's specific CMI configures which power supplies are connected to the nRESET functionality. After startup, nRESET de-asserts after a programmable delay time when VIN and all connected power supply outputs are above their respective UVLO thresholds. The reset delay time, 20ms to 100ms, is controlled by the I²C TRST_DLY register bits. The IC's CMI programs the specific GPIOx pin used for the reset functionality. The CMI also programs which regulators outputs are monitored for the reset functionality.

EXT_EN

The ACT88325 provides an external power supply enable function, EXT_EN. EXT_EN is used to control an external regulator or to provide a control signal to other system components. It is used as part of the sequencing profile and can be programmed to have different input triggers as well as delay times. The IC's CMI programs the specific GPIOx pin used for the EXT_EN functionality.

EXT_PG

The ACT88325 provides an external input trigger, EXT_PG, for startup sequencing. EXT_PG can be used as the startup trigger for one or of the power supplies. EXT_EN and EXT_PG allow the IC to fully incorporate one or more external power supplies into the startup sequence. The IC's CMI programs the specific GPIOx pin used for the EXT_EN functionality.

Output Under/Over Voltage

The ACT88325 monitors the output voltages for under voltage and over voltage conditions. If an output enters an UV/OV fault condition, the IC shuts down all outputs for 100ms and restarts with the programmed power up sequence. If an output is in current limit, it is possible that its voltage can drop below the UV threshold which

also shuts down all outputs. If that behavior is not desired, mask the appropriate fault bit. Each output still provides its real-time UV/OV fault status via its fault flag, even if the fault is masked. Masking an OV/UV fault just prevents the fault from being reported via the IRQ pin. A UV/OV fault condition pulls the nRESET pin low. Note that the IC's specific CMI sets the defaults for which regulators mask the UV and OV fault conditions.

Output Current Limit

The ACT88325 incorporates a three level overcurrent protection scheme for the buck converters and a single level scheme for the LDOs. For the buck converters, the overcurrent current threshold refers to the peak switch current. The first protection level is when a buck converter's peak switch current reaches 75% of the Cycle-by-Cycle current limit threshold for greater than 16 switching cycles. Under this condition, the IC reports the fault via the appropriate fault flag bit. If the fault is unmasked, it asserts the nIRQ pin. The next level is when the current increases to the Cycle-by-Cycle threshold. The buck converter limits the peak switch current in each switching cycle. This reduces the effective duty cycle and causes the output voltage to drop, potentially creating an undervoltage condition. When the overcurrent condition results in an UV condition, and UV is not masked, the IC turns off all supplies for 100ms and restarts. The third level is when the peak switch current reaches 122% of the Cycle-by-Cycle current limit threshold. This immediately shuts down the regulator and waits 14ms before restarting.

For LDOs, the overcurrent thresholds are set by each LDO's Output Current Limit setting. When the output current reaches the Current Limit threshold, the LDO limits the output current. This reduces the output voltage, creating an undervoltage condition, causing all supplies to turn off for 100ms before restarting.

The overcurrent fault limits for the buck converters are adjustable via I^2C. LDO current limit is fixed. Overcurrent fault reporting can be masked via I^2C, but the overcurrent limits are always active and will shut down the IC when exceeded.

Thermal Warning and Thermal Shutdown

The ACT88325 monitors its internal die temperature and reports a warning via nIRQ when the temperature rises above the Thermal Interrupt Threshold of typically 135 deg C. It reports a fault when the temperature rises above the Thermal Shutdown Temperature of typically 160 deg C. A temperature fault shuts down all outputs unless the fault is masked. Both the fault and the warning can be masked via I2C. The temperature warning and fault flags still provide real-time status even if the faults are masked. Masking just prevents the faults from being reported via the nIRQ pin.

Pin Descriptions

Many of the ACT88325 input and output pins are configurable via CMI configurations. The following descriptions are refer to basic pin functions and capabilities. Refer to the CMI Options section in the back of the datasheet for specific pin functionality for each CMI.

VIN_Bx

VIN_Bx pins are the dedicated input power to the buck converters. Each buck converter must be bypassed directly to its PGNDx pin on the top PCB layer with a 10uF capacitor.

AVIN

AVIN is the input power to the LDOs. It also powers the IC's analog circuitry. AVIN must be bypassed directly to AGND on the top PCB layer with a 1uF ceramic capacitor.

VIN_IO

This is the bias supply input to the IC's digital circuitry. It powers the GPIO pins. VIN_IO is typically connected to the VIN_Bx pins, but can be powered from a different voltage rail if desired. VIN_IO should be bypassed to PGNDx with a 1uF ceramic capacitor.

PWREN

PWREN is a digital input that helps determine if the IC operates in POWER ON mode or DPSLP mode. Refer to the DPSLP State section for details. Refer to the EC table to ensure that the PWREN input voltage meets the IC's logic level requirements.

PWREN is referenced to the AVIN pin, and is 5.5V tolerant meaning that PWREN can go to 5.5V even if AVIN is less than 5.5V. PWREN has a 10us bidirectional filter to prevent unwanted triggering from noise.

GPIOx

The ACT88325 has four GPIO pins. Each GPIO is programmed for a specific function by the IC's CMI. The available functions are input triggers for sequencing (EXT_PG), output triggers for sequencing (EXT_EN), nRESET, nIRQ, DVS, voltage select pins for the voltage regulators, LED drivers, and GPIO.

GPIO1 (pin D7). GPIO1 can be programmed for any of the above functions except the LED drivers. It can be programmed as an input or an open drain or push-pull output.

GPIO2 (pin D6). GPIO2 is the same as GPIO1

GPIO3 (pin E6). GPIO3 can be programmed for all the above functions including the LED drivers. It can be programmed as an input or an open drain output.

GPIO4 (pin C7). GPIO4 is the same as GPIO3

The GPIOs are 5.5V tolerant meaning they can go to 5.5V even if VIN_IO is less than 5.5V.

SCL, SDA

These are the I²C clock and data pins to the IC. They have standard I²C functionality.

PGNDx

The PGNDx pins are the buck converter power ground pins. They connect directly to the buck converters' low side FETs. Buck1 and Buck2 use pins D4, E4, and F4 (PGND12). Buck3 uses pin A5 (PGND3).

SWx

SWx are the switch nodes for the buck converters. They connect directly to the buck inductor on the top layer.

FB_Bx

These are the feedback pins for the buck regulators. They should be kelvin connected to the buck output capacitors.

LSG

LSG is the load switch FET gate drive pin.

LDOx

These are the LDO output pins. Each LDO output must be bypassed to AGND with a 1uF capacitor.

AGND

AGND is the ground pin for the IC's analog circuitry and LDOs. AGND must be connected to the IC's PGNDx pins. The connection between AGND and the PGNDx pins should not have high currents flowing through it.

Step-down DC/DC Converters

General Description

The ACT88325 contains three fully integrated step-down converters. Buck1 is a 4A output, Buck2 and Buck3 are 3A outputs. All buck converters are fixed frequency, current-mode controlled, synchronous PWM converters that achieve peak efficiencies of up to 95%. The buck converters switch at 1.125MHz or 2.25MHz and are internally compensated, requiring only three small external components (Cin, Cout, and L) for operation. The buck regulators minimize noise in sensitive applications with the use of a switching phase delay and offset. Additionally, all regulators are available with a variety of standard and custom output voltages, and may be software-controlled via the I²C interface for systems that require advanced power management functions.

The ACT88325 buck regulators are highly configurable and can be quickly and easily reconfigured via I²C. This allows them to support changes in hardware requirements without the need for PCB changes. Examples of I²C functionality are given below:

Real-time power good, OV, and current limit status

Ability to mask individual faults

Dynamically change output voltage

On/Off control

Softstart ramp

Switching delay and phase control

Low power mode

Overcurrent thresholds

Refer to the Active-Semi Application Note describing the Register Map for full details on I²C functionality and programming ranges.

100% Duty Cycle Operation

All buck converters are capable of 100% duty cycle operation. During 100% duty cycle operation, the high-side power MOSFETs are held on continuously, providing a direct connection from the input to the output (through the inductor), ensuring the lowest possible dropout voltage in battery powered applications.

Operating Mode

By default, all buck converters operate in fixed-frequency PWM mode at medium to heavy loads, then transition to a proprietary power-saving mode at light loads in order to save power. Power-save mode reduces conduction losses by preventing the inductor current from going negative.

To further optimize efficiency and reduce power losses at extremely light loads, an additional lower power mode, LPM, is available. LPM minimizes quiescent current in between switching cycles. This reduces input current by approximately 200µA in LPM mode. Light load output voltage ripple increases from approximately 5mV to 10mV when in LPM mode. Light load voltage droop when going from light load to heavier loads is only increased by 2-3mV when in LPM mode. LPM allows the customer to test the IC in their use case and optimize the balance between power consumption, voltage ripple, and transient response in their system. LPM is enabled when I2C bits DISLPM = 0 and LP_MODE = 1.

The buck converters can also be forced to operate in PWM mode at light load by setting I²C bit ForcePWM = 1. This results in slightly lower efficiency at light loads, but improves transient response.

Synchronous Rectification

Buck1/2/3 each feature integrated synchronous rectifiers (or LS FET drivers), maximizing efficiency and minimizing the total solution size and cost by eliminating the need for external rectifiers.

Soft-Start

Buck1/2/3 include internal 600us soft-start ramps which limit the rate of change of the output voltage, minimizing input inrush current and ensuring that the output powers up in a monotonic manner that is independent of loading on the outputs. This circuitry is effective any time the regulator is enabled, as well as after responding to a short-circuit or other fault condition. A single I²C register, ALL_BUCKS_FASTER_SS, adjusts softstart between 600us when = 0 and 250us when = 1.

Output Voltage Setting

Buck1/2/3 regulate to the voltage defined by I²C register VSET0 in normal operation and by VSET1 in DVS mode. The ACT88325 has two output voltage programing ranges.

Output range 1 is available to Buck1/2. This range can be programmed between 0.6V and 2.991V in 9.376mV steps.

Vbuck1=0.6V + VOUTx * 0.009376V

Where VOUTx is the decimal equivalent of the value in each regulator's I²C VOUTx register. The VOUTx registers contain an unsigned 8-bit binary value. As an example, if Buck 1's VOUT0 register contains 01000000b (128 decimal), the output voltage is 1.8V.

Output range 2 is available to Buck1/2/3. This range can be programmed between 0.8V to 3.9875V in 12.5mV steps.

Vbuck1 = 0.8V + VOUTx * 0.0125V

The following table summarizes the buck reference voltage options.

Buck1 Voltage Reference Selections

	BUCK1_VREF_MUX = 0	BUCK1_VREF_MUX = 1
Vref (V)	0.8	0.6
Vout Range (V)	0.8 – 3.9875	0.6 – 2.991
Vout Step Size (mV)	12.5	9.375

Buck2 Voltage Reference Selections

	VREF_SEL_BUCK2 = 0	VREF_SEL_BUCK2 = 1
Vref (V)	0.6	0.8
Vout Range (V)	0.6 – 2.991	0.8 – 3.9875
Vout Step Size (mV)	9.375	12.5

See each IC's CMI for each buck converter programing range. Note that the Buck1 programming range is not customer accessible. The Buck2 programming range is customer accessible, but should NOT be changed. Changing this register value may result in unexpected IC behavior.

Active Semi recommends that the buck converter's output voltage be kept within +/- 25% of the default output voltage to maintain accuracy. Voltage changes larger than +/- 25% may require different factory trim settings (new CMI) to maintain accuracy.

DVS

Each buck converter supports Dynamic Voltage Scaling (DVS). In normal operation for most CMI options, each output regulates to the voltage programmed by its VSET0 I²C register. During DVS, each output can be programmed to regulate to its VSET1 voltage.

During the voltage transition between VSET0 to VSET1 and VSET1 to VSET0, the I²C bit FORCEPWM is set to 1 to force the buck converters into PWM mode. This ensures that the output transition to the new voltage level as quickly as possible. The outputs transition between

the two set points at a defined slew rate to minimize in-rush currents. Note that VSET0 must be set higher than VSET1. Violating this requirement results in an OV fault during DVS.

For fault free operation, the user must ensure output load conditions plus the current required to charge the output capacitance during a DVS rising voltage condition does not exceed the current limit setting of the regulator. As with any power supply, changing an output voltage too fast can require a current higher than the current limit setting. The user must ensure that the voltage step, slew rate, and load current conditions do not result in an instantaneous loading that results in a current limit condition. See paragraph Dynamic Voltage Scaling for options to enter and exit DVS.

Enable / Disable Control

During normal operation, each buck may be enabled or disabled via the I²C interface by writing to that regulator's ON bit. Note that disabling a regulator that is used as an input trigger to another regulator may or may not disable the other regulators following it, depending on the specific CMI settings. Each buck converter has a load discharge function designed to quickly pull the output voltage to ground when the converter is disabled. The circuit connects an internal resistor (4.4ohm for Buck1 and 9.4ohms for Buck2/3) from the output to PGND when the converter is disabled.

POK and Output Fault Interrupt

Each DC/DC features a power-OK status bit, POK, which can be read by the system microprocessor via the I²C interface. If an output voltage is lower than the POK threshold, typically 7% below the programmed regulation voltage, that regulator's POK bit will be 0.

If a DC/DC's nFLTMSK[ ] bit is set to 1, the ACT88325 will interrupt the processor if the DC/DC's output voltage falls below the power-OK threshold. In this case, nIRQ asserts low and remains asserted until either the regulator is turned off or goes back into regulation, and the POK [ ] bit has been read via I²C.

Optimizing Noise

Each buck converter contains several features available via I²C to further optimize functionality. The top P-ch FET's turn-on timing can be shifted approximately 110ns from the master clock edge via the PHASE_DELAY I²C bit. It can also be aligned to the rising or falling clock edge via the PHASE I²C bit.

Minimum On-Time

The ACT88325 minimum on-time is approximately 125ns. If a buck converter's calculated on-time is less than 125ns with 2.25MHz operation, then the buck converter must be operated at 1.125MHz. Active Semi will generate the IC CMIs to ensure that the buck converters do not run into the minimum on-time limitations. The following equation calculates the on-time.

$$T_{ON} = \frac{V_{OUT}}{V_{IN} * F_{SW}}$$

Where Vout is the output voltage, VIN is the input voltage, and FSW is the switching frequency.

Overcurrent and Short Circuit Protection

Each buck converter provides overcurrent and short circuit protection with built in foldback protection. Overcurrent protection is achieved with cycle-by-cycle current limiting. The peak current threshold is set by the ILIM_SET I²C bits.

If the peak current reaches 75% of the programmed threshold for 16 consecutive switching cycles, the IC asserts nIRQ low and changes I²C bit ILIM_WARN = 1, but continues to operate normally.

If the peak current reaches the programmed threshold, the IC turns off the power FET for that switching cycle. If the peak current reaches the threshold 16 consecutive switching cycles, the IC asserts nIRQ low. This condition typically results in shutdown due to an UV condition due to the shortened switching cycle.

A short circuit condition that results in the peak switch current being 122.5% of ILIM_SET immediately shuts down the supply and asserts nIRQ low if the fault bit is not masked. The supply tries to restart in 14ms. If the fault condition is not masked, the IC transitions to the OVUV State, turns off all supplies, and restarts the system in 100ms.

The buck converters also have built in current foldback protection. After softstart is complete, if a short circuit or overload condition causes the output to go out of regulation for > 28us, the IC reduces the peak-to-peak current limit to 1.5A. This reduces system level power dissipation in short circuit or overload conditions. If the load current drops low enough to allow the output voltage to enter regulation with the reduced peak-to-peak current limit, the output restarts and the IC resets the peak-to-peak current limit to the default value

If a buck converter reaches overcurrent or short circuit protection, the status is reported in the ILIM I²C registers. The contents of these registers are latched until

read via I²C. Overcurrent and short circuit conditions can be masked via the I²C bit ILIM_FLTMSK. The IC's specific CMI determines which regulators mask the current limit fault.

Compensation

The buck converters utilize current-mode control and a proprietary internal compensation scheme to simultaneously simplify external component selection and optimize transient performance over their full operating range. No compensation design is required; simply follow a few simple guide lines described below when choosing external components.

Input Capacitor Selection

Each buck converter has a dedicated input pin and power ground pin. Each buck converter should have a dedicated input capacitor that is optimally placed to minimize the power routing loops for each buck converter. Note that even though each buck converter has separate inputs, all buck converter inputs must be connected to the same voltage potential.

Each regulator requires a high quality, low-ESR, ceramic input capacitor. 10uF capacitors are typically suitable, but this value can be increased without limit. Smaller capacitor values can be used with lighter output loads. Choose the input capacitor value to keep the input voltage ripple less than 50mV.

$$V_{ripple} = Iout * \frac{\frac{Vout}{Vin} * \left(1 - \frac{Vout}{Vin}\right)}{Fsw * Cin}$$

Be sure to consider the capacitor's DC bias effects and maximum ripple current rating when using capacitors smaller than 0805.

A capacitor's actual capacitance is strongly affected by its DC bias characteristics. The input capacitor is typically an X5R, X7R, or similar dielectric. Use of Y5U, Z5U, or similar dielectrics is not recommended. Input capacitor placement is critical for proper operation. Each buck's input capacitor must be placed as close to the IC as possible. The traces from VIN to the capacitor and from the capacitor to PGND should as short and wide as possible.

Inductor Selection

The Buck converters utilize current-mode control and a proprietary internal compensation scheme to simultaneously simplify external component selection and optimize transient performance over their full operating range. The ACT88325 is optimized for operation with 1.0µH inductors, but can be used with inductor values 1uH to 2.2uH. Choose an inductor with a low DC-resistance, and avoid inductor saturation by choosing inductors with DC ratings that exceed the maximum output current by at least 30%. The following equation calculates the inductor ripple current.

$$\Delta I_L = \frac{\left(1 - \frac{V_{OUT}}{V_{IN}}\right) * V_{OUT}}{F_{SW} * L}$$

Where V_{OUT} is the output voltage, V_{IN} is the input voltage, F_{SW} is the switching frequency, and L is the inductor value.

Output Capacitor Selection

The ACT88325 is designed to use small, low ESR, ceramic output capacitors. Buck1 typically requires 2x22uF or a single 47uF output capacitor while Buck2 and Buck3 require a 22uF output capacitor each. In order to ensure stability, the Buck1 effective capacitance must be greater than 20uF while Buck2 and Buck3 effective capacitance must be greater than 12uF. The output capacitance can be increased to reduce output voltage ripple and improve load transients if needed. Design for an output ripple voltage less than 1% of the output voltage. The following equation calculates the output voltage ripple as a function of output capacitance.

$$V_{RIPPLE} = \frac{\Delta I_L}{8 * F_{SW} * C_{OUT}}$$

Where ΔI_L is the inductor ripple current, F_{SW} is the switching frequency, and C_{OUT} is the output capacitance after taking DC bias into account.

Be sure to consider the capacitor's DC bias effects and maximum ripple current rating when using capacitors smaller than 0805.

A capacitor's actual capacitance is strongly affected by its DC bias characteristics. The output capacitor is typically an X5R, X7R, or similar dielectric. Use of Y5U, Z5U, or similar dielectrics are not recommended due to their wide variation in capacitance over temperature and voltage ranges.

Buck1 Bypass mode

General Description

Buck1 is configurable as a bypass switch for systems with a 3.3V bus voltage. The bypass switch provides full sequencing capability by allowing the 3.3V bus to be used as the input to the other supplies and still be properly sequenced to the downstream load. In bypass mode, the Buck1 P-ch FET acts as a switch and the N-ch FET is disabled. The bypass switch turns on the 3.3V rail with the programmed delay and softstart time.

In bypass mode, the ACT88325 Buck 1 I²C registers are reconfigured to the following.

1. ILIM bit is the output of the PMOS Current Detection circuit. In an overcurrent condition, ILIM triggers the nIRQ output. ILIM is latched until read via I²C. ILIM can be masked with the ILIM_FLTMSK register.
2. The UV register bit is reconfigured to the output of the PMOS Current Shutdown circuit. This is set to 5.6A typical. If the bypass switch current exceeds 5.6A, it limits the current which triggers an under voltage fault condition and moves the IC into the OVUV FAULT state. This immediately shuts down all regulators including the bypass switch. The system restarts in 100mS, following the programmed startup sequencing. This fault can be masked with I²C bit UV_FLTMASK. This fault is latched in the UV_REG I²C bit.
3. OV is disabled. There is no overvoltage detection circuitry on the output of the bypass switch.

LDO Converters

General Description

The ACT88325 contains two fully integrated, 300mA, low dropout linear regulators (LDO). LDOs have been optimized to achieve low dropout and high PSRR. The LDOs can also be configured in load switch mode to behave like load switches.

The LDOs require only two small external components (Cin, Cout) for operation. They ship with default output voltages that can be modified via the I²C interface for systems that require advanced power management functions.

Soft-Start

Each LDO contains a softstart circuit that limits the rate of change of the output voltage, minimizing input inrush current and ensuring that the outputs power up monotonically. This circuitry is effective any time the LDO is enabled, as well as after responding to a short circuit or other fault condition. Each LDO's softstart time is fixed to 275us.

Output Voltage Setting

The LDOs regulate to the voltage defined by their I²C registers LDO1_VSET and LDO2_VSET. The LDOs do not have a second VSET register like the buck converters. The LDOs can be configured with two different output voltage range settings. I²C register bit VREF_CTRL controls the two settings. This bit is factory set and is not user configurable.

	VREF_CTRL = 0	VREF_CTRL = 1
Vref (V)	0.8	0.6
Vout Range (V)	0.8 – 3.9875	0.6 – 2.991
Vout Step Size (mV)	12.5	9.375

The following equation determines the LDO output voltages when VREF_CTRL = 0.

VLDOx = 0.8V + LDOx_VSET * 0.0125V

The following equation determines the LDO output voltages when VREF_CTRL = 1.

VLDOx = 0.6V + LDOx_VSET * 0.009375V

Active Semi recommends that the LDO's output voltage be kept within +/- 25% of the default output voltage to maintain accuracy. Voltage changes larger than +/- 25% may require different factory trim settings (new CMI) to maintain accuracy.

Enable / Disable Control

During normal operation, each LDO may be enabled or disabled via the I²C interface by writing to that regulator's ON bit. Note that disabling an LDO that is used as an input trigger to another regulator may or may not disable the other regulators following it, depending on the specific CMI settings. Each LDO has a load discharge function designed to quickly pull the output voltage to ground when the LDO is disabled. The circuit connects an internal resistor (50ohm) from the output to AGND when the LDO is disabled.

POK and Output Fault Interrupt

Each LDO features a power-OK status bit, POK, which can be read by the system microprocessor via the I²C interface. If an output voltage is lower than the POK threshold, typically 11% below the programmed regulation voltage, that regulator's POK bit will be 0.

If an LDO's nFLTMSK[ ] bit is set to 1, the ACT88325 will interrupt the processor if that LDO's output voltage falls below the power-OK threshold. In this case, nIRQ asserts low and remains asserted until either the LDO is turned off or goes back into regulation, and the POK [ ] bit has been read via I²C.

Overcurrent and Short Circuit Protection

Each LDO provides overcurrent detection and short circuit protection featuring a current-limit foldback function. When current limit is reached, the IC can either shut the output off or limit the output current until the overload condition is removed. This is controlled by I2C bits LDOx_ILIM_SHUTDOWN_DIS.

The overcurrent threshold is set by the ILIM1 and ILIM2 I²C bits. In both an overload and a short circuit condition, the LDO limits the output current which causes the output voltage to drop. This can result in an undervoltage fault in addition to the current limit fault. If an LDO load reaches overcurrent detection threshold, the status is reported in the ILIM_LDOx I²C registers. The contents of these registers are latched until read via I²C. When the current limiting results in a drop in output voltage that triggers an undervoltage condition, the IC shuts down all power supplies, asserts nIRQ low, and enters the UVLOFLT state provided the faults are not masked. Once in the OVUVFLT state, the IC restarts in 100ms and starts up with default sequencing. Overcurrent and short circuit conditions can be masked via the I²C bit ILIMFLTMSK_LDOx. When masked, the LDO still shuts down or limits current (based on the LDOx_ILIM_SHUTDOWN_DIS bit). In this condition, it does not enter the OVUVFLT state due to the faults being masked. If it shuts down, it automatically restarts in 14ms.

Input Capacitor Selection

The AVIN pins supplies the input power to both LDO. AVIN requires a high quality, low-ESR, ceramic input capacitor. A 1uF is typically suitable, but this value can be increased without limit. The input capacitor is should be a X5R, X7R, or similar dielectric.

Output Capacitor Selection

Each LDO requires a high quality, low-ESR, ceramic output capacitor. A 1uF is typically suitable, but this value can be increased without limit. The input capacitor is should be a X5R, X7R, or similar dielectric. The LDO effective output capacitance must be greater than 0.7uF.

Load Switch Mode

LDO2 can be configured as a load switch. In this mode, the device still monitors the load current and shuts off when the current goes above 500mA. It then enters hiccup mode until the fault has cleared. The LDO2 load switch does not monitor the output voltage. It monitors the input voltage and disables its internal power good signal when the voltage drops below 2.6V. It also disables the power good when the load current exceeds the current limit threshold. When in load switch mode, the LDOs pass the input voltage directly to the output voltage. Put LDO1 into load switch mode by setting I²C bit LDO2_LSW_MODE in register 0xECh to 1.

LOAD SWITCH

General Description

The ACT88325 features a Load Switch gate driver, LSG, to power an external n-ch FET. The Load Switch allows a common power rail to be switched on/off to create a power "island" for system loads. This "island" can be turned off to minimize power consumption when those loads are not needed. The Load Switch can also be incorporated into the ICs startup sequencing with programmable turn-on and turn-off delay times. It can also be programed to be turned on or off in SLEEP and DPSLP states.

Softstart

The LSG incorporates a programmable slew rate to control the turn-on speed of the external FET. The LSG output consists of a current source to linearly charge the external FET gate voltage. The slew rate is controlled via the I²C bits GATE1_SLEW[1:0]. The current source is programmable between 2.5uA and 10uA in 2.5uA increments. The slew rate is

$$\mathrm{SLEW} = \frac{I_{LSG}}{C_{FET\_GATE}}$$

Where SLEW is the LSG slew rate in V/s, I_{LSG} is the gate drive current in Amps, and C_{FET_GATE} is the external FET gate capacitance in Farads. Adding a discrete gate capacitor will provide more consistent Load Switch turn on characteristics.

LSG has an active 75 ohm pulldown resistor when disabled to quickly turn off the external FET.

Current Limit

Because LSG only connects to the external FET gate, Load Switch does not have a current limit function. The input to the Load Switch should come from an ACT88325 Buck, LDO, or other current limited source.

Load Switch POK

The load switch internal Power OK, POK, signal can be used in the sequencing of other power supplies. The load switch POK signal goes active when the load switch gate drive voltage at the LSG pin is greater than VIN + 1V and VIN – VOUT < 100mV. Note that the actual load switch may or may not be fully on at this time depending on the FET used for the load switch or any additional filtering or delay circuitry connected to LSG.

PC board layout guidance

Proper parts placement and PCB layout are critical to the operation of switching power supplies. Follow the following layout guidelines when designing the ACT88325 PCB. Refer to the Active-Semi ACT88325 Evaluation Kits for layout examples. The ACT88325 pinout is designed so the optimal PCB layout is still compatible with low-cost, plated through hole (PTH) PCBs and assembly processes.

1. Place the buck input capacitors as close as possible to the IC. Refer to the Pin Descriptions for each buck converter's dedicated VINx and PGNDx pins. Connect the input capacitors directly to the corresponding VINx and PGNDx power ground pin on the top layer. Routing these traces on the top layer eliminates the need for vias.
2. Minimize the switch node trace length between each SW_Bx pin and the inductor. Optimal switch node routing is to run the trace between the input capacitor's pads. Using 0805 sized input capacitors is recommended. Avoid routing sensitive analog signals near these high frequency, high dV/dt traces.
3. Place the LDO input capacitor close to the AVIN pin. Connect the capacitor directly to AVIN and AGND on the top layer.
4. The Buck output capacitors should be placed by the inductor and connected directly to the inductor and ground plane with short and wide traces. The output capacitor ground should make a short connection to the input capacitor ground. If required, use multiple vias.
5. Each regulator's FB_Bx should be Kelvin connected to its output capacitor through the shortest possible route, while keeping sufficient distance from switching nodes to prevent noise injection. The IC regulates the output voltage to this Kelvin connection.
6. The PGNDx and AGND ground pins must be electrically connected together. Because the AGND ground plane is used for analog, digital, and LDO grounds, it does not need to be completely isolated from the rest of the PCB grounds. However, take care to avoid routing the buck converter switching currents through the analog ground connections.
7. Connect the VIN_IO input capacitor to the AGND ground pin.
8. Remember that all open drain outputs need pull-up resistors.
9. Figure 4 shows the recommended power and signal connections and routing from under the IC. Refer to the ACT88325 evaluation kit for a full, detailed routing example.

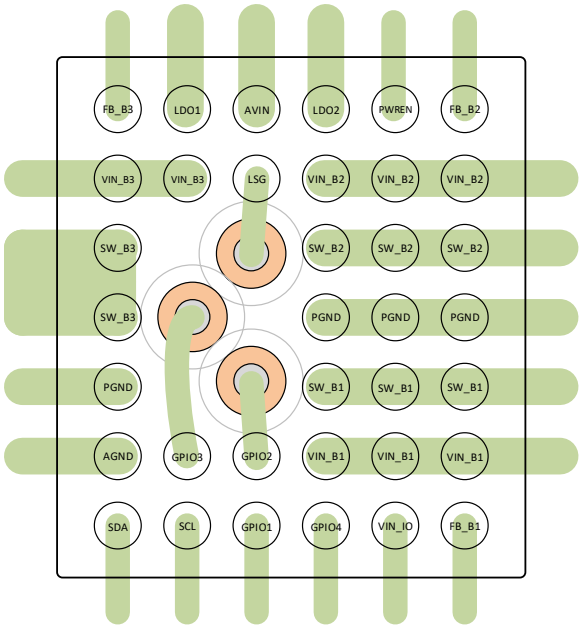
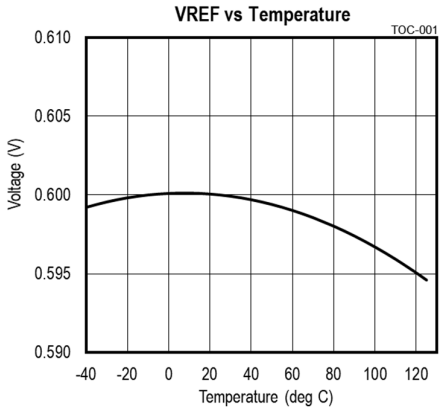
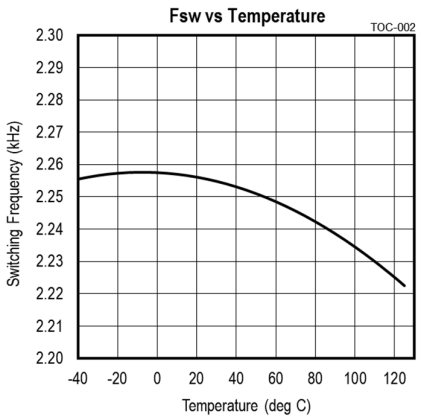
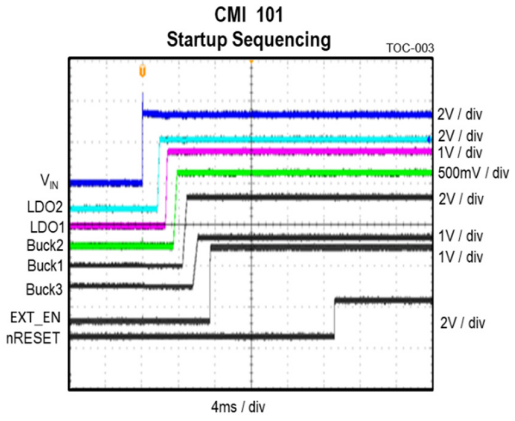


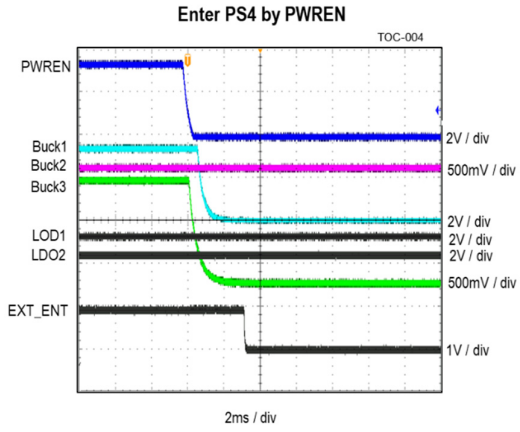
Figure 4: Recommended Routing

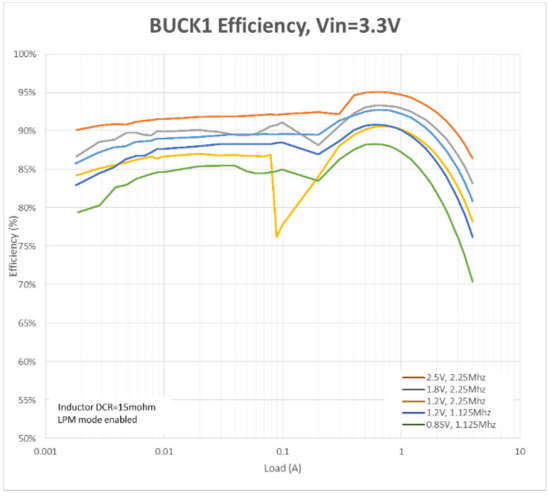
Typical Operating Characteristics

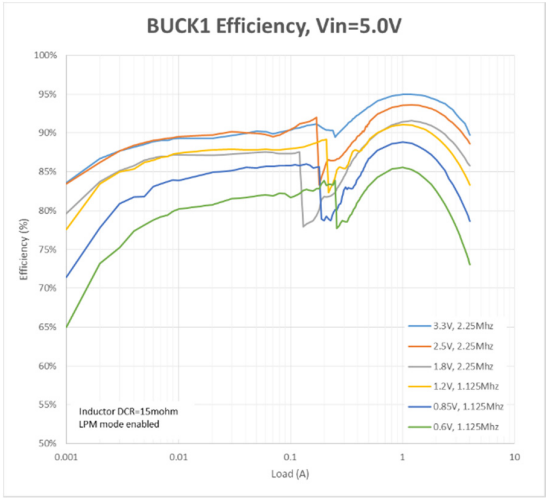


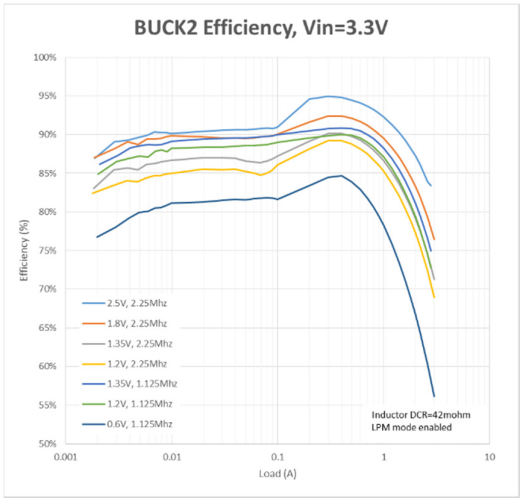


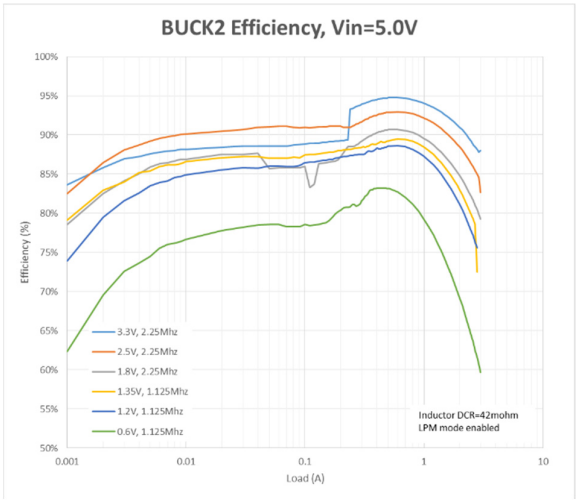


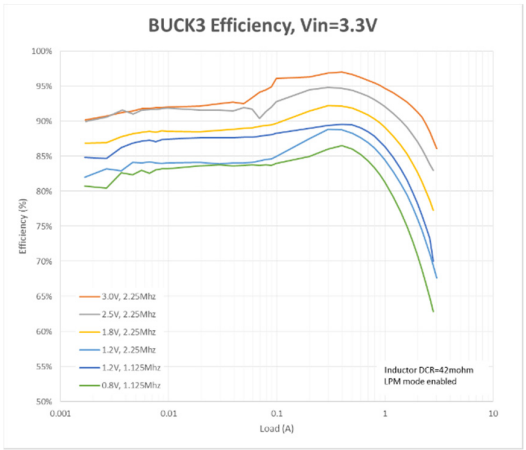


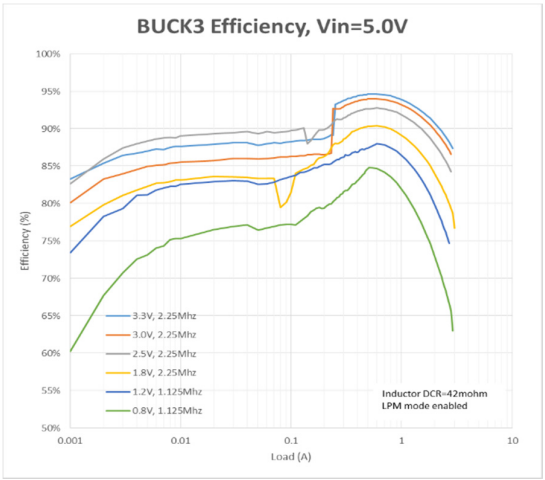


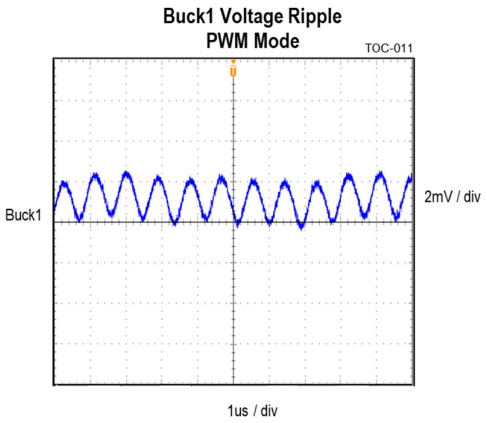


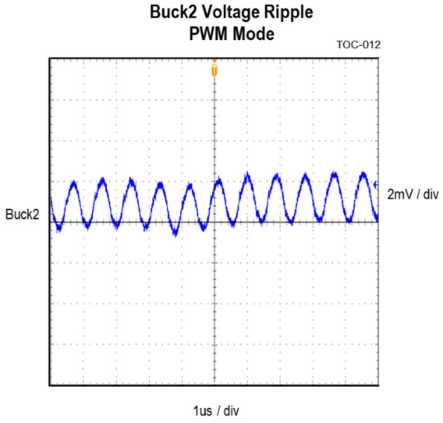


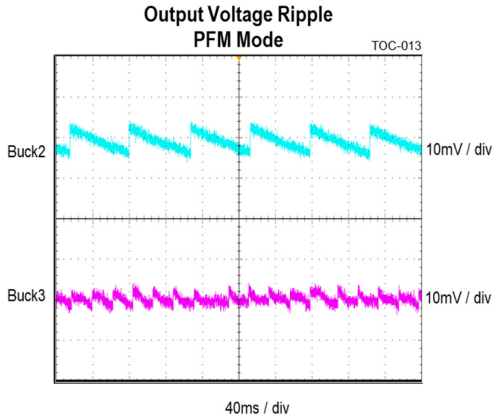


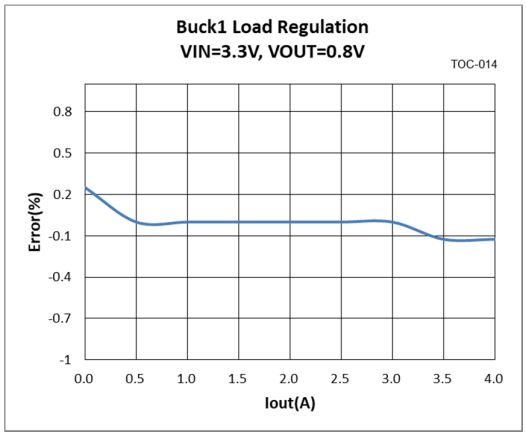


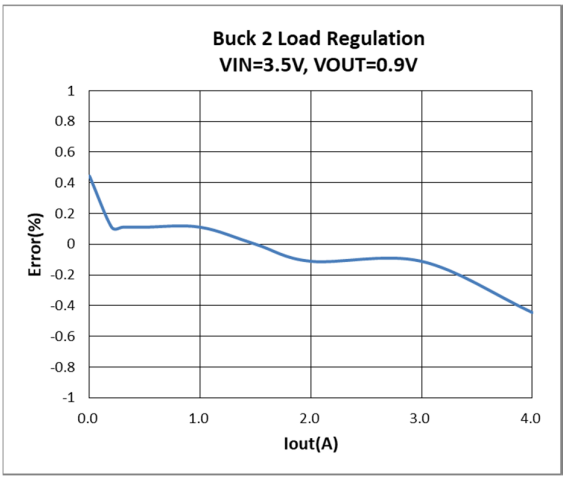


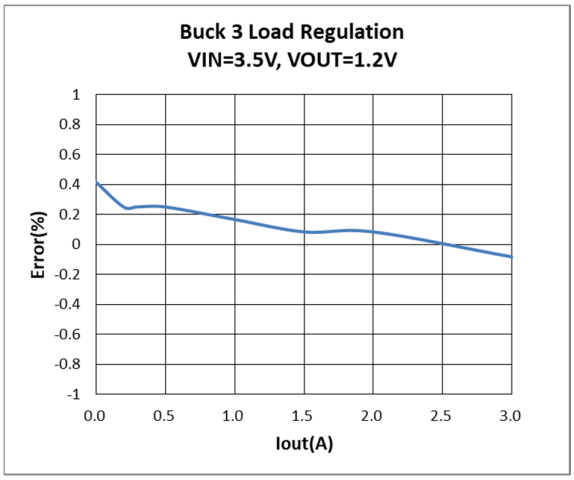


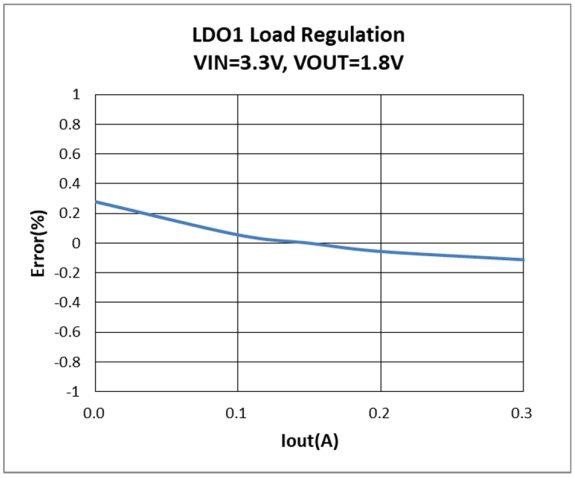


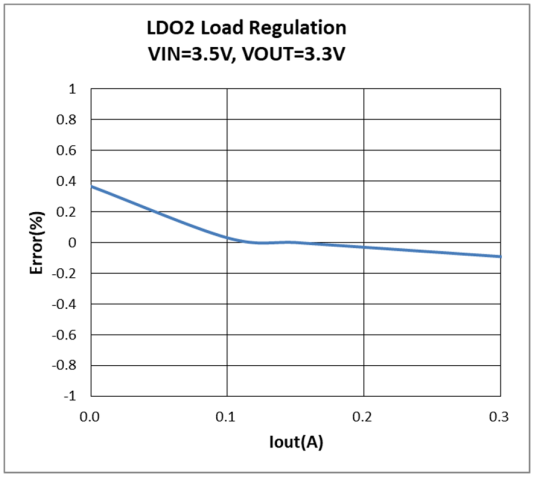




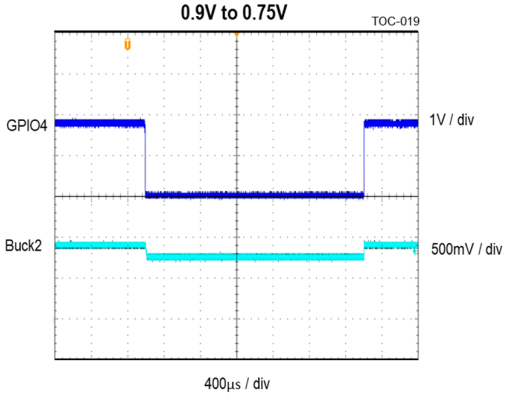




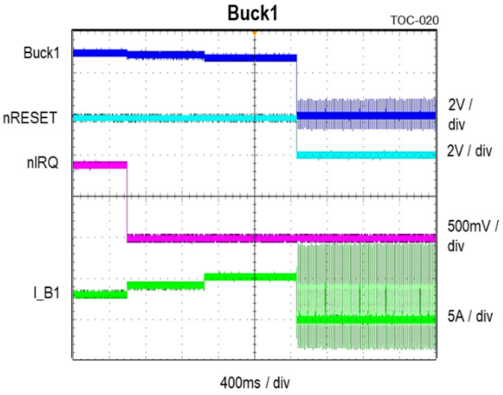




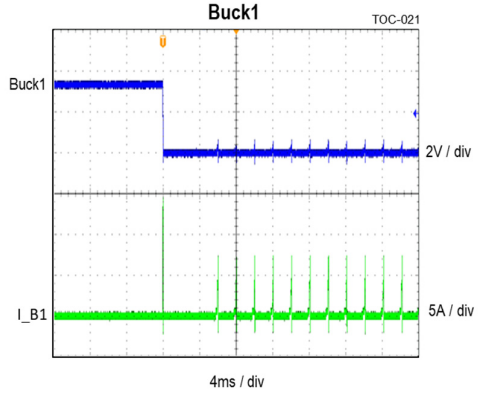
DVS Transition
Buck2
0.9V to 0.75V



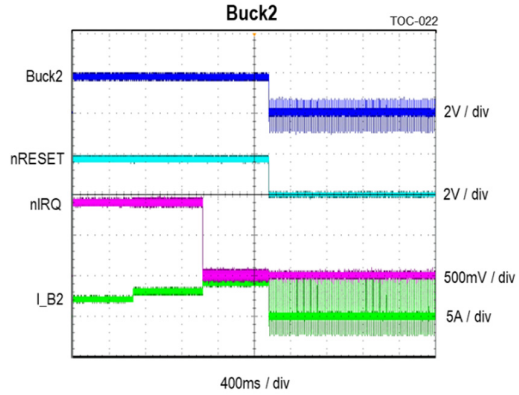
Overcurrent
Buck1



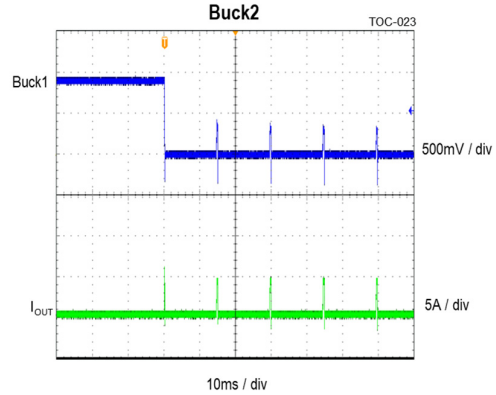
Short Circuit
Buck1



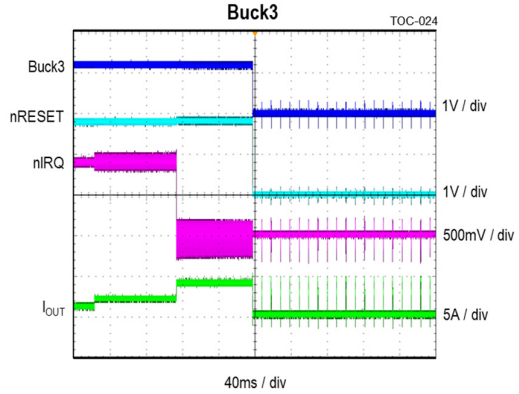
Overcurrent
Buck2



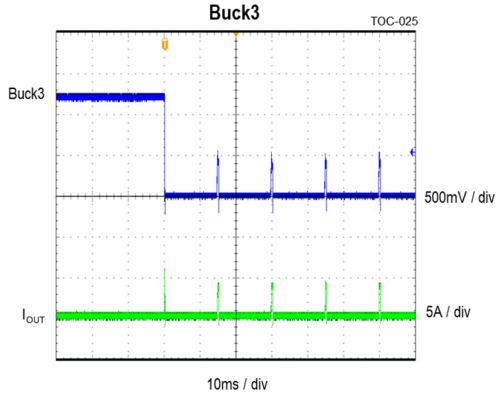
Short Circuit
Buck2



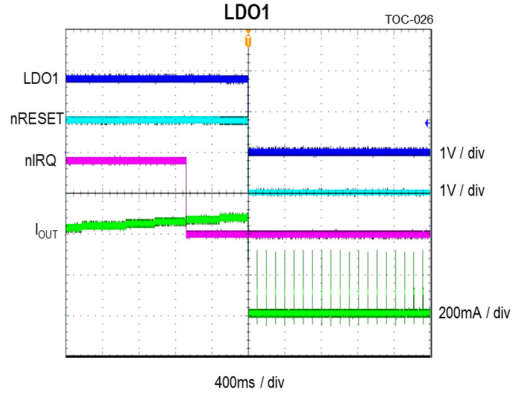
Overcurrent
Buck3



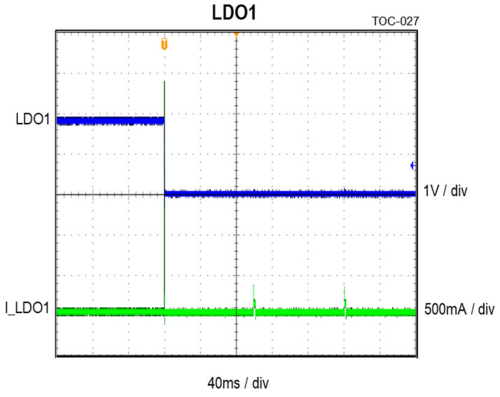
Short Circuit
Buck3



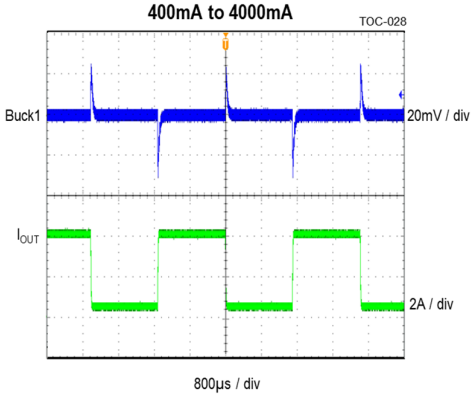
Overcurrent
LDO1



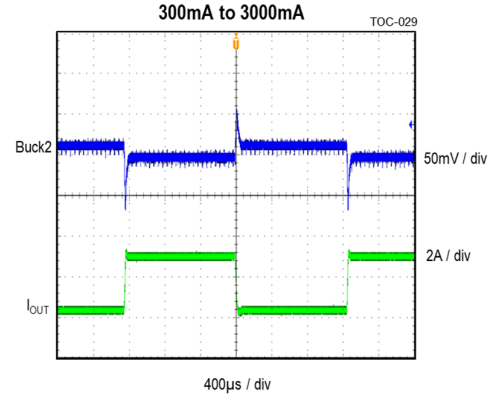
Short Circuit
LDO1



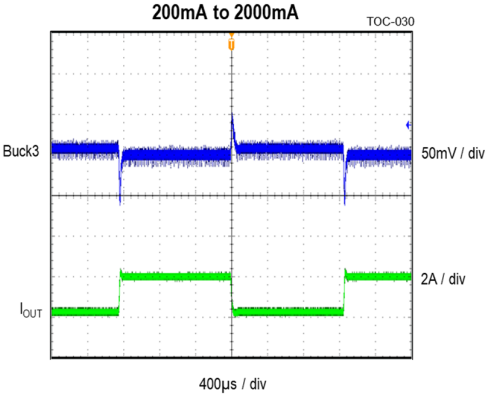
Load Transient
Buck1 Vout=0.8V
400mA to 4000mA

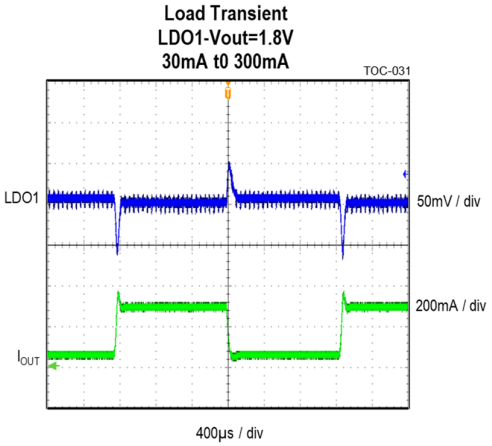


Load Transient
Buck2 Vout=0.9V
300mA to 3000mA



Load Transient
Buck3 Vout=1.2V
200mA to 2000mA





The following components have been used with the ACT88325.

REFERENCE	DESCRIPTION	MANUFACTURER
Input Capacitor, Buck1	22uF, 10V, X5R	Standard
Input Capacitor, Buck2/3	22uF, 10V, X5R	Standard
Input Capacitor, LDO1/2	1uF, 10V, X5R	Standard
Output Capacitor, Buck1	2x22uF, 10V, X5R	Standard
Output Capacitor, Buck2/3	22uF, 10V, X5R	Standard
Output Capacitor, LDO1/2	1uF, 10V, X5R	Standard
Inductor, Buck1	1uH, 12mΩ	Wurth 74438356010
Inductor, Buck2/3/4	1uH, 63mΩ	Wurth 74438323010
VIN_IO	1uF, 10V, X5R	Standard

CMI OPTIONS

This section provides the basic default configuration settings for each available ACT88325 CMI option. IC functionality in this section supersedes functionality in the main datasheet. Generating the desired functionality for a custom CMI sometimes requires reassigning internal resources, resulting in removal of base IC functionality. The following sections attempt to describe any removed functionality from the base IC functionality. The user is required to fully test all required functionality to ensure the CMI fully meets their requirements.

CMI 101: ACT88325VA101-T

CMI 101 is optimized for SMI SM2262, SM2263, SM2263XT processors. The GPIOs are programmed to allow the microprocessor to program the ACT88325 for the three SMI processor operating modes: Normal Mode, PS3.5, and PS4. It also allows programming for 1.2V or 1.8V NAND I/O. CMI 101 is only configured for a 3.3V input voltage.

The following tables describe the ACT88325VA101 IC settings.

Voltage and Currents

Rail	Active Mode Voltage VSET0 (V)	DVS Voltage VSET1 (V)	DVS Input Trigger	Sleep Mode Voltage (V)	DPSLP Mode Voltage (V)	Current Limit (A)	Fsw (kHz)
Buck1	Load Switch ON	Load Switch ON	n/a	OFF	OFF	5.4	n/a
Buck2	0.9	0.75	GPIO4	OFF	ON	4.6	1125
Buck3	1.8	1.2	GPIO3	OFF	OFF	3.9	2250
LDO1	1.8	1.8	n/a	1.8	1.8	0.465	n/a
LDO2	Load Switch ON	Load Switch ON	n/a	Load Switch ON	Load Switch ON	0.465	n/a
EXT_EN	ON	n/a	n/a	OFF	OFF	n/a	n/a
LS1	OFF	n/a	n/a	OFF	OFF	n/a	n/a

Startup and Sequencing

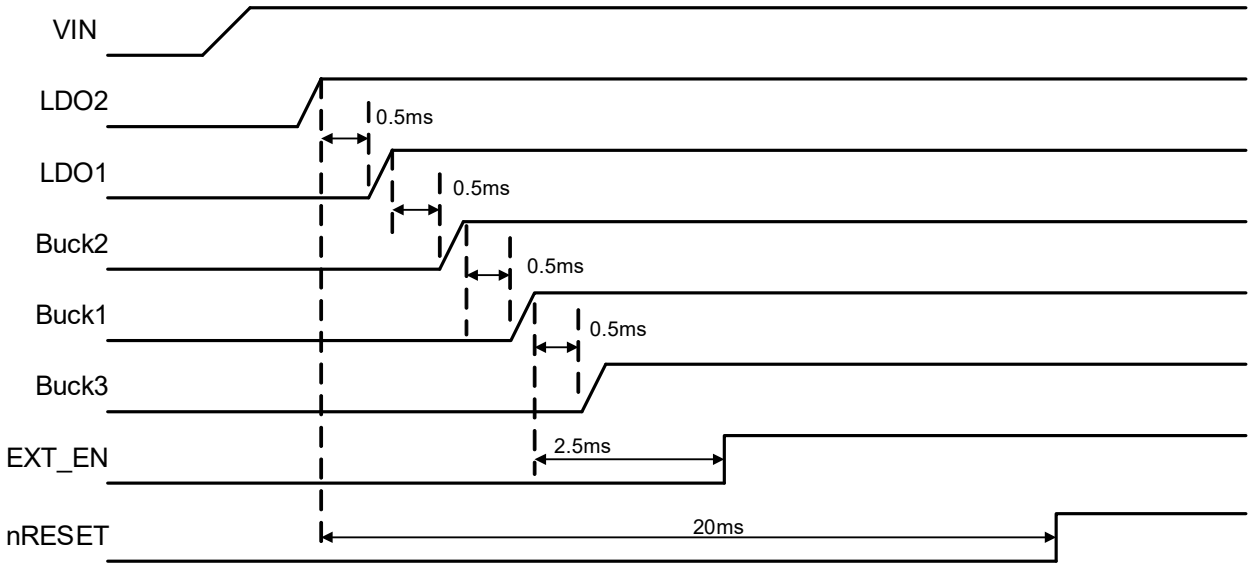
Rail	Sequence Order	Sequencing Input Trigger	StartUp Delay (us)	Soft-Start (us)	Shutdown Delay (us)
LDO2	1	VIN_UVLO	0	275	1500
LDO1	2	LDO2	0	275	2000
Buck2	3	LDO1	500	600	1000
Buck1	4	Buck2	500	600	500
Buck3	5	Buck1	500	600	0
EXT_EN	6	Buck1	2500	n/a	2500
LS1	off	n/a	0	0	0

The following table shows how to configure CMI 101 into operate in each of the three SMI processor power modes. The combination of the PWREN and GPIO4 settings determine the specific power state. When in the Normal or PS3.5 power states, the GPIO3 pin sets Buck3 NAND flash voltage. When GPIO3 = L, Buck3 = 1.8V. When GPIO3 = H, Buck3 = 1.2V. The table does not reflect the Buck3 configurability. It shows the voltages for 1.8V NAND flash.

SMI Processor Power Modes

	Normal Mode GPIO4 = H PWREN = H	**PS 3.5** GPIO4 = L PWREN = H	**PS 4** GPIO4 = L PWREN = L
Buck1	3.3V	3.3V	0V
Buck2	0.9V	0.75V	0.75V
Buck3	1.8V	1.8V	0V
LDO1	1.8V	1.8V	1.8V
LDO2	3.3V	3.3V	3.3V
EXT_EN	H	H	L

CMI 101 Startup



I²C Address

The ACT88325 7-bit I²C address is 0x25h. Use address 0x4Ah when writing and 0x4Bh when reading.

GPIO1 (pin C7) - nRESET

GPIO1 is configured as an open drain nRESET. nRESET goes open drain 20ms after Buck3 goes into regulation.

GPIO2 (pin C6) – EXT_EN

GPIO2 is configured as an open drain EXT_EN. EXT_EN goes high 2.5ms after Buck2 goes into regulation and is intended to sequence an external supply.

GPIO3 (pin B6) – Buck3 DVS Voltage Select

GPIO3 is configured as an input to select the Buck3 output voltage for different NAND memory voltages. When GPIO3 is L, VSET0 sets Buck3 to 1.8V. When GPIO3 is H, VSET1 sets Buck3 to 1.2V. GPIO3 is intended to be pulled high or low by resistor stuffing option at PCB assembly, but can be changed at any time.

GPIO4 (pin D7) – Buck2 DVS Voltage Select

GPIO4 is configured as an input to select the Buck2 output voltage. When GPIO4 is H, VSET0 sets Buck2 to 0.9V. When GPIO4 is L, VSET1 sets Buck2 to 0.75V. GPIO4 in combination with PWREN sets the SMI processor power modes.

PWREN (pin E1) – DPSLP Mode Select

When PWREN is H, the IC is in Active Mode. When PWREN is L, the IC is in DPSLP Mode. GPIO4 in combination with PWREN set the SMI processor power modes.

SLEEP MODE

I²C default settings are SLEEP_MODE=0, SLEEP_EN=0, and SLEEP=0. Refer to the SLEEP State paragraph for details on how to enter SLEEP Mode.

DPSLP MODE

I²C default settings are DPSLP_MODE=1, DPSLP_EN=0, and DPSLP=0. Refer to the DPSLP State paragraph for details on how to enter DPSLP Mode.

VSYSMON

VSYSMON = 2.7V

Buck1 Voltage Setting

Buck1 reference voltage is 0.8V. This sets the allowable voltage range between 0.8V and 3.998V in 12.5mV steps.

Buck2 Voltage Setting

Buck2 reference voltage is 0.6V. This sets the allowable voltage range between 0.6V and 2.991V in 9.376mV steps.

LDO Voltage Setting

The LDO reference voltage is 0.8V. This sets the allowable voltage range between 0.8V and 3.998V in 12.5mV steps.

CMI 105: ACT88325VA105-T

CMI 105 is optimized for the SMI SM2263XT processor. The GPIOs are programmed to allow the microprocessor to program the ACT88325 for the three SMI processor operating modes: Normal Mode, PS3.5, and PS4. It also allows programming for 1.2V or 1.8V NAND I/O. CMI 105 is only configured for a 3.3V input voltage.

The following tables describe the ACT88325VA105 IC settings.

Voltage and Currents

Rail	Active Mode Voltage VSET0 (V)	DVS Voltage VSET1 (V)	DVS Input Trigger	Sleep Mode Voltage (V)	DPSLP Mode Voltage (V)	Current Limit (A)	Fsw (kHz)
Buck1	Load Switch ON	Load Switch ON	n/a	OFF	OFF	5.4	n/a
Buck2	0.9	0.75	GPIO4	OFF	ON	4.6	1125
Buck3	1.8	1.2	GPIO3	OFF	OFF	3.9	2250
LDO1	1.8	1.8	n/a	1.8	1.8	0.465	n/a
LDO2	Load Switch ON	Load Switch ON	n/a	Load Switch ON	Load Switch ON	0.465	n/a
EXT_EN	ON	n/a	n/a	OFF	OFF	n/a	n/a
LS1	ON	n/a	n/a	OFF	OFF	n/a	n/a

Startup and Sequencing

Rail	Sequence Order	Sequencing Input Trigger	StartUp Delay (us)	Soft-Start (us)	Shutdown Delay (us)
LDO2	1	VIN_UVLO	0	275	1500
LDO1	2	LDO2	500	275	2000
Buck2	3	LDO1	500	600	1000
Buck1	4	Buck2	500	600	500
Buck3	5	Buck1	500	600	0
EXT_EN	6	Buck1	2500	n/a	2500
LS1	7	Buck3	500	n/a	2500

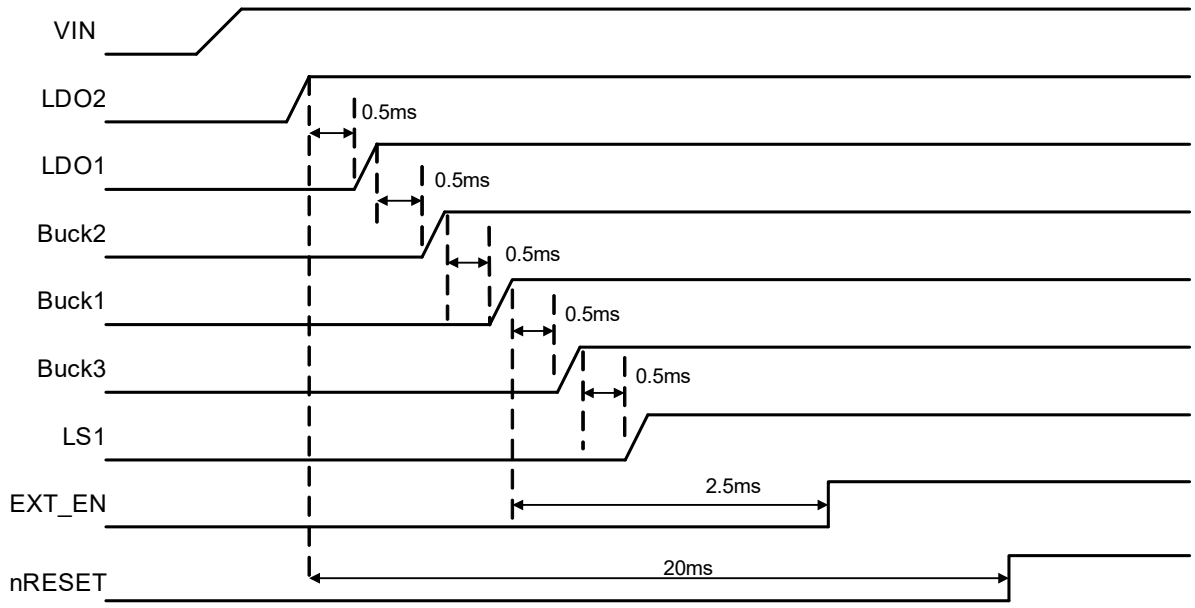
The following table shows how to configure CMI 105 into operate in each of the three SMI processor power modes. The combination of the PWREN and GPIO4 settings determine the specific power state. When in the Normal or PS3.5 power states, the GPIO3 pin sets Buck3 NAND flash voltage. When GPIO3 = L, Buck3 = 1.2V. When GPIO3 = H, Buck3 = 1.8V. The table below does not reflect the Buck3 configurability. It shows the voltages for 1.8V NAND flash.

SMI Processor Power Modes

	Normal Mode GPIO4 = H PWREN = H	**PS 3.5** GPIO4 = L PWREN = H	**PS 4** GPIO4 = L PWREN = L
Buck1	3.3V	3.3V	0V
Buck2	0.9V	0.75V	0.75V
Buck3	1.8V	1.8V	0V
LDO1	1.8V	1.8V	1.8V
LDO2	3.3V	3.3V	3.3V
LS1	ON	OFF	OFF
EXT_EN	H	H	L

Note: Buck2 default voltage for PS 3.5 and PS4 is 0.9V. The uP must reprogram Buck2's VSET1 to 0.75V to properly enable these power modes.

CMI 105 Startup



I²C Address

The ACT88325 7-bit I²C address is 0x25h. Use address 0x4Ah when writing and 0x4Bh when reading.

GPIO1 (pin C7) - nRESET

GPIO1 is configured as an open drain nRESET. nRESET goes open drain 20ms after LDO2 goes into regulation.

GPIO2 (pin C6) – EXT_EN

GPIO2 is configured as an open drain EXT_EN. EXT_EN goes high 2.5ms after Buck1 goes into regulation and is intended to sequence an external supply.

GPIO3 (pin B6) – Buck3 DVS Voltage Select

GPIO3 is configured as an input to select the Buck3 output voltage for different NAND memory voltages. When GPIO3 is H, VSET0 sets Buck3 to 1.8V. When GPIO3 is L, VSET1 sets Buck3 to 1.2V. GPIO3 is intended to be pulled high or low by resistor stuffing option at PCB assembly, but can be changed at any time.

GPIO4 (pin D7) – Buck2 DVS Voltage Select

GPIO4 is configured as an input to select the Buck2 output voltage. When GPIO4 is H, VSET0 regulates Buck2 to 0.9V. When GPIO4 is L, VSET1 regulates the Buck2 voltage. Note that the default VSET1 voltage is 0.9V. After power up, the uP should reprogram VSET1 to 0.75V to enable the SMI SM2263XT processor PS3.5 and PS4 power modes. GPIO4 in combination with PWREN set the SMI processor power modes.

PWREN (pin E1) – DPSLP Mode Select

When PWREN is H, the IC is in Active Mode. When PWREN is L, the IC is in DPSLP Mode. GPIO4 in combination with PWREN set the SMI processor power modes.

SLEEP MODE

I²C default settings are SLEEP_MODE=0, SLEEP_EN=0, and SLEEP=0. Refer to the SLEEP State paragraph for details on how to enter SLEEP Mode.

DPSLP MODE

I²C default settings are DPSLP_MODE=1, DPSLP_EN=0, and DPSLP=0. Refer to the DPSLP State paragraph for details on how to enter DPSLP Mode. Note that the intended method to enter DPSLP Mode with CMI 105 and the SM2263XT processor is to pull the PWREN pin low.

VSYSMON

VSYSMON = 2.7V

Buck1 Voltage Setting

Buck 1 reference voltage is 0.8V. This sets the allowable voltage range between 0.8V and 3.998V in 12.5mV steps.

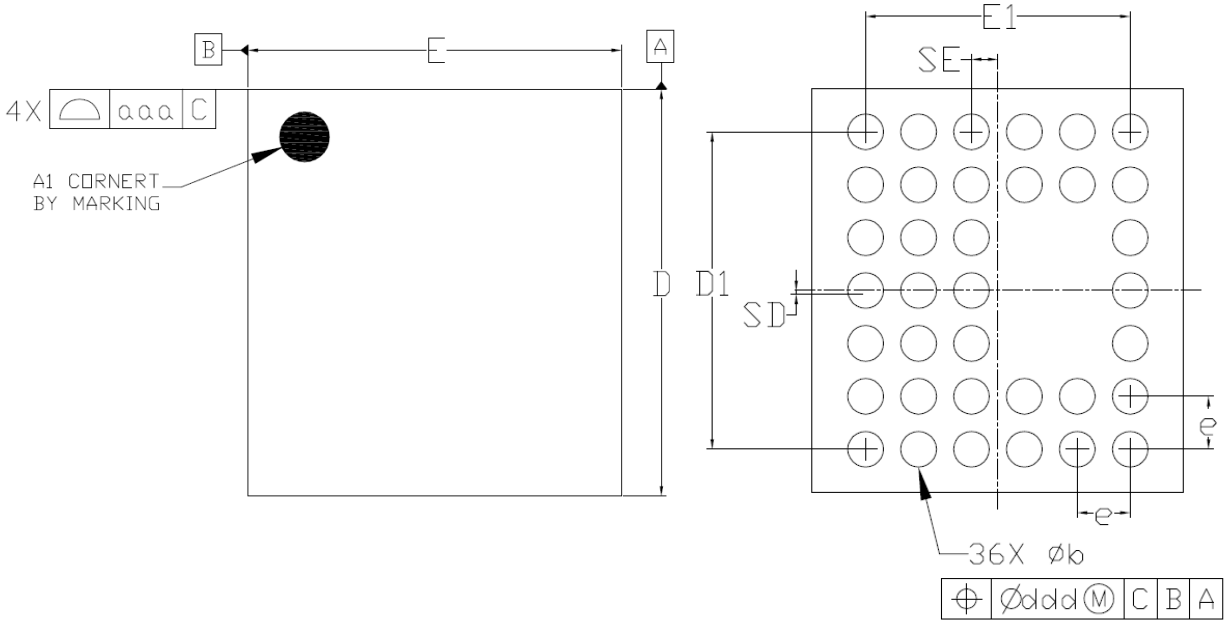
Buck2 Voltage Setting

Buck2 reference voltage is 0.6V. This sets the allowable voltage range between 0.6V and 2.991V in 9.376mV steps.

LDO Voltage Setting

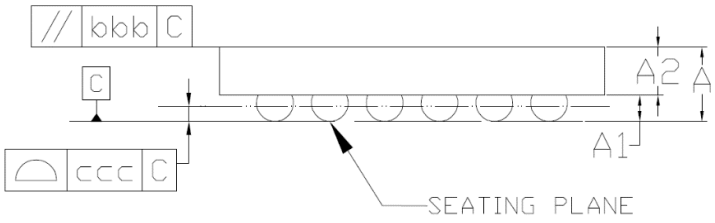
The LDO reference voltage is 0.8V. This sets the allowable voltage range between 0.8V and 3.998V in 12.5mV steps.

PACKAGE OUTLINE AND DIMENSIONS – 36 BALL WLCSP



Top View

Bottom View



Side View

Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	0.490	0.540	0.590
A1	0.165	0.190	0.215
A2	0.325	0.350	0.375
D	3.013	3.028	3.043
E	2.763	2.778	2.793
D1	2.350	2.400	2.450
E1	1.950	2.000	2.050
b	0.230	0.270	0.310
e	0.400 BSC		
SD	0.000 BSC		
SE	0.200 BSC		
Tol. of Form&Position			
aaa	0.10		
bbb	0.10		
ccc	0.05		
ddd	0.05		

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