ULTRA PRECISION DIFFERENTIAL LVPECL 4:1 MUX with 1:2 FANOUT and INTERNAL TERMINATION

Precision Edge® SY58029U

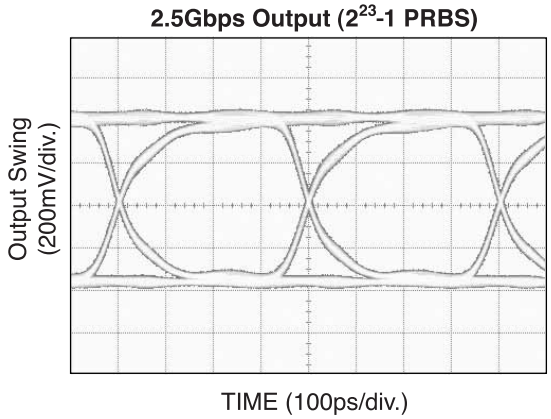
FEATURES

- Selects 1 of 4 differential inputs
- Provides two copies of the selected input
- Guaranteed AC performance over temperature and voltage:
  - DC-to-> 5Gbps data rate throughput
  - < 390ps IN-to-Out t_{pd}
  - < 110ps t_r / t_f times
- Ultra low-jitter design:
  - < 10ps$_{PP}$ total jitter (clock)
  - < 1ps$_{RMS}$ random jitter
  - < 10ps$_{PP}$ deterministic jitter
  - < 0.7ps$_{RMS}$ crosstalk-induced jitter
- Unique patended input design minimizes crosstalk
- Accepts an input signal as low as 100mV
- Unique patented input termination and V_T pin accepts DC- and AC-coupled inputs (CML, LVPECL, LVDS)
- 800mV 100K LVPECL output swing
- Power supply 2.5V ±5% or 3.3V ±10%
- –40°C to +85°C temperature range
- Available in 32-pin (5mm ∞ 5mm) MLF® package

APPLICATIONS

- Redundant clock and/or distribution
- All SONET/SDH clock/data distribution
- Loopback
- All Fibre Channel distribution
- All Gigabit Ethernet clock and/or data distribution

TYPICAL PERFORMANCE



Precision Edge®

DESCRIPTION

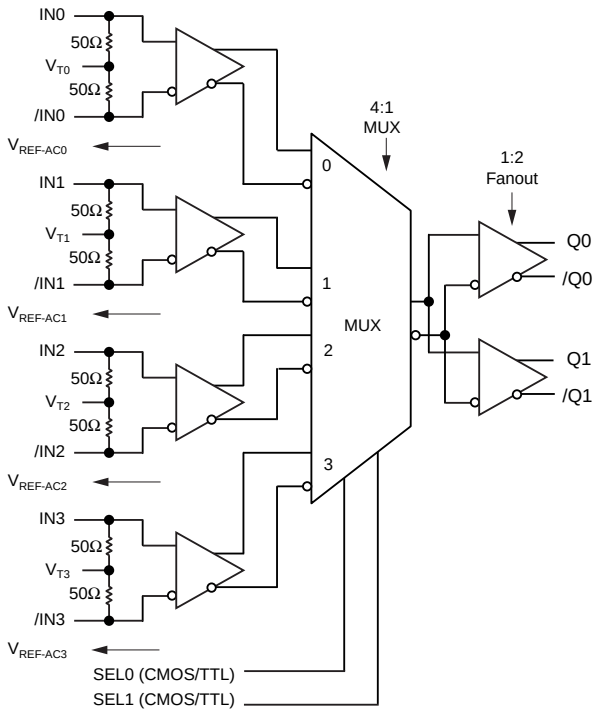
The SY58029U is a 2.5V/3.3V precision, high-speed, 4:1 differential multiplexer with 100k LVPECL (800mV) compatible outputs, capable of handling clocks up to 4GHz and data streams up to 5Gbps. In addition, a 1:2 fanout buffer provides two copies of the selected inputs.

The differential input includes Micrel's unique, 3-pin input termination architecture that allows customers to interface to any differential signal (AC- or DC-coupled) as small as 100mV without any level shifting or termination resistor networks in the signal path. The result is a clean, stub-free, low-jitter interface solution. The outputs are 800mV LVPECL, (100k temperature compensated) with extremely fast rise/fall times guaranteed to be less than 110ps.

The SY58029U operates from a 2.5V ±5% supply or a 3.3V ±10% supply and is guaranteed over the full industrial temperature range of –40°C to +85°C. For applications that require CML outputs, consider the SY58028U. For 400mV LVPECL outputs, consider the SY58030U. The SY58029U is part of Micrel's high-speed, Precision Edge® product line.

All support documentation can be found on Micrel's web site at www.micrel.com.

FUNCTIONAL BLOCK DIAGRAM



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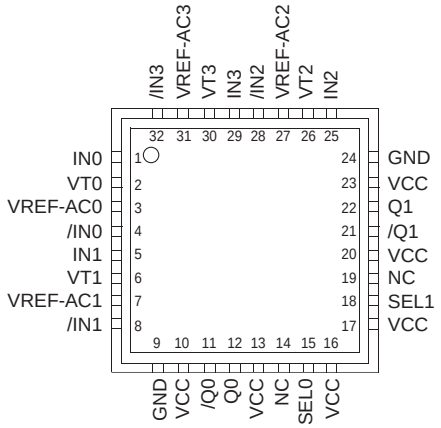
*Micro*LeadFrame and MLF are registered trademarks of Amkor Technology, Inc.

PACKAGE/ORDERING INFORMATION



32-Pin MLF® (MLF-32)

Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY58029UMI	MLF-32	Industrial	SY58029U	Sn-Pb
SY58029UMITR[2]	MLF-32	Industrial	SY58029U	Sn-Pb
SY58029UMG[3]	MLF-32	Industrial	SY58029U with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY58029UMGTR[2, 3]	MLF-32	Industrial	SY58029U with Pb-Free bar-line indicator	Pb-Free NiPdAu

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC electricals only.
2. Tape and Reel.
3. Pb-Free package recommended for new designs.

PIN DESCRIPTION

Pin Number	Pin Name	Pin Function
1, 4 5, 8 25, 28 29, 32	IN0, /IN0 IN1, /IN1 IN2, /IN2 IN3, /IN3	Differential Input: Each pair accepts AC- or DC-coupled signals as small as 100mV. Each pin of a pair internally terminates to a V_T pin through 50ý. Note that these inputs will default to an indeterminate state if left open. If an input is not used, connect one end of the differential pairs to ground through a 1ký resistor, and leave the other end to V_{CC} through a 825ý resistor. Unused V_T and V_{REF-AC} pins may also be left floating. Please refer to the “Input Interface Applications” section for more details.
2, 6, 26, 30	VT0, VT1 VT2, VT3	Input Termination Center-Tap: Each side of the differential input pair terminates to a V_T pin. The V_T pin provides a center-tap to the termination network for maximum interface flexibility. See “Input Interface Applications” section for more details.
15, 18	SEL0, SEL1	This Single-Ended TTL/CMOS compatible input selects the inputs to the multiplexer. Note that this input is internally connected to a 25ký pull-up resistor and will default to a logic HIGH state if left open. Input logic threshold is V_{CC}/2. See “Truth Table” for select control.
14, 19	NC	No Connect.
10, 13, 16 17, 20, 23	VCC	Positive Power Supply: Bypass with 0.1µF™0.01µF low ESR capacitors.
11, 12 21, 22	/Q0, Q0 /Q1, Q1	Differential Outputs: These 100k compatible (internally temperature compensated) LVPECL output pairs are copies of the selected input. Unused output pins may be left floating. See “Output Interface” for terminating guidelines.
9, 24	GND, Exposed Pad	Ground. Ground pin and exposed pad must be connected to the same ground plane.
3, 7, 27, 31	VREF-AC0 VREF-AC1 VREF-AC2 VREF-AC3	Reference Voltage: This reference output is equivalent to V_{CC}–1.4V. It is used for AC-coupled inputs. When interfacing to AC input signals, connect V_{REF-AC} directly to the V_T pin and bypass with 0.01µF low ESR capacitor to V_{CC}. See “Input Interface Applications” section. Maximum sink/source current is 0.5mA.

TRUTH TABLE

SEL1	SEL0	
0	0	IN0 Input Selected
0	1	IN1 Input Selected
1	0	IN2 Input Selected
1	1	IN3 Input Selected

Absolute Maximum Ratings[1]

Power Supply Voltage (V_{CC}) ..... –0.5V to +4.0V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC}
LVPECL Output Current (I_{OUT})
  Continuous 50mA
  Surge 100mA
Termination Current[3]
  Source or sink current on V_T pin ..... ±100mA
Input Current
  Source or sink current on IN, /IN pin ..... ±50mA
Lead Temperature (soldering, 20 sec.) ..... 260°C
Storage Temperature Range (T_S) ..... –65°C to +150°C

Operating Ratings[2]

Power Supply Voltage (V_{CC}) ..... +2.375V to +2.625V
  ..... +3.0V to +3.6V
Ambient Temperature Range (T_A) ..... –40°C to +85°C
Package Thermal Resistance[4]
  MLF® (θ_{JA})
    Still-Air ..... 50°C/W
  MLF® (ψ_{JB})
    Junction-to-Board ..... 20°C/W

DC ELECTRICAL CHARACTERISTICS[5]

T_A= –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply Voltage	V_{CC} = 2.5V	2.375	2.5	2.625	V
		V_{CC} = 3.3V	3.0	3.3	3.6	V
I_{CC}	Power Supply Current	No load, max. V_{CC}		110	140	mA
R_{DIFF_IN}	Differential Input Resistance (IN-to-/IN)		80	100	120	ý
R_{IN}	Input Resistance (IN-to-/IN, /IN-to-V_T)		40	50	60	ý
V_{IH}	Input HIGH Voltage (IN-to-/IN)	**Note 6**	V_{CC}–1.6		V_{CC}	V
V_{IL}	Input LOW Voltage (IN-to-/IN)		0		V_{IH}–0.1	V
V_{IN}	Input Voltage Swing (IN-to-/IN)	See Figure 1a.	0.1		1.7	V
V_{DIFF_IN}	Differential Input Voltage Swing (IN-to-/IN)	See Figure 1b.	0.2			V
$V_{T\ IN}$	Max Input Voltage (IN-to-V_T)				1.28	V
V_{REF-AC}	Reference Voltage		V_{CC}–1.3	V_{CC}–1.2	V_{CC}–1.1	V

Notes:

1. Permanent device damage may occur if ratings in the “Absolute Maximum Ratings” section are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Due to the limited drive capability, use for input of the same package only.
4. Thermal performance assumes exposed pad is soldered (or equivalent) to the device’s most negative potential (GND) on the PCB. ψ_{JB} uses 4-layer θ_{JA} in still air number unless otherwise stated.
5. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
6. V_{IH} (min) not lower than 1.2V.

LVPECL OUTPUT DC ELECTRICAL CHARACTERISTICS[7]

V_{CC} = 2.5V ±5% or 3.3V ±10%; T_A= –40°C to +85°C; R_L = 50ý to V_{CC} –2V across each output pair, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage		V_{CC}–1.145		V_{CC}–0.895	V
V_{OL}	Output LOW Voltage		V_{CC}–1.945		V_{CC}–1.695	V
V_{OUT}	Output Voltage Swing	See Figure 1a.	550	800		mV
V_{DIFF_OUT}	Differential Output Voltage Swing	See Figure 1b.	1100	1600		mV

LVTTL/CMOS DC ELECTRICAL CHARACTERISTICS[7]

V_{CC} = 2.5V ±5% or 3.3V ±10%; T_A= –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage	SEL0, SEL1	2.0			V
V_{IL}	Input LOW Voltage	SEL0, SEL1			0.8	V
I_{IH}	Input HIGH Current				40	µA
I_{IL}	Input LOW Current				–300	µA

Note:

7. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC ELECTRICAL CHARACTERISTICS[8]

V_{CC} = 2.5V ±5% or 3.3V ±10%; R_L = 50ý to V_{CC}–2V; T_A= –40°C to +85°C, V_{IN} ž 100mV, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Operating Frequency	NRZ Data	5			Gbps
		V_{OUT} ž 400mV Clock		4		GHz
t_{pd}	Propagation Delay (Diff) (IN-to-Q)	V_{IN} ž 100mV	215		390	ps
	(SEL-to-Q)		100		500	ps
t_{pd} Tempco	Differential Propagation Delay Temperature Coefficient			115		fs/°C
t_{SKEW}	Output-to-Output	**Note 9**		7	15	ps
	Part-to-Part	**Note 10**			100	ps
t_{JITTER}	Data Random Jitter	**Note 11** 2.5Gbps to 3.2Gbps			1	ps_{RMS}
	Deterministic Jitter	**Note 12** 2.5Gbps to 3.2Gbps			10	ps_{PP}
	Clock Cycle-to-Cycle Jitter	**Note 13**			1	ps_{RMS}
	Total Jitter	**Note 14**			10	ps_{PP}
	Crosstalk Induced Jitter (Adjacent Channel)	**Note 15**			0.7	ps_{RMS}
t_r, t_f	Output Rise/Fall Time	20% to 80%, V_{IN} = 800mV, full output swing	35	60	110	ps

Notes:

8. High frequency AC electricals are guaranteed by design and characterization.
9. Output-to-output skew is measured between outputs under identical input conditions.
10. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs.
11. Random jitter is measured with a K28.7 comma detect character pattern, measured at 2.5Gbps to 3.2Gbps.
12. Deterministic jitter is measured at 2.5Gbps to 3.2Gbps, with both K28.5 and 2^{23}–1 PRBS pattern.
13. Cycle-to-cycle jitter definition: the variation of periods between adjacent cycles, T_n–T_{n-1} where T is the time between rising edges of the output signal.
14. Total jitter definition: with an ideal clock input of frequency - f_{MAX}, no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.
15. Crosstalk is measured at the output while applying two similar clock frequencies that are asynchronous with respect to each other at the inputs.

SINGLE-ENDED AND DIFFERENTIAL SWINGS

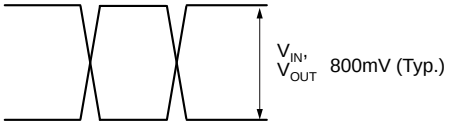


Figure 1a. Single-Ended Voltage Swing

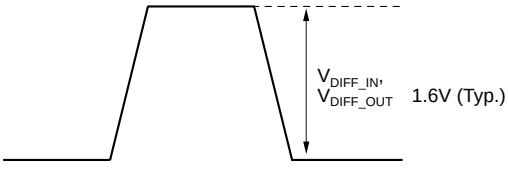


Figure 1b. Differential Voltage Swing

TIMING DIAGRAMS

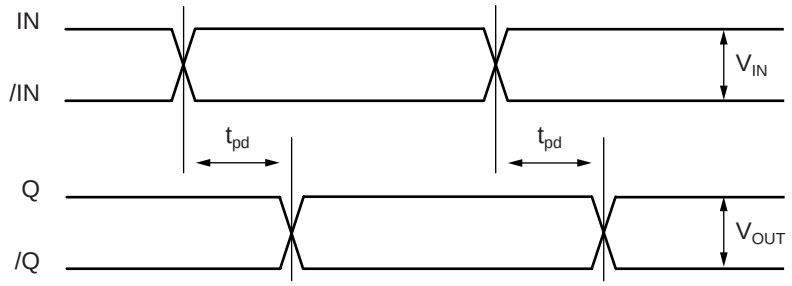


Figure 2a. IN-to-Q Timing Diagram

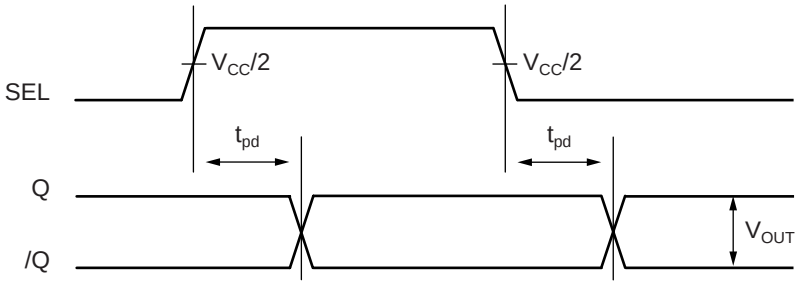


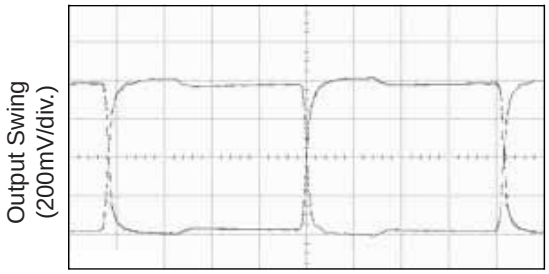
Figure 2b. SEL-to-Q Timing Diagram

SEL0 Q:		SEL1 = LOW;	IN0, /IN1 = LOW;	/IN0, IN1 = HIGH
	or:	SEL1 = HIGH;	IN2, /IN3 = LOW;	/IN2, IN3 = HIGH
SEL1 Q:		SEL0 = LOW;	IN0, /IN2 = LOW;	/IN0, IN2 = HIGH
	or:	SEL0 = HIGH;	IN1, /IN3 = LOW;	/IN1, IN3 = HIGH

FUNCTIONAL CHARACTERISTICS

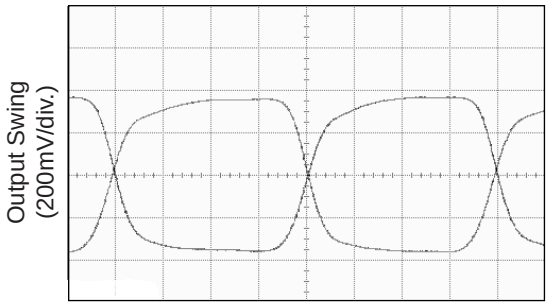
V_{CC} = 2.5V, GND = 0, V_{IN} = 100mV, T_A = 25°C, unless otherwise stated.

200MHz Output



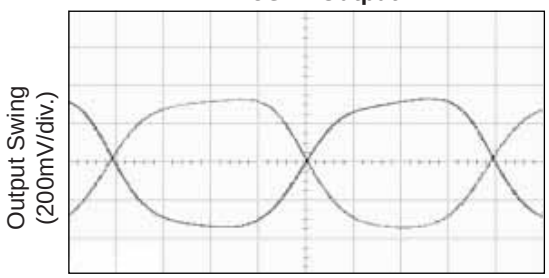
TIME (600ps/div.)

1.25GHz Output



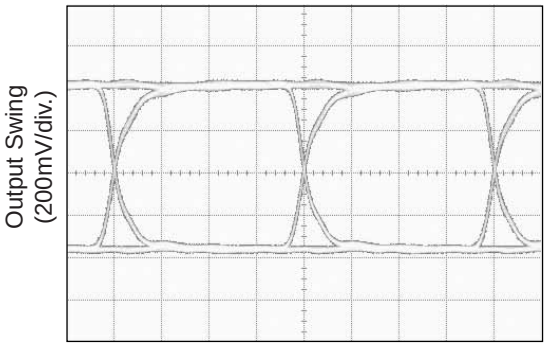
TIME (100ps/div.)

2.5GHz Output



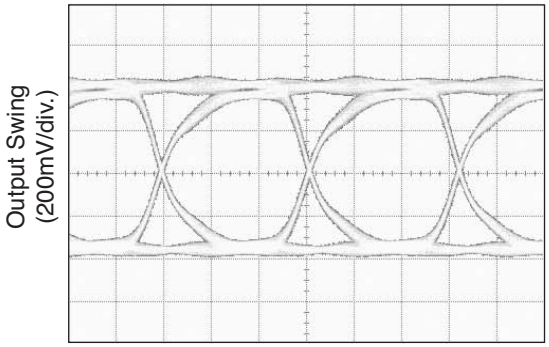
TIME (50ps/div.)

1.25Gbps Output (2^{23}–1 PRBS)



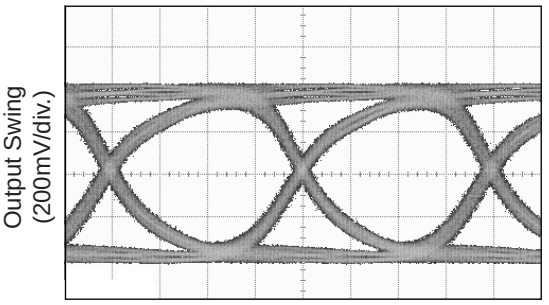
TIME (200ps/div.)

3.2Gbps Output (2^{23} –1 PRBS)



TIME (100ps/div.)

5Gbps Output (2^{23}–1 PRBS)

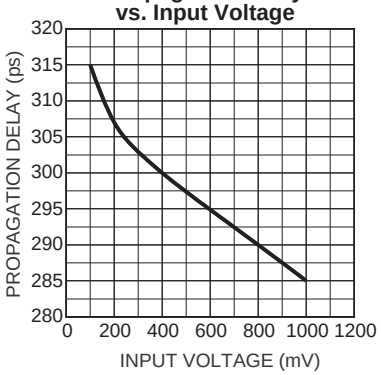


TIME (50ps/div.)

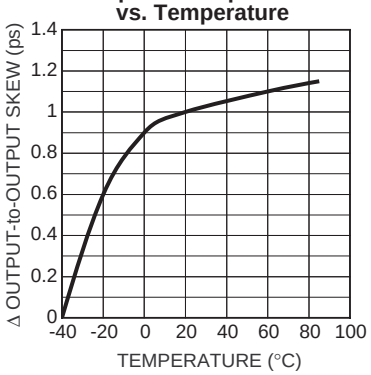
TYPICAL OPERATING CHARACTERISTICS

V_{CC} = 2.5V, GND = 0, V_{IN} = 100mV, T_A = 25°C, unless otherwise stated.

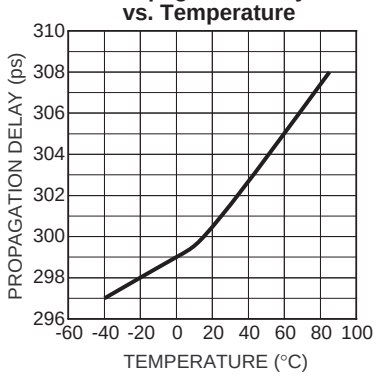
Propagation Delay vs. Input Voltage



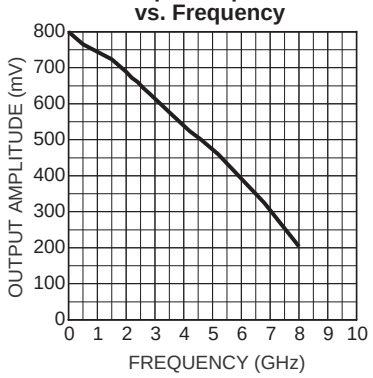
Output-to-Output Skew vs. Temperature



Propagation Delay vs. Temperature



Output Amplitude vs. Frequency



INPUT STAGE

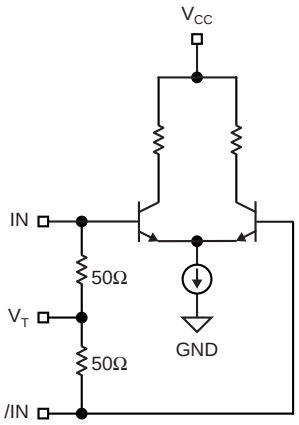


Figure 3. Simplified Differential Input Stage

INPUT INTERFACE APPLICATIONS

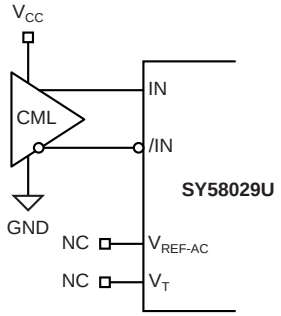


Figure 4a. CML Interface (DC-coupled)
Option: May connect V_T to V_{CC}

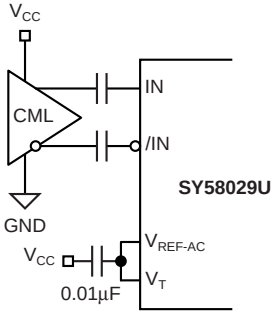


Figure 4b. CML Interface (AC-coupled)

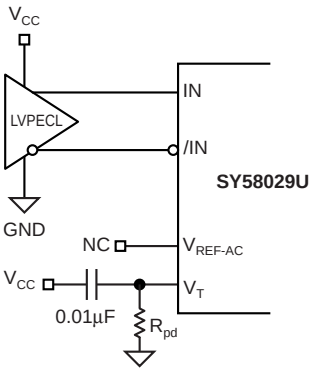


Figure 4c. PECL Interface (DC-coupled)

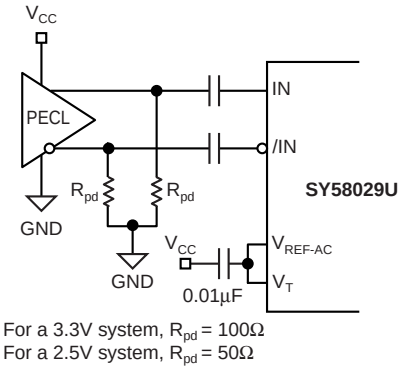


Figure 4d. LVPECL Interface (AC-coupled)

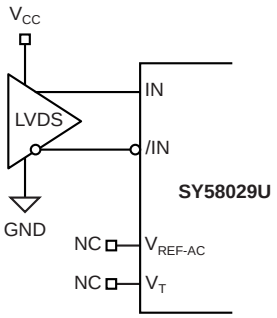


Figure 4e. LVDS Interface

OUTPUT INTERFACE APPLICATIONS

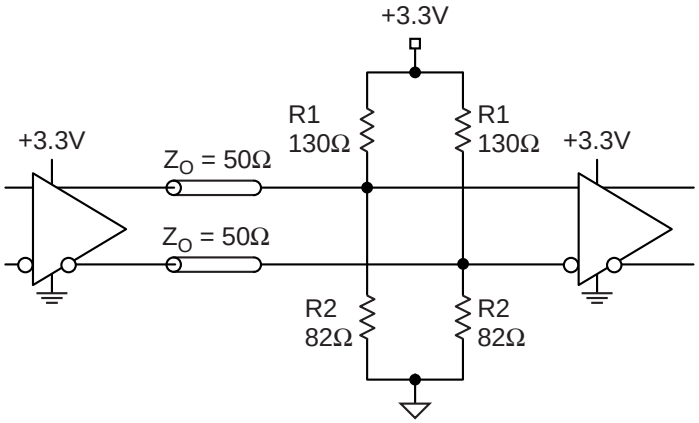


Figure 5a. Parallel Thevenin-Equivalent Termination

Note:

1. For a 2.5V system, R1 = 250ý, R2 = 62.5ý.
   For a 3.3V system, R1 = 130ý, R2 = 82ý.

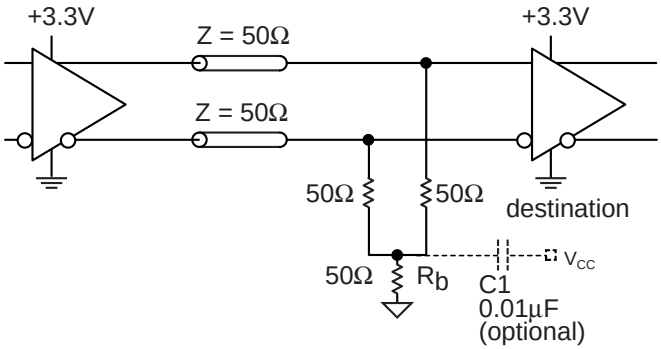


Figure 5b. Parallel Termination (Three-Resistor "Y")

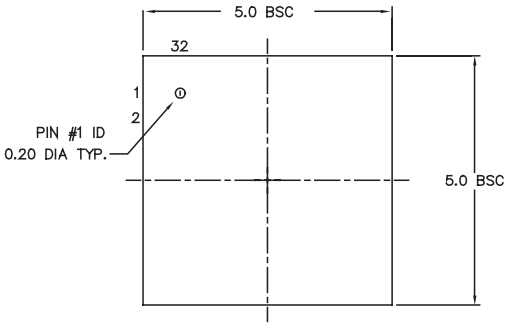
Note:

1. For a 2.5V system, Rb = 19ý.
   For a 3.3V system, Rb = 50ý.

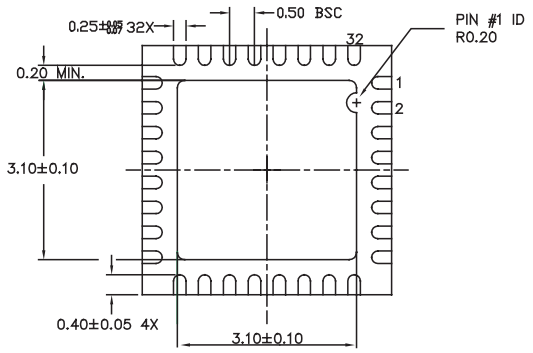
RELATED MICREL PRODUCTS AND SUPPORT DOCUMENTATION

Part Number	Function	Data Sheet Link
SY58028U	Ultra Precision Differential CML 4:1 MUX with 1:2 Fanout and Internal I/O Termination	http://www.micrel.com/product-info/products/sy58028u.shtml
SY58029U	Ultra Precision Differential LVPECL 4:1 MUX with 1:2 Fanout and Internal Termination	http://www.micrel.com/product-info/products/sy58029u.shtml
SY58030U	Ultra Precision, 400mV Differential LVPECL 4:1 MUX with 1:2 Fanout and Internal Termination	http://www.micrel.com/product-info/products/sy58030u.shtml
	MLF® Application Note	www.amkor.com/products/notes_papers/MLF_AppNote_0902.pdf
HBW Solutions	New Products and Applications	www.micrel.com/product-info/products/solutions.shtml

32-PIN *Micro*LeadFrame® (MLF-32)

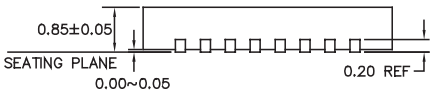


TOP VIEW

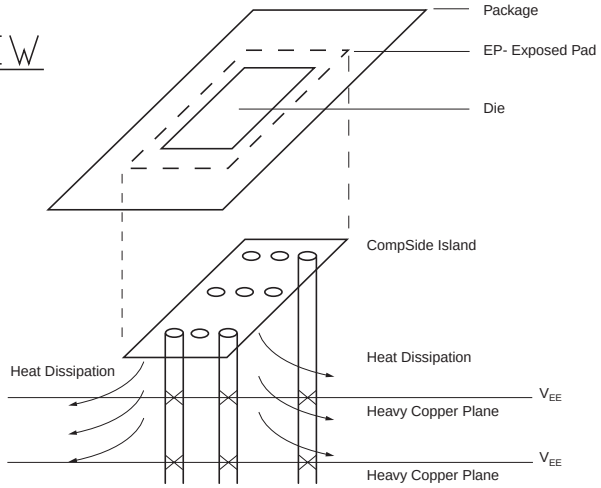


BOTTOM VIEW

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.



SIDE VIEW



PCB Thermal Consideration for 32-Pin MLF® Package
(Always solder, or equivalent, the exposed pad to the PCB)

Package Notes:

1. Package meets Level 2 qualification.
2. All parts are dry-packaged before shipment.
3. Exposed pads must be soldered to a ground for proper thermal management.

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