

# 74AHC374; 74AHCT374

Octal D-type flip-flop; positive edge-trigger; 3-state

Rev. 03 — 12 June 2008

Product data sheet

## 1. General description

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The 74AHC374; 74AHCT374 is a high-speed Si-gate CMOS device and is pin compatible with Low-power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard No. 7-A.

The 74AHC374; 74AHCT374 comprises eight D-type flip-flops featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A clock input (CP) and an output enable input ( $\overline{OE}$ ) are common to all flip-flops.

The eight flip-flops will store the state of their individual D inputs that meet the set-up and hold times requirements for the LOW-to-HIGH CP transition.

When  $\overline{OE}$  is LOW the content of the eight flip-flops is available at the outputs. When  $\overline{OE}$  is HIGH, the outputs go to the high-impedance OFF-state. Operation of the  $\overline{OE}$  input does not affect the state of the flip-flops.

## 2. Features

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- Balanced propagation delays
- All inputs have Schmitt-trigger actions
- Inputs accept voltages higher than  $V_{CC}$
- Common 3-state output enable input
- Input levels:
  - ◆ For 74AHC374: CMOS level
  - ◆ For 74AHCT374: TTL level
- ESD protection:
  - ◆ HBM EIA/JESD22-A114E exceeds 2000 V
  - ◆ MM EIA/JESD22-A115-A exceeds 200 V
  - ◆ CDM EIA/JESD22-C101C exceeds 1000 V
- Multiple package options
- Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$  and from  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$

### 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
<b>74AHC374</b>				
74AHC374D	−40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74AHC374PW	−40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
<b>74AHCT374</b>				
74AHCT374D	−40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74AHCT374PW	−40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1

### 4. Functional diagram



Fig 1. Functional diagram

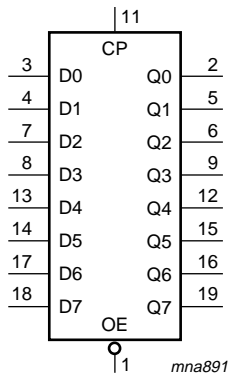


Fig 2. Logic symbol



Fig 3. IEC logic symbol



Fig 4. Logic diagram

## 5. Pinning information

### 5.1 Pinning

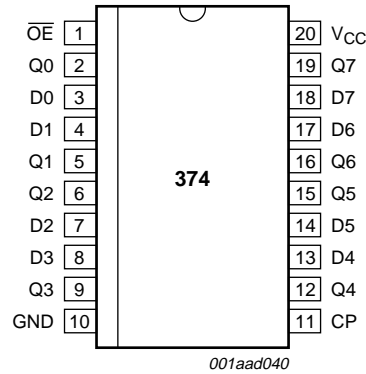


Fig 5. Pin configuration SO20 and TSSOP20

### 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
OE	1	3-state output enable input (active LOW)
Q0	2	3-state flip-flop output
D0	3	data input
D1	4	data input
Q1	5	3-state flip-flop output
Q2	6	3-state flip-flop output
D2	7	data input
D3	8	data input
Q3	9	3-state flip-flop output
GND	10	ground (0 V)
CP	11	clock input (LOW-to-HIGH, edge triggered)
Q4	12	3-state flip-flop output
D4	13	data input
D5	14	data input
Q5	15	3-state flip-flop output
Q6	16	3-state flip-flop output
D6	17	data input
D7	18	data input
Q7	19	3-state flip-flop output
VCC	20	supply voltage

## 6. Functional description

Table 3. Function table<sup>[1]</sup>

Operating mode	Control		Input	Internal flip-flop	Output
	$\overline{OE}$	CP	Dn		Q0 to Q7
Load and read register	L	↑	l	L	L
	L	↑	h	H	H
Load register and disable outputs	H	↑	l	L	Z
	H	↑	h	H	Z

- [1] H = HIGH voltage level;  
 h = HIGH voltage level one setup time prior to the LOW-to-HIGH CP transition;  
 L = LOW voltage level;  
 l = LOW voltage level one setup time prior to the LOW-to-HIGH CP transition;  
 X = don't care;  
 ↑ = LOW-to-HIGH CP transition;  
 Z = high-impedance OFF-state.

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7.0	V
$V_I$	input voltage		-0.5	+7.0	V
$I_{IK}$	input clamping current	$V_I < -0.5$ V	<sup>[1]</sup> -20	-	mA
$I_{OK}$	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	<sup>[1]</sup> -20	+20	mA
$I_O$	output current	$V_O = -0.5$ V to $(V_{CC} + 0.5)$ V	-25	+25	mA
$I_{CC}$	supply current		-	+75	mA
$I_{GND}$	ground current		-75	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +125 °C	<sup>[2]</sup> -	500	mW

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 [2] For SO20 packages: above 70 °C the value of  $P_{tot}$  derates linearly at 8 mW/K.  
 For TSSOP20 packages: above 60 °C the value of  $P_{tot}$  derates linearly at 5.5 mW/K.

## 8. Recommended operating conditions

Table 5. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>74AHC374</b>						
$V_{CC}$	supply voltage		2.0	5.0	5.5	V
$V_I$	input voltage		0	-	5.5	V
$V_O$	output voltage		0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	-	-	100	ns/V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	-	20	ns/V
<b>74AHCT374</b>						
$V_{CC}$	supply voltage		4.5	5.0	5.5	V
$V_I$	input voltage		0	-	5.5	V
$V_O$	output voltage		0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	-	20	ns/V

## 9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74AHC374</b>										
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 2.0\text{ V}$	1.5	-	-	1.5	-	1.5	-	V
		$V_{CC} = 3.0\text{ V}$	2.1	-	-	2.1	-	2.1	-	V
		$V_{CC} = 5.5\text{ V}$	3.85	-	-	3.85	-	3.85	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 2.0\text{ V}$	-	-	0.5	-	0.5	-	0.5	V
		$V_{CC} = 3.0\text{ V}$	-	-	0.9	-	0.9	-	0.9	V
		$V_{CC} = 5.5\text{ V}$	-	-	1.65	-	1.65	-	1.65	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$								
		$I_O = -50\ \mu\text{A}; V_{CC} = 2.0\text{ V}$	1.9	2.0	-	1.9	-	1.9	-	V
		$I_O = -50\ \mu\text{A}; V_{CC} = 3.0\text{ V}$	2.9	3.0	-	2.9	-	2.9	-	V
		$I_O = -50\ \mu\text{A}; V_{CC} = 4.5\text{ V}$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -4.0\text{ mA}; V_{CC} = 3.0\text{ V}$	2.58	-	-	2.48	-	2.40	-	V
	$I_O = -8.0\text{ mA}; V_{CC} = 4.5\text{ V}$	3.94	-	-	3.80	-	3.70	-	V	
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$								
		$I_O = 50\ \mu\text{A}; V_{CC} = 2.0\text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 50\ \mu\text{A}; V_{CC} = 3.0\text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 50\ \mu\text{A}; V_{CC} = 4.5\text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 4.0\text{ mA}; V_{CC} = 3.0\text{ V}$	-	-	0.36	-	0.44	-	0.55	V
	$I_O = 8.0\text{ mA}; V_{CC} = 4.5\text{ V}$	-	-	0.36	-	0.44	-	0.55	V	

**Table 6. Static characteristics ...continued**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
$I_I$	input leakage current	$V_I = 5.5 \text{ V}$ or GND; $V_{CC} = 0 \text{ V}$ to 5.5 V	-	-	0.1	-	1.0	-	2.0	$\mu\text{A}$
$I_{OZ}$	OFF-state output current	$V_I = V_{IH}$ or $V_{IL}$ ; $V_O = V_{CC}$ or GND; $V_{CC} = 5.5 \text{ V}$	-	-	$\pm 0.25$	-	$\pm 2.5$	-	$\pm 10.0$	$\mu\text{A}$
$I_{CC}$	supply current	$V_I = V_{CC}$ or GND; $I_O = 0 \text{ A}$ ; $V_{CC} = 5.5 \text{ V}$	-	-	4.0	-	40	-	80	$\mu\text{A}$
$C_I$	input capacitance	$V_I = V_{CC}$ or GND	-	3	10	-	10	-	10	pF
$C_O$	output capacitance		-	4	-	-	-	-	-	pF
<b>74AHCT374</b>										
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 4.5 \text{ V}$ to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 4.5 \text{ V}$ to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5 \text{ V}$ $I_O = -50 \mu\text{A}$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -8.0 \text{ mA}$	3.94	-	-	3.80	-	3.70	-	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5 \text{ V}$ $I_O = 50 \mu\text{A}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 8.0 \text{ mA}$	-	-	0.36	-	0.44	-	0.55	V
$I_I$	input leakage current	$V_I = 5.5 \text{ V}$ or GND; $V_{CC} = 0 \text{ V}$ to 5.5 V	-	-	0.1	-	1.0	-	2.0	$\mu\text{A}$
$I_{OZ}$	OFF-state output current	$V_I = V_{IH}$ or $V_{IL}$ ; $V_O = V_{CC}$ or GND per input pin; other inputs at $V_{CC}$ or GND; $I_O = 0 \text{ A}$ ; $V_{CC} = 5.5 \text{ V}$	-	-	$\pm 0.25$	-	$\pm 2.5$	-	$\pm 10.0$	$\mu\text{A}$
$I_{CC}$	supply current	$V_I = V_{CC}$ or GND; $I_O = 0 \text{ A}$ ; $V_{CC} = 5.5 \text{ V}$	-	-	4.0	-	40	-	80	$\mu\text{A}$
$\Delta I_{CC}$	additional supply current	per input pin; $V_I = V_{CC} - 2.1 \text{ V}$ ; other pins at $V_{CC}$ or GND; $I_O = 0 \text{ A}$ ; $V_{CC} = 4.5 \text{ V}$ to 5.5 V	-	-	1.35	-	1.5	-	1.5	mA
$C_I$	input capacitance	$V_I = V_{CC}$ or GND	-	3	10	-	10	-	10	pF
$C_O$	output capacitance		-	4	-	-	-	-	-	pF

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 9](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	Min	Max	
<b>74AHC374</b>										
$t_{pd}$	propagation delay	CP to Qn; see <a href="#">Figure 6</a> and <a href="#">Figure 8</a> <sup>[2]</sup>								
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$								
		$C_L = 15\text{ pF}$	-	6.4	12.7	1.0	15.0	1.0	16.0	ns
		$C_L = 50\text{ pF}$	-	8.4	16.2	1.0	18.5	1.0	20.5	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$								
$t_{en}$	enable time	$\overline{OE}$ to Qn; see <a href="#">Figure 7</a> <sup>[3]</sup>								
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$								
		$C_L = 15\text{ pF}$	-	5.5	11.0	1.0	13.0	1.0	14.0	ns
		$C_L = 50\text{ pF}$	-	7.3	14.5	1.0	16.5	1.0	18.0	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$								
$t_{dis}$	disable time	$\overline{OE}$ to Qn; see <a href="#">Figure 7</a> <sup>[4]</sup>								
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$								
		$C_L = 15\text{ pF}$	-	5.6	10.5	1.0	12.5	1.0	13.0	ns
		$C_L = 50\text{ pF}$	-	9.4	14.0	1.0	16.0	1.0	17.5	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$								
$f_{max}$	maximum frequency	see <a href="#">Figure 6</a>								
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$								
		$C_L = 15\text{ pF}$	80	130	-	70	-	70	-	MHz
		$C_L = 50\text{ pF}$	55	85	-	50	-	50	-	MHz
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$								
$t_W$	pulse width	CP HIGH or LOW; see <a href="#">Figure 6</a>								
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	5.0	-	-	5.5	-	5.5	-	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	5.0	-	-	5.0	-	5.0	-	ns
$t_{su}$	set-up time	Dn to CP; see <a href="#">Figure 8</a>								
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	4.5	-	-	4.0	-	4.0	-	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	3.0	-	-	3.0	-	3.0	-	ns



**Table 7. Dynamic characteristics ...continued**Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 9](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	Min	Max	
$t_h$	hold time	Dn to CP; see <a href="#">Figure 8</a>								
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	2.0	-	-	2.0	-	2.0	-	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	2.0	-	-	2.0	-	2.0	-	ns
$C_{PD}$	power dissipation capacitance	$f_i = 1\text{ MHz}; V_I = \text{GND to }V_{CC}$ <sup>[5]</sup>	-	10	-	-	-	-	-	pF
<b>74AHCT374; <math>V_{CC} = 4.5\text{ V to }5.5\text{ V}</math></b>										
$t_{pd}$	propagation delay	CP to Qn; see <a href="#">Figure 6</a> and <a href="#">Figure 8</a> <sup>[2]</sup>								
		$C_L = 15\text{ pF}$	-	4.3	9.4	1.0	10.5	1.0	12.0	ns
		$C_L = 50\text{ pF}$	-	5.6	10.4	1.0	11.5	1.0	13.0	ns
$t_{en}$	enable time	$\overline{\text{OE}}$ to Qn; see <a href="#">Figure 7</a> <sup>[3]</sup>								
		$C_L = 15\text{ pF}$	-	3.5	10.2	1.0	11.5	1.0	13.0	ns
		$C_L = 50\text{ pF}$	-	4.8	11.2	1.0	12.5	1.0	14.0	ns
$t_{dis}$	disable time	$\overline{\text{OE}}$ to Qn; see <a href="#">Figure 7</a> <sup>[4]</sup>								
		$C_L = 15\text{ pF}$	-	3.6	10.2	1.0	11.0	1.0	13.0	ns
		$C_L = 50\text{ pF}$	-	5.7	11.2	1.0	12.0	1.0	14.0	ns
$f_{max}$	maximum frequency	see <a href="#">Figure 6</a>								
		$C_L = 15\text{ pF}$	90	140	-	80	-	80	-	MHz
		$C_L = 50\text{ pF}$	85	130	-	75	-	75	-	MHz
$t_W$	pulse width	CP HIGH or LOW; see <a href="#">Figure 6</a>	6.5	-	-	6.5	-	6.5	-	ns
$t_{su}$	set-up time	Dn to CP; see <a href="#">Figure 8</a>	2.5	-	-	2.5	-	2.5	-	ns
$t_h$	hold time	Dn to CP; see <a href="#">Figure 8</a>	2.5	-	-	2.5	-	2.5	-	ns
$C_{PD}$	power dissipation capacitance	$f_i = 1\text{ MHz}; V_I = \text{GND to }V_{CC}$ <sup>[5]</sup>	-	12	-	-	-	-	-	pF

[1] Typical values are measured at nominal supply voltage ( $V_{CC} = 3.3\text{ V}$  and  $V_{CC} = 5.0\text{ V}$ ).

[2]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .

[3]  $t_{en}$  is the same as  $t_{PZH}$  and  $t_{PZL}$ .

[4]  $t_{dis}$  is the same as  $t_{PHZ}$  and  $t_{PLZ}$ .

[5]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

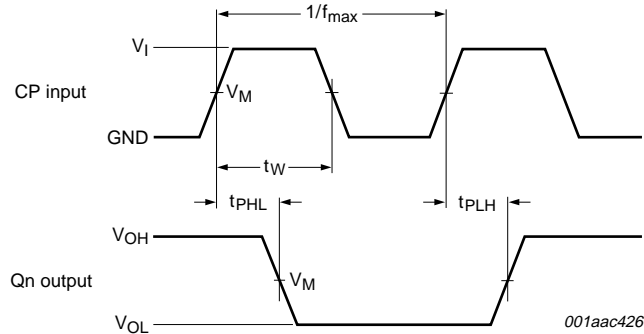
$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in V;

$N$  = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

## 10.1 Waveforms



Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig 6. Clock pulse width, maximum frequency and input to output propagation delays**



Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig 7. Enable and disable times**



Measurement points are given in [Table 8](#).

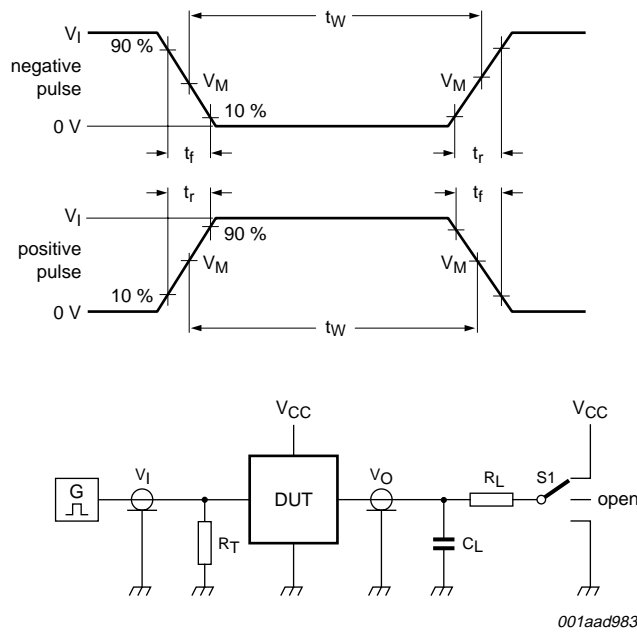
The shaded areas indicate when the input is permitted to change for predictable output performance.

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig 8. Data set-up and hold times**

**Table 8. Measurement points**

Type	Input	Output		
	$V_M$	$V_M$	$V_X$	$V_Y$
74AHC374	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$
74AHCT374	1.5 V	$0.5 \times V_{CC}$	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$



Test data is given in [Table 9](#).

Definitions test circuit:

$R_T$  = termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$C_L$  = load capacitance including jig and probe capacitance.

$R_L$  = load resistance.

S1 = test selection switch.

**Fig 9. Test circuitry for measuring switching times**

**Table 9. Test data**

Type	Input		Load		S1 position		
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHL}, t_{PLH}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$
74AHC374	$V_{CC}$	$\leq 3.0$ ns	15 pF, 50 pF	1 k $\Omega$	open	GND	$V_{CC}$
74AHCT374	3.0 V	$\leq 3.0$ ns	15 pF, 50 pF	1 k $\Omega$	open	GND	$V_{CC}$

## 11. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



Fig 10. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



Fig 11. Package outline SOT360-1 (TSSOP20)

## 12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
LSTTL	Low-power Schottky Transistor-Transistor Logic
MM	Machine Model

## 13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT374_3	20080612	Product data sheet	-	74AHC_AHCT374_2
Modifications:	<ul style="list-style-type: none"> <li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>• Legal texts have been adapted to the new company name where appropriate.</li> <li>• <a href="#">Table 6</a>: the conditions for input leakage current have been changed.</li> </ul>			
74AHC_AHCT374_2	19990928	Product specification	-	74AHC_AHCT374_1
74AHC_AHCT374_1	19981211	Product specification	-	-

## 14. Legal information

### 14.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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**Телефон:** +7 812 627 14 35

**Электронная почта:** [sales@st-electron.ru](mailto:sales@st-electron.ru)

**Адрес:** 198099, Санкт-Петербург,  
Промышленная ул, дом № 19, литера Н,  
помещение 100-Н Офис 331