2N6667, 2N6668

Darlington Silicon Power Transistors

Designed for general−purpose amplifier and low speed switching applications.

- High DC Current Gain −
  h_{FE} = 3500 (Typ) @ I_C = 4.0 Adc
- Collector−Emitter Sustaining Voltage − @ 200 mAdc
  $V_{CEO(sus)}$ = 60 Vdc (Min) − 2N6667
  = 80 Vdc (Min) − 2N6668
- Low Collector−Emitter Saturation Voltage −
  $V_{CE(sat)}$ = 2.0 Vdc (Max)@ I_C = 5.0 Adc
- Monolithic Construction with Built−In Base−Emitter Shunt Resistors
- TO−220AB Compact Package
- Complementary to 2N6387, 2N6388
- Pb−Free Packages are Available*

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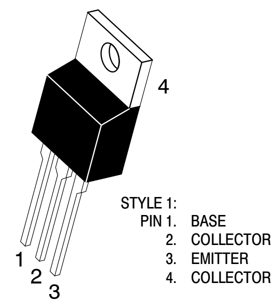
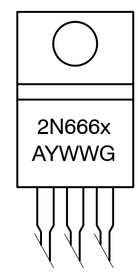
PNP SILICON DARLINGTON POWER TRANSISTORS 10 A, 60−80 V, 65 W



CASE 221A−09 TO−220AB

MARKING DIAGRAM



x = 7 or 8
A = Assembly Location
Y = Year
WW = Work Week
G = Pb−Free Package

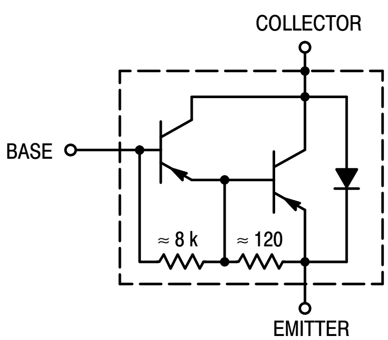


Figure 1. Darlington Schematic

ORDERING INFORMATION

Device	Package	Shipping
2N6667	TO−220AB	50 Units/Rail
2N6667G	TO−220AB (Pb−Free)	50 Units/Rail
2N6668	TO−220AB	50 Units/Rail
2N6668G	TO−220AB (Pb−Free)	50 Units/Rail

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MAXIMUM RATINGS (Note 1)

Rating	Symbol	2N6667	2N6668	Unit
Collector−Emitter Voltage	V_{CEO}	60	80	Vdc
Collector−Base Voltage	V_{CB}	60	80	Vdc
Emitter−Base Voltage	V_{EB}	5.0		Vdc
Collector Current − Continuous − Peak	I_C	10 15		Adc
Base Current	I_B	250		mAdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	65 0.52		W W/°C
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	2.0 0.016		W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150		°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.92	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

ELECTRICAL CHARACTERISTICS (Note 1) (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (Note 2) (I_C = 200 mAdc, I_B = 0)	2N6667 2N6668	$V_{CEO(sus)}$	60 80	− −	Vdc
Collector Cutoff Current (V_{CE} = 60 Vdc, I_B = 0) (V_{CE} = 80 Vdc, I_B = 0)	2N6667 2N6668	I_{CEO}	− −	1.0 1.0	mAdc
Collector Cutoff Current (V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = 60 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C) (V_{CE} = 80 Vdc, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)	 2N6667 2N6668 2N6667 2N6668	I_{CEX}	 − − − −	 300 300 3.0 3.0	 μAdc mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	−	5.0	mAdc
ON CHARACTERISTICS (Note 1)					
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 3.0 Vdc) (I_C = 10 Adc, V_{CE} = 3.0 Vdc)		h_{FE}	1000 100	20000 −	−
Collector−Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 0.01 Adc) (I_C = 10 Adc, I_B = 0.1 Adc)		$V_{CE(sat)}$	− −	2.0 3.0	Vdc
Base−Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 0.01 Adc) (I_C = 10 Adc, I_B = 0.1 Adc)		$V_{BE(sat)}$	− −	2.8 4.5	Vdc
DYNAMIC CHARACTERISTICS					
Current Gain − Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc, f_{test} = 1.0 MHz)		$\lvert h_{fe} \rvert$	20	−	−
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)		C_{ob}	−	200	pF
Small−Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 5.0 Vdc, f = 1.0 kHz)		h_{fe}	1000	−	−

1. Indicates JEDEC Registered Data.
2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

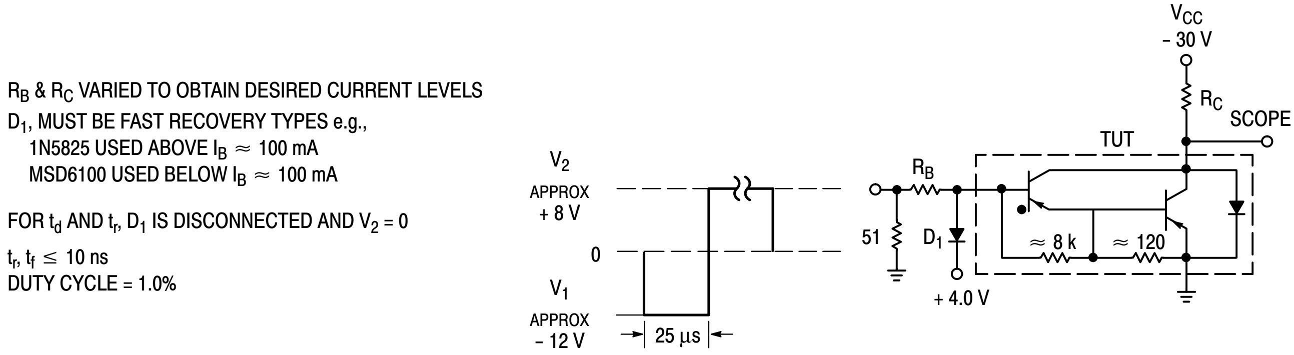


Figure 2. Switching Times Test Circuit

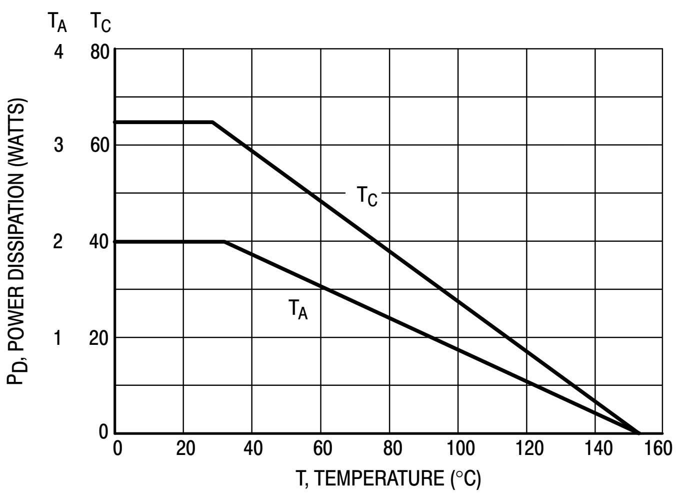


Figure 3. Power Derating

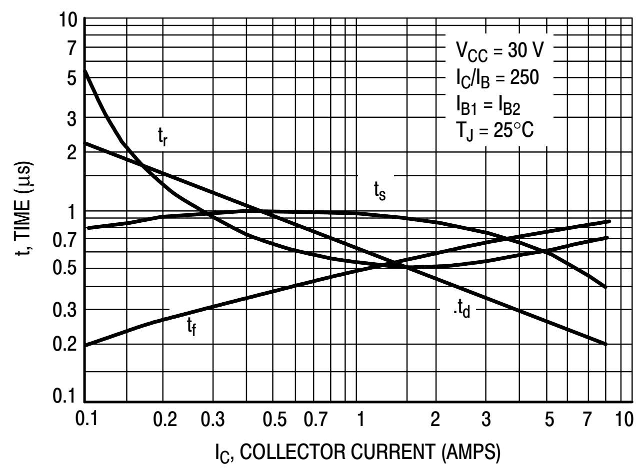


Figure 4. Typical Switching Times

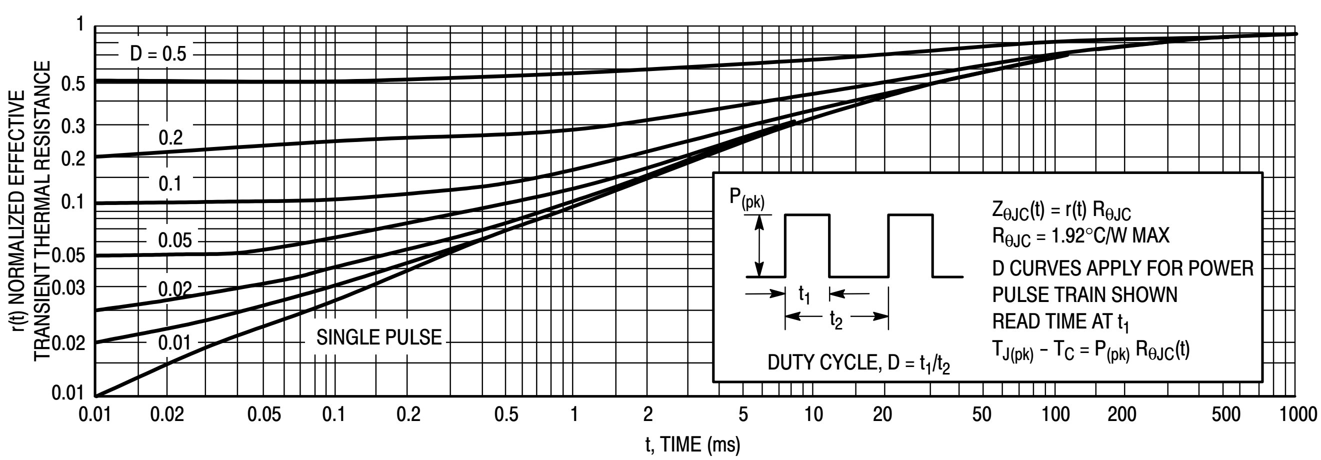


Figure 5. Thermal Response

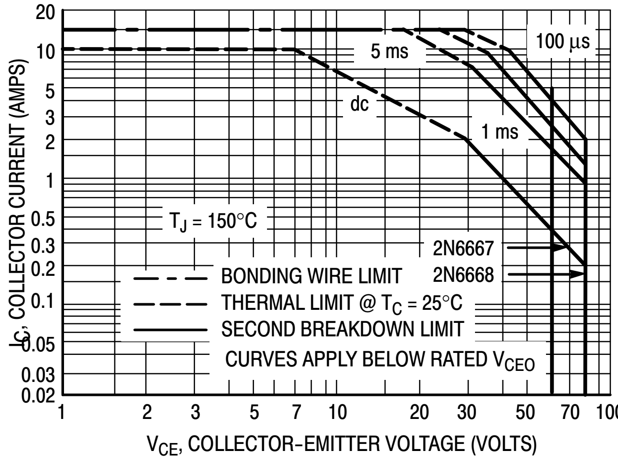


Figure 6. Maximum Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

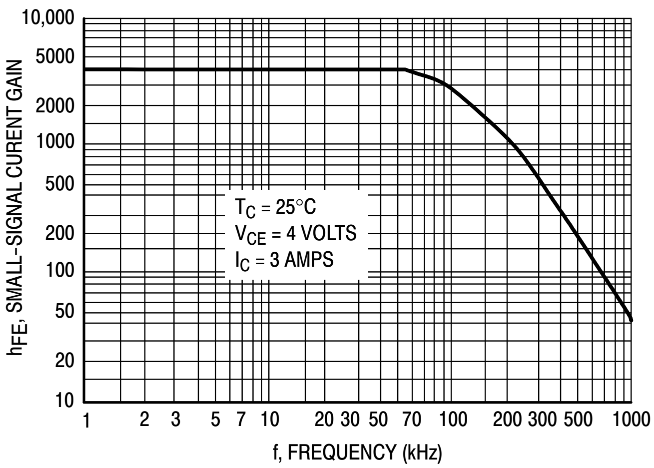


Figure 7. Typical Small−Signal Current Gain

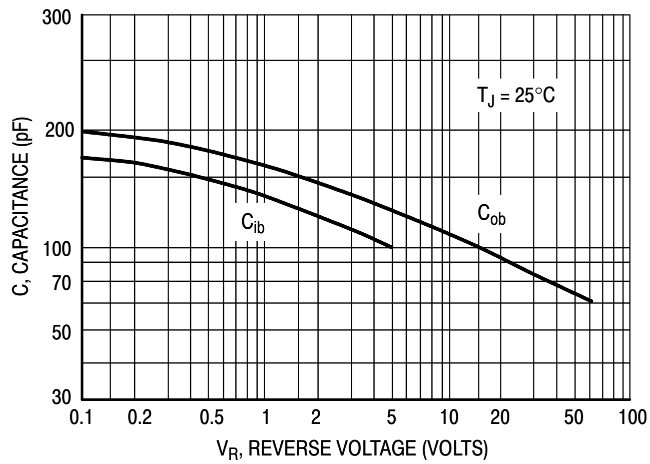


Figure 8. Typical Capacitance

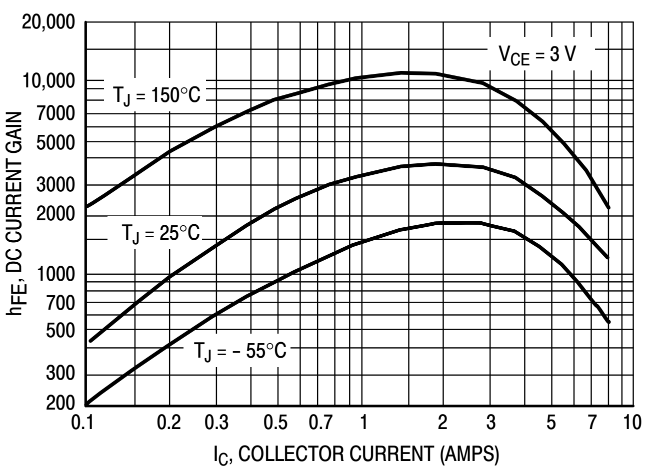


Figure 9. Typical DC Current Gain

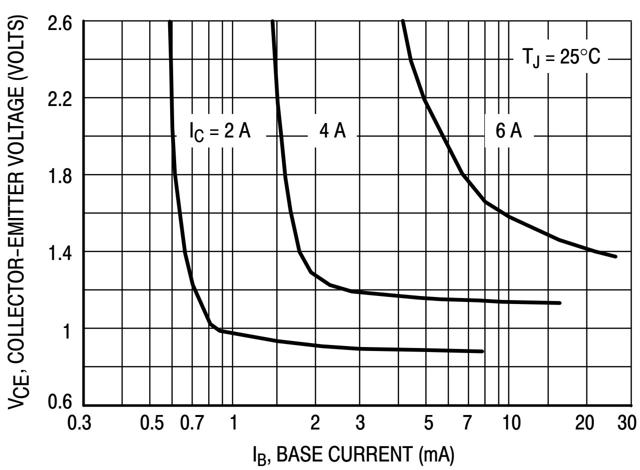


Figure 10. Typical Collector Saturation Region

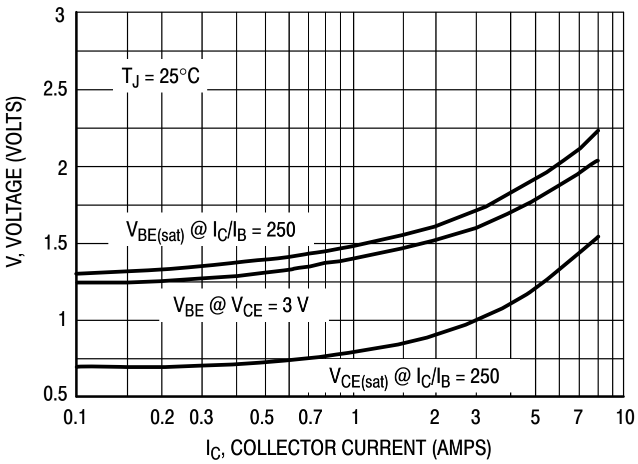


Figure 11. Typical "On" Voltages

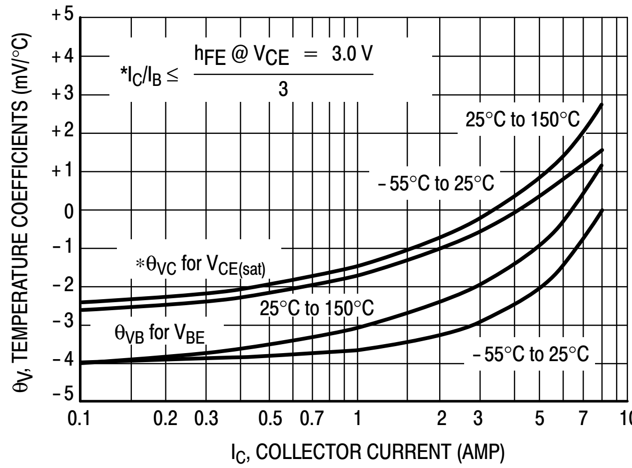


Figure 12. Typical Temperature Coefficients

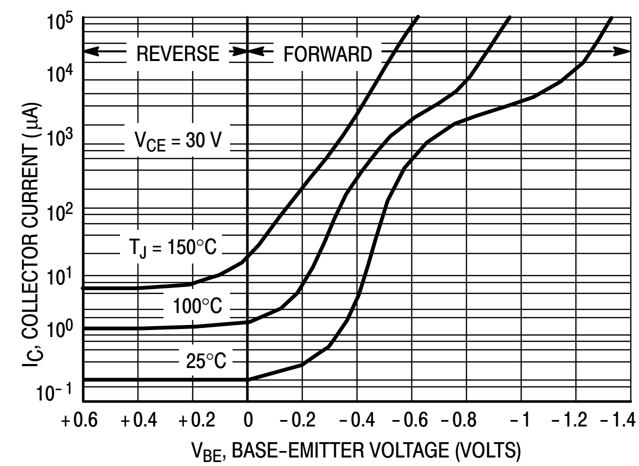
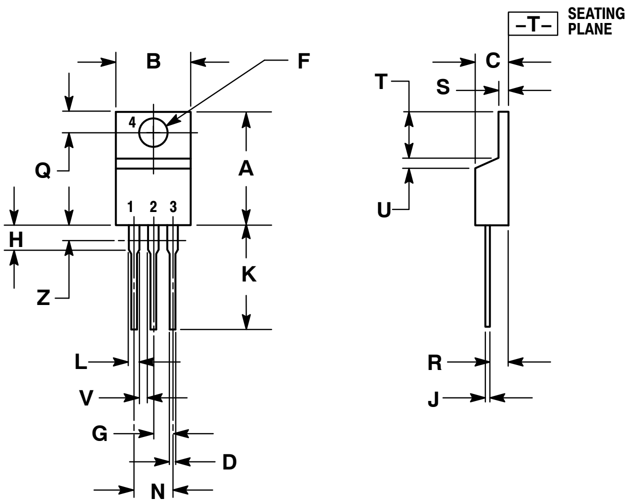


Figure 13. Typical Collector Cut−Off Region

PACKAGE DIMENSIONS

TO−220
CASE 221A−09
ISSUE AG



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.036	0.64	0.91
F	0.142	0.161	3.61	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.161	2.80	4.10
J	0.014	0.025	0.36	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

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