VCU1287 Characterization Board

User Guide

UG1121 (v1.0) December 11, 2015

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
12/11/2015	1.0	Initial Xilinx release.

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Introduction

Overview

This user guide describes the components, features, and operation of the VCU1287 UltraScale® FPGA GTH and GTY transceivers characterization board. The VCU1287 board provides the hardware environment for characterizing and evaluating the GTH and GTY transceivers available on the UltraScale XCVU095-FFVB2104E FPGA. The VCU1287 board schematic, bill-of-material (BOM), layout files, and reference designs are available online at the VCU1287 Characterization Kit website.

FPGA Compatibility

The VCU1287 board is provided with the Virtex UltraScale XCVU095-FFVB2104E FPGA. The board also supports other Virtex UltraScale device densities (XCVU080, XCVU125, and XCVU160), as well as the Kintex® UltraScale XCKU115 device in the pin-compatible FFVB2104 package. However, some transceivers available in large density devices are not available in the XCVU095 device (for example, GTH QUAD_232 and QUAD_233).

Block Diagram

The VCU1287 board block diagram is shown in Figure 1-1.

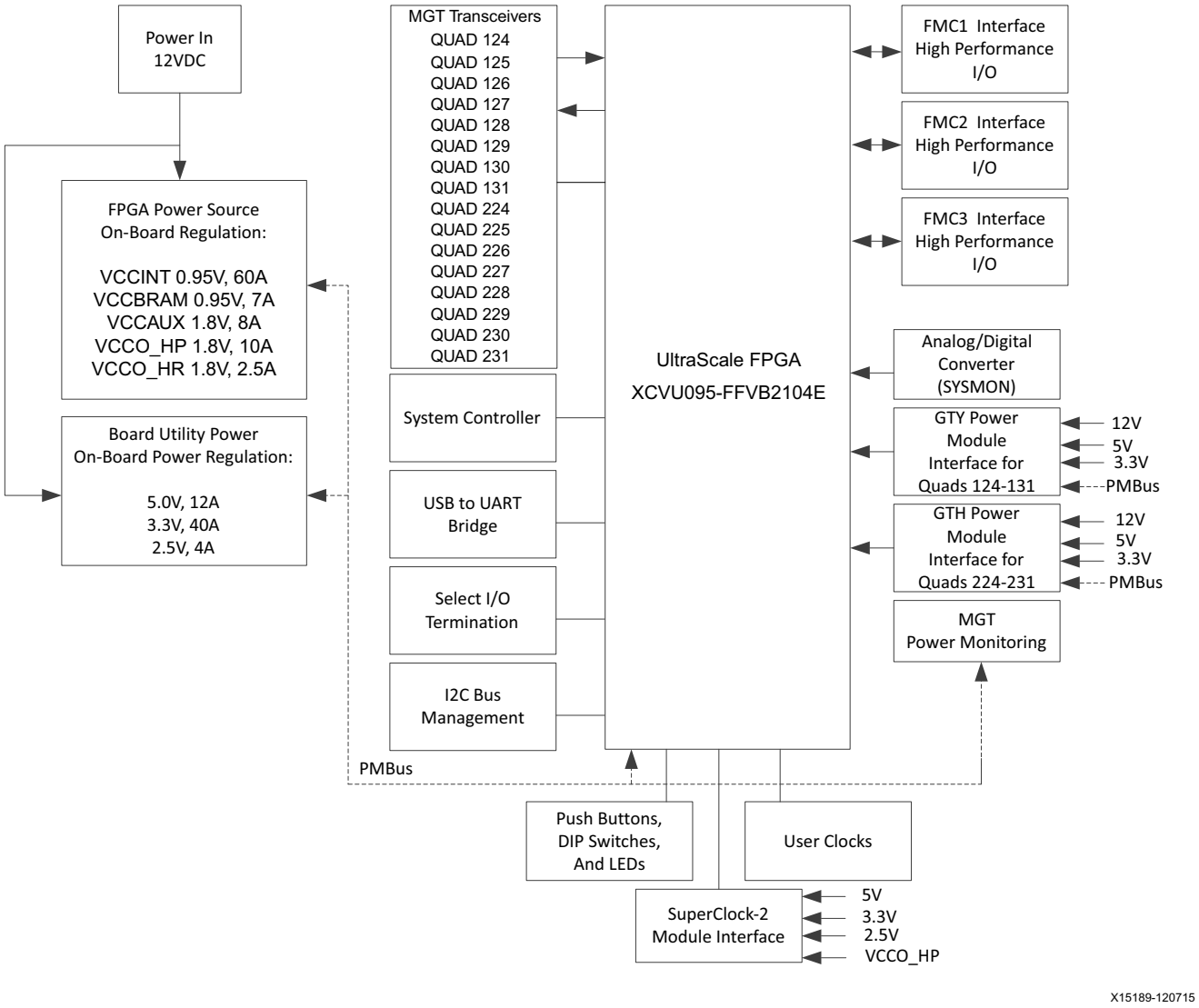

Figure 1-1: **VCU1287 Board Block Diagram**

Board Features

The VCU1287 characterization board features are listed here. Detailed information for each feature is provided in Chapter 3, Board Component Descriptions.

- UltraScale XCVU095-FFVB2104E FPGA
- BullsEye cable access to all 32 GTH and 32 GTY transceivers on the UltraScale XCVU095-FFVB2104E FPGA
- Onboard power supplies for all necessary voltages
- Power connectors for optional use of external power supplies
- Digilent USB JTAG programming port
- System controller (Zynq-7000 AP SoC XC7Z010-CLG225 FPGA)
- Two MGT power modules supporting UltraScale FPGA GTY and GTH transceiver power requirements
- A fixed 300 MHz 2.5V LVDS oscillator wired to multi-region clock capable (MRCC) inputs
- Two pairs of differential MRCC inputs with SMA connectors
- SuperClock-2 module supporting programmable clock outputs
- Samtec BullsEye connector pads for the GTY and GTH transceivers and reference clocks
- General purpose DIP switches, LEDs, pushbuttons, and test I/O
- Three VITA 57.1 FPGA mezzanine card (FMC) high pin count (HPC) connectors
- USB-to-UART bridge
- I2C bus
- PMBus connectivity to the boards digital power supplies
- Active cooling for the FPGA

Board Setup and Configuration

Board Component Location

Figure 2-1 shows the VCU1287 board component locations. Each numbered component shown in the figure is keyed to Table 2-1. Table 2-1 identifies the components and links to a detailed functional description of the components and board features in Chapter 3, Board Component Descriptions.

IMPORTANT: *Figure 2-1 is for visual reference only and might not reflect the current revision of the board.*

CAUTION! *The VCU1287 board can be damaged by electrostatic discharge (ESD). Follow standard ESD prevention measures when handling the board.*

CAUTION! *Do not remove the rubber feet from the board. The feet provide clearance to prevent short circuits on the back side of the board.*

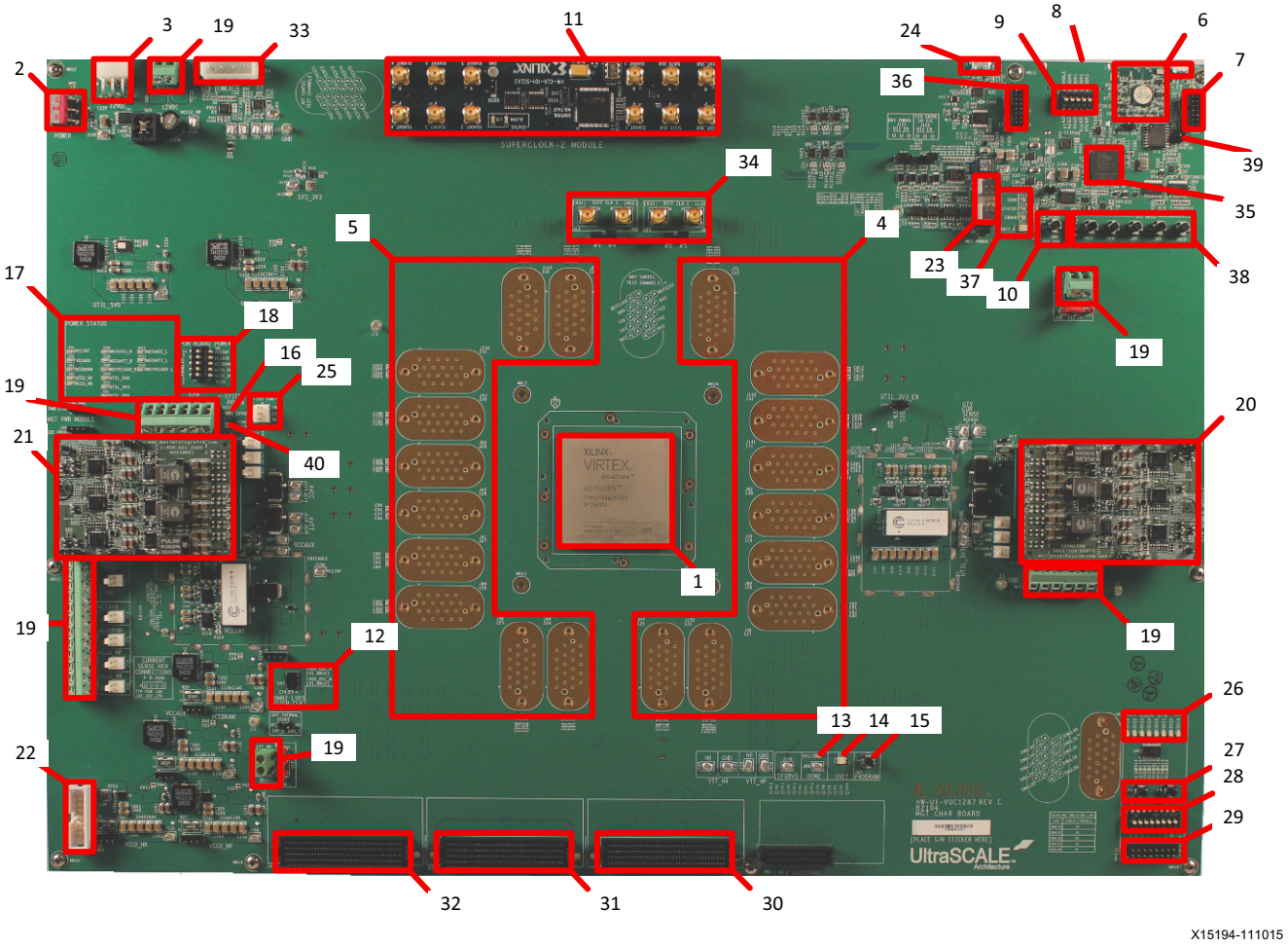

Figure 2-1: **VCU1287 Characterization Board Components**

Table 2-1: **VCU1287 Board Components**

Callout	Reference Designator	Feature Description
1	U1	Virtex UltraScale XCVU095-FFVB2104E Device
2	SW1	Power Switch
3	J28	12V mini-fit connector (12V Input Power)
4	J37, J155, J38, J80, J39, J82, J141, J142, J71	GTY transceiver connector pads Q124, Q125, Q126, Q127, Q128, Q129, Q130, Q131, Q132 (MGT Transceivers and Reference Clocks)
5	J40, J88, J89, J41, J42, J92, J43, J156, J143, J68	GTH transceiver connector pads Q224, Q225, Q226, Q227, Q228, Q229, Q230, Q231, Q232, Q233 (MGT Transceivers and Reference Clocks)
6	U80	Digilent USB JTAG connector (micro-B receptacle) (A list of jumpers and switches and their required positions for normal board operation is provided in Appendix A, Default Jumper Settings.)
7	J2	Platform USB JTAG connector (alternate access for programming cables) (A list of jumpers and switches and their required positions for normal board operation is provided in Appendix A, Default Jumper Settings.)
8	J10	SD card connector (back-side of board) (A list of jumpers and switches and their required positions for normal board operation is provided in Appendix A, Default Jumper Settings.)
9	SW13	System Controller Configuration DIP Switches
10	SW4	System Controller Reset
11	J36	SuperClock-2 Module
12	U42	300 MHz LVDS Oscillator
13	DS17	FPGA DONE status LED (DONE LED)
14	DS3	FPGA INIT_B status LED (INIT LED)
15	SW7	FPGA PROG_B pushbutton (PROGRAM Pushbutton)
16	DS18	12V power status LED (Power Switch)
17	DS4, DS5, DS6, DS7, DS8, DS9, DS10, DS11, DS13, DS14, DS15, DS28, DS29, DS30, DS32	Status LEDs for FPGA logic, transceiver, and utility power
18	SW2	Power regulation inhibitor switch for onboard regulators (Using External Power Sources)
19	J5, J18, J19, J20, J22, J23, J26, J27, J67, J69	External power supply connectors (Using External Power Sources)
20	J93, J138	Bank 124-132 GTY transceiver power supply module (Onboard Power Regulation and A list of jumpers and switches and their required positions for normal board operation is provided in Appendix A, Default Jumper Settings.)

Table 2-1: **VCU1287 Board Components *(Cont'd)***

Callout	Reference Designator	Feature Description
21	J46, J124	Bank 224-233 GTH transceiver power supply module (A list of jumpers and switches and their required positions for normal board operation is provided in Appendix A, Default Jumper Settings.)
22	J21	FPGA and utility rails PMBUS connector (A list of jumpers and switches and their required positions for normal board operation is provided in Appendix A, Default Jumper Settings.)
23	J4	MGT rails PMBus connector (A list of jumpers and switches and their required positions for normal board operation is provided in Appendix A, Default Jumper Settings.)
24	J1	Connector for USB to Dual UART Bridge (mini-B receptacle)
25	J99	Active Heat Sink Power Connector
26	DS19, DS20, DS21, DS22, DS23, DS24, DS25, DS26	User LEDs (Active-High)
27	SW8, SW9	User Pushbuttons (Active-High)
28	SW3	User DIP Switches (Active-High) and I/O Header
29	J95	User DIP Switches (Active-High) and I/O Header
30	JA2	FMC1 connector (I2C Bus Management)
31	JA3	FMC2 connector (I2C Bus Management)
32	JA4	FMC3 connector (I2C Bus Management)
33	J73	ATX power connector (12V Input Power)
34	J13, J14, J84, J85	Differential SMA MRCC Pin Inputs
35	U38	System controller
36	J3	System controller JTAG connector
37	DS1, DS12, DS16, DS27	System controller status LEDs
38	SW5, SW6, SW10, SW11, SW12	System controller GPIO pushbuttons
39	J6	JTAG chain select
40	DS2	PowerGood LED

Default Jumper and Switch Positions

A list of jumpers and switches and their required positions for normal board operation is provided in Appendix A, Default Jumper Settings.

Board Component Descriptions

Overview

This chapter provides a detailed functional description of the board's components and features. Table 2-1, page 10 identifies the components and links to the corresponding detailed functional description in this chapter. Component locations are shown in Figure 2-1, page 9.

Component Descriptions

Virtex UltraScale XCVU095-FFVB2104E Device

The VCU1287 board is populated with the UltraScale XCVU095-FFVB2104E FPGA at U1 (callout 1, Figure 2-1). For further information on UltraScale FPGAs, see *UltraScale Architecture and Product Overview* (DS890) [Ref 1].

Power Management

12V Input Power

The VCU1287 board receives 12V main power through J28 (callout 3, Figure 2-1) using the 12V AC adapter that is provided with the VCU1287 board characterization kit. J28 is a 6-pin (2 x 3), right angle, mini-fit connector.

CAUTION! *When supplying 12V through J28, use only the power supply provided for use with this board (Xilinx part number 3800033).*

CAUTION! *Do NOT use a 6-pin, PC ATX power supply connector with J28. The pinout of the 6-pin, PC ATX connector is not compatible. J28 and the board will be damaged if an attempt is made to power it from a PC ATX power supply connector.*

12V power can also be provided through:

- Connector J73 (callout 33, Figure 2-1) which accepts an ATX hard drive 4-pin power plug.
- Connector J27 (callout 19, Figure 2-1) which can be connected to a bench-top power supply.

CAUTION! *Because connector J73 provides no reverse polarity protection, use a power supply with a current limit set at 6A maximum.*

CAUTION! *Do NOT apply 12V power to more than a single input source. For example, do not apply power to J73 and J27 at the same time.*

CAUTION! *If J73 or J27 is used to supply the 12V input power, the board consumption should NOT exceed 75W because of Q1 limitation.*

Power Switch

The VCU1287 board main power is turned On or Off using switch SW1 (callout 2, Figure 2-1). When the switch is in the ON position, power is applied to the board and the green LED DS18 illuminates (callout 16, Figure 2-1).

Onboard Power Regulation

Figure 3-1 shows the onboard power supply architecture.

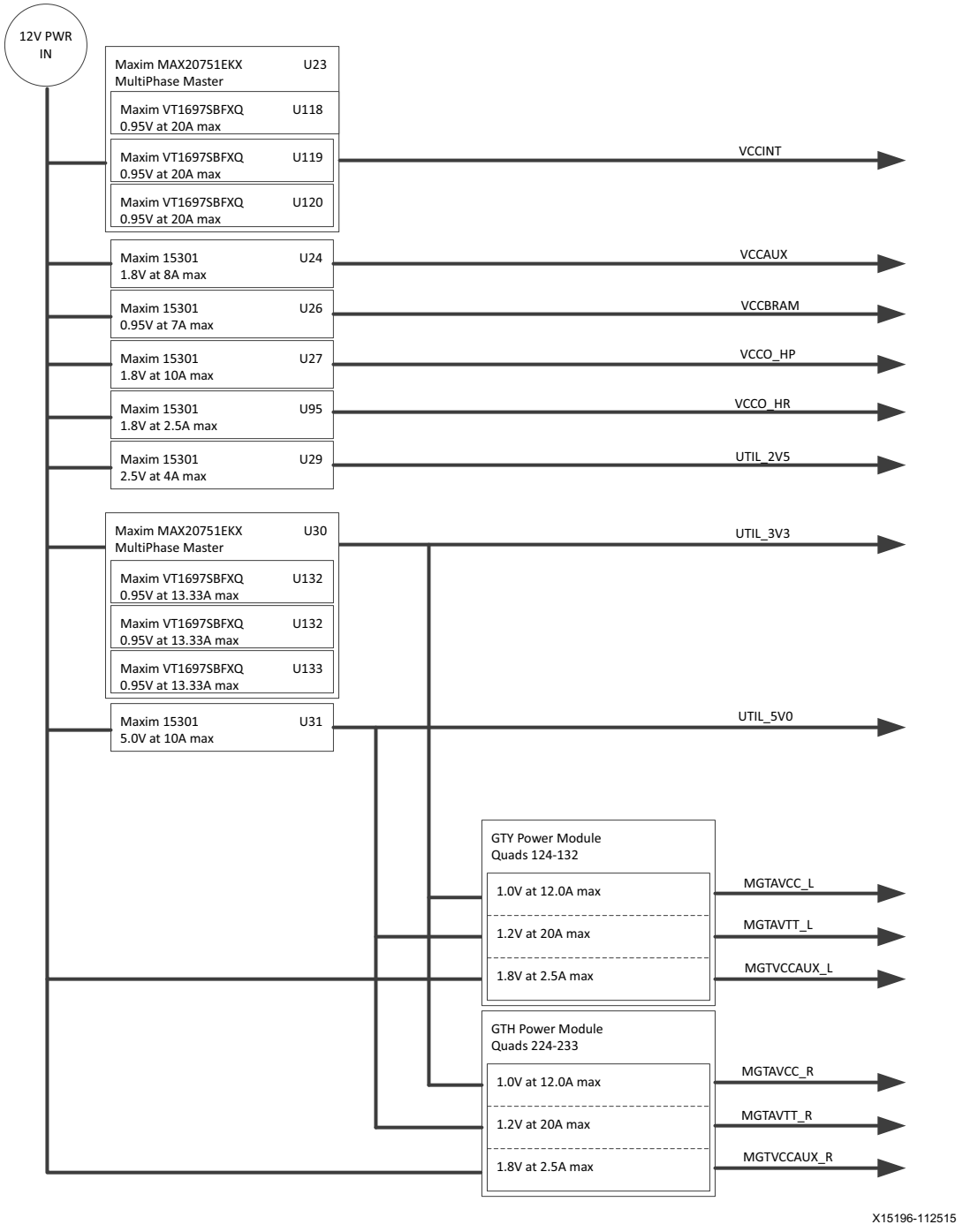

Figure 3-1: **VCU1287 Board Power Supply Block Diagram**

The VCU1287 board uses power regulators and PMBus compliant digital PWM system controllers from Maxim Integrated to supply the FPGA logic and utilities voltages listed in Table 3-1. The board can also be configured to use an external bench power supply for each voltage. See Onboard Power Regulation.

Table 3-1: **Onboard Power System Devices**

Device Part Number	Reference Designator	Description	Power Rail Net Name	Voltage
FPGA Logic				
Maxim MAX20751EKX	U23	MultiPhase master with PMBus interface controller (60A three phases at 20A/phase	VCCINT	0.95V
Maxim MAX15301	U24	InTune digital point of load (PoL) controller, 8A	VCCAUX	1.8V
Maxim MAX15301	U26	InTune digital point of load (PoL) controller, 7A	VCCBRAM	0.95V
Maxim MAX15301	U27	InTune digital point of load (PoL) controller, 10A	VCCO_HP	1.8V
Maxim MAX15301	U95	InTune digital point of load (PoL) controller, 2.5A	VCCO_HR	1.8V
Utility				
Maxim MAX15301	U29	InTune digital point of load (PoL) controller, 10A	UTIL_2V5	2.5V
Maxim MAX20751EKX	U30	MultiPhase Master with PMBus Interface Controller (40A three phases at 13.33A/phase)	UTIL_3V3	3.3V
Maxim MAX15301	U31	InTune digital point of load (PoL) controller, 12A	UTIL_5V0	5.0V
GTY Transceivers (monitoring only)				
INA226	U99	Current shunt and power monitor with I2C interface	MGTAVCC_L	1.0V
INA226	U97	Current shunt and power monitor with I2C interface	MGTAVTT_L	1.2V
INA226	U98	Current shunt and power monitor with I2C interface	MGTVCCAUX_L	1.8V
GTH Transceivers (monitoring only)				
INA226	U50	Current shunt and power monitor with I2C interface	MGTAVCC_R	1.0V
INA226	U51	Current shunt and power monitor with I2C interface	MGTAVTT_R	1.2V
INA226	U52	Current shunt and power monitor with I2C interface	MGTVCCAUX_R	1.8V
System Controller				
Maxim MAX15053	U13	Fixed LDO regulator	SYS_1V0	1.0V
Maxim MAX15027	U33	Fixed LDO regulator	VCC_1V2	1.2V

Table 3-1: **Onboard Power System Devices *(Cont'd)***

Device Part Number	Reference Designator	Description	Power Rail Net Name	Voltage
Maxim MAX15027	U25	Fixed LDO regulator	VCC_1V8	1.8V

CAUTION! *The output voltages of the Max15301 can be reprogrammed using the Maxim InTune Digital Power Tool [Ref 5]. However,* ***extreme caution*** *must be taken when attempting to modify any of the onboard regulators. An incorrectly programmed regulator can damage onboard components.*

Notes:

1. The MAX20751EKX device has limited nonvolatile memory reprogramming saves (four counts).

Using External Power Sources

Callout 19, Figure 2-1

Each voltage rail for the FPGA logic and MGT transceiver has an associated Euro-Mag spring-clamp terminal block that can be used to provide power from an external source (Table 3-2).

CAUTION! *Do NOT apply power to any of the FPGA logic external power supply connectors without first disabling the associated regulator or regulators. Failing to disable the regulator can damage the board.*

Each onboard FPGA logic regulator can be disabled using its respective power regulation inhibitor dip switch (callout 18, Figure 2-1). A regulator is disabled when the power regulation inhibitor switch is set to the ON position. Table 3-2 shows a list of external power connections for the different power rails.

Table 3-2: **FPGA Logic and MGT Transceiver Rails**

	Power Rail Net Name	External Supply Connector (s)	Power Regulation Jumper
FPGA Logic	VCCINT	J25	J22
	VCCAUX		J23
	VCCBRAM		J20
	VCCO_HP		J19
	VCCO_HR		J18
GTH Transceiver	MGTAVCC_R	J26	J15
	MGTAVTT_R		J16
	MGTVCCAUX_R		J17

Table 3-2: **FPGA Logic and MGT Transceiver Rails *(Cont'd)***

	Power Rail Net Name	External Supply Connector (s)	Power Regulation Jumper
GTY Transceiver	MGTAVCC_L	J67	J62
	MGTAVTT_L		J63
	MGTVCCAUX_L		J64

Notes:

1. The MGT power module must be removed before providing external power to any of the transceiver rails (see FPGA Configuration).

Monitoring Voltage and Current

Voltage and current monitoring and control for Maxim power system is available through either the VCU1287 board system controller or the MaximPower Tool software GUI. The VCU1287 board system controller is the most convenient way to monitor the voltage and current values for the power rails listed in Table 3-2. For details on how to use this built-in feature, see Power Monitoring Data Menu in Appendix D, System Controller.

The VCU1287 board includes these PMBus connectors:

- J21 (callout 20, Figure 1-2), for use with the Maxim USB-to-PMBus interface dongle (MAXPOWERTOOL002 [Ref 5]) and the InTune Digital Power GUI.
- J4 (callout 21, Figure 1-2) is used to connect to the MGT power module PMBus using the Maxim USB-to-PMBus interface dongle (MAXPOWERTOOL002 [Ref 5]) and the InTune Digital Power GUI.

Note: Use wires to connect the J4 pins to the Maxim MAXPOWERTOOL002 dongle as shown in Figure 3-2.

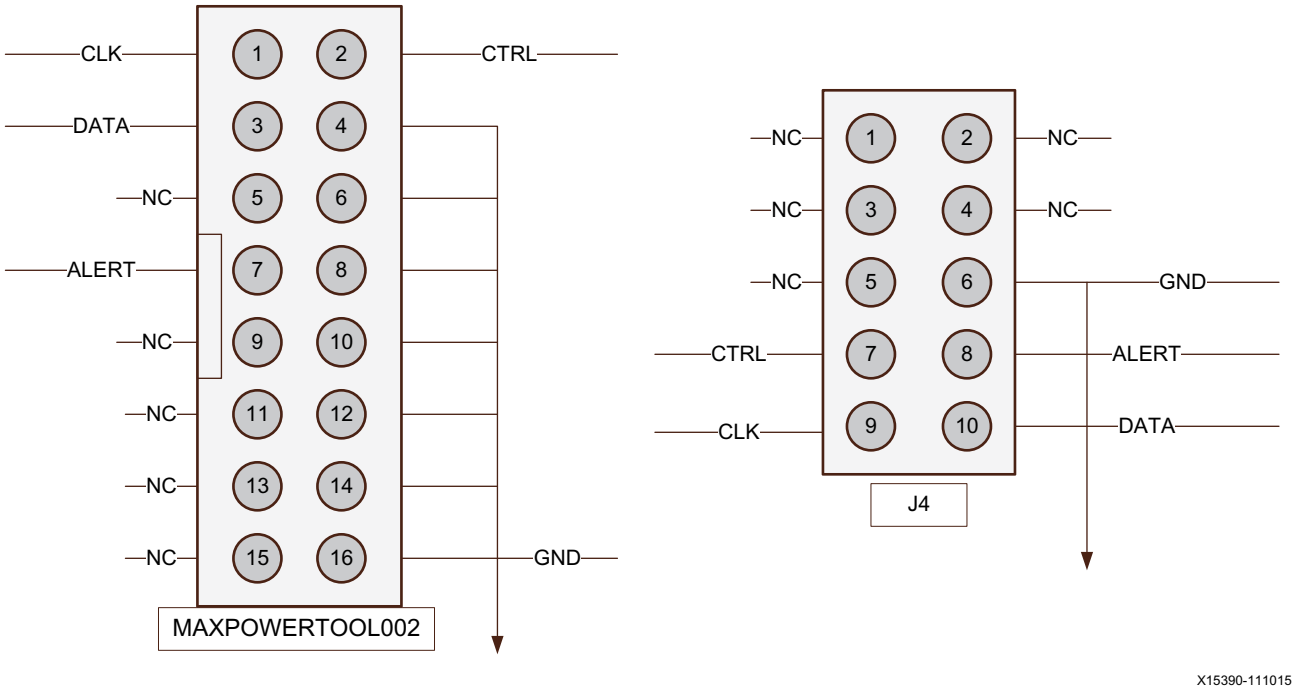

Figure 3-2: **Connecting MAXPOWERTOOL002 to J4**

The onboard Maxim power controllers (U23, U24, U26, U27, U29, U30, U31, and U95) by default are isolated from the MGT power modules PMBus. However, the two interfaces can be linked by removing J8 next to the MGT power module PMBus connector J4. This configuration is required when using Maxim power tools to monitor and control both the FPGA power rails and the transceiver power rails using the Maxim InTune digital power GUI.

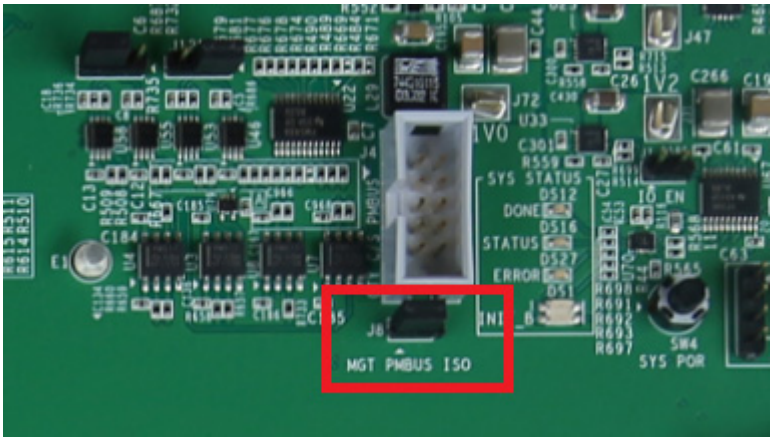

Figure 3-3: **MGT PMBus isolation**

More information about the power system components used by the VCU1287 board is available from the Maxim Integrated InTune digital power website [Ref 5].

MGT Transceiver Power Module

There are two MGT transceiver power modules (callout 20 and 21, Figure 2-1). The GTY power modules supply the MGTAVCC_L, MGTAVTT_L, and MGTVCCAUX_L power rails, which connect to the FPGA GTY transceivers. The GTH power module supplies the MGTAVCC_R, MGTAVTT_R, and MGTVCCAUX_R power rails, which connect to the FPGA GTH transceivers. Two MGT power modules from Maxim Integrated are provided with the VCU1287 board for evaluation. The modules can be plugged into connectors J138 and J93 or J46 and J124 in the outlined and labeled power module locations shown in Figure 3-3 and Figure 3-4.

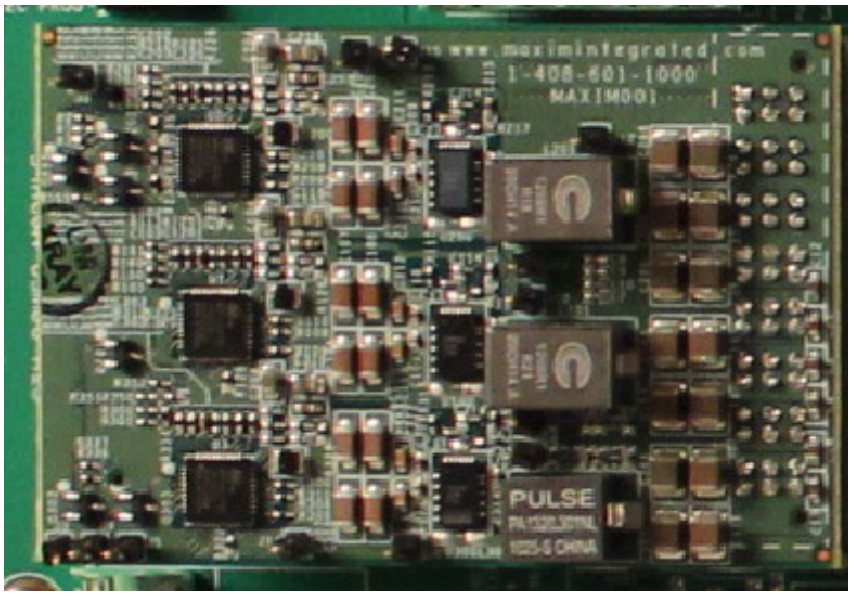

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Figure 3-4: **Maxim Integrated MGT Power Module**

Table 3-3 lists the nominal voltage values for MGTAVCC_L, MGTAVTT_L, MGTVCCAUX_L, MGTAVCC_R, MGTAVTT_R, and MGTVCCAUX_R power rails. It also lists the maximum current rating for each rail supplied by MGT modules included with the VCU1287 board.

Table 3-3: **MGT Power Modules**

MGT Transceiver Rail Net Name	Nominal Voltage	Maximum Current Rating
MGTAVCC_R	1.0V	12A
MGTAVTT_R	1.2V	20A
MGTVCCAUX_R	1.8V	2.5A
MGTAVCC_L	1.0V	12A
MGTAVTT_L	1.2V	20A
MGTVCCAUX_L	1.8V	2.5A

The MGT transceiver power rails can also be supplied externally. The external supply connectors are described in Table 3-2.

CAUTION! *The MGT Power Module MUST be removed when providing external power to the MGT transceiver rails.*

Information about the available MGT power modules included with the VCU1287 board characterization kit is available from the vendor websites [Ref 5].

Active Heat Sink Power Connector

Callout 25, Figure 2-1

An active heat sink (Figure 3-5) is provided for the FPGA. A 12V fan is affixed to the heat sink and is powered from the 3-pin friction lock header J99 (Figure 3-6).

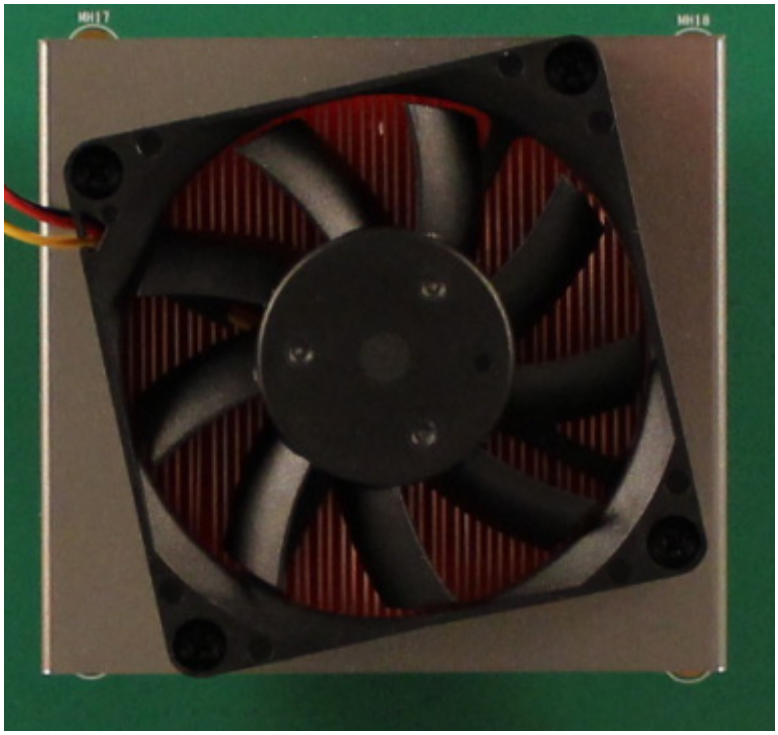

Figure 3-5: **Active FPGA Heat Sink**

The fan power connections are detailed in Table 3-4:

Table 3-4: **Fan Power Connections**

Fan Wire	Header Pin
Black	J99.1 - GND
Red	J99.2 - 12V
Blue	J99.3 - NC

Figure 3-6 shows the heat sink fan power connector J99.

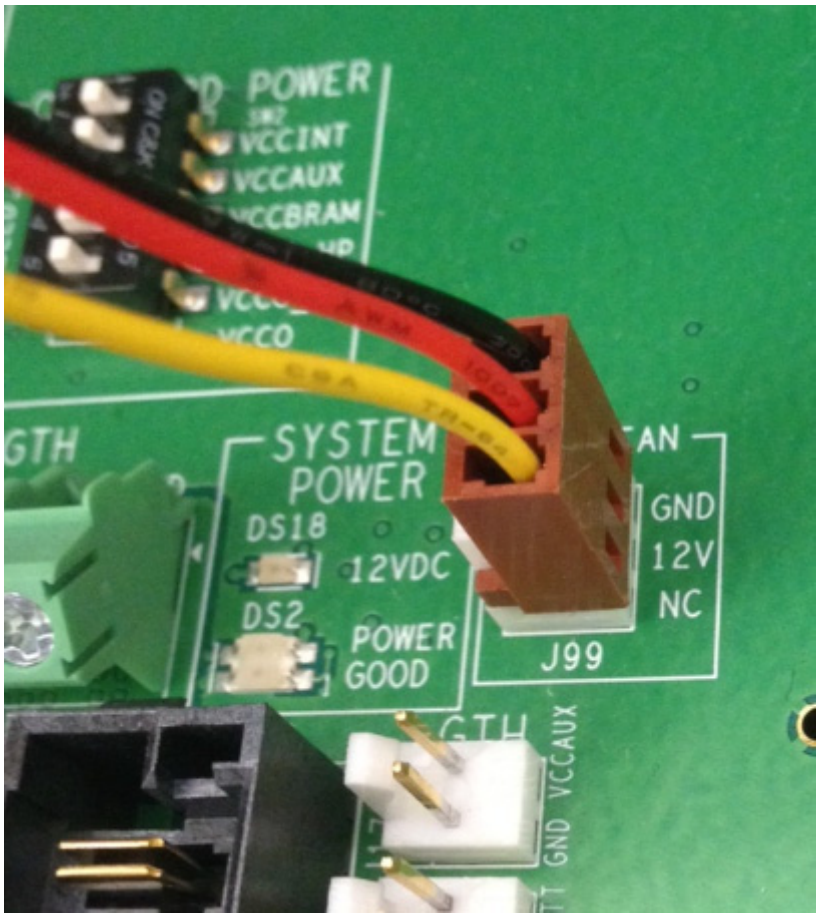

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Figure 3-6: **Heat Sink Fan Power Connector J99**

FPGA Configuration

The FPGA is configured using one of the following options:

- Digilent embedded USB JTAG connector (callout 6, Figure 2-1).

  The VCU1287 board comes with an embedded USB-to-JTAG configuration module (Digilent, U80), which allows a host computer to access the board JTAG chain using a Standard A to Micro-B USB cable.

- Platform cable USB JTAG cable connector (callout 7, Figure 2-1).

  A JTAG connector (J2) can be used to provide access to the JTAG chain using the Xilinx Platform Cable USB, Platform Cable USB II, or Parallel Cable IV (PCIV) configuration cable.

- SD card using the Zynq-7000 AP SoC system controller in 8-bit SelectMAP mode (callout 8, Figure 2-1).

  The FPGA can be configured from an SD memory card installed in J10 with the help of the system controller U38, which reads a predefined bit file from the SD card and configures the FPGA in 8-bit SelectMAP configuration mode. See FPGA CONFIG Menu.

The JTAG chain of the board is illustrated in Figure 3-7. By default, only the UltraScale FPGA is part of the chain (J6 jumper uninstalled). Installing the J6 jumper enables an 8-bit bus transceiver (U69, SN74AVC8T245) and adds the FMC interfaces to the chain.

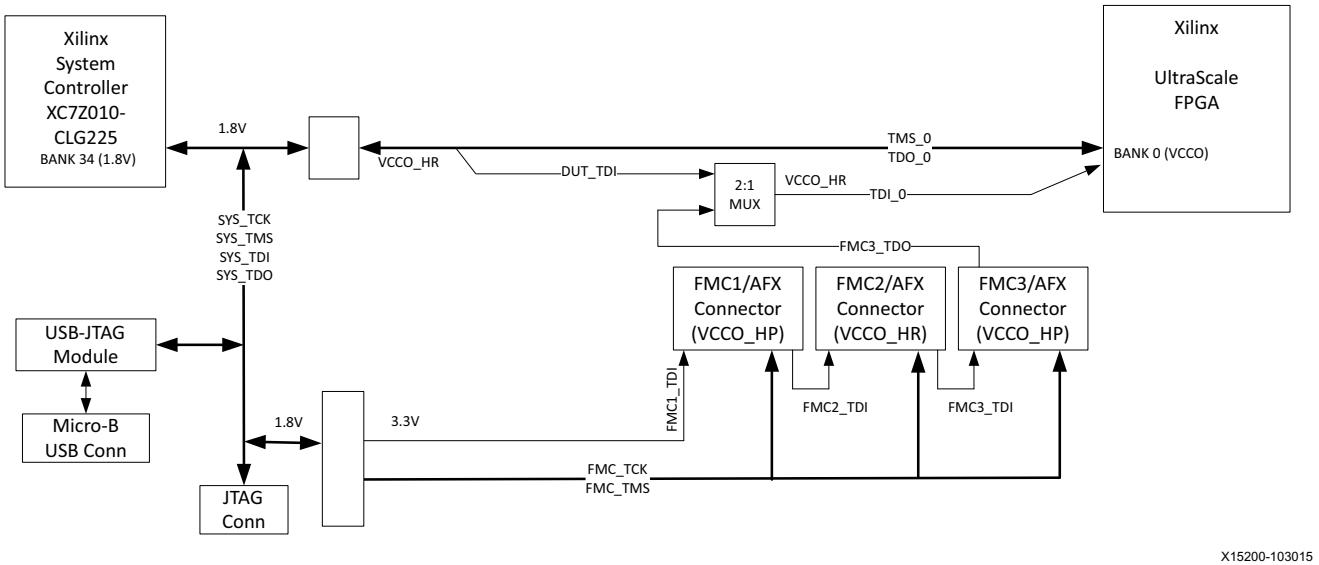


Figure 3-7: **JTAG Chain**

PROGRAM Pushbutton

Pressing the PROGRAM pushbutton SW7 (callout 15, Figure 2-1) asserts the active-Low program pin of the FPGA.

DONE LED

The DONE LED DS17 (callout 13, Figure 2-1) indicates the state of the DONE pin of the FPGA. When the DONE pin is High, DS17 lights indicating the FPGA is successfully configured.

INIT LED

The dual-color INIT LED DS3 (callout 14, Figure 2-1) indicates the FPGA initialization status. During FPGA initialization, the INIT LED illuminates RED. When FPGA initialization has completed, the LED illuminates GREEN.

System Controller

The VCU1287 board utilizes a Xilinx XC7Z010-CLG225 Zynq-7000 AP SoC U38 (callout 35, Figure 2-1) system controller that can be used to:

- Configure the FPGA using predefined selection of configuration bit files on an SD card using 8-bit SelectMAP configuration
- Select the output frequencies of the Super-Clock2 module over I2C
- Monitor the onboard power system (PMBus)

See Appendix D, System Controller for information on the system controller menu options.

System Controller Reset

The SYS_POR pushbutton SW4 (callout 10, Figure 2-1) asserts the active-Low system controller power-on reset (SYS_POR). When SYS_POR is reasserted, the system controller is reconfigured using the controller design stored on an attached SPI flash.

System Controller Status LEDs

DS1, DS12, DS16, and DS27 (callout 37, Figure 2-1) show the system controller INIT_B, DONE, STATUS, and ERROR status, respectively.

System Controller Configuration DIP Switches

DIP switch SW13 (callout 9, Figure 2-1), shown in Figure 3-8, selects the address of the UltraScale FPGA configuration bitstream to be loaded from the SD card. The switch ON position is indicated by the arrow next to bit 1 of the switch. The ENABLE bit (switch position 1) is used to enable the SD card configuration mode.

Figure 3-8: **Configuration DIP Switch (SW13)**

The switch settings for selecting each address are shown in Table 3-5.

Table 3-5: **SW13 DIP Switch Configuration**

Configuration Bitstream Address	ADDR3	ADDR2	ADDR1	ADDR0
0	OFF	OFF	OFF	OFF
1	OFF	OFF	OFF	ON
2	OFF	OFF	ON	OFF
3	OFF	OFF	ON	ON
4	OFF	ON	OFF	OFF
5	OFF	ON	OFF	ON
6	OFF	ON	ON	OFF
7	OFF	ON	ON	ON
8	ON	OFF	OFF	OFF
9	ON	OFF	OFF	ON
10	ON	OFF	ON	OFF
11	ON	OFF	ON	ON
12	ON	ON	OFF	OFF
13	ON	ON	OFF	ON
14	ON	ON	ON	OFF
15	ON	ON	ON	ON

System Controller GPIO Pushbuttons

SW5, SW6, SW10, SW11, SW12 (callout 38, Figure 2-1) are active-high pushbuttons connected to GPIO pins on the system controller. See GPIO Data Menu for more details.

USB to Dual UART Bridge

Callout 24, Figure 2-1

VCU1287 uses a single chip USB-to-dual UART bridge (U32, Silicon Laboratories CP2105) for simultaneous serial communication between a host terminal and the UltraScale FPGA, and between a host terminal and the system controller. The onboard micro-B receptacle USB connector J1 (callout 23, Figure 2-1) pinout is connected to the dual-UART bridge.

The FPGA connects through a serial communication terminal connection (115200-8-N-1) using the standard communication port of the Silicon Labs USB to dual-UART bridge using four signal pins:

- Transmit (TX)
- Receive (RX)
- Request to send (RTS)
- Clear to send (CTS)

The dual-UART interface connections are split between two components:

- UART1 SCI (standard) interface is connected to the XCVU095 FPGA
- UART2 ECI (enhanced) interface is connected to the XC7Z010 system controller

Silicon Labs provides royalty-free virtual COM port (VCP) drivers for the host computer. These drivers permit the CP2105GM dual USB-to-UART bridge to appear as a pair of COM ports to communications application software (for example, TeraTerm or HyperTerm) that runs on the host computer.

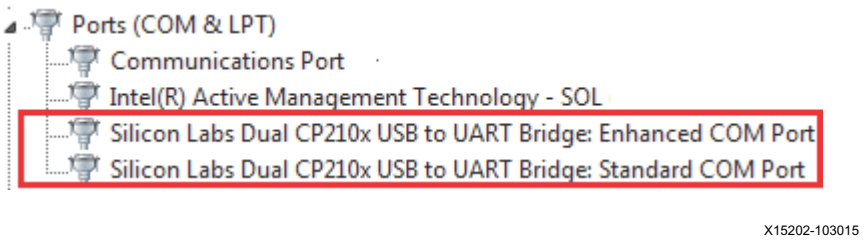


Figure 3-9: **Silicon Labs USB to UART Bridge Standard COM Port**

IMPORTANT: *The VCP device drivers must be installed on the host PC prior to establishing communications with the VCU1287 board.*

The driver assigns the higher PC COM port number to UART1 (SCI) and the lower PC COM port number to UART (ECI).

The connections of these signals between the FPGA and the CP2105 are listed in Table 3-6.

Table 3-6: **FPGA to UART Connection**

FPGA(U1)				Schematic Net Name	Device(U32)		
Pin	Function	Direction	IOSTANDARD		Pin	Function	Direction
BA12	RTS	Output	LVCMOS18	UART_CTS_I_B	18	CTS	Input
BB12	CTS	Input	LVCMOS18	UART_RTS_O_B	19	RTS	Output
BF13	TX	Output	LVCMOS18	UART_RXD_I	20	RXD	Input
BF14	RX	Input	LVCMOS18	UART_TXD_O	21	TXD	Output

The bridge device also provides as many as four GPIO signals that can be defined for status and control information (Table 3-7).

Table 3-7: **CP2105 USB-to-UART Bridge User GPIO**

FPGA(U1)				Schematic Net Name	Device(U32)		
Pin	Function	Direction	IOSTANDARD		Pin	Function	Direction
AY15	SelectIO	IN/OUT	LVCMOS18	UART_GPIO_0	24	GPIO	IN/OUT
AV13	SelectIO	IN/OUT	LVCMOS18	UART_GPIO_1	23	GPIO	IN/OUT
AR15	SelectIO	IN/OUT	LVCMOS18	UART_GPIO_2	22	GPIO	IN/OUT
AR16	SelectIO	IN/OUT	LVCMOS18	UART_GPIO_3	15	GPIO	IN/OUT

The second port of the CP2105 USB-to-dual UART is connected to the onboard system controller. See Appendix D, System Controller.

300 MHz LVDS Oscillator

The VCU1287 board has one 300 MHz LVDS oscillator U42 (callout 12, Figure 2-1) connected to multi-region clock capable (MRCC) inputs on the FPGA. Table 3-8 lists the FPGA pin connections to the LVDS oscillator.

Table 3-8: **LVDS Oscillator MRCC Connections**

FPGA (U1)				Schematic Net Name	Device (42)		
Pin	Function	Direction	I/O Standard		Pin	Function	Direction
AW14	SYSTEM CLOCK_P	Input	LVDS	LVDS_OSC_P	4	300 MHz LVDS oscillator	Output
AW13	SYSTEM CLOCK_N	Input	LVDS	LVDS_OSC_N	5	300 MHz LVDS oscillator	Output

Differential SMA MRCC Pin Inputs

The VCU1287 board provides two pairs of differential SMA transceiver clock inputs (callout 34, Figure 2-1) that can be used for connecting to an external clock source. The FPGA MRCC pins are connected to the SMA connectors as shown in Table 3-9.

Table 3-9: **Differential SMA Clock Connections**

FPGA(U1)				Schematic Net Name	SMA Connector
Pin	Function	Direction	IOSTANDARD		
L32	USER CLOCK_1_P	INPUT	LVDS	CLK_DIFF_1_P	J84
K32	USER CLOCK_1_N	INPUT	LVDS	CLK_DIFF_1_N	J85
M31	USER CLOCK_2_P	INPUT	LVDS	CLK_DIFF_2_P	J83
M32	USER CLOCK_2_N	INPUT	LVDS	CLK_DIFF_2_N	J86

SuperClock-2 Module

The SuperClock-2 module (callout 11, Figure 2-1) connects to the clock module interface connector (J36) and provides a programmable, low-noise and low-jitter clock source for the VCU1287 board. The clock module maps to FPGA I/O by way of 14 control pins, 2 LVDS pairs, 1 regional clock pair, and 1 reset pin. Table 3-10 shows the FPGA I/O mapping for the SuperClock-2 module interface. The VCU1287 board supplies UTIL_5V0, UTIL_3V3, UTIL_2V5 and VCCO_HP input power to the Table 3-10 clock module interface.

Table 3-10: **SuperClock-2 FPGA I/O Mapping**

FPGA(U1)				Schematic Net Name	J36 Pin		
Pin	Function	Direction	IOSTANDARD		Pin	Function	Direction
L13	Clock recovery	Input	LVDS	CM_LVDS1_P	1	Clock recovery	Output
K13	Clock recovery	Input	LVDS	CM_LVDS1_N	3	Clock recovery	Output
J33	Clock recovery	Input	LVDS	CM_LVDS2_P	9	Clock recovery	Output
H33	Clock recovery	Input	LVDS	CM_LVDS2_N	11	Clock recovery	Output
G26	Regional clock	Input	LVDS	CM_GCLK_P	25	Global clock	Output
G27	Regional clock	Input	LVDS	CM_GCLK_N	27	Global clock	Output
B30	Control I/O	Output	LVCMOS	CM_H_DEC	67	DEC	Input
A30	Control I/O	Output	LVCMOS	CM_H_INC	69	INC	Input
B29	Control I/O	Output	LVCMOS	CM_FS_ALIGN	71	ALIGN	Input
A29	Control I/O	Input	LVCMOS	CM_H_LOL	79	LOL	Output
A27	Control I/O	Output	LVCMOS	CM_H_INT_ALRM	81	INT_ALRM	Input
A28	Control I/O	Output	LVCMOS	CM_C1B	83	C1B	Input
E30	Control I/O	Output	LVCMOS	CM_C2B	85	C2B	Input
D30	Control I/O	Output	LVCMOS	CM_C3B	87	C3B	Input
D29	CONTROL I/O	Output	LVCMOS	CM_C1A	89	C1A	Input
C29	CONTROL I/O	Output	LVCMOS	CM_C2A	91	C2A	Input
C27	CONTROL I/O	Output	LVCMOS	CM_H_CS0_C3A	95	CS0_C3A	Input
B27	CONTROL I/O	Output	LVCMOS	CM_H_CS1_C4A	97	CS1_C4A	Input
C28	CM_RESET	Output	LVCMOS	CM_RST	66	RESET_B	Input

User LEDs (Active-High)

DS19 through DS26 (callout 24, Figure 2-1) are eight active-High LEDs that are connected to user I/O pins on the FPGA as shown in Table 3-11. These LEDs can be used to indicate status or for other purposes.

Table 3-11: **User LEDs**

FPGA(U1)				Schematic Net Name	Reference Designator
Pin	Function	Direction	IOSTANDARD		
BD14	User LED	Output	LVCMOS18	APP_LED1	DS19
BF15	User LED	Output	LVCMOS18	APP_LED2	DS20
BE15	User LED	Output	LVCMOS18	APP_LED3	DS21
BE13	User LED	Output	LVCMOS18	APP_LED4	DS25
BD13	User LED	Output	LVCMOS18	APP_LED5	DS24
BC14	User LED	Output	LVCMOS18	APP_LED6	DS23
BB15	User LED	Output	LVCMOS18	APP_LED7	DS22
BB14	User LED	Output	LVCMOS18	APP_LED8	DS26

User DIP Switches (Active-High) and I/O Header

The DIP switch SW3 (callout 28, Figure 2-1) provides a set of eight active-High switches that connect to user I/O pins on the FPGA as shown in Table 3-12. These pins can be used to set control pins or for other purposes. The eight I/Os also map to a test header J95 (callout 29, Figure 2-1) providing external access for these pins. The I/O pins can be connected to the onboard system controller as additional GPIO between the two devices.

IMPORTANT: *Install J7 to connect the user DIP switches to the system controller.*

Table 3-12: **User DIP Switches**

FPGA(U1)				Schematic Net Name	DIP Switch Reference Designator	J95 Test Header Pin	Device(U38) Pin
Pin	Function	Direction	IOSTANDARD				
AP13	User switch	Input	LVCMOS18	USER_SW1	SW3	1	F12
AU16	User switch	Input	LVCMOS18	USER_SW2		3	E13
AU14	User switch	Input	LVCMOS18	USER_SW3		5	E11
AV14	User switch	Input	LVCMOS18	USER_SW4		7	E12
AR13	User switch	Input	LVCMOS18	USER_SW5		9	F13
AV16	User switch	Input	LVCMOS18	USER_SW6		11	F14
AW16	User switch	Input	LVCMOS18	USER_SW7		13	G15
AW15	User switch	Input	LVCMOS18	USER_SW8		15	F15

Figure 3-10 shows the user I/O connector J95 (callout 29, Figure 2-1).

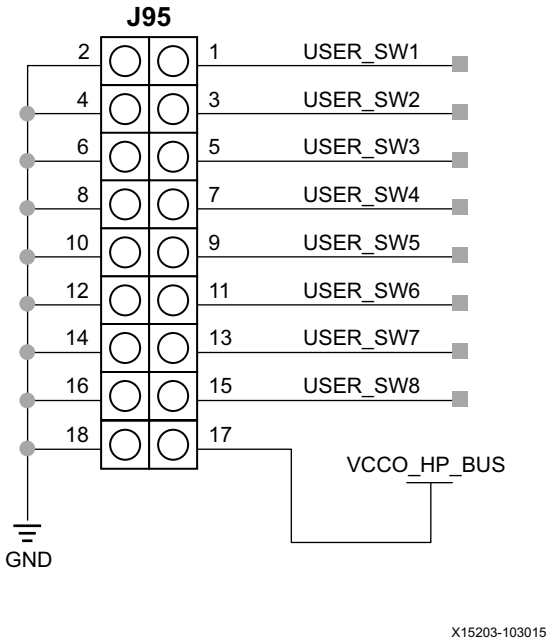


Figure 3-10: **User I/O (J95)**

User Pushbuttons (Active-High)

SW8 and SW9 (callout 27, Figure 2-1) are active-High user push buttons that are connected to user I/O pins on the FPGA as shown in Table 3-13. These switches can be used for any purpose.

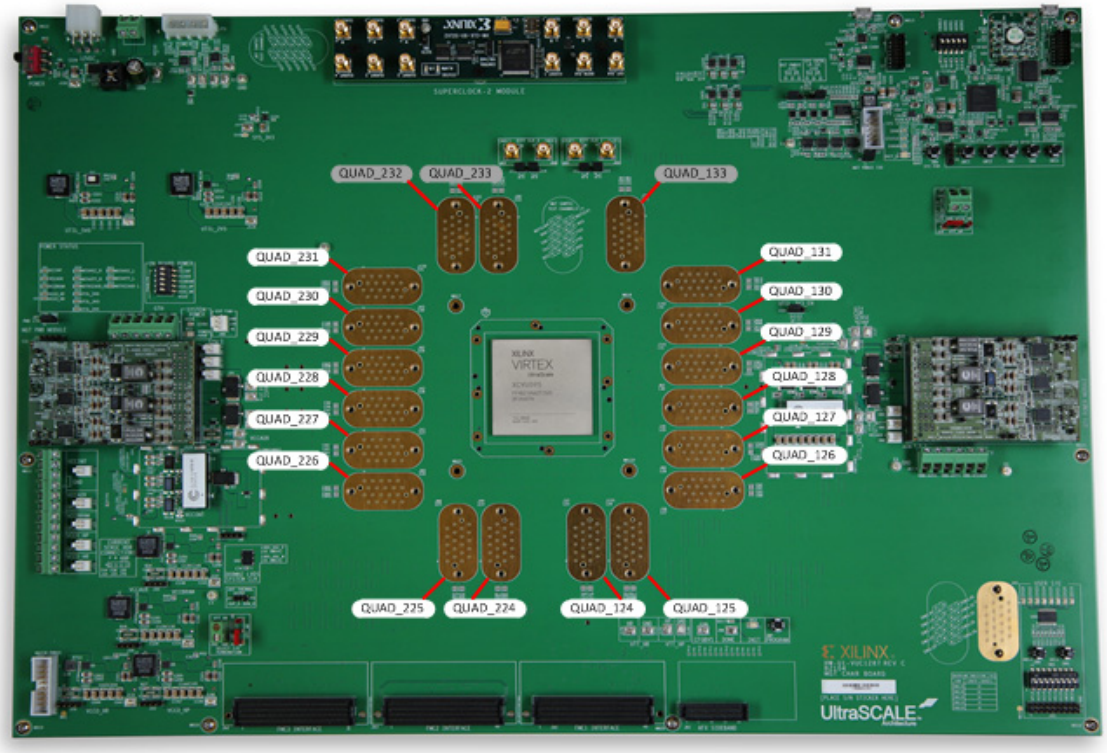
Table 3-13: **User Pushbuttons**

FPGA(U1)				Schematic Net Name	Reference Designator
Pin	Function	Direction	IOSTANDARD		
AN14	User push button	Input	LVCMOS18	USER_PB1	SW9
AM14	User push button	Input	LVCMOS18	USER_PB2	SW8

MGT Transceivers and Reference Clocks

The VCU1287 board provides access to all GTY and GTH transceiver and reference clock pins on the XCVU095 FPGA as shown in Figure 3-11. The MGT transceivers are grouped into eight sets of four TX-RX lanes, referred to as a GTY Quads (Q124 - Q131) on the right side of the board and eight TX-RX lanes, referred to as GTH Quads (Q224 - Q231) on the left side of the board.

IMPORTANT: *Figure 3-11 is for reference only and might not reflect the current revision of the board. Quad 132, Quad 232, and Quad 233 are not available on the XCVU095 FPGA device density.*



X15205-112515

Figure 3-11: **MGT Quad Locations**

Each MGT Quad and its associated reference clocks (CLK0 and CLK1) are brought out to a connector pad that interfaces with Samtec BullsEye connectors used with the Samtec HDR-155805-01-BEYE cable assembly. Contact Samtec, Inc. [Ref 6], for information about this or other cable assemblies. Figure 3-12 shows the connector pad (A) and the connector pinout (B).

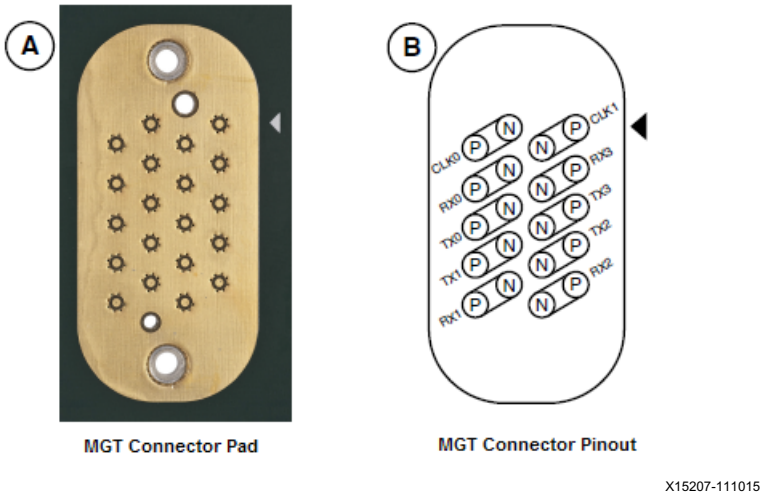


Figure 3-12: **MGT Connector Pad and Pinout**

The information for each GTY transceiver pin is shown in Table 3-14.

Table 3-14: **GTY Transceiver Pins**

U1 FPGA Pin	Net Name	Quad	Connector	Trace Length (mils)
BC46	124_RX0_N	124	J37	3477.529
BC45	124_RX0_P	124	J37	3477.391
BA46	124_RX1_N	124	J37	3067.521
BA45	124_RX1_P	124	J37	3067.805
AW46	124_RX2_N	124	J37	2493.979
AW45	124_RX2_P	124	J37	2494.19
AV44	124_RX3_N	124	J37	3018.544
AV43	124_RX3_P	124	J37	3019.123
BF43	124_TX0_N	124	J37	2556.328
BF42	124_TX0_P	124	J37	2556.96
BD43	124_TX1_N	124	J37	2363.323
BD42	124_TX1_P	124	J37	2362.718
BB43	124_TX2_N	124	J37	3014.59
BB42	124_TX2_P	124	J37	3015.086
AW41	124_TX3_N	124	J37	2748.806

Table 3-14: **GTY Transceiver Pins *(Cont'd)***

U1 FPGA Pin	Net Name	Quad	Connector	Trace Length (mils)
AW40	124_TX3_P	124	J37	2749.537
AU46	125_RX0_N	125	J155	3750.557
AU45	125_RX0_P	125	J155	3750.103
AT44	125_RX1_N	125	J155	2810.965
AT43	125_RX1_P	125	J155	2810.765
AR46	125_RX2_N	125	J155	3229.887
AR45	125_RX2_P	125	J155	3230.134
AP44	125_RX3_N	125	J155	3936.612
AP43	125_RX3_P	125	J155	3936.649
AU41	125_TX0_N	125	J155	3410.04
AU40	125_TX0_P	125	J155	3410.339
AT39	125_TX1_N	125	J155	3813.106
AT38	125_TX1_P	125	J155	3813.465
AR41	125_TX2_N	125	J155	2999.356
AR40	125_TX2_P	125	J155	3000.31
AP39	125_TX3_N	125	J155	3244.309
AP38	125_TX3_P	125	J155	3244.427
AN46	126_RX0_N	126	J38	4561.993
AN45	126_RX0_P	126	J38	4562.337
AM44	126_RX1_N	126	J38	2911.304
AM43	126_RX1_P	126	J38	2912.135
AL46	126_RX2_N	126	J38	3395.032
AL45	126_RX2_P	126	J38	3394.083
AK44	126_RX3_N	126	J38	3654.241
AK43	126_RX3_P	126	J38	3654.316
AN41	126_TX0_N	126	J38	4402.107
AN40	126_TX0_P	126	J38	4403.051
AM39	126_TX1_N	126	J38	4652.186
AM38	126_TX1_P	126	J38	4652.806
AL41	126_TX2_N	126	J38	3654.072
AL40	126_TX2_P	126	J38	3653.646
AK39	126_TX3_N	126	J38	3798.355
AK38	126_TX3_P	126	J38	3797.947
AJ46	127_RX0_N	127	J80	3978.188
AJ45	127_RX0_P	127	J80	3977.562

Table 3-14: **GTY Transceiver Pins *(Cont'd)***

U1 FPGA Pin	Net Name	Quad	Connector	Trace Length (mils)
AH44	127_RX1_N	127	J80	2362.889
AH43	127_RX1_P	127	J80	2363.814
AG46	127_RX2_N	127	J80	2753.07
AG45	127_RX2_P	127	J80	2752.326
AF44	127_RX3_N	127	J80	3151.59
AF43	127_RX3_P	127	J80	3150.669
AJ41	127_TX0_N	127	J80	3731.685
AJ40	127_TX0_P	127	J80	3732.499
AH39	127_TX1_N	127	J80	3884.662
AH38	127_TX1_P	127	J80	3885.13
AG41	127_TX2_N	127	J80	3011.906
AG40	127_TX2_P	127	J80	3011.524
AF39	127_TX3_N	127	J80	3213.572
AF38	127_TX3_P	127	J80	3212.71
AE46	128_RX0_N	128	J39	3318.099
AE45	128_RX0_P	128	J39	3318.535
AD44	128_RX1_N	128	J39	2091.1
AD43	128_RX1_P	128	J39	2092.008
AC46	128_RX2_N	128	J39	2134.481
AC45	128_RX2_P	128	J39	2133.745
AB44	128_RX3_N	128	J39	2893.257
AB43	128_RX3_P	128	J39	2893.03
AE41	128_TX0_N	128	J39	3129.947
AE40	128_TX0_P	128	J39	3130.745
AD39	128_TX1_N	128	J39	3551.521
AD38	128_TX1_P	128	J39	3551.324
AC41	128_TX2_N	128	J39	2497.894
AC40	128_TX2_P	128	J39	2497.382
AB39	128_TX3_N	128	J39	2753.954
AB38	128_TX3_P	128	J39	2753.46
AA46	129_RX0_N	129	J82	3187.684
AA45	129_RX0_P	129	J82	3188.041
Y44	129_RX1_N	129	J82	2165.289
Y43	129_RX1_P	129	J82	2166.051
W46	129_RX2_N	129	J82	2023.319

Table 3-14: **GTY Transceiver Pins *(Cont'd)***

U1 FPGA Pin	Net Name	Quad	Connector	Trace Length (mils)
W45	129_RX2_P	129	J82	2023.05
V44	129_RX3_N	129	J82	3046.191
V43	129_RX3_P	129	J82	3046.306
AA41	129_TX0_N	129	J82	3002.091
AA40	129_TX0_P	129	J82	3003.087
Y39	129_TX1_N	129	J82	3343.115
Y38	129_TX1_P	129	J82	3343.158
W41	129_TX2_N	129	J82	2342.961
W40	129_TX2_P	129	J82	2343.407
V39	129_TX3_N	129	J82	2587.768
V38	129_TX3_P	129	J82	2587.296
U46	130_RX0_N	130	J141	3321.572
U45	130_RX0_P	130	J141	3325.599
T44	130_RX1_N	130	J141	2555.132
T43	130_RX1_P	130	J141	2550.918
R46	130_RX2_N	130	J141	2199.702
R45	130_RX2_P	130	J141	2195.953
P44	130_RX3_N	130	J141	3405.875
P43	130_RX3_P	130	J141	3409.978
U41	130_TX0_N	130	J141	3153.762
U40	130_TX0_P	130	J141	3149.532
T39	130_TX1_N	130	J141	3439.944
T38	130_TX1_P	130	J141	3444.249
R41	130_TX2_N	130	J141	2570.09
R40	130_TX2_P	130	J141	2570.197
P39	130_TX3_N	130	J141	2786.723
P38	130_TX3_P	130	J141	2788.314
N46	131_RX0_N	131	J142	3483.317
N45	131_RX0_P	131	J142	3450.975
M44	131_RX1_N	131	J142	3131.583
M43	131_RX1_P	131	J142	3127.369
L46	131_RX2_N	131	J142	2636.221
L45	131_RX2_P	131	J142	2632.322
K44	131_RX3_N	131	J142	4093.547
K43	131_RX3_P	131	J142	4093.919

Table 3-14: **GTY Transceiver Pins *(Cont'd)***

U1 FPGA Pin	Net Name	Quad	Connector	Trace Length (mils)
N41	131_TX0_N	131	J142	3721.238
N40	131_TX0_P	131	J142	3717.005
M39	131_TX1_N	131	J142	3832.522
M38	131_TX1_P	131	J142	3832.749
L41	131_TX2_N	131	J142	2937.637
L40	131_TX2_P	131	J142	2939.024
J41	131_TX3_N	131	J142	3452.601
J40	131_TX3_P	131	J142	3448.136

Information for each GTH transceiver pin is shown in Table 3-15.

Table 3-15: **GTH Transceiver Pins**

U1 FPGA Pin	Net Name	Quad	Connector	Trace Length (mils)
BC1	224_RX0_N	224	J40	2684.206
BC2	224_RX0_P	224	J40	2687.895
BA1	224_RX1_N	224	J40	2268.14
BA2	224_RX1_P	224	J40	2263.637
AW3	224_RX2_N	224	J40	2373.569
AW4	224_RX2_P	224	J40	2371.689
AV1	224_RX3_N	224	J40	2920.877
AV2	224_RX3_P	224	J40	2922.567
BF4	224_TX0_N	224	J40	2428.943
BF5	224_TX0_P	224	J40	2433.409
BD4	224_TX1_N	224	J40	2468.88
BD5	224_TX1_P	224	J40	2464.789
BB4	224_TX2_N	224	J40	2500.467
BB5	224_TX2_P	224	J40	2503.893
AV6	224_TX3_N	224	J40	3016.944
AV7	224_TX3_P	224	J40	3017.689
AU3	225_RX0_N	225	J88	3181.169
AU4	225_RX0_P	225	J88	3177.517
AT1	225_RX1_N	225	J88	2570.369
AT2	225_RX1_P	225	J88	2567.203
AR3	225_RX2_N	225	J88	3343.092
AR4	225_RX2_P	225	J88	3341.453
AP1	225_RX3_N	225	J88	3319.371

Table 3-15: **GTH Transceiver Pins *(Cont'd)***

U1 FPGA Pin	Net Name	Quad	Connector	Trace Length (mils)
AP2	225_RX3_P	225	J88	3319.691
AU8	225_TX0_N	225	J88	3131.768
AU9	225_TX0_P	225	J88	3131.785
AT6	225_TX1_N	225	J88	3023.646
AT7	225_TX1_P	225	J88	3019.34
AR8	225_TX2_N	225	J88	3187.463
AR9	225_TX2_P	225	J88	3190.387
AP6	225_TX3_N	225	J88	3314.607
AP7	225_TX3_P	225	J88	3318.826
AN3	226_RX0_N	226	J89	3817.157
AN4	226_RX0_P	226	J89	3812.927
AM1	226_RX1_N	226	J89	2944.792
AM2	226_RX1_P	226	J89	2949.191
AL3	226_RX2_N	226	J89	2955.76
AL4	226_RX2_P	226	J89	2959.423
AK1	226_RX3_N	226	J89	3406.548
AK2	226_RX3_P	226	J89	3403.205
AN8	226_TX0_N	226	J89	3882.696
AN9	226_TX0_P	226	J89	3878.481
AM6	226_TX1_N	226	J89	3307.026
AM7	226_TX1_P	226	J89	3302.81
AL8	226_TX2_N	226	J89	3364.517
AL9	226_TX2_P	226	J89	3362.592
AK6	226_TX3_N	226	J89	3317.108
AK7	226_TX3_P	226	J89	3312.975
AJ3	227_RX0_N	227	J41	3227.755
AJ4	227_RX0_P	227	J41	3223.526
AH1	227_RX1_N	227	J41	2709.811
AH2	227_RX1_P	227	J41	2710.042
AG3	227_RX2_N	227	J41	2362.249
AG4	227_RX2_P	227	J41	2365.911
AF1	227_RX3_N	227	J41	3215.269
AF2	227_RX3_P	227	J41	3210.717
AJ8	227_TX0_N	227	J41	3241.15
AJ9	227_TX0_P	227	J41	3236.92

Table 3-15: **GTH Transceiver Pins *(Cont'd)***

U1 FPGA Pin	Net Name	Quad	Connector	Trace Length (mils)
AH6	227_TX1_N	227	J41	2917.227
AH7	227_TX1_P	227	J41	2913.018
AG8	227_TX2_N	227	J41	2738.559
AG9	227_TX2_P	227	J41	2734.645
AF6	227_TX3_N	227	J41	2825.741
AF7	227_TX3_P	227	J41	2822.504
AE3	228_RX0_N	228	J42	2654.909
AE4	228_RX0_P	228	J42	2650.701
AD1	228_RX1_N	228	J42	2445.73
AD2	228_RX1_P	228	J42	2442.263
AC3	228_RX2_N	228	J42	2149.729
AC4	228_RX2_P	228	J42	2153.392
AB1	228_RX3_N	228	J42	2722.54
AB2	228_RX3_P	228	J42	2718.416
AE8	228_TX0_N	228	J42	2695.046
AE9	228_TX0_P	228	J42	2690.838
AD6	228_TX1_N	228	J42	2548.702
AD7	228_TX1_P	228	J42	2544.475
AC8	228_TX2_N	228	J42	2521.896
AC9	228_TX2_P	228	J42	2519.007
AB6	228_TX3_N	228	J42	2650.866
AB7	228_TX3_P	228	J42	2646.679
AA3	229_RX0_N	229	J92	2529.004
AA4	229_RX0_P	229	J92	2524.797
Y1	229_RX1_N	229	J92	2091.731
Y2	229_RX1_P	229	J92	2095.424
W3	229_RX2_N	229	J92	2137.807
W4	229_RX2_P	229	J92	2141.003
V1	229_RX3_N	229	J92	2511.348
V2	229_RX3_P	229	J92	2508.271
AA8	229_TX0_N	229	J92	2571.308
AA9	229_TX0_P	229	J92	2567.078
Y6	229_TX1_N	229	J92	2368.077
Y7	229_TX1_P	229	J92	2363.848
W8	229_TX2_N	229	J92	2502.29

Table 3-15: **GTH Transceiver Pins *(Cont'd)***

U1 FPGA Pin	Net Name	Quad	Connector	Trace Length (mils)
W9	229_TX2_P	229	J92	2499.054
V6	229_TX3_N	229	J92	2554.534
V7	229_TX3_P	229	J92	2551.833
U3	230_RX0_N	230	J43	2781.446
U4	230_RX0_P	230	J43	2777.238
T1	230_RX1_N	230	J43	2224.642
T2	230_RX1_P	230	J43	2227.812
R3	230_RX2_N	230	J43	2398.967
R4	230_RX2_P	230	J43	2402.608
P1	230_RX3_N	230	J43	2923.14
P2	230_RX3_P	230	J43	2918.284
U8	230_TX0_N	230	J43	2836.832
U9	230_TX0_P	230	J43	2832.603
T6	230_TX1_N	230	J43	2578.719
T7	230_TX1_P	230	J43	2574.504
R8	230_TX2_N	230	J43	2851.124
R9	230_TX2_P	230	J43	2846.931
P6	230_TX3_N	230	J43	3003.18
P7	230_TX3_P	230	J43	3000.284
N3	231_RX0_N	231	J156	3378.75
N4	231_RX0_P	231	J156	3374.541
M1	231_RX1_N	231	J156	2790.609
M2	231_RX1_P	231	J156	2794.86
L3	231_RX2_N	231	J156	3071.766
L4	231_RX2_P	231	J156	3075.405
K1	231_RX3_N	231	J156	3460.674
K2	231_RX3_P	231	J156	3456.005
N8	231_TX0_N	231	J156	3456.058
N9	231_TX0_P	231	J156	3451.829
M6	231_TX1_N	231	J156	3099.879
M7	231_TX1_P	231	J156	3095.669
L8	231_TX2_N	231	J156	3466.734
L9	231_TX2_P	231	J156	3462.857
K6	231_TX3_N	231	J156	3619.237
K7	231_TX3_P	231	J156	3619.035

Information for each GTY transceiver clock input is shown in Table 3-16.

Table 3-16: **GTY Transceiver Reference Clock Inputs**

U1 FPGA Pin	Net Name	Quad	Connector
BA41	124_REFCLK0_N	124	J37
BA40	124_REFCLK0_P	124	J37
AY39	124_REFCLK1_N	124	J37
AY38	124_REFCLK1_P	124	J37
AV39	125_REFCLK0_N	125	J155
AV38	125_REFCLK0_P	125	J155
AU37	125_REFCLK1_N	125	J155
AU36	125_REFCLK1_P	125	J155
AR37	126_REFCLK0_N	126	J38
AR36	126_REFCLK0_P	126	J38
AN37	126_REFCLK1_N	126	J38
AN36	126_REFCLK1_P	126	J38
AL37	127_REFCLK0_N	127	J80
AL36	127_REFCLK0_P	127	J80
AJ37	127_REFCLK1_N	127	J80
AJ36	127_REFCLK1_P	127	J80
AG37	128_REFCLK0_N	128	J39
AG36	128_REFCLK0_P	128	J39
AE37	128_REFCLK1_N	128	J39
AE36	128_REFCLK1_P	128	J39
AC37	129_REFCLK0_N	129	J82
AC36	129_REFCLK0_P	129	J82
AA37	129_REFCLK1_N	129	J82
AA36	129_REFCLK1_P	129	J82
W37	130_REFCLK0_N	130	J141
W36	130_REFCLK0_P	130	J141
U37	130_REFCLK1_N	130	J141
U36	130_REFCLK1_P	130	J141
R37	131_REFCLK0_N	131	J142
R36	131_REFCLK0_P	131	J142
N37	131_REFCLK1_N	131	J142
N36	131_REFCLK1_P	131	J142

Information for each GTH transceiver clock input is shown in Table 3-17.

Table 3-17: **GTH Transceiver Reference Clock Inputs**

U1 FPGA Pin	Net Name	Quad	Connector
AW8	224_REFCLK0_N	224	J40
AW9	224_REFCLK0_P	224	J40
AV10	224_REFCLK1_N	224	J40
AV11	224_REFCLK1_P	224	J40
AT10	225_REFCLK0_N	225	J88
AT11	225_REFCLK0_P	225	J88
AP10	225_REFCLK1_N	225	J88
AP11	225_REFCLK1_P	225	J88
AM10	226_REFCLK0_N	226	J89
AM11	226_REFCLK0_P	226	J89
AK10	226_REFCLK1_N	226	J89
AK11	226_REFCLK1_P	226	J89
AH10	227_REFCLK0_N	227	J41
AH11	227_REFCLK0_P	227	J41
AF10	227_REFCLK1_N	227	J41
AF11	227_REFCLK1_P	227	J41
AD10	228_REFCLK0_N	228	J42
AD11	228_REFCLK0_P	228	J42
AB10	228_REFCLK1_N	228	J42
AB11	228_REFCLK1_P	228	J42
Y11	229_REFCLK0_P	229	J92
Y10	229_REFCLK0_N	229	J92
V10	229_REFCLK1_N	229	J92
V11	229_REFCLK1_P	229	J92
T10	230_REFCLK0_N	230	J43
T11	230_REFCLK0_P	230	J43
P10	230_REFCLK1_N	230	J43
P11	230_REFCLK1_P	230	J43
M10	231_REFCLK0_N	231	J156
M11	231_REFCLK0_P	231	J156
K10	231_REFCLK1_N	231	J156
K11	231_REFCLK1_P	231	J156

FPGA Mezzanine Card HPC Interface

Callout 30, 31, and 32, Figure 2-1

The VCU1287 board features two high pin count (HPC) connectors as defined by the VITA 57.1 FPGA Mezzanine card (FMC) specification. The FMC HPC connector is a 10 x 40 position socket. See Appendix B, VITA 57.1 FMC Connector Pinouts for a cross-reference of signal names to pin coordinates.

The FMC1 HPC connector JA2 provides connectivity for:

- 75 differential user defined pairs:
  - 34 LA pairs
  - 24 HA pairs
  - 17 HB pairs
- 4 differential clocks

The FMC2 HPC connector JA3 provides connectivity for:

- 20 differential user defined pairs:
  - 20 LA pairs
- 2 differential clocks

The FMC3 HPC connector JA4 provides connectivity for:

- 80 differential user defined pairs:
  - 34 LA pairs
  - 24 HA pairs
  - 22 HB pairs
- 4 differential clocks

IMPORTANT: *The V_{ADJ} voltage on the FMC1 and FMC3 HPC connectors tracks VCCO_HP. While the V_{ADJ} voltage on the FMC2 HPC connectors tracks VCCO_HR.*

The FMC HPC connectors on the VCU1287 board are identified as FMC1 at JA2, FMC2 at JA3, and FMC3 at JA4. The connections for each of these connectors are listed in Table 3-18, Table 3-19 and Table 3-20, respectively.

Table 3-18: **VITA 57.1 FMC1 HPC Connections at JA2**

U1 FPGA Pin	Net Name	FMC Pin
AF32	FMC1_CLK0_M2C_P	H4
AF33	FMC1_CLK0_M2C_N	H5
AG31	FMC1_CLK1_M2C_P	G2
AG32	FMC1_CLK1_M2C_N	G3
N32	FMC1_CLK2_BIDIR_P	K4
N33	FMC1_CLK2_BIDIR_N	K5
P31	FMC1_CLK3_BIDIR_P	J2
N31	FMC1_CLK3_BIDIR_N	J3
E36	FMC1_HA00_CC_P	F4
D36	FMC1_HA00_CC_N	F5
C36	FMC1_HA01_CC_P	E2
C37	FMC1_HA01_CC_N	E3
D31	FMC1_HA02P	K7
C31	FMC1_HA02N	K8
C32	FMC1_HA03P	J6
B32	FMC1_HA03N	J7
A32	FMC1_HA04P	F7
A33	FMC1_HA04N	F8
D33	FMC1_HA05P	E6
C33	FMC1_HA05N	E7
D34	FMC1_HA06P	K10
C34	FMC1_HA06N	K11
B34	FMC1_HA07P	J9
A34	FMC1_HA07N	J10
E35	FMC1_HA08P	F10
D35	FMC1_HA08N	F11
B35	FMC1_HA09P	E9
A35	FMC1_HA09N	E10
B36	FMC1_HA10P	K13
B37	FMC1_HA10N	K14
A37	FMC1_HA11P	J12
A38	FMC1_HA11N	J13

Table 3-18: **VITA 57.1 FMC1 HPC Connections at JA2 *(Cont'd)***

U1 FPGA Pin	Net Name	FMC Pin
B39	FMC1_HA12P	F13
A39	FMC1_HA12N	F14
B40	FMC1_HA13P	E12
A40	FMC1_HA13N	E13
E39	FMC1_HA14P	J15
D39	FMC1_HA14N	J16
E40	FMC1_HA15P	F16
D40	FMC1_HA15N	F17
F34	FMC1_HA16P	E15
F35	FMC1_HA16N	E16
C38	FMC1_HA17_CC_P	K16
C39	FMC1_HA17_CC_N	K17
E38	FMC1_HA18P	J18
D38	FMC1_HA18N	J19
H34	FMC1_HA19P	F19
G34	FMC1_HA19N	F20
H36	FMC1_HA20P	E18
G36	FMC1_HA20N	E19
J35	FMC1_HA21P	K19
J36	FMC1_HA21N	K20
G37	FMC1_HA22P	J21
F37	FMC1_HA22N	J22
H37	FMC1_HA23P	K22
H38	FMC1_HA23N	K23
J26	FMC1_HB00_CC_P	K25
H26	FMC1_HB00_CC_N	K26
J28	FMC1_HB01_CC_P	J24
J29	FMC1_HB01_CC_N	J25
E28	FMC1_HB02P	F22
D28	FMC1_HB02N	F23
F27	FMC1_HB03P	E21
E27	FMC1_HB03N	E22
F28	FMC1_HB04P	F25
F29	FMC1_HB04N	F26
H29	FMC1_HB05P	E24

Table 3-18: **VITA 57.1 FMC1 HPC Connections at JA2 *(Cont'd)***

U1 FPGA Pin	Net Name	FMC Pin
G29	FMC1_HB05N	E25
H27	FMC1_HB06P	K28
H28	FMC1_HB06N	K29
K26	FMC1_HB07P	J27
K27	FMC1_HB07N	J28
M27	FMC1_HB08P	F28
L27	FMC1_HB08N	F29
L28	FMC1_HB09P	E27
K28	FMC1_HB09N	E28
M29	FMC1_HB10P	K31
L29	FMC1_HB10N	K32
P26	FMC1_HB11P	J30
N26	FMC1_HB11N	J31
P28	FMC1_HB12P	F31
N28	FMC1_HB12N	F32
P29	FMC1_HB13P	E30
N29	FMC1_HB13N	E31
T26	FMC1_HB14P	K34
R26	FMC1_HB14N	K35
T27	FMC1_HB15P	J33
R27	FMC1_HB15N	J34
T28	FMC1_HB16P	F34
R28	FMC1_HB16N	F35
AD33	FMC1_LA00_CC_P	G6
AE33	FMC1_LA00_CC_N	G7
AE31	FMC1_LA01_CC_P	D8
AE32	FMC1_LA01_CC_N	D9
W33	FMC1_LA02P	H7
W34	FMC1_LA02N	H8
Y32	FMC1_LA03P	G9
Y33	FMC1_LA03N	G10
W31	FMC1_LA04P	H10
Y31	FMC1_LA04N	H11
W30	FMC1_LA05P	D11
Y30	FMC1_LA05N	D12

Table 3-18: **VITA 57.1 FMC1 HPC Connections at JA2 *(Cont'd)***

U1 FPGA Pin	Net Name	FMC Pin
AA34	FMC1_LA06P	C10
AB34	FMC1_LA06N	C11
AA32	FMC1_LA07P	H13
AA33	FMC1_LA07N	H14
AC34	FMC1_LA08P	G12
AD34	FMC1_LA08N	G13
AC32	FMC1_LA09P	D14
AC33	FMC1_LA09N	D15
AC31	FMC1_LA10P	C14
AD31	FMC1_LA10N	C15
AE30	FMC1_LA11P	H16
AF30	FMC1_LA11N	H17
AH31	FMC1_LA12P	G15
AH32	FMC1_LA12N	G16
AF34	FMC1_LA13P	D17
AG34	FMC1_LA13N	D18
AH33	FMC1_LA14P	C18
AJ33	FMC1_LA14N	C19
AH34	FMC1_LA15P	H19
AJ34	FMC1_LA15N	H20
AJ31	FMC1_LA16P	G18
AK31	FMC1_LA16N	G19
L32	FMC1_LA17_CC_P	D20
K32	FMC1_LA17_CC_N	D21
M31	FMC1_LA18_CC_P	C22
M32	FMC1_LA18_CC_N	C23
F33	FMC1_LA19P	H22
E33	FMC1_LA19N	H23
F32	FMC1_LA20P	G21
E32	FMC1_LA20N	G22
H32	FMC1_LA21P	H25
G32	FMC1_LA21N	H26
H31	FMC1_LA22P	G24
G31	FMC1_LA22N	G25
G30	FMC1_LA23P	D23

Table 3-18: **VITA 57.1 FMC1 HPC Connections at JA2 *(Cont'd)***

U1 FPGA Pin	Net Name	FMC Pin
F30	FMC1_LA23N	D24
L33	FMC1_LA24P	H28
K33	FMC1_LA24N	H29
K31	FMC1_LA25P	G27
J31	FMC1_LA25N	G28
K30	FMC1_LA26P	D26
J30	FMC1_LA26N	D27
M30	FMC1_LA27P	C26
L30	FMC1_LA27N	C27
M34	FMC1_LA28P	H31
L34	FMC1_LA28N	H32
P34	FMC1_LA29P	G30
N34	FMC1_LA29N	G31
R31	FMC1_LA30P	H34
R32	FMC1_LA30N	H35
R30	FMC1_LA31P	G33
P30	FMC1_LA31N	G34
U30	FMC1_LA32P	H37
T30	FMC1_LA32N	H38
V31	FMC1_LA33P	G36
U31	FMC1_LA33N	G37
AB32	FMC1_PRSNT_M2C_L	H2

Table 3-19: **VITA 57.1 FMC2 HPC Connections at JA3**

U1 FPGA Pin	Net Name	FMC Pin
AV26	FMC2_CLK0_M2C_P	H4
AW26	FMC2_CLK0_M2C_N	H5
AW28	FMC2_CLK1_M2C_P	G2
AY28	FMC2_CLK1_M2C_N	G3
AY26	FMC2_LA00_CC_P	G6
AY27	FMC2_LA00_CC_N	G7
AW25	FMC2_LA01_CC_P	D8
AY25	FMC2_LA01_CC_N	D9
AL27	FMC2_LA02P	H7
AL28	FMC2_LA02N	H8

Table 3-19: **VITA 57.1 FMC2 HPC Connections at JA3 *(Cont'd)***

U1 FPGA Pin	Net Name	FMC Pin
AM27	FMC2_LA03P	G9
AN27	FMC2_LA03N	G10
AN28	FMC2_LA04P	H10
AP28	FMC2_LA04N	H11
AP25	FMC2_LA05P	D11
AP26	FMC2_LA05N	D12
AR28	FMC2_LA06P	C10
AT28	FMC2_LA06N	C11
AR27	FMC2_LA07P	H13
AT27	FMC2_LA07N	H14
AR25	FMC2_LA08P	G12
AT25	FMC2_LA08N	G13
AU26	FMC2_LA09P	D14
AU27	FMC2_LA09N	D15
AV27	FMC2_LA10P	C14
AV28	FMC2_LA10N	C15
BA27	FMC2_LA11P	H16
BA28	FMC2_LA11N	H17
BB26	FMC2_LA12P	G15
BB27	FMC2_LA12N	G16
BA25	FMC2_LA13P	D17
BB25	FMC2_LA13N	D18
BC26	FMC2_LA14P	C18
BC27	FMC2_LA14N	C19
BE25	FMC2_LA15P	H19
BF25	FMC2_LA15N	H20
BD26	FMC2_LA16P	G18
BE26	FMC2_LA16N	G19
BD28	FMC2_LA17_CC_P	D20
BE28	FMC2_LA17_CC_N	D21
BE27	FMC2_LA18_CC_P	C22
BF27	FMC2_LA18_CC_N	C23
BF28	FMC2_LA19P	H22
BF29	FMC2_LA19N	H23
AR26	FMC2_PRSNT_M2C_L	H2

Table 3-20: **VITA 57.1 FMC3 HPC Connections at JA4**

U1 FPGA Pin	Net Name	FMC Pin
J16	FMC3_CLK0_M2C_P	H4
J15	FMC3_CLK0_M2C_N	H5
J14	FMC3_CLK1_M2C_P	G2
H14	FMC3_CLK1_M2C_N	G3
J24	FMC3_CLK2_BIDIR_P	K4
H24	FMC3_CLK2_BIDIR_N	K5
J23	FMC3_CLK3_BIDIR_P	J2
H23	FMC3_CLK3_BIDIR_N	J3
G20	FMC3_HA00_CC_P	F4
G19	FMC3_HA00_CC_N	F5
H19	FMC3_HA01_CC_P	E2
H18	FMC3_HA01_CC_N	E3
B20	FMC3_HA02P	K7
A20	FMC3_HA02N	K8
B19	FMC3_HA03P	J6
A19	FMC3_HA03N	J7
D18	FMC3_HA04P	F7
C18	FMC3_HA04N	F8
C21	FMC3_HA05P	E6
B21	FMC3_HA05N	E7
D21	FMC3_HA06P	K10
D20	FMC3_HA06N	K11
D19	FMC3_HA07P	J9
C19	FMC3_HA07N	J10
F18	FMC3_HA08P	F10
F17	FMC3_HA08N	F11
E21	FMC3_HA09P	E9
E20	FMC3_HA09N	E10
E18	FMC3_HA10P	K13
E17	FMC3_HA10N	K14
F20	FMC3_HA11P	J12
F19	FMC3_HA11N	J13
K18	FMC3_HA12P	F13
J18	FMC3_HA12N	F14
J21	FMC3_HA13P	E12

Table 3-20: **VITA 57.1 FMC3 HPC Connections at JA4 *(Cont'd)***

U1 FPGA Pin	Net Name	FMC Pin
H21	FMC3_HA13N	E13
L20	FMC3_HA14P	J15
K20	FMC3_HA14N	J16
L19	FMC3_HA15P	F16
L18	FMC3_HA15N	F17
L17	FMC3_HA16P	E15
K17	FMC3_HA16N	E16
J20	FMC3_HA17_CC_P	K16
J19	FMC3_HA17_CC_N	K17
N21	FMC3_HA18P	J18
M21	FMC3_HA18N	J19
R20	FMC3_HA19P	F19
P20	FMC3_HA19N	F20
P19	FMC3_HA20P	E18
N19	FMC3_HA20N	E19
M20	FMC3_HA21P	K19
M19	FMC3_HA21N	K20
P18	FMC3_HA22P	J21
N18	FMC3_HA22N	J22
N17	FMC3_HA23P	K22
M17	FMC3_HA23N	K23
AY35	FMC3_HB00_CC_P	K25
AY36	FMC3_HB00_CC_N	K26
BA34	FMC3_HB01_CC_P	J24
BB34	FMC3_HB01_CC_N	J25
AL34	FMC3_HB02P	F22
AM34	FMC3_HB02N	F23
AL32	FMC3_HB03P	E21
AM32	FMC3_HB03N	E22
AN32	FMC3_HB04P	F25
AN33	FMC3_HB04N	F26
AN34	FMC3_HB05P	E24
AP34	FMC3_HB05N	E25
AP33	FMC3_HB06P	K28
AR33	FMC3_HB06N	K29

Table 3-20: **VITA 57.1 FMC3 HPC Connections at JA4 *(Cont'd)***

U1 FPGA Pin	Net Name	FMC Pin
AT33	FMC3_HB07P	J27
AT34	FMC3_HB07N	J28
AV33	FMC3_HB08P	F28
AW33	FMC3_HB08N	F29
AV34	FMC3_HB09P	E27
AW34	FMC3_HB09N	E28
AW35	FMC3_HB10P	K31
AW36	FMC3_HB10N	K32
AY33	FMC3_HB11P	J30
BA33	FMC3_HB11N	J31
BB36	FMC3_HB12P	F31
BC36	FMC3_HB12N	F32
BB37	FMC3_HB13P	E30
BC37	FMC3_HB13N	E31
BD36	FMC3_HB14P	K34
BE36	FMC3_HB14N	K35
BD35	FMC3_HB15P	J33
BE35	FMC3_HB15N	J34
BC34	FMC3_HB16P	F34
BD34	FMC3_HB16N	F35
BA35	FMC3_HB17_CC_P	K37
BB35	FMC3_HB17_CC_N	K38
BB38	FMC3_HB18P	J36
BC38	FMC3_HB18N	J37
BC39	FMC3_HB19P	E33
BD39	FMC3_HB19N	E34
BD40	FMC3_HB20P	F37
BE40	FMC3_HB20N	F38
BE37	FMC3_HB21P	E36
BF37	FMC3_HB21N	E37
G15	FMC3_LA00_CC_P	G6
F15	FMC3_LA00_CC_N	G7
G14	FMC3_LA01_CC_P	D8
F14	FMC3_LA01_CC_N	D9
B17	FMC3_LA02P	H7

Table 3-20: **VITA 57.1 FMC3 HPC Connections at JA4 *(Cont'd)***

U1 FPGA Pin	Net Name	FMC Pin
A17	FMC3_LA02N	H8
C16	FMC3_LA03P	G9
B16	FMC3_LA03N	G10
B15	FMC3_LA04P	H10
A15	FMC3_LA04N	H11
A14	FMC3_LA05P	D11
A13	FMC3_LA05N	D12
C14	FMC3_LA06P	C10
B14	FMC3_LA06N	C11
D13	FMC3_LA07P	H13
C13	FMC3_LA07N	H14
E16	FMC3_LA08P	G12
D16	FMC3_LA08N	G13
E15	FMC3_LA09P	D14
D15	FMC3_LA09N	D15
G17	FMC3_LA10P	C14
G16	FMC3_LA10N	C15
F13	FMC3_LA11P	H16
E13	FMC3_LA11N	H17
H17	FMC3_LA12P	G15
H16	FMC3_LA12N	G16
J13	FMC3_LA13P	D17
H13	FMC3_LA13N	D18
K16	FMC3_LA14P	C18
K15	FMC3_LA14N	C19
N16	FMC3_LA15P	H19
M16	FMC3_LA15N	H20
M14	FMC3_LA16P	G18
L14	FMC3_LA16N	G19
F24	FMC3_LA17_CC_P	D20
F23	FMC3_LA17_CC_N	D21
G25	FMC3_LA18_CC_P	C22
G24	FMC3_LA18_CC_N	C23
B25	FMC3_LA19P	H22
A25	FMC3_LA19N	H23

Table 3-20: **VITA 57.1 FMC3 HPC Connections at JA4 *(Cont'd)***

U1 FPGA Pin	Net Name	FMC Pin
B24	FMC3_LA20P	G21
A24	FMC3_LA20N	G22
A23	FMC3_LA21P	H25
A22	FMC3_LA21N	H26
C26	FMC3_LA22P	G24
B26	FMC3_LA22N	G25
C24	FMC3_LA23P	D23
C23	FMC3_LA23N	D24
C22	FMC3_LA24P	H28
B22	FMC3_LA24N	H29
E25	FMC3_LA25P	G27
D25	FMC3_LA25N	G28
D24	FMC3_LA26P	D26
D23	FMC3_LA26N	D27
E23	FMC3_LA27P	C26
E22	FMC3_LA27N	C27
G22	FMC3_LA28P	H31
F22	FMC3_LA28N	H32
K25	FMC3_LA29P	G30
J25	FMC3_LA29N	G31
L23	FMC3_LA30P	H34
K23	FMC3_LA30N	H35
L22	FMC3_LA31P	G33
K22	FMC3_LA31N	G34
L25	FMC3_LA32P	H37
L24	FMC3_LA32N	H38
R25	FMC3_LA33P	G36
P25	FMC3_LA33N	G37
C17	FMC3_PRSNT_M2C_L	H2

System Monitor

The SYSMON monitors the physical environment using on-chip temperature and supply sensors, up to 17 external analog inputs, and an integrated analog-to-digital converter (ADC). The SYSMON is powered using the on-chip reference (VREF) shown in Figure 3-13. More information about the system monitor is available in the *UltraScale Architecture System Monitor User Guide* (UG580) [Ref 2].

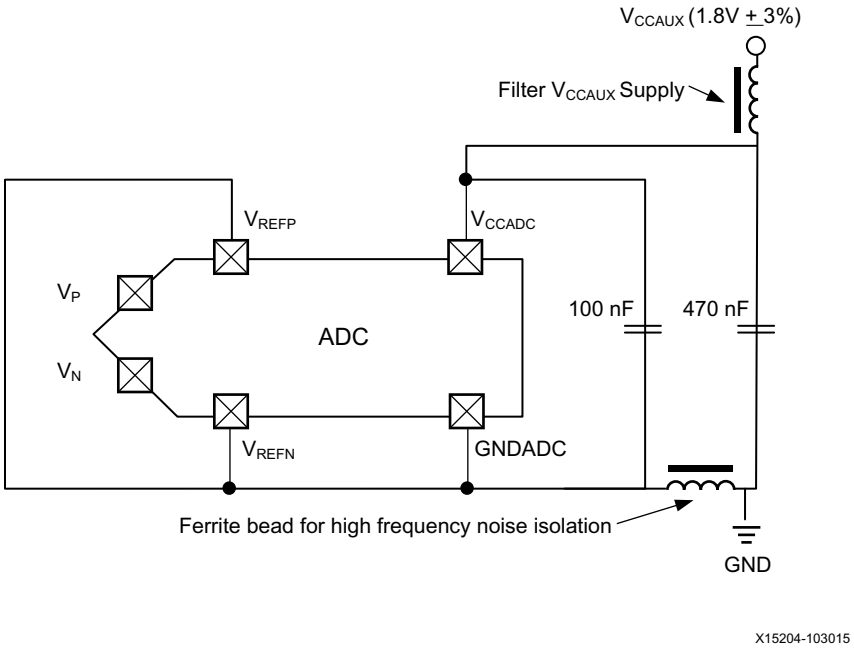


Figure 3-13: **SYSMON On-Chip Reference**

I2C Bus Management

The I2C bus is routed through U22, an 8-channel I2C-bus multiplexer (NXP Semiconductor TCA9548). The I2C IDcode for the PCA9548 device is 0x75. The multiplexer provides I2C/PMBus communication between the bus master (system controller or FPGA) and six sub-systems:

- Onboard regulators and power monitoring
- SuperClock-2 module
- System controller EEPROM
- FMC1 connector
- FMC2 connector
- FMC3 connector

Table 3-21 shows the I2C channel assignments.

Table 3-21: **I2C Channel Assignments**

U22 Channel	I2C Component
0	System PMBus
1	SuperClock-2 module
2	System controller EEPROM
3	FMC1
4	FMC2
5	FMC3

The upstream port of the TCA9548 multiplexer connects to PCA9306 (U46, U53, U55, and U58) dual bidirectional I2C and SMBus voltage-level translator and bus repeaters, with an enable (EN) signal (see Figure 3-14). J121 and J125 are used to enable or disable the bus repeaters and isolate the system controller or the UltraScale FPGA I2C bus.

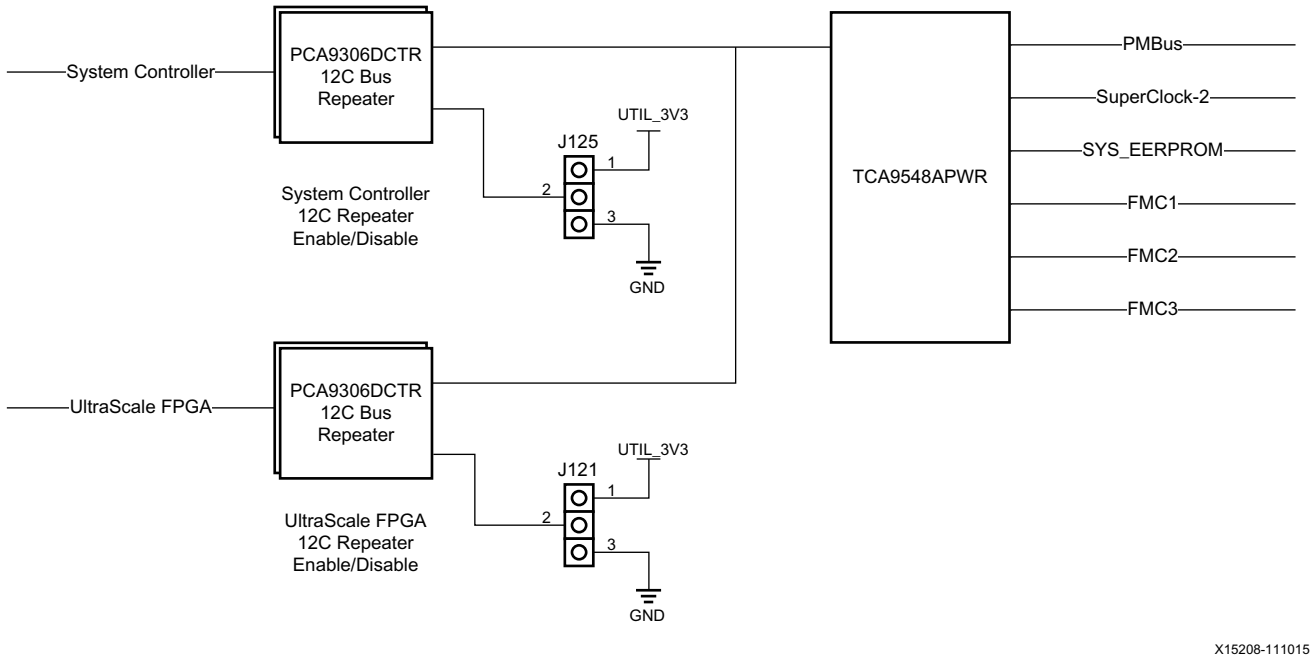


Figure 3-14: **I2C Bus Multiplexer and Upstream Repeater**

Default Jumper Settings

Introduction

Table A-1 lists the jumpers that must be installed on the VCU1287 board for proper operation. These jumpers must be installed except where specifically noted in this user guide.

Note: Any jumper not listed in Table A-1 should be left open for normal operation.

Table A-1: **Default Jumper Settings**

Reference Designator	Name	Board Location	Jumper/Dip-switch Position	Comments
SW2.1	VCCINT	Upper Left	OFF	
SW2.2	VCCBRAM	Upper Left	OFF	
SW2.3	VCCAUX	Upper Left	OFF	
SW2.4	VCCO_HP	Upper Left	OFF	
SW2.5	VCCO_HR	Upper Left	OFF	
J87	MGT PMBUS CTRL	Upper Left	GND (2-3)	
J8	MGT PMBUS ISO	Center Right	Installed	
J121	DUT I2C	Upper Right	GND (2-3) DIS	Disabled
J125	SYS I2C	Upper Right	PWR (1-2) EN	Enabled
J24	VTT_HP SOURCE	Upper Center	GND (1-2)	Red 20A jumper
J66	VTT_HR SOURCE	Lower Left	GND (1-2)	Red 20A jumper
J11	AFX	Upper-Middle	Installed	DIFF CLK 1 P
J12	AFX	Upper-Middle	Installed	DIFF CLK 1 N
J13	AFX	Upper-Middle	Installed	DIFF CLK 2 P
J14	AFX	Upper-Middle	Installed	DIFF CLK 2 N
J160	UTIL_3V3_EN	Center-Right	EN (1-2)	
SW13.1	Enable	Upper Right	OFF	Enable SD card configuration mode
SW13.2	ADDR0	Upper Right	OFF	
SW13.3	ADDR1	Upper Right	OFF	

Table A-1: **Default Jumper Settings *(Cont'd)***

Reference Designator	Name	Board Location	Jumper/Dip-switch Position	Comments
SW13.4	ADDR2	Upper Right	OFF	
SW13.5	ADDR3	Upper Right	OFF	

VITA 57.1 FMC Connector Pinouts

Introduction

Figure B-1 provides a cross-reference of signal names to pin coordinates for the VITA 57.1 FMC HPC connector.

	K	J	H	G	F	E	D	C	B	A
1	VREF_B_M2C	GND	VREF_A_M2C	GND	PG_M2C	GND	PG_C2M	GND	RES1	GND
2	GND	CLK3_M2C_P	PRSNT_M2C_L	CLK1_M2C_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	DP1_M2C_P
3	GND	CLK3_M2C_N	GND	CLK1_M2C_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	DP1_M2C_N
4	CLK2_M2C_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	GBTCLK0_M2C_P	GND	DP9_M2C_P	GND
5	CLK2_M2C_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	GBTCLK0_M2C_N	GND	DP9_M2C_N	GND
6	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P
7	HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	DP0_M2C_N	GND	DP2_M2C_N
8	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	DP8_M2C_P	GND
9	GND	HA07_P	GND	LA03_P	GND	HA09_P	LA01_N_CC	GND	DP8_M2C_N	GND
10	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	DP3_M2C_P
11	HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA06_N	GND	DP3_M2C_N
12	GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND
13	HA10_P	HA11_N	LA07_P	LA08_N	HA12_P	HA13_N	GND	GND	DP7_M2C_N	GND
14	HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P
15	GND	HA14_P	GND	LA12_P	GND	HA16_P	LA09_N	LA10_N	GND	DP4_M2C_N
16	HA17_P_CC	HA14_N	LA11_P	LA12_N	HA15_P	HA16_N	GND	GND	DP6_M2C_P	GND
17	HA17_N_CC	GND	LA11_N	GND	HA15_N	GND	LA13_P	GND	DP6_M2C_N	GND
18	GND	HA18_P	GND	LA16_P	GND	HA20_P	LA13_N	LA14_P	GND	DP5_M2C_P
19	HA21_P	HA18_N	LA15_P	LA16_N	HA19_P	HA20_N	GND	LA14_N	GND	DP5_M2C_N
20	HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND
21	GND	HA22_P	GND	LA20_P	GND	HB03_P	LA17_N_CC	GND	GBTCLK1_M2C_N	GND
22	HA23_P	HA22_N	LA19_P	LA20_N	HB02_P	HB03_N	GND	LA18_P_CC	GND	DP1_C2M_P
23	HA23_N	GND	LA19_N	GND	HB02_N	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N
24	GND	HB01_P	GND	LA22_P	GND	HB05_P	LA23_N	GND	DP9_C2M_P	GND
25	HB00_P_CC	HB01_N	LA21_P	LA22_N	HB04_P	HB05_N	GND	GND	DP9_C2M_N	GND
26	HB00_N_CC	GND	LA21_N	GND	HB04_N	GND	LA26_P	LA27_P	GND	DP2_C2M_P
27	GND	HB07_P	GND	LA25_P	GND	HB09_P	LA26_N	LA27_N	GND	DP2_C2M_N
28	HB06_P_CC	HB07_N	LA24_P	LA25_N	HB08_P	HB09_N	GND	GND	DP8_C2M_P	GND
29	HB06_N_CC	GND	LA24_N	GND	HB08_N	GND	TCK	GND	DP8_C2M_N	GND
30	GND	HB11_P	GND	LA29_P	GND	HB13_P	TDI	SCL	GND	DP3_C2M_P
31	HB10_P	HB11_N	LA28_P	LA29_N	HB12_P	HB13_N	TDO	SDA	GND	DP3_C2M_N
32	HB10_N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_P	GND
33	GND	HB15_P	GND	LA31_P	GND	HB19_P	TMS	GND	DP7_C2M_N	GND
34	HB14_P	HB15_N	LA30_P	LA31_N	HB16_P	HB19_N	TRST_L	GA0	GND	DP4_C2M_P
35	HB14_N	GND	LA30_N	GND	HB16_N	GND	GA1	12P0V	GND	DP4_C2M_N
36	GND	HB18_P	GND	LA33_P	GND	HB21_P	3P3V	GND	DP6_C2M_P	GND
37	HB17_P_CC	HB18_N	LA32_P	LA33_N	HB20_P	HB21_N	GND	12P0V	DP6_C2M_N	GND
38	HB17_N_CC	GND	LA32_N	GND	HB20_N	GND	3P3V	GND	GND	DP5_C2M_P
39	GND	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N
40	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND

X15206-111115

Figure B-1: **FMC HPC Connector Pinout**

Master Constraints File Listing

Introduction

The VCU1287 board master Xilinx design constraints (XDC) file template provides for designs targeting the VCU1287 UltraScale FPGA GTH and GTY Transceiver Characterization Board. Net names in the listed constraints correlate with net names on the VCU1287 board schematic. Identify the appropriate pins and replace the net names with net names in the user RTL. See the *Vivado Design Suite User Guide: Using Constraints* (UG903) [Ref 3] for more information.

IMPORTANT: *See the Xilinx Virtex UltraScale FPGA VCU1287 Characterization Kit website for the latest XDC file.*

VCU1287 Board XDC Listing

```
#FMC1
set_property PACKAGE_PIN AB32     [get_ports "FMC1_PRSNT_M2C_L"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_PRSNT_M2C_L"]
set_property PACKAGE_PIN AF32     [get_ports "FMC1_CLK0_M2C_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_CLK0_M2C_P"]
set_property PACKAGE_PIN AF33     [get_ports "FMC1_CLK0_M2C_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_CLK0_M2C_N"]
set_property PACKAGE_PIN AG31     [get_ports "FMC1_CLK1_M2C_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_CLK1_M2C_P"]
set_property PACKAGE_PIN AG32     [get_ports "FMC1_CLK1_M2C_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_CLK1_M2C_N"]
set_property PACKAGE_PIN N32      [get_ports "FMC1_CLK2_BIDIR_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_CLK2_BIDIR_P"]
set_property PACKAGE_PIN N33      [get_ports "FMC1_CLK2_BIDIR_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_CLK2_BIDIR_N"]
set_property PACKAGE_PIN P31      [get_ports "FMC1_CLK3_BIDIR_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_CLK3_BIDIR_P"]
set_property PACKAGE_PIN N31      [get_ports "FMC1_CLK3_BIDIR_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_CLK3_BIDIR_N"]

#FMC1 LA
set_property PACKAGE_PIN AD33     [get_ports "FMC1_LA00_CC_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA00_CC_P"]
set_property PACKAGE_PIN AE33     [get_ports "FMC1_LA00_CC_N"]
```

```
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA00_CC_N"]
set_property PACKAGE_PIN AE31     [get_ports "FMC1_LA01_CC_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA01_CC_P"]
set_property PACKAGE_PIN AE32     [get_ports "FMC1_LA01_CC_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA01_CC_N"]
set_property PACKAGE_PIN W33      [get_ports "FMC1_LA02P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA02P"]
set_property PACKAGE_PIN W34      [get_ports "FMC1_LA02N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA02N"]
set_property PACKAGE_PIN Y32      [get_ports "FMC1_LA03P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA03P"]
set_property PACKAGE_PIN Y33      [get_ports "FMC1_LA03N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA03N"]
set_property PACKAGE_PIN W31      [get_ports "FMC1_LA04P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA04P"]
set_property PACKAGE_PIN Y31      [get_ports "FMC1_LA04N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA04N"]
set_property PACKAGE_PIN W30      [get_ports "FMC1_LA05P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA05P"]
set_property PACKAGE_PIN Y30      [get_ports "FMC1_LA05N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA05N"]
set_property PACKAGE_PIN AA34     [get_ports "FMC1_LA06P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA06P"]
set_property PACKAGE_PIN AB34     [get_ports "FMC1_LA06N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA06N"]
set_property PACKAGE_PIN AA32     [get_ports "FMC1_LA07P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA07P"]
set_property PACKAGE_PIN AA33     [get_ports "FMC1_LA07N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA07N"]
set_property PACKAGE_PIN AC34     [get_ports "FMC1_LA08P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA08P"]
set_property PACKAGE_PIN AD34     [get_ports "FMC1_LA08N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA08N"]
set_property PACKAGE_PIN AC32     [get_ports "FMC1_LA09P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA09P"]
set_property PACKAGE_PIN AC33     [get_ports "FMC1_LA09N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA09N"]
set_property PACKAGE_PIN AC31     [get_ports "FMC1_LA10P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA10P"]
set_property PACKAGE_PIN AD31     [get_ports "FMC1_LA10N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA10N"]
set_property PACKAGE_PIN AE30     [get_ports "FMC1_LA11P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA11P"]
set_property PACKAGE_PIN AF30     [get_ports "FMC1_LA11N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA11N"]
set_property PACKAGE_PIN AH31     [get_ports "FMC1_LA12P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA12P"]
set_property PACKAGE_PIN AH32     [get_ports "FMC1_LA12N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA12N"]
set_property PACKAGE_PIN AF34     [get_ports "FMC1_LA13P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA13P"]
set_property PACKAGE_PIN AG34     [get_ports "FMC1_LA13N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA13N"]
set_property PACKAGE_PIN AH33     [get_ports "FMC1_LA14P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA14P"]
set_property PACKAGE_PIN AJ33     [get_ports "FMC1_LA14N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA14N"]
set_property PACKAGE_PIN AH34     [get_ports "FMC1_LA15P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA15P"]
```

```
set_property PACKAGE_PIN AJ34     [get_ports "FMC1_LA15N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA15N"]
set_property PACKAGE_PIN AJ31     [get_ports "FMC1_LA16P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA16P"]
set_property PACKAGE_PIN AK31     [get_ports "FMC1_LA16N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA16N"]
set_property PACKAGE_PIN F33      [get_ports "FMC1_LA19P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA19P"]
set_property PACKAGE_PIN E33      [get_ports "FMC1_LA19N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA19N"]
set_property PACKAGE_PIN F32      [get_ports "FMC1_LA20P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA20P"]
set_property PACKAGE_PIN E32      [get_ports "FMC1_LA20N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA20N"]
set_property PACKAGE_PIN H32      [get_ports "FMC1_LA21P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA21P"]
set_property PACKAGE_PIN G32      [get_ports "FMC1_LA21N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA21N"]
set_property PACKAGE_PIN H31      [get_ports "FMC1_LA22P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA22P"]
set_property PACKAGE_PIN G31      [get_ports "FMC1_LA22N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA22N"]
set_property PACKAGE_PIN G30      [get_ports "FMC1_LA23P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA23P"]
set_property PACKAGE_PIN F30      [get_ports "FMC1_LA23N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA23N"]
set_property PACKAGE_PIN L33      [get_ports "FMC1_LA24P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA24P"]
set_property PACKAGE_PIN K33      [get_ports "FMC1_LA24N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA24N"]
set_property PACKAGE_PIN K31      [get_ports "FMC1_LA25P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA25P"]
set_property PACKAGE_PIN J31      [get_ports "FMC1_LA25N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA25N"]
set_property PACKAGE_PIN K30      [get_ports "FMC1_LA26P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA26P"]
set_property PACKAGE_PIN J30      [get_ports "FMC1_LA26N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA26N"]
set_property PACKAGE_PIN M30      [get_ports "FMC1_LA27P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA27P"]
set_property PACKAGE_PIN L30      [get_ports "FMC1_LA27N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA27N"]
set_property PACKAGE_PIN M34      [get_ports "FMC1_LA28P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA28P"]
set_property PACKAGE_PIN L34      [get_ports "FMC1_LA28N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA28N"]
set_property PACKAGE_PIN P34      [get_ports "FMC1_LA29P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA29P"]
set_property PACKAGE_PIN N34      [get_ports "FMC1_LA29N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA29N"]
set_property PACKAGE_PIN R31      [get_ports "FMC1_LA30P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA30P"]
set_property PACKAGE_PIN R32      [get_ports "FMC1_LA30N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA30N"]
set_property PACKAGE_PIN R30      [get_ports "FMC1_LA31P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA31P"]
set_property PACKAGE_PIN P30      [get_ports "FMC1_LA31N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA31N"]
set_property PACKAGE_PIN U30      [get_ports "FMC1_LA32P"]
```

```
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA32P"]
set_property PACKAGE_PIN T30      [get_ports "FMC1_LA32N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA32N"]
set_property PACKAGE_PIN V31      [get_ports "FMC1_LA33P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA33P"]
set_property PACKAGE_PIN U31      [get_ports "FMC1_LA33N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_LA33N"]

#FMC1 HA
set_property PACKAGE_PIN E36      [get_ports "FMC1_HA00_CC_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA00_CC_P"]
set_property PACKAGE_PIN D36      [get_ports "FMC1_HA00_CC_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA00_CC_N"]
set_property PACKAGE_PIN C36      [get_ports "FMC1_HA01_CC_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA01_CC_P"]
set_property PACKAGE_PIN C37      [get_ports "FMC1_HA01_CC_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA01_CC_N"]
set_property PACKAGE_PIN D31      [get_ports "FMC1_HA02P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA02P"]
set_property PACKAGE_PIN C31      [get_ports "FMC1_HA02N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA02N"]
set_property PACKAGE_PIN C32      [get_ports "FMC1_HA03P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA03P"]
set_property PACKAGE_PIN B32      [get_ports "FMC1_HA03N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA03N"]
set_property PACKAGE_PIN A32      [get_ports "FMC1_HA04P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA04P"]
set_property PACKAGE_PIN A33      [get_ports "FMC1_HA04N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA04N"]
set_property PACKAGE_PIN D33      [get_ports "FMC1_HA05P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA05P"]
set_property PACKAGE_PIN C33      [get_ports "FMC1_HA05N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA05N"]
set_property PACKAGE_PIN D34      [get_ports "FMC1_HA06P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA06P"]
set_property PACKAGE_PIN C34      [get_ports "FMC1_HA06N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA06N"]
set_property PACKAGE_PIN B34      [get_ports "FMC1_HA07P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA07P"]
set_property PACKAGE_PIN A34      [get_ports "FMC1_HA07N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA07N"]
set_property PACKAGE_PIN E35      [get_ports "FMC1_HA08P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA08P"]
set_property PACKAGE_PIN D35      [get_ports "FMC1_HA08N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA08N"]
set_property PACKAGE_PIN B35      [get_ports "FMC1_HA09P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA09P"]
set_property PACKAGE_PIN A35      [get_ports "FMC1_HA09N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA09N"]
set_property PACKAGE_PIN B36      [get_ports "FMC1_HA10P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA10P"]
set_property PACKAGE_PIN B37      [get_ports "FMC1_HA10N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA10N"]
set_property PACKAGE_PIN A37      [get_ports "FMC1_HA11P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA11P"]
set_property PACKAGE_PIN A38      [get_ports "FMC1_HA11N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA11N"]
set_property PACKAGE_PIN B39      [get_ports "FMC1_HA12P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA12P"]
```

```
set_property PACKAGE_PIN A39      [get_ports "FMC1_HA12N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA12N"]
set_property PACKAGE_PIN B40      [get_ports "FMC1_HA13P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA13P"]
set_property PACKAGE_PIN A40      [get_ports "FMC1_HA13N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA13N"]
set_property PACKAGE_PIN E39      [get_ports "FMC1_HA14P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA14P"]
set_property PACKAGE_PIN D39      [get_ports "FMC1_HA14N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA14N"]
set_property PACKAGE_PIN E40      [get_ports "FMC1_HA15P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA15P"]
set_property PACKAGE_PIN D40      [get_ports "FMC1_HA15N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA15N"]
set_property PACKAGE_PIN F34      [get_ports "FMC1_HA16P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA16P"]
set_property PACKAGE_PIN F35      [get_ports "FMC1_HA16N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA16N"]
set_property PACKAGE_PIN C38      [get_ports "FMC1_HA17_CC_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA17_CC_P"]
set_property PACKAGE_PIN C39      [get_ports "FMC1_HA17_CC_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA17_CC_N"]
set_property PACKAGE_PIN E38      [get_ports "FMC1_HA18P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA18P"]
set_property PACKAGE_PIN D38      [get_ports "FMC1_HA18N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA18N"]
set_property PACKAGE_PIN H34      [get_ports "FMC1_HA19P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA19P"]
set_property PACKAGE_PIN G34      [get_ports "FMC1_HA19N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA19N"]
set_property PACKAGE_PIN H36      [get_ports "FMC1_HA20P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA20P"]
set_property PACKAGE_PIN G36      [get_ports "FMC1_HA20N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA20N"]
set_property PACKAGE_PIN J35      [get_ports "FMC1_HA21P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA21P"]
set_property PACKAGE_PIN J36      [get_ports "FMC1_HA21N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA21N"]
set_property PACKAGE_PIN G37      [get_ports "FMC1_HA22P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA22P"]
set_property PACKAGE_PIN F37      [get_ports "FMC1_HA22N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA22N"]
set_property PACKAGE_PIN H37      [get_ports "FMC1_HA23P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA23P"]
set_property PACKAGE_PIN H38      [get_ports "FMC1_HA23N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HA23N"]

#FMC1 HB
set_property PACKAGE_PIN J26      [get_ports "FMC1_HB00_CC_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HB00_CC_P"]
set_property PACKAGE_PIN H26      [get_ports "FMC1_HB00_CC_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HB00_CC_N"]
set_property PACKAGE_PIN J28      [get_ports "FMC1_HB01_CC_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HB01_CC_P"]
set_property PACKAGE_PIN J29      [get_ports "FMC1_HB01_CC_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HB01_CC_N"]
set_property PACKAGE_PIN E28      [get_ports "FMC1_HB02P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HB02P"]
set_property PACKAGE_PIN D28      [get_ports "FMC1_HB02N"]
```

```
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HB02N"]
set_property PACKAGE_PIN F27      [get_ports "FMC1_HB03P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HB03P"]
set_property PACKAGE_PIN E27      [get_ports "FMC1_HB03N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HB03N"]
set_property PACKAGE_PIN F28      [get_ports "FMC1_HB04P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HB04P"]
set_property PACKAGE_PIN F29      [get_ports "FMC1_HB04N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HB04N"]
set_property PACKAGE_PIN H29      [get_ports "FMC1_HB05P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HB05P"]
set_property PACKAGE_PIN G29      [get_ports "FMC1_HB05N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HB05N"]
set_property PACKAGE_PIN H27      [get_ports "FMC1_HB06P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HB06P"]
set_property PACKAGE_PIN H28      [get_ports "FMC1_HB06N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HB06N"]
set_property PACKAGE_PIN K26      [get_ports "FMC1_HB07P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HB07P"]
set_property PACKAGE_PIN K27      [get_ports "FMC1_HB07N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HB07N"]
set_property PACKAGE_PIN M27      [get_ports "FMC1_HB08P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HB08P"]
set_property PACKAGE_PIN L27      [get_ports "FMC1_HB08N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HB08N"]
set_property PACKAGE_PIN L28      [get_ports "FMC1_HB09P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HB09P"]
set_property PACKAGE_PIN K28      [get_ports "FMC1_HB09N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HB09N"]
set_property PACKAGE_PIN M29      [get_ports "FMC1_HB10P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HB10P"]
set_property PACKAGE_PIN L29      [get_ports "FMC1_HB10N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HB10N"]
set_property PACKAGE_PIN P26      [get_ports "FMC1_HB11P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HB11P"]
set_property PACKAGE_PIN N26      [get_ports "FMC1_HB11N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HB11N"]
set_property PACKAGE_PIN P28      [get_ports "FMC1_HB12P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HB12P"]
set_property PACKAGE_PIN N28      [get_ports "FMC1_HB12N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HB12N"]
set_property PACKAGE_PIN P29      [get_ports "FMC1_HB13P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HB13P"]
set_property PACKAGE_PIN N29      [get_ports "FMC1_HB13N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HB13N"]
set_property PACKAGE_PIN T26      [get_ports "FMC1_HB14P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HB14P"]
set_property PACKAGE_PIN R26      [get_ports "FMC1_HB14N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HB14N"]
set_property PACKAGE_PIN T27      [get_ports "FMC1_HB15P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HB15P"]
set_property PACKAGE_PIN R27      [get_ports "FMC1_HB15N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HB15N"]
set_property PACKAGE_PIN T28      [get_ports "FMC1_HB16P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HB16P"]
set_property PACKAGE_PIN R28      [get_ports "FMC1_HB16N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC1_HB16N"]
```

```
#FMC2
set_property PACKAGE_PIN AR26     [get_ports "FMC2_PRSNT_M2C_L"]
set_property IOSTANDARD  LVCMOSxx [get_ports "FMC2_PRSNT_M2C_L"]
set_property PACKAGE_PIN AV26     [get_ports "FMC2_CLK0_M2C_P"]
set_property IOSTANDARD  LVCMOSxx [get_ports "FMC2_CLK0_M2C_P"]
set_property PACKAGE_PIN AW26     [get_ports "FMC2_CLK0_M2C_N"]
set_property IOSTANDARD  LVCMOSxx [get_ports "FMC2_CLK0_M2C_N"]
set_property PACKAGE_PIN AW28     [get_ports "FMC2_CLK1_M2C_P"]
set_property IOSTANDARD  LVCMOSxx [get_ports "FMC2_CLK1_M2C_P"]
set_property PACKAGE_PIN AY28     [get_ports "FMC2_CLK1_M2C_N"]
set_property IOSTANDARD  LVCMOSxx [get_ports "FMC2_CLK1_M2C_N"]

#FMC2 LA
set_property PACKAGE_PIN AY26     [get_ports "FMC2_LA00_CC_P"]
set_property IOSTANDARD  LVCMOSxx [get_ports "FMC2_LA00_CC_P"]
set_property PACKAGE_PIN AY27     [get_ports "FMC2_LA00_CC_N"]
set_property IOSTANDARD  LVCMOSxx [get_ports "FMC2_LA00_CC_N"]
set_property PACKAGE_PIN AW25     [get_ports "FMC2_LA01_CC_P"]
set_property IOSTANDARD  LVCMOSxx [get_ports "FMC2_LA01_CC_P"]
set_property PACKAGE_PIN AY25     [get_ports "FMC2_LA01_CC_N"]
set_property IOSTANDARD  LVCMOSxx [get_ports "FMC2_LA01_CC_N"]
set_property PACKAGE_PIN AL27     [get_ports "FMC2_LA02P"]
set_property IOSTANDARD  LVCMOSxx [get_ports "FMC2_LA02P"]
set_property PACKAGE_PIN AL28     [get_ports "FMC2_LA02N"]
set_property IOSTANDARD  LVCMOSxx [get_ports "FMC2_LA02N"]
set_property PACKAGE_PIN AM27     [get_ports "FMC2_LA03P"]
set_property IOSTANDARD  LVCMOSxx [get_ports "FMC2_LA03P"]
set_property PACKAGE_PIN AN27     [get_ports "FMC2_LA03N"]
set_property IOSTANDARD  LVCMOSxx [get_ports "FMC2_LA03N"]
set_property PACKAGE_PIN AN28     [get_ports "FMC2_LA04P"]
set_property IOSTANDARD  LVCMOSxx [get_ports "FMC2_LA04P"]
set_property PACKAGE_PIN AP28     [get_ports "FMC2_LA04N"]
set_property IOSTANDARD  LVCMOSxx [get_ports "FMC2_LA04N"]
set_property PACKAGE_PIN AP25     [get_ports "FMC2_LA05P"]
set_property IOSTANDARD  LVCMOSxx [get_ports "FMC2_LA05P"]
set_property PACKAGE_PIN AP26     [get_ports "FMC2_LA05N"]
set_property IOSTANDARD  LVCMOSxx [get_ports "FMC2_LA05N"]
set_property PACKAGE_PIN AR28     [get_ports "FMC2_LA06P"]
set_property IOSTANDARD  LVCMOSxx [get_ports "FMC2_LA06P"]
set_property PACKAGE_PIN AT28     [get_ports "FMC2_LA06N"]
set_property IOSTANDARD  LVCMOSxx [get_ports "FMC2_LA06N"]
set_property PACKAGE_PIN AR27     [get_ports "FMC2_LA07P"]
set_property IOSTANDARD  LVCMOSxx [get_ports "FMC2_LA07P"]
set_property PACKAGE_PIN AT27     [get_ports "FMC2_LA07N"]
set_property IOSTANDARD  LVCMOSxx [get_ports "FMC2_LA07N"]
set_property PACKAGE_PIN AR25     [get_ports "FMC2_LA08P"]
set_property IOSTANDARD  LVCMOSxx [get_ports "FMC2_LA08P"]
set_property PACKAGE_PIN AT25     [get_ports "FMC2_LA08N"]
set_property IOSTANDARD  LVCMOSxx [get_ports "FMC2_LA08N"]
set_property PACKAGE_PIN AU26     [get_ports "FMC2_LA09P"]
set_property IOSTANDARD  LVCMOSxx [get_ports "FMC2_LA09P"]
set_property PACKAGE_PIN AU27     [get_ports "FMC2_LA09N"]
set_property IOSTANDARD  LVCMOSxx [get_ports "FMC2_LA09N"]
set_property PACKAGE_PIN AV27     [get_ports "FMC2_LA10P"]
set_property IOSTANDARD  LVCMOSxx [get_ports "FMC2_LA10P"]
set_property PACKAGE_PIN AV28     [get_ports "FMC2_LA10N"]
set_property IOSTANDARD  LVCMOSxx [get_ports "FMC2_LA10N"]
set_property PACKAGE_PIN BA27     [get_ports "FMC2_LA11P"]
set_property IOSTANDARD  LVCMOSxx [get_ports "FMC2_LA11P"]
```

```
set_property PACKAGE_PIN BA28     [get_ports "FMC2_LA11N"]
set_property IOSTANDARD  LVCMOSxx [get_ports "FMC2_LA11N"]
set_property PACKAGE_PIN BB26     [get_ports "FMC2_LA12P"]
set_property IOSTANDARD  LVCMOSxx [get_ports "FMC2_LA12P"]
set_property PACKAGE_PIN BB27     [get_ports "FMC2_LA12N"]
set_property IOSTANDARD  LVCMOSxx [get_ports "FMC2_LA12N"]
set_property PACKAGE_PIN BA25     [get_ports "FMC2_LA13P"]
set_property IOSTANDARD  LVCMOSxx [get_ports "FMC2_LA13P"]
set_property PACKAGE_PIN BB25     [get_ports "FMC2_LA13N"]
set_property IOSTANDARD  LVCMOSxx [get_ports "FMC2_LA13N"]
set_property PACKAGE_PIN BC26     [get_ports "FMC2_LA14P"]
set_property IOSTANDARD  LVCMOSxx [get_ports "FMC2_LA14P"]
set_property PACKAGE_PIN BC27     [get_ports "FMC2_LA14N"]
set_property IOSTANDARD  LVCMOSxx [get_ports "FMC2_LA14N"]
set_property PACKAGE_PIN BE25     [get_ports "FMC2_LA15P"]
set_property IOSTANDARD  LVCMOSxx [get_ports "FMC2_LA15P"]
set_property PACKAGE_PIN BF25     [get_ports "FMC2_LA15N"]
set_property IOSTANDARD  LVCMOSxx [get_ports "FMC2_LA15N"]
set_property PACKAGE_PIN BD26     [get_ports "FMC2_LA16P"]
set_property IOSTANDARD  LVCMOSxx [get_ports "FMC2_LA16P"]
set_property PACKAGE_PIN BE26     [get_ports "FMC2_LA16N"]
set_property IOSTANDARD  LVCMOSxx [get_ports "FMC2_LA16N"]
set_property PACKAGE_PIN BD28     [get_ports "FMC2_LA17_CC_P"]
set_property IOSTANDARD  LVCMOSxx [get_ports "FMC2_LA17_CC_P"]
set_property PACKAGE_PIN BE28     [get_ports "FMC2_LA17_CC_N"]
set_property IOSTANDARD  LVCMOSxx [get_ports "FMC2_LA17_CC_N"]
set_property PACKAGE_PIN BE27     [get_ports "FMC2_LA18_CC_P"]
set_property IOSTANDARD  LVCMOSxx [get_ports "FMC2_LA18_CC_P"]
set_property PACKAGE_PIN BF27     [get_ports "FMC2_LA18_CC_N"]
set_property IOSTANDARD  LVCMOSxx [get_ports "FMC2_LA18_CC_N"]
set_property PACKAGE_PIN BF28     [get_ports "FMC2_LA19P"]
set_property IOSTANDARD  LVCMOSxx [get_ports "FMC2_LA19P"]
set_property PACKAGE_PIN BF29     [get_ports "FMC2_LA19N"]
set_property IOSTANDARD  LVCMOSxx [get_ports "FMC2_LA19N"]

#FMC3
set_property PACKAGE_PIN C17      [get_ports "FMC3_PRSNT_M2C_L"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_PRSNT_M2C_L"]
set_property PACKAGE_PIN J16      [get_ports "FMC3_CLK0_M2C_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_CLK0_M2C_P"]
set_property PACKAGE_PIN J15      [get_ports "FMC3_CLK0_M2C_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_CLK0_M2C_N"]
set_property PACKAGE_PIN J14      [get_ports "FMC3_CLK1_M2C_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_CLK1_M2C_P"]
set_property PACKAGE_PIN H14      [get_ports "FMC3_CLK1_M2C_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_CLK1_M2C_N"]
set_property PACKAGE_PIN J24      [get_ports "FMC3_CLK2_BIDIR_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_CLK2_BIDIR_P"]
set_property PACKAGE_PIN H24      [get_ports "FMC3_CLK2_BIDIR_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_CLK2_BIDIR_N"]
set_property PACKAGE_PIN J23      [get_ports "FMC3_CLK3_BIDIR_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_CLK3_BIDIR_P"]
set_property PACKAGE_PIN H23      [get_ports "FMC3_CLK3_BIDIR_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_CLK3_BIDIR_N"]

#FMC3 LA
set_property PACKAGE_PIN G15      [get_ports "FMC3_LA00_CC_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA00_CC_P"]
set_property PACKAGE_PIN F15      [get_ports "FMC3_LA00_CC_N"]
```

```
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA00_CC_N"]
set_property PACKAGE_PIN G14      [get_ports "FMC3_LA01_CC_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA01_CC_P"]
set_property PACKAGE_PIN F14      [get_ports "FMC3_LA01_CC_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA01_CC_N"]
set_property PACKAGE_PIN B17      [get_ports "FMC3_LA02P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA02P"]
set_property PACKAGE_PIN A17      [get_ports "FMC3_LA02N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA02N"]
set_property PACKAGE_PIN C16      [get_ports "FMC3_LA03P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA03P"]
set_property PACKAGE_PIN B16      [get_ports "FMC3_LA03N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA03N"]
set_property PACKAGE_PIN B15      [get_ports "FMC3_LA04P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA04P"]
set_property PACKAGE_PIN A15      [get_ports "FMC3_LA04N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA04N"]
set_property PACKAGE_PIN A14      [get_ports "FMC3_LA05P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA05P"]
set_property PACKAGE_PIN A13      [get_ports "FMC3_LA05N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA05N"]
set_property PACKAGE_PIN C14      [get_ports "FMC3_LA06P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA06P"]
set_property PACKAGE_PIN B14      [get_ports "FMC3_LA06N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA06N"]
set_property PACKAGE_PIN D13      [get_ports "FMC3_LA07P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA07P"]
set_property PACKAGE_PIN C13      [get_ports "FMC3_LA07N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA07N"]
set_property PACKAGE_PIN E16      [get_ports "FMC3_LA08P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA08P"]
set_property PACKAGE_PIN D16      [get_ports "FMC3_LA08N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA08N"]
set_property PACKAGE_PIN E15      [get_ports "FMC3_LA09P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA09P"]
set_property PACKAGE_PIN D15      [get_ports "FMC3_LA09N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA09N"]
set_property PACKAGE_PIN G17      [get_ports "FMC3_LA10P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA10P"]
set_property PACKAGE_PIN G16      [get_ports "FMC3_LA10N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA10N"]
set_property PACKAGE_PIN F13      [get_ports "FMC3_LA11P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA11P"]
set_property PACKAGE_PIN E13      [get_ports "FMC3_LA11N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA11N"]
set_property PACKAGE_PIN H17      [get_ports "FMC3_LA12P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA12P"]
set_property PACKAGE_PIN H16      [get_ports "FMC3_LA12N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA12N"]
set_property PACKAGE_PIN J13      [get_ports "FMC3_LA13P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA13P"]
set_property PACKAGE_PIN H13      [get_ports "FMC3_LA13N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA13N"]
set_property PACKAGE_PIN K16      [get_ports "FMC3_LA14P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA14P"]
set_property PACKAGE_PIN K15      [get_ports "FMC3_LA14N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA14N"]
set_property PACKAGE_PIN N16      [get_ports "FMC3_LA15P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA15P"]
```

```
set_property PACKAGE_PIN M16      [get_ports "FMC3_LA15N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA15N"]
set_property PACKAGE_PIN M14      [get_ports "FMC3_LA16P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA16P"]
set_property PACKAGE_PIN L14      [get_ports "FMC3_LA16N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA16N"]
set_property PACKAGE_PIN F24      [get_ports "FMC3_LA17_CC_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA17_CC_P"]
set_property PACKAGE_PIN F23      [get_ports "FMC3_LA17_CC_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA17_CC_N"]
set_property PACKAGE_PIN G25      [get_ports "FMC3_LA18_CC_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA18_CC_P"]
set_property PACKAGE_PIN G24      [get_ports "FMC3_LA18_CC_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA18_CC_N"]
set_property PACKAGE_PIN B25      [get_ports "FMC3_LA19P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA19P"]
set_property PACKAGE_PIN A25      [get_ports "FMC3_LA19N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA19N"]
set_property PACKAGE_PIN B24      [get_ports "FMC3_LA20P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA20P"]
set_property PACKAGE_PIN A24      [get_ports "FMC3_LA20N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA20N"]
set_property PACKAGE_PIN A23      [get_ports "FMC3_LA21P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA21P"]
set_property PACKAGE_PIN A22      [get_ports "FMC3_LA21N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA21N"]
set_property PACKAGE_PIN C26      [get_ports "FMC3_LA22P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA22P"]
set_property PACKAGE_PIN B26      [get_ports "FMC3_LA22N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA22N"]
set_property PACKAGE_PIN C24      [get_ports "FMC3_LA23P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA23P"]
set_property PACKAGE_PIN C23      [get_ports "FMC3_LA23N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA23N"]
set_property PACKAGE_PIN C22      [get_ports "FMC3_LA24P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA24P"]
set_property PACKAGE_PIN B22      [get_ports "FMC3_LA24N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA24N"]
set_property PACKAGE_PIN E25      [get_ports "FMC3_LA25P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA25P"]
set_property PACKAGE_PIN D25      [get_ports "FMC3_LA25N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA25N"]
set_property PACKAGE_PIN D24      [get_ports "FMC3_LA26P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA26P"]
set_property PACKAGE_PIN D23      [get_ports "FMC3_LA26N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA26N"]
set_property PACKAGE_PIN E23      [get_ports "FMC3_LA27P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA27P"]
set_property PACKAGE_PIN E22      [get_ports "FMC3_LA27N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA27N"]
set_property PACKAGE_PIN G22      [get_ports "FMC3_LA28P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA28P"]
set_property PACKAGE_PIN F22      [get_ports "FMC3_LA28N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA28N"]
set_property PACKAGE_PIN K25      [get_ports "FMC3_LA29P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA29P"]
set_property PACKAGE_PIN J25      [get_ports "FMC3_LA29N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA29N"]
set_property PACKAGE_PIN L23      [get_ports "FMC3_LA30P"]
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```
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA30P"]
set_property PACKAGE_PIN K23      [get_ports "FMC3_LA30N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA30N"]
set_property PACKAGE_PIN L22      [get_ports "FMC3_LA31P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA31P"]
set_property PACKAGE_PIN K22      [get_ports "FMC3_LA31N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA31N"]
set_property PACKAGE_PIN L25      [get_ports "FMC3_LA32P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA32P"]
set_property PACKAGE_PIN L24      [get_ports "FMC3_LA32N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA32N"]
set_property PACKAGE_PIN R25      [get_ports "FMC3_LA33P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA33P"]
set_property PACKAGE_PIN P25      [get_ports "FMC3_LA33N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_LA33N"]

#FMC3 HA
set_property PACKAGE_PIN G20      [get_ports "FMC3_HA00_CC_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA00_CC_P"]
set_property PACKAGE_PIN G19      [get_ports "FMC3_HA00_CC_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA00_CC_N"]
set_property PACKAGE_PIN H19      [get_ports "FMC3_HA01_CC_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA01_CC_P"]
set_property PACKAGE_PIN H18      [get_ports "FMC3_HA01_CC_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA01_CC_N"]
set_property PACKAGE_PIN B20      [get_ports "FMC3_HA02P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA02P"]
set_property PACKAGE_PIN A20      [get_ports "FMC3_HA02N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA02N"]
set_property PACKAGE_PIN B19      [get_ports "FMC3_HA03P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA03P"]
set_property PACKAGE_PIN A19      [get_ports "FMC3_HA03N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA03N"]
set_property PACKAGE_PIN D18      [get_ports "FMC3_HA04P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA04P"]
set_property PACKAGE_PIN C18      [get_ports "FMC3_HA04N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA04N"]
set_property PACKAGE_PIN C21      [get_ports "FMC3_HA05P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA05P"]
set_property PACKAGE_PIN B21      [get_ports "FMC3_HA05N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA05N"]
set_property PACKAGE_PIN D21      [get_ports "FMC3_HA06P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA06P"]
set_property PACKAGE_PIN D20      [get_ports "FMC3_HA06N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA06N"]
set_property PACKAGE_PIN D19      [get_ports "FMC3_HA07P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA07P"]
set_property PACKAGE_PIN C19      [get_ports "FMC3_HA07N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA07N"]
set_property PACKAGE_PIN F18      [get_ports "FMC3_HA08P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA08P"]
set_property PACKAGE_PIN F17      [get_ports "FMC3_HA08N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA08N"]
set_property PACKAGE_PIN E21      [get_ports "FMC3_HA09P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA09P"]
set_property PACKAGE_PIN E20      [get_ports "FMC3_HA09N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA09N"]
set_property PACKAGE_PIN E18      [get_ports "FMC3_HA10P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA10P"]
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```
set_property PACKAGE_PIN E17      [get_ports "FMC3_HA10N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA10N"]
set_property PACKAGE_PIN F20      [get_ports "FMC3_HA11P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA11P"]
set_property PACKAGE_PIN F19      [get_ports "FMC3_HA11N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA11N"]
set_property PACKAGE_PIN K18      [get_ports "FMC3_HA12P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA12P"]
set_property PACKAGE_PIN J18      [get_ports "FMC3_HA12N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA12N"]
set_property PACKAGE_PIN J21      [get_ports "FMC3_HA13P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA13P"]
set_property PACKAGE_PIN H21      [get_ports "FMC3_HA13N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA13N"]
set_property PACKAGE_PIN L20      [get_ports "FMC3_HA14P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA14P"]
set_property PACKAGE_PIN K20      [get_ports "FMC3_HA14N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA14N"]
set_property PACKAGE_PIN L19      [get_ports "FMC3_HA15P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA15P"]
set_property PACKAGE_PIN L18      [get_ports "FMC3_HA15N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA15N"]
set_property PACKAGE_PIN L17      [get_ports "FMC3_HA16P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA16P"]
set_property PACKAGE_PIN K17      [get_ports "FMC3_HA16N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA16N"]
set_property PACKAGE_PIN J20      [get_ports "FMC3_HA17_CC_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA17_CC_P"]
set_property PACKAGE_PIN J19      [get_ports "FMC3_HA17_CC_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA17_CC_N"]
set_property PACKAGE_PIN N21      [get_ports "FMC3_HA18P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA18P"]
set_property PACKAGE_PIN M21      [get_ports "FMC3_HA18N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA18N"]
set_property PACKAGE_PIN R20      [get_ports "FMC3_HA19P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA19P"]
set_property PACKAGE_PIN P20      [get_ports "FMC3_HA19N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA19N"]
set_property PACKAGE_PIN P19      [get_ports "FMC3_HA20P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA20P"]
set_property PACKAGE_PIN N19      [get_ports "FMC3_HA20N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA20N"]
set_property PACKAGE_PIN M20      [get_ports "FMC3_HA21P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA21P"]
set_property PACKAGE_PIN M19      [get_ports "FMC3_HA21N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA21N"]
set_property PACKAGE_PIN P18      [get_ports "FMC3_HA22P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA22P"]
set_property PACKAGE_PIN N18      [get_ports "FMC3_HA22N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA22N"]
set_property PACKAGE_PIN N17      [get_ports "FMC3_HA23P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA23P"]
set_property PACKAGE_PIN M17      [get_ports "FMC3_HA23N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HA23N"]

#FMC3 HB
set_property PACKAGE_PIN AY35     [get_ports "FMC3_HB00_CC_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HB00_CC_P"]
set_property PACKAGE_PIN AY36     [get_ports "FMC3_HB00_CC_N"]
```

```
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HB00_CC_N"]
set_property PACKAGE_PIN BA34     [get_ports "FMC3_HB01_CC_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HB01_CC_P"]
set_property PACKAGE_PIN BB34     [get_ports "FMC3_HB01_CC_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HB01_CC_N"]
set_property PACKAGE_PIN AL34     [get_ports "FMC3_HB02P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HB02P"]
set_property PACKAGE_PIN AM34     [get_ports "FMC3_HB02N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HB02N"]
set_property PACKAGE_PIN AL32     [get_ports "FMC3_HB03P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HB03P"]
set_property PACKAGE_PIN AM32     [get_ports "FMC3_HB03N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HB03N"]
set_property PACKAGE_PIN AN32     [get_ports "FMC3_HB04P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HB04P"]
set_property PACKAGE_PIN AN33     [get_ports "FMC3_HB04N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HB04N"]
set_property PACKAGE_PIN AN34     [get_ports "FMC3_HB05P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HB05P"]
set_property PACKAGE_PIN AP34     [get_ports "FMC3_HB05N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HB05N"]
set_property PACKAGE_PIN AP33     [get_ports "FMC3_HB06P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HB06P"]
set_property PACKAGE_PIN AR33     [get_ports "FMC3_HB06N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HB06N"]
set_property PACKAGE_PIN AT33     [get_ports "FMC3_HB07P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HB07P"]
set_property PACKAGE_PIN AT34     [get_ports "FMC3_HB07N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HB07N"]
set_property PACKAGE_PIN AV33     [get_ports "FMC3_HB08P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HB08P"]
set_property PACKAGE_PIN AW33     [get_ports "FMC3_HB08N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HB08N"]
set_property PACKAGE_PIN AV34     [get_ports "FMC3_HB09P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HB09P"]
set_property PACKAGE_PIN AW34     [get_ports "FMC3_HB09N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HB09N"]
set_property PACKAGE_PIN AW35     [get_ports "FMC3_HB10P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HB10P"]
set_property PACKAGE_PIN AW36     [get_ports "FMC3_HB10N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HB10N"]
set_property PACKAGE_PIN AY33     [get_ports "FMC3_HB11P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HB11P"]
set_property PACKAGE_PIN BA33     [get_ports "FMC3_HB11N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HB11N"]
set_property PACKAGE_PIN BB36     [get_ports "FMC3_HB12P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HB12P"]
set_property PACKAGE_PIN BC36     [get_ports "FMC3_HB12N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HB12N"]
set_property PACKAGE_PIN BB37     [get_ports "FMC3_HB13P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HB13P"]
set_property PACKAGE_PIN BC37     [get_ports "FMC3_HB13N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HB13N"]
set_property PACKAGE_PIN BD36     [get_ports "FMC3_HB14P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HB14P"]
set_property PACKAGE_PIN BE36     [get_ports "FMC3_HB14N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HB14N"]
set_property PACKAGE_PIN BD35     [get_ports "FMC3_HB15P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HB15P"]
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```
set_property PACKAGE_PIN BE35      [get_ports "FMC3_HB15N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HB15N"]
set_property PACKAGE_PIN BC34      [get_ports "FMC3_HB16P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HB16P"]
set_property PACKAGE_PIN BD34      [get_ports "FMC3_HB16N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HB16N"]
set_property PACKAGE_PIN BA35      [get_ports "FMC3_HB17_CC_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HB17_CC_P"]
set_property PACKAGE_PIN BB35      [get_ports "FMC3_HB17_CC_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HB17_CC_N"]
set_property PACKAGE_PIN BB38      [get_ports "FMC3_HB18P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HB18P"]
set_property PACKAGE_PIN BC38      [get_ports "FMC3_HB18N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HB18N"]
set_property PACKAGE_PIN BC39      [get_ports "FMC3_HB19P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HB19P"]
set_property PACKAGE_PIN BD39      [get_ports "FMC3_HB19N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HB19N"]
set_property PACKAGE_PIN BD40      [get_ports "FMC3_HB20P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HB20P"]
set_property PACKAGE_PIN BE40      [get_ports "FMC3_HB20N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HB20N"]
set_property PACKAGE_PIN BE37      [get_ports "FMC3_HB21P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HB21P"]
set_property PACKAGE_PIN BF37      [get_ports "FMC3_HB21N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "FMC3_HB21N"]

#SUPERCLOCK-2 MODULE
set_property PACKAGE_PIN C28       [get_ports "CM_RST_B"]
set_property IOSTANDARD  LVCMOS18 [get_ports "CM_RST_B"]
set_property PACKAGE_PIN D29       [get_ports "CM_C1A"]
set_property IOSTANDARD  LVCMOS18 [get_ports "CM_C1A"]
set_property PACKAGE_PIN C29       [get_ports "CM_C2A"]
set_property IOSTANDARD  LVCMOS18 [get_ports "CM_C2A"]
set_property PACKAGE_PIN C27       [get_ports "CM_H_CS0_C3A"]
set_property IOSTANDARD  LVCMOS18 [get_ports "CM_H_CS0_C3A"]
set_property PACKAGE_PIN B27       [get_ports "CM_H_CS1_C4A"]
set_property IOSTANDARD  LVCMOS18 [get_ports "CM_H_CS1_C4A"]
set_property PACKAGE_PIN A28       [get_ports "CM_C1B"]
set_property IOSTANDARD  LVCMOS18 [get_ports "CM_C1B"]
set_property PACKAGE_PIN E30       [get_ports "CM_C2B"]
set_property IOSTANDARD  LVCMOS18 [get_ports "CM_C2B"]
set_property PACKAGE_PIN D30       [get_ports "CM_C3B"]
set_property IOSTANDARD  LVCMOS18 [get_ports "CM_C3B"]
set_property PACKAGE_PIN B30       [get_ports "CM_H_DEC"]
set_property IOSTANDARD  LVCMOS18 [get_ports "CM_H_DEC"]
set_property PACKAGE_PIN A30       [get_ports "CM_H_INC"]
set_property IOSTANDARD  LVCMOS18 [get_ports "CM_H_INC"]
set_property PACKAGE_PIN B29       [get_ports "CM_FS_ALIGN"]
set_property IOSTANDARD  LVCMOS18 [get_ports "CM_FS_ALIGN"]
set_property PACKAGE_PIN A29       [get_ports "CM_H_LOL"]
set_property IOSTANDARD  LVCMOS18 [get_ports "CM_H_LOL"]
set_property PACKAGE_PIN A27       [get_ports "CM_H_INT_ALRM"]
set_property IOSTANDARD  LVCMOS18 [get_ports "CM_H_INT_ALRM"]
set_property PACKAGE_PIN L13       [get_ports "CM_LVDS1_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "CM_LVDS1_P"]
set_property PACKAGE_PIN K13       [get_ports "CM_LVDS1_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "CM_LVDS1_N"]
set_property PACKAGE_PIN J33       [get_ports "CM_LVDS2_P"]
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set_property IOSTANDARD  LVCMOS18 [get_ports "CM_LVDS2_P"]
set_property PACKAGE_PIN H33      [get_ports "CM_LVDS2_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "CM_LVDS2_N"]
set_property PACKAGE_PIN G26      [get_ports "CM_GCLK_P"]
set_property IOSTANDARD  LVCMOS18 [get_ports "CM_GCLK_P"]
set_property PACKAGE_PIN G27      [get_ports "CM_GCLK_N"]
set_property IOSTANDARD  LVCMOS18 [get_ports "CM_GCLK_N"]

#SWITCHES
set_property PACKAGE_PIN AP13     [get_ports "USER_SW1"]
set_property IOSTANDARD  LVCMOS18 [get_ports "USER_SW1"]
set_property PACKAGE_PIN AU16     [get_ports "USER_SW2"]
set_property IOSTANDARD  LVCMOS18 [get_ports "USER_SW2"]
set_property PACKAGE_PIN AU14     [get_ports "USER_SW3"]
set_property IOSTANDARD  LVCMOS18 [get_ports "USER_SW3"]
set_property PACKAGE_PIN AV14     [get_ports "USER_SW4"]
set_property IOSTANDARD  LVCMOS18 [get_ports "USER_SW4"]
set_property PACKAGE_PIN AR13     [get_ports "USER_SW5"]
set_property IOSTANDARD  LVCMOS18 [get_ports "USER_SW5"]
set_property PACKAGE_PIN AV16     [get_ports "USER_SW6"]
set_property IOSTANDARD  LVCMOS18 [get_ports "USER_SW6"]
set_property PACKAGE_PIN AW16     [get_ports "USER_SW7"]
set_property IOSTANDARD  LVCMOS18 [get_ports "USER_SW7"]
set_property PACKAGE_PIN AW15     [get_ports "USER_SW8"]
set_property IOSTANDARD  LVCMOS18 [get_ports "USER_SW8"]

#PUSH BUTTONS
set_property PACKAGE_PIN AN14     [get_ports "USER_PB1"]
set_property IOSTANDARD  LVCMOS18 [get_ports "USER_PB1"]
set_property PACKAGE_PIN AM14     [get_ports "USER_PB2"]
set_property IOSTANDARD  LVCMOS18 [get_ports "USER_PB2"]

#LEDs
set_property PACKAGE_PIN BB14     [get_ports "APP_LED1"]
set_property IOSTANDARD  LVCMOS18 [get_ports "APP_LED1"]
set_property PACKAGE_PIN BB15     [get_ports "APP_LED2"]
set_property IOSTANDARD  LVCMOS18 [get_ports "APP_LED2"]
set_property PACKAGE_PIN BC14     [get_ports "APP_LED3"]
set_property IOSTANDARD  LVCMOS18 [get_ports "APP_LED3"]
set_property PACKAGE_PIN BD13     [get_ports "APP_LED4"]
set_property IOSTANDARD  LVCMOS18 [get_ports "APP_LED4"]
set_property PACKAGE_PIN BE13     [get_ports "APP_LED5"]
set_property IOSTANDARD  LVCMOS18 [get_ports "APP_LED5"]
set_property PACKAGE_PIN BE15     [get_ports "APP_LED6"]
set_property IOSTANDARD  LVCMOS18 [get_ports "APP_LED6"]
set_property PACKAGE_PIN BF15     [get_ports "APP_LED7"]
set_property IOSTANDARD  LVCMOS18 [get_ports "APP_LED7"]
set_property PACKAGE_PIN BD14     [get_ports "APP_LED8"]
set_property IOSTANDARD  LVCMOS18 [get_ports "APP_LED8"]

#SMAs
set_property PACKAGE_PIN L32      [get_ports "CLK_DIFF_1_P"]
set_property IOSTANDARD  LVDS     [get_ports "CLK_DIFF_1_P"]
set_property PACKAGE_PIN K32      [get_ports "CLK_DIFF_1_N"]
set_property IOSTANDARD  LVDS     [get_ports "CLK_DIFF_1_N"]
set_property PACKAGE_PIN M31      [get_ports "CLK_DIFF_2_P"]
set_property IOSTANDARD  LVDS     [get_ports "CLK_DIFF_2_P"]
set_property PACKAGE_PIN M32      [get_ports "CLK_DIFF_2_N"]
set_property IOSTANDARD  LVDS   [get_ports "CLK_DIFF_2_N"]
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#SYSTEM CLOCK
set_property PACKAGE_PIN AW14     [get_ports "LVDS_OSC_P"]
set_property IOSTANDARD  LVDS  [get_ports "LVDS_OSC_P"]
set_property PACKAGE_PIN AW13     [get_ports "LVDS_OSC_N"]
set_property IOSTANDARD  LVDS     [get_ports "LVDS_OSC_N"]

#PMBUS
set_property PACKAGE_PIN AY12     [get_ports "DUT_PMBUS_ALERT"]
set_property IOSTANDARD  LVCMOS18 [get_ports "DUT_PMBUS_ALERT"]
set_property PACKAGE_PIN BD16     [get_ports "DUT_PMBUS_CLK"]
set_property IOSTANDARD  LVCMOS18 [get_ports "DUT_PMBUS_CLK"]
set_property PACKAGE_PIN BE16     [get_ports "DUT_PMBUS_DATA"]
set_property IOSTANDARD  LVCMOS18 [get_ports "DUT_PMBUS_DATA"]

set_property PACKAGE_PIN AU25     [get_ports "DUT_SMAP_CSI_B"]
set_property IOSTANDARD  LVCMOS18 [get_ports "DUT_SMAP_CSI_B"]
set_property PACKAGE_PIN AM26     [get_ports "DUT_SMAP_D4"]
set_property IOSTANDARD  LVCMOS18 [get_ports "DUT_SMAP_D4"]
set_property PACKAGE_PIN AN26     [get_ports "DUT_SMAP_D5"]
set_property IOSTANDARD  LVCMOS18 [get_ports "DUT_SMAP_D5"]
set_property PACKAGE_PIN AL25     [get_ports "DUT_SMAP_D6"]
set_property IOSTANDARD  LVCMOS18 [get_ports "DUT_SMAP_D6"]
set_property PACKAGE_PIN AM25     [get_ports "DUT_SMAP_D7"]
set_property IOSTANDARD  LVCMOS18 [get_ports "DUT_SMAP_D7"]
set_property PACKAGE_PIN AL15     [get_ports "DUT_FREQ_CLK"]
set_property IOSTANDARD  LVCMOS18 [get_ports "DUT_FREQ_CLK"]
set_property PACKAGE_PIN AN13     [get_ports "DUT_FREQ_DATA"]
set_property IOSTANDARD  LVCMOS18 [get_ports "DUT_FREQ_DATA"]
set_property PACKAGE_PIN AP15     [get_ports "DUT_FREQ_BSY"]
set_property IOSTANDARD  LVCMOS18 [get_ports "DUT_FREQ_BSY"]
set_property PACKAGE_PIN AP14     [get_ports "DUT_FREQ_RDY"]
set_property IOSTANDARD  LVCMOS18 [get_ports "DUT_FREQ_RDY"]

#UART
set_property PACKAGE_PIN BF14     [get_ports "UART_TXD_O"]
set_property IOSTANDARD  LVCMOS18 [get_ports "UART_TXD_O"]
set_property PACKAGE_PIN BF13     [get_ports "UART_RXD_I"]
set_property IOSTANDARD  LVCMOS18 [get_ports "UART_RXD_I"]
set_property PACKAGE_PIN BB12     [get_ports "UART_RTS_O_B"]
set_property IOSTANDARD  LVCMOS18 [get_ports "UART_RTS_O_B"]
set_property PACKAGE_PIN BA12     [get_ports "UART_CTS_I_B"]
set_property IOSTANDARD  LVCMOS18 [get_ports "UART_CTS_I_B"]

#USB_GPIOs
set_property PACKAGE_PIN AY15     [get_ports "UART_GPIO_0"]
set_property IOSTANDARD  LVCMOS18 [get_ports "UART_GPIO_0"]
set_property PACKAGE_PIN AV13     [get_ports "UART_GPIO_1"]
set_property IOSTANDARD  LVCMOS18 [get_ports "UART_GPIO_1"]
set_property PACKAGE_PIN AR15     [get_ports "UART_GPIO_2"]
set_property IOSTANDARD  LVCMOS18 [get_ports "UART_GPIO_2"]
set_property PACKAGE_PIN AR16     [get_ports "UART_GPIO_3"]
set_property IOSTANDARD  LVCMOS18 [get_ports "UART_GPIO_3"]

#MGTs
set_property PACKAGE_PIN AY38     [get_ports "124_REFCLK1_P"]
set_property PACKAGE_PIN AY39     [get_ports "124_REFCLK1_N"]
set_property PACKAGE_PIN BA40     [get_ports "124_REFCLK0_P"]
set_property PACKAGE_PIN BA41     [get_ports "124_REFCLK0_N"]
set_property PACKAGE_PIN AW40     [get_ports "124_TX3_P"]
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set_property PACKAGE_PIN AW41     [get_ports "124_TX3_N"]
set_property PACKAGE_PIN AV43     [get_ports "124_RX3_P"]
set_property PACKAGE_PIN AV44     [get_ports "124_RX3_N"]
set_property PACKAGE_PIN BB42     [get_ports "124_TX2_P"]
set_property PACKAGE_PIN BB43     [get_ports "124_TX2_N"]
set_property PACKAGE_PIN AW45     [get_ports "124_RX2_P"]
set_property PACKAGE_PIN AW46     [get_ports "124_RX2_N"]
set_property PACKAGE_PIN BD42     [get_ports "124_TX1_P"]
set_property PACKAGE_PIN BD43     [get_ports "124_TX1_N"]
set_property PACKAGE_PIN BA45     [get_ports "124_RX1_P"]
set_property PACKAGE_PIN BA46     [get_ports "124_RX1_N"]
set_property PACKAGE_PIN BC45     [get_ports "124_RX0_P"]
set_property PACKAGE_PIN BC46     [get_ports "124_RX0_N"]
set_property PACKAGE_PIN BF42     [get_ports "124_TX0_P"]
set_property PACKAGE_PIN BF43     [get_ports "124_TX0_N"]
set_property PACKAGE_PIN AU36     [get_ports "125_REFCLK1_P"]
set_property PACKAGE_PIN AU37     [get_ports "125_REFCLK1_N"]
set_property PACKAGE_PIN AV38     [get_ports "125_REFCLK0_P"]
set_property PACKAGE_PIN AV39     [get_ports "125_REFCLK0_N"]
set_property PACKAGE_PIN AP38     [get_ports "125_TX3_P"]
set_property PACKAGE_PIN AP39     [get_ports "125_TX3_N"]
set_property PACKAGE_PIN AP43     [get_ports "125_RX3_P"]
set_property PACKAGE_PIN AP44     [get_ports "125_RX3_N"]
set_property PACKAGE_PIN AR40     [get_ports "125_TX2_P"]
set_property PACKAGE_PIN AR41     [get_ports "125_TX2_N"]
set_property PACKAGE_PIN AR45     [get_ports "125_RX2_P"]
set_property PACKAGE_PIN AR46     [get_ports "125_RX2_N"]
set_property PACKAGE_PIN AT38     [get_ports "125_TX1_P"]
set_property PACKAGE_PIN AT39     [get_ports "125_TX1_N"]
set_property PACKAGE_PIN AT43     [get_ports "125_RX1_P"]
set_property PACKAGE_PIN AT44     [get_ports "125_RX1_N"]
set_property PACKAGE_PIN AU40     [get_ports "125_TX0_P"]
set_property PACKAGE_PIN AU41     [get_ports "125_TX0_N"]
set_property PACKAGE_PIN AU45     [get_ports "125_RX0_P"]
set_property PACKAGE_PIN AU46     [get_ports "125_RX0_N"]
set_property PACKAGE_PIN AN36     [get_ports "126_REFCLK1_P"]
set_property PACKAGE_PIN AN37     [get_ports "126_REFCLK1_N"]
set_property PACKAGE_PIN AR36     [get_ports "126_REFCLK0_P"]
set_property PACKAGE_PIN AR37     [get_ports "126_REFCLK0_N"]
set_property PACKAGE_PIN AK38     [get_ports "126_TX3_P"]
set_property PACKAGE_PIN AK39     [get_ports "126_TX3_N"]
set_property PACKAGE_PIN AK43     [get_ports "126_RX3_P"]
set_property PACKAGE_PIN AK44     [get_ports "126_RX3_N"]
set_property PACKAGE_PIN AL40     [get_ports "126_TX2_P"]
set_property PACKAGE_PIN AL41     [get_ports "126_TX2_N"]
set_property PACKAGE_PIN AL45     [get_ports "126_RX2_P"]
set_property PACKAGE_PIN AL46     [get_ports "126_RX2_N"]
set_property PACKAGE_PIN AM38     [get_ports "126_TX1_P"]
set_property PACKAGE_PIN AM39     [get_ports "126_TX1_N"]
set_property PACKAGE_PIN AM43     [get_ports "126_RX1_P"]
set_property PACKAGE_PIN AM44     [get_ports "126_RX1_N"]
set_property PACKAGE_PIN AN40     [get_ports "126_TX0_P"]
set_property PACKAGE_PIN AN41     [get_ports "126_TX0_N"]
set_property PACKAGE_PIN AN45     [get_ports "126_RX0_P"]
set_property PACKAGE_PIN AN46     [get_ports "126_RX0_N"]
set_property PACKAGE_PIN AJ36     [get_ports "127_REFCLK1_P"]
set_property PACKAGE_PIN AJ37     [get_ports "127_REFCLK1_N"]
set_property PACKAGE_PIN AL36     [get_ports "127_REFCLK0_P"]
set_property PACKAGE_PIN AL37     [get_ports "127_REFCLK0_N"]
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set_property PACKAGE_PIN AF38     [get_ports "127_TX3_P"]
set_property PACKAGE_PIN AF39     [get_ports "127_TX3_N"]
set_property PACKAGE_PIN AF43     [get_ports "127_RX3_P"]
set_property PACKAGE_PIN AF44     [get_ports "127_RX3_N"]
set_property PACKAGE_PIN AG40     [get_ports "127_TX2_P"]
set_property PACKAGE_PIN AG41     [get_ports "127_TX2_N"]
set_property PACKAGE_PIN AG45     [get_ports "127_RX2_P"]
set_property PACKAGE_PIN AG46     [get_ports "127_RX2_N"]
set_property PACKAGE_PIN AH38     [get_ports "127_TX1_P"]
set_property PACKAGE_PIN AH39     [get_ports "127_TX1_N"]
set_property PACKAGE_PIN AH43     [get_ports "127_RX1_P"]
set_property PACKAGE_PIN AH44     [get_ports "127_RX1_N"]
set_property PACKAGE_PIN AJ40     [get_ports "127_TX0_P"]
set_property PACKAGE_PIN AJ41     [get_ports "127_TX0_N"]
set_property PACKAGE_PIN AJ45     [get_ports "127_RX0_P"]
set_property PACKAGE_PIN AJ46     [get_ports "127_RX0_N"]
set_property PACKAGE_PIN AE36     [get_ports "128_REFCLK1_P"]
set_property PACKAGE_PIN AE37     [get_ports "128_REFCLK1_N"]
set_property PACKAGE_PIN AG36     [get_ports "128_REFCLK0_P"]
set_property PACKAGE_PIN AG37     [get_ports "128_REFCLK0_N"]
set_property PACKAGE_PIN AB38     [get_ports "128_TX3_P"]
set_property PACKAGE_PIN AB39     [get_ports "128_TX3_N"]
set_property PACKAGE_PIN AB43     [get_ports "128_RX3_P"]
set_property PACKAGE_PIN AB44     [get_ports "128_RX3_N"]
set_property PACKAGE_PIN AC40     [get_ports "128_TX2_P"]
set_property PACKAGE_PIN AC41     [get_ports "128_TX2_N"]
set_property PACKAGE_PIN AC45     [get_ports "128_RX2_P"]
set_property PACKAGE_PIN AC46     [get_ports "128_RX2_N"]
set_property PACKAGE_PIN AD38     [get_ports "128_TX1_P"]
set_property PACKAGE_PIN AD39     [get_ports "128_TX1_N"]
set_property PACKAGE_PIN AD43     [get_ports "128_RX1_P"]
set_property PACKAGE_PIN AD44     [get_ports "128_RX1_N"]
set_property PACKAGE_PIN AE40     [get_ports "128_TX0_P"]
set_property PACKAGE_PIN AE41     [get_ports "128_TX0_N"]
set_property PACKAGE_PIN AE45     [get_ports "128_RX0_P"]
set_property PACKAGE_PIN AE46     [get_ports "128_RX0_N"]
set_property PACKAGE_PIN AA36     [get_ports "129_REFCLK1_P"]
set_property PACKAGE_PIN AA37     [get_ports "129_REFCLK1_N"]
set_property PACKAGE_PIN AC36     [get_ports "129_REFCLK0_P"]
set_property PACKAGE_PIN AC37     [get_ports "129_REFCLK0_N"]
set_property PACKAGE_PIN V38      [get_ports "129_TX3_P"]
set_property PACKAGE_PIN V39      [get_ports "129_TX3_N"]
set_property PACKAGE_PIN V43      [get_ports "129_RX3_P"]
set_property PACKAGE_PIN V44      [get_ports "129_RX3_N"]
set_property PACKAGE_PIN W40      [get_ports "129_TX2_P"]
set_property PACKAGE_PIN W41      [get_ports "129_TX2_N"]
set_property PACKAGE_PIN W45      [get_ports "129_RX2_P"]
set_property PACKAGE_PIN W46      [get_ports "129_RX2_N"]
set_property PACKAGE_PIN Y38      [get_ports "129_TX1_P"]
set_property PACKAGE_PIN Y39      [get_ports "129_TX1_N"]
set_property PACKAGE_PIN Y43      [get_ports "129_RX1_P"]
set_property PACKAGE_PIN Y44      [get_ports "129_RX1_N"]
set_property PACKAGE_PIN AA40     [get_ports "129_TX0_P"]
set_property PACKAGE_PIN AA41     [get_ports "129_TX0_N"]
set_property PACKAGE_PIN AA45     [get_ports "129_RX0_P"]
set_property PACKAGE_PIN AA46     [get_ports "129_RX0_N"]
set_property PACKAGE_PIN U36      [get_ports "130_REFCLK1_P"]
set_property PACKAGE_PIN U37      [get_ports "130_REFCLK1_N"]
set_property PACKAGE_PIN W36      [get_ports "130_REFCLK0_P"]
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set_property PACKAGE_PIN W37      [get_ports "130_REFCLK0_N"]
set_property PACKAGE_PIN P38      [get_ports "130_TX3_P"]
set_property PACKAGE_PIN P39      [get_ports "130_TX3_N"]
set_property PACKAGE_PIN P43      [get_ports "130_RX3_P"]
set_property PACKAGE_PIN P44      [get_ports "130_RX3_N"]
set_property PACKAGE_PIN R40      [get_ports "130_TX2_P"]
set_property PACKAGE_PIN R41      [get_ports "130_TX2_N"]
set_property PACKAGE_PIN R45      [get_ports "130_RX2_P"]
set_property PACKAGE_PIN R46      [get_ports "130_RX2_N"]
set_property PACKAGE_PIN T38      [get_ports "130_TX1_P"]
set_property PACKAGE_PIN T39      [get_ports "130_TX1_N"]
set_property PACKAGE_PIN T43      [get_ports "130_RX1_P"]
set_property PACKAGE_PIN T44      [get_ports "130_RX1_N"]
set_property PACKAGE_PIN U40      [get_ports "130_TX0_P"]
set_property PACKAGE_PIN U41      [get_ports "130_TX0_N"]
set_property PACKAGE_PIN U45      [get_ports "130_RX0_P"]
set_property PACKAGE_PIN U46      [get_ports "130_RX0_N"]
set_property PACKAGE_PIN N36      [get_ports "131_REFCLK1_P"]
set_property PACKAGE_PIN N37      [get_ports "131_REFCLK1_N"]
set_property PACKAGE_PIN R36      [get_ports "131_REFCLK0_P"]
set_property PACKAGE_PIN R37      [get_ports "131_REFCLK0_N"]
set_property PACKAGE_PIN J40      [get_ports "131_TX3_P"]
set_property PACKAGE_PIN J41      [get_ports "131_TX3_N"]
set_property PACKAGE_PIN K43      [get_ports "131_RX3_P"]
set_property PACKAGE_PIN K44      [get_ports "131_RX3_N"]
set_property PACKAGE_PIN L40      [get_ports "131_TX2_P"]
set_property PACKAGE_PIN L41      [get_ports "131_TX2_N"]
set_property PACKAGE_PIN L45      [get_ports "131_RX2_P"]
set_property PACKAGE_PIN L46      [get_ports "131_RX2_N"]
set_property PACKAGE_PIN M38      [get_ports "131_TX1_P"]
set_property PACKAGE_PIN M39      [get_ports "131_TX1_N"]
set_property PACKAGE_PIN M43      [get_ports "131_RX1_P"]
set_property PACKAGE_PIN M44      [get_ports "131_RX1_N"]
set_property PACKAGE_PIN N40      [get_ports "131_TX0_P"]
set_property PACKAGE_PIN N41      [get_ports "131_TX0_N"]
set_property PACKAGE_PIN N45      [get_ports "131_RX0_P"]
set_property PACKAGE_PIN N46      [get_ports "131_RX0_N"]
set_property PACKAGE_PIN AV11     [get_ports "224_REFCLK1_P"]
set_property PACKAGE_PIN AV10     [get_ports "224_REFCLK1_N"]
set_property PACKAGE_PIN AW9      [get_ports "224_REFCLK0_P"]
set_property PACKAGE_PIN AW8      [get_ports "224_REFCLK0_N"]
set_property PACKAGE_PIN AV7      [get_ports "224_TX3_P"]
set_property PACKAGE_PIN AV6      [get_ports "224_TX3_N"]
set_property PACKAGE_PIN AV2      [get_ports "224_RX3_P"]
set_property PACKAGE_PIN AV1      [get_ports "224_RX3_N"]
set_property PACKAGE_PIN BB5      [get_ports "224_TX2_P"]
set_property PACKAGE_PIN BB4      [get_ports "224_TX2_N"]
set_property PACKAGE_PIN AW4      [get_ports "224_RX2_P"]
set_property PACKAGE_PIN AW3      [get_ports "224_RX2_N"]
set_property PACKAGE_PIN BD5      [get_ports "224_TX1_P"]
set_property PACKAGE_PIN BD4      [get_ports "224_TX1_N"]
set_property PACKAGE_PIN BA2      [get_ports "224_RX1_P"]
set_property PACKAGE_PIN BA1      [get_ports "224_RX1_N"]
set_property PACKAGE_PIN BF5      [get_ports "224_TX0_P"]
set_property PACKAGE_PIN BF4      [get_ports "224_TX0_N"]
set_property PACKAGE_PIN BC2      [get_ports "224_RX0_P"]
set_property PACKAGE_PIN BC1      [get_ports "224_RX0_N"]
set_property PACKAGE_PIN AP11     [get_ports "225_REFCLK1_P"]
set_property PACKAGE_PIN AP10     [get_ports "225_REFCLK1_N"]
```

```
set_property PACKAGE_PIN AT11     [get_ports "225_REFCLK0_P"]
set_property PACKAGE_PIN AT10     [get_ports "225_REFCLK0_N"]
set_property PACKAGE_PIN AP7      [get_ports "225_TX3_P"]
set_property PACKAGE_PIN AP6      [get_ports "225_TX3_N"]
set_property PACKAGE_PIN AP2      [get_ports "225_RX3_P"]
set_property PACKAGE_PIN AP1      [get_ports "225_RX3_N"]
set_property PACKAGE_PIN AR9      [get_ports "225_TX2_P"]
set_property PACKAGE_PIN AR8      [get_ports "225_TX2_N"]
set_property PACKAGE_PIN AR4      [get_ports "225_RX2_P"]
set_property PACKAGE_PIN AR3      [get_ports "225_RX2_N"]
set_property PACKAGE_PIN AT7      [get_ports "225_TX1_P"]
set_property PACKAGE_PIN AT6      [get_ports "225_TX1_N"]
set_property PACKAGE_PIN AT2      [get_ports "225_RX1_P"]
set_property PACKAGE_PIN AT1      [get_ports "225_RX1_N"]
set_property PACKAGE_PIN AU9      [get_ports "225_TX0_P"]
set_property PACKAGE_PIN AU8      [get_ports "225_TX0_N"]
set_property PACKAGE_PIN AU4      [get_ports "225_RX0_P"]
set_property PACKAGE_PIN AU3      [get_ports "225_RX0_N"]
set_property PACKAGE_PIN AK11     [get_ports "226_REFCLK1_P"]
set_property PACKAGE_PIN AK10     [get_ports "226_REFCLK1_N"]
set_property PACKAGE_PIN AM11     [get_ports "226_REFCLK0_P"]
set_property PACKAGE_PIN AM10     [get_ports "226_REFCLK0_N"]
set_property PACKAGE_PIN AK7      [get_ports "226_TX3_P"]
set_property PACKAGE_PIN AK6      [get_ports "226_TX3_N"]
set_property PACKAGE_PIN AK2      [get_ports "226_RX3_P"]
set_property PACKAGE_PIN AK1      [get_ports "226_RX3_N"]
set_property PACKAGE_PIN AL9      [get_ports "226_TX2_P"]
set_property PACKAGE_PIN AL8      [get_ports "226_TX2_N"]
set_property PACKAGE_PIN AL4      [get_ports "226_RX2_P"]
set_property PACKAGE_PIN AL3      [get_ports "226_RX2_N"]
set_property PACKAGE_PIN AM7      [get_ports "226_TX1_P"]
set_property PACKAGE_PIN AM6      [get_ports "226_TX1_N"]
set_property PACKAGE_PIN AM2      [get_ports "226_RX1_P"]
set_property PACKAGE_PIN AM1      [get_ports "226_RX1_N"]
set_property PACKAGE_PIN AN9      [get_ports "226_TX0_P"]
set_property PACKAGE_PIN AN8      [get_ports "226_TX0_N"]
set_property PACKAGE_PIN AN4      [get_ports "226_RX0_P"]
set_property PACKAGE_PIN AN3      [get_ports "226_RX0_N"]
set_property PACKAGE_PIN AF11     [get_ports "227_REFCLK1_P"]
set_property PACKAGE_PIN AF10     [get_ports "227_REFCLK1_N"]
set_property PACKAGE_PIN AH11     [get_ports "227_REFCLK0_P"]
set_property PACKAGE_PIN AH10     [get_ports "227_REFCLK0_N"]
set_property PACKAGE_PIN AF7      [get_ports "227_TX3_P"]
set_property PACKAGE_PIN AF6      [get_ports "227_TX3_N"]
set_property PACKAGE_PIN AF2      [get_ports "227_RX3_P"]
set_property PACKAGE_PIN AF1      [get_ports "227_RX3_N"]
set_property PACKAGE_PIN AG9      [get_ports "227_TX2_P"]
set_property PACKAGE_PIN AG8      [get_ports "227_TX2_N"]
set_property PACKAGE_PIN AG4      [get_ports "227_RX2_P"]
set_property PACKAGE_PIN AG3      [get_ports "227_RX2_N"]
set_property PACKAGE_PIN AH7      [get_ports "227_TX1_P"]
set_property PACKAGE_PIN AH6      [get_ports "227_TX1_N"]
set_property PACKAGE_PIN AH2      [get_ports "227_RX1_P"]
set_property PACKAGE_PIN AH1      [get_ports "227_RX1_N"]
set_property PACKAGE_PIN AJ9      [get_ports "227_TX0_P"]
set_property PACKAGE_PIN AJ8      [get_ports "227_TX0_N"]
set_property PACKAGE_PIN AJ4      [get_ports "227_RX0_P"]
set_property PACKAGE_PIN AJ3      [get_ports "227_RX0_N"]
set_property PACKAGE_PIN AB11     [get_ports "228_REFCLK1_P"]
```

```
set_property PACKAGE_PIN AB10     [get_ports "228_REFCLK1_N"]
set_property PACKAGE_PIN AD11     [get_ports "228_REFCLK0_P"]
set_property PACKAGE_PIN AD10     [get_ports "228_REFCLK0_N"]
set_property PACKAGE_PIN AB7      [get_ports "228_TX3_P"]
set_property PACKAGE_PIN AB6      [get_ports "228_TX3_N"]
set_property PACKAGE_PIN AB2      [get_ports "228_RX3_P"]
set_property PACKAGE_PIN AB1      [get_ports "228_RX3_N"]
set_property PACKAGE_PIN AC9      [get_ports "228_TX2_P"]
set_property PACKAGE_PIN AC8      [get_ports "228_TX2_N"]
set_property PACKAGE_PIN AC4      [get_ports "228_RX2_P"]
set_property PACKAGE_PIN AC3      [get_ports "228_RX2_N"]
set_property PACKAGE_PIN AD7      [get_ports "228_TX1_P"]
set_property PACKAGE_PIN AD6      [get_ports "228_TX1_N"]
set_property PACKAGE_PIN AD2      [get_ports "228_RX1_P"]
set_property PACKAGE_PIN AD1      [get_ports "228_RX1_N"]
set_property PACKAGE_PIN AE9      [get_ports "228_TX0_P"]
set_property PACKAGE_PIN AE8      [get_ports "228_TX0_N"]
set_property PACKAGE_PIN AE4      [get_ports "228_RX0_P"]
set_property PACKAGE_PIN AE3      [get_ports "228_RX0_N"]
set_property PACKAGE_PIN V11      [get_ports "229_REFCLK1_P"]
set_property PACKAGE_PIN V10      [get_ports "229_REFCLK1_N"]
set_property PACKAGE_PIN Y11      [get_ports "229_REFCLK0_P"]
set_property PACKAGE_PIN Y10      [get_ports "229_REFCLK0_N"]
set_property PACKAGE_PIN V7       [get_ports "229_TX3_P"]
set_property PACKAGE_PIN V6       [get_ports "229_TX3_N"]
set_property PACKAGE_PIN V2       [get_ports "229_RX3_P"]
set_property PACKAGE_PIN V1       [get_ports "229_RX3_N"]
set_property PACKAGE_PIN W9       [get_ports "229_TX2_P"]
set_property PACKAGE_PIN W8       [get_ports "229_TX2_N"]
set_property PACKAGE_PIN W4       [get_ports "229_RX2_P"]
set_property PACKAGE_PIN W3       [get_ports "229_RX2_N"]
set_property PACKAGE_PIN Y7       [get_ports "229_TX1_P"]
set_property PACKAGE_PIN Y6       [get_ports "229_TX1_N"]
set_property PACKAGE_PIN Y2       [get_ports "229_RX1_P"]
set_property PACKAGE_PIN Y1       [get_ports "229_RX1_N"]
set_property PACKAGE_PIN AA9      [get_ports "229_TX0_P"]
set_property PACKAGE_PIN AA8      [get_ports "229_TX0_N"]
set_property PACKAGE_PIN AA4      [get_ports "229_RX0_P"]
set_property PACKAGE_PIN AA3      [get_ports "229_RX0_N"]
set_property PACKAGE_PIN P11      [get_ports "230_REFCLK1_P"]
set_property PACKAGE_PIN P10      [get_ports "230_REFCLK1_N"]
set_property PACKAGE_PIN T11      [get_ports "230_REFCLK0_P"]
set_property PACKAGE_PIN T10      [get_ports "230_REFCLK0_N"]
set_property PACKAGE_PIN P7       [get_ports "230_TX3_P"]
set_property PACKAGE_PIN P6       [get_ports "230_TX3_N"]
set_property PACKAGE_PIN P2       [get_ports "230_RX3_P"]
set_property PACKAGE_PIN P1       [get_ports "230_RX3_N"]
set_property PACKAGE_PIN R9       [get_ports "230_TX2_P"]
set_property PACKAGE_PIN R8       [get_ports "230_TX2_N"]
set_property PACKAGE_PIN R4       [get_ports "230_RX2_P"]
set_property PACKAGE_PIN R3       [get_ports "230_RX2_N"]
set_property PACKAGE_PIN T7       [get_ports "230_TX1_P"]
set_property PACKAGE_PIN T6       [get_ports "230_TX1_N"]
set_property PACKAGE_PIN T2       [get_ports "230_RX1_P"]
set_property PACKAGE_PIN T1       [get_ports "230_RX1_N"]
set_property PACKAGE_PIN U9       [get_ports "230_TX0_P"]
set_property PACKAGE_PIN U8       [get_ports "230_TX0_N"]
set_property PACKAGE_PIN U4       [get_ports "230_RX0_P"]
set_property PACKAGE_PIN U3       [get_ports "230_RX0_N"]
```

```
set_property PACKAGE_PIN K11      [get_ports "231_REFCLK1_P"]
set_property PACKAGE_PIN K10      [get_ports "231_REFCLK1_N"]
set_property PACKAGE_PIN M11      [get_ports "231_REFCLK0_P"]
set_property PACKAGE_PIN M10      [get_ports "231_REFCLK0_N"]
set_property PACKAGE_PIN K7       [get_ports "231_TX3_P"]
set_property PACKAGE_PIN K6       [get_ports "231_TX3_N"]
set_property PACKAGE_PIN K2       [get_ports "231_RX3_P"]
set_property PACKAGE_PIN K1       [get_ports "231_RX3_N"]
set_property PACKAGE_PIN L9       [get_ports "231_TX2_P"]
set_property PACKAGE_PIN L8       [get_ports "231_TX2_N"]
set_property PACKAGE_PIN L4       [get_ports "231_RX2_P"]
set_property PACKAGE_PIN L3       [get_ports "231_RX2_N"]
set_property PACKAGE_PIN M7       [get_ports "231_TX1_P"]
set_property PACKAGE_PIN M6       [get_ports "231_TX1_N"]
set_property PACKAGE_PIN M2       [get_ports "231_RX1_P"]
set_property PACKAGE_PIN M1       [get_ports "231_RX1_N"]
set_property PACKAGE_PIN N9       [get_ports "231_TX0_P"]
set_property PACKAGE_PIN N8       [get_ports "231_TX0_N"]
set_property PACKAGE_PIN N4       [get_ports "231_RX0_P"]
set_property PACKAGE_PIN N3       [get_ports "231_RX0_N"]
```

System Controller

Overview

The Xilinx system controller is an ease-of-use application that runs on a Zynq-7000 AP SoC at power-up on the VCU1287 board. The system controller command line can be accessed through a serial communication terminal connection (115200-8-N-1) using the enhanced communication port of the Silicon Labs USB to Dual UART described in USB to Dual UART Bridge.

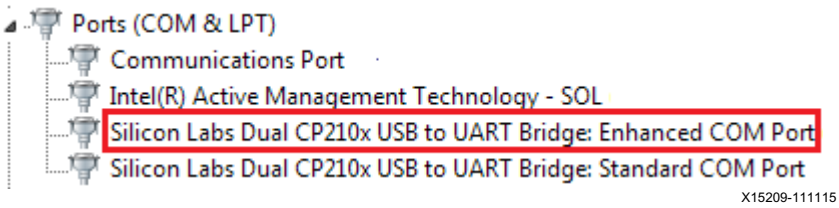

Figure D-1: **Silicon Labs Enhancement COM Port**

The main menu lists the available options:

```
VCU1287 System Controller v1.0

      - Main Menu -

-----------------------------

1. Set Programmable Clocks

2. Get Power System (PMBUS) Voltages

3. Get Power Monitoring Data (INA226)

4. Adjust FPGA Mezzanine Card (FMC) Settings

5. Get GPIO Data

6. Get EEPROM Data

7. Configure UltraScale FPGA
```

Programmable Clocks Menu

The clock menu is used to set the frequency of the Super Clock-2 module (see SuperClock-2 Module) clock sources.

```
VCU1287 System Controller v1.0

-----------------------------

   - Clock Menu-

1. Set VCU1287 Si570 Frequency

2. Set VCU1287 Si5368 Frequency

3. Save VCU1287 Clock Frequency to EEPROM

4. Restore VCU1287 Clock Frequency from EEPROM

5. View VCU1287 Saved Clocks in EEPROM

6. Set VCU1287 Clock Restore Options

7. Read VCU1287 Si570 Frequency

8. Read VCU1287 Si5368 Frequency

0. Return to Main Menu
```

Clock Menu Options

This section includes a description of the clock menu options using arbitrary sample value entries and system controller responses. The entry value commentary is shown in parentheses.

Option 1: Set VCU1287 Si570 Frequency

```
Enter the Si570 frequency <10-810MHz>:
```

(enter a value between 10 and 810)

```
200

RFreq_Cal[0]=0x02, RFreq_Cal[1]=0xBB, RFreq_Cal[2]=0xFF, RFreq_Cal[3]=0x8F,
RFreq_Cal[4]=0xC9


Freq:200.0000000000 HS_DIV=7 N1=4 DCO=5600.0 RFREQ=0x030FFF8251
```

(The returned values include diagnostic information.)

Option 2: Set VCU1287 Si5368 Frequency

```
Enter the Si5368 frequency (0.002-808MHz):
```

200

```
Choose Si5368 operating mode:
1 - Auto-Select
2- Free-Run using XA-XB crystal
```

1

```
Freq:200.0000000000 fosc=5600.000MHz f3= 5.000KHz LBW=0.200KHz N1=28 N1_HS=7
NC1_LS=4 N2=1120000 N2_HS=4 N2_LS=280000 N31=40000 N32=22857
```

(The returned values include diagnostic information.)

Note: Several seconds might elapse before the result is returned.

IMPORTANT: *Make sure J121 is set to position (2-3) DUT I2C DIS to isolate the DUT I2C signals and prevent bus contention. If contention occurs, the system controller will hang up while executing these commands.*

Option 3: Save VCU1287 Clock Frequency to EEPROM

```
VCU1287 System Controller
        - Save Menu -
-----------------------------
1. Save VCU1287 Si570 Frequency to EEPROM
2. Save VCU1287 Si5368 Frequency to EEPROM
0. Return to Clock Menu
```

1

```
Saving Si570 Frequency = 200.000 MHz to EEPROM
```

2

```
Saving Si5368 Frequency = 200.000 MHz to EEPROM
```

Option 4: Restore VCU1287 Clock Frequency from EEPROM

```
1. Restore VCU1287 Si570 Frequency from EEPROM
2. Restore VCU1287 Si5368 Frequency from EEPROM
0. Return to Clock Menu
```

1

```
RFreq_Cal[0]=0x02, RFreq_Cal[1]=0xBB, RFreq_Cal[2]=0xFF, RFreq_Cal[3]=0x8F,
RFreq_Cal[4]=0xC9


Freq:200.0000000000 HS_DIV=7 N1=4 DCO=5600.0 RFREQ=0x030FFF8251
Restored Si570 Frequency = 200.000 MHz from EEPROM
```

(The returned values include diagnostic information)

2

```
Freq:200.0000000000 fosc=5600.000MHz f3= 5.000KHz LBW=0.200KHz N1=28 N1_HS=7
NC1_LS=4 N2=1120000 N2_HS=4 N2_LS=280000 N31=40000 N32=22857
```

(The returned values include diagnostic information)

Note: Several seconds might elapse before the result is returned.

Option 5: View VCU1287 Saved Clocks in EEPROM

```
Saved Clocks in EEPROM
------------------------------
Si570 User Clock: 200.00000000 MHz
Si5328 MGT Clock: 200.00000000 MHz
```

Option 6: Set VCU1287 Clock Restore Options

```
1. View VCU1287 Clock Restore Options
2. Enable VCU1287 Si570 Automatic Restore at Power-Up/Reset
3. Enable VCU1287 Si5328 Automatic Restore at Power-Up/Reset
4. Disable VCU1287 Si570 Automatic Restore at Power-Up/Reset
5. Disable VCU1287 Si5328 Automatic Restore at Power-Up/Reset
0. Return to Clock Menu
```

Option 7: Read VCU1287 Si570 Frequency

7

```
Si570 Current Frequency = 2.000000E+02 MHz
```

Option 8: Read VCU1287 Si5328 Frequency

8

```
Si5368 CKOUT1 Current Frequency = 2.000000E+02 MHz
Si5368 CKOUT2 Current Frequency = 2.000000E+02 MHz
Si5368 CKOUT3 Current Frequency = 2.000000E+02 MHz
Si5368 CKOUT4 Current Frequency = 2.000000E+02 MHz
```

```
Si5368 CKOUT5 Current Frequency = 2.000000E+02 MHz
```

Option 0: Return to Main Menu

This option returns to the menu level above.

PMBus Menu

The PMBus bus commands are used to read the voltage settings of the VCU1287 power rails controlled by the Maxim power system. Through the PMBus menu, these power rails can be read once or scanned continuously until stopped by a key press. Table D-1 lists the voltage rails accessible through the system controller's interface to the Maxim PMBus.

Table D-1: **Maxim Power Supply Rail**

Maxim Power Supply Rail	I2C Address	Nominal Voltage
VCCINT	0x70	0.95V
VCCAUX	0x0B	1.80V
VCCBRAM	0x0F	0.95V
VCCO_HP	0x13	1.80V
VCCO_HR	0x11	1.80V
UTIL_5V0	0x1C	5.00V
UTIL_3V3	0x71	3.30V
UTIL_2V5	0x1A	2.50V

PMBus Menu Options

```
VCU1287 System Controller v1.0

- PMBus Menu-

1. Get PMBUS Voltages

2. Continuous Scan PMBUS Voltages

3. Get VCCINT Voltage

4. Get VCCAUX Voltage

5. Get VCCBRAM Voltage

6. Get VCCOHP Voltage

7. Get VCCOHR Voltage
```

```
8. Get UTIL5V0 Voltage

9. Get UTIL3V3 Voltage

A. Get UTIL2V5 Voltage

0. Return to Main Menu
```

Option 1: Get PMBus Voltages

```
VCCINT =  0.950 V
VCCAUX =  1.800 V
VCCBRAM =  0.950 V
VCCO_HP =  1.800 V
VCCO_HR =  1.800 V
UTIL2V5 =  2.499 V
UTIL3V3 =  3.300 V
UTIL5V0 =  5.000 V
```

Option 2: Continuous Scan PMBUS Voltages

The list of voltages shown in option 1 is displayed and updated about once per second. Pressing any key displays the PMBus menu.

Option 3: Get VCCINT Voltage

```
VCCINT =  0.950 V
Unscaled Hex: MSB = 0x00, LSB = 0x8D
```

(The returned values include configuration setting details.)

Option 4: Get VCCAUX Voltage

```
VCCAUX = 1.800 V
Unscaled Hex: MSB = 0x1C, LSB = 0xC9
```

(The returned values include configuration setting details.)

Option 5: Get VCC_BRAM Voltage

```
VCCBRAM = 0.950 V
Unscaled Hex: MSB = 0x0F, LSB = 0x34
```

(The returned values include configuration setting details.)

Option 6: Get VCCO_HP Voltage

```
VCCO_HP = 1.800 V
Unscaled Hex: MSB = 0x1C, LSB = 0xCD
```

(The returned values include diagnostic information.)

Option 7: Get VCCO_HR Voltage

```
VCCO_HR = 1.800 V
Unscaled Hex: MSB = 0x1C, LSB = 0xCB
```

(The returned values include diagnostic information.)

Option 8: Get UTIL5V0 Voltage

```
UTIL5V0 = 5.000 V
Unscaled Hex: MSB = 0x50, LSB = 0x00
```

(The returned values include diagnostic information.)

Option 9: Get UTIL3V3 Voltage

```
UTIL3V3 = 3.300 V
Unscaled Hex: MSB = 0x00, LSB = 0xFB
```

(The returned values include diagnostic information.)

Option A: Get UTIL2V5 Voltage

```
UTIL2V5 = 2.500 V
Unscaled Hex: MSB = 0x27, LSB = 0xFB
```

(The returned values include diagnostic information.)

Option 0: Return to Main Menu

This option returns to the menu level above.

Power Monitoring Data Menu

The VCU1287 includes the Texas Instrument INA226 power monitoring devices. The Power Monitoring Data menu, unlike the PMBus menu, provides both voltage and current monitoring for the MGT power modules, as well as the FPGA power rails.

```
VCU1287 System Controller v1.0

     - INA226 Menu -

-----------------------------

1. Continuous Scan Voltage and Current

2. Advanced Settings

0. Return to Main Menu
```

Option 1: Continuous Scan Voltage and Current

This option lists the voltages shown in Option 1: Get PMBus Voltages and displays the average, minimum, and maximum current of each rail. The list is updated about once per second. Pressing any key displays the PMBus menu.

Option 2: Advanced Setting

This option can be used to select one of the PMBus power monitors and explore additional user settings such as monitor calibration. Refer to the INA226 data sheet [Ref 7] for device registers information.

Select the advanced setting operation

```
VCU1287 System Controller v1.0
    - INA226 Advanced Menu -
-----------------------------
1. Select INA226 Device
2. Get    INA226 Register
3. Set    INA226 Register
0. Return to Previous Menu
```

Select the device

```
VCU1287 System Controller v1.0
    - Select INA226  Menu -
-----------------------------
1. Select VCCINT       Monitor
2. Select VCCAUX       Monitor
3. Select VCCBRAM      Monitor
4. Select VCCO_HP      Monitor
5. Select VCCO_HR      Monitor
6. Select MGTAVCC_R    Monitor
7. Select MGTAVTT_R    Monitor
8. Select MGTVCCAUX_R  Monitor
9. Select MGTAVCC_L    Monitor
A. Select MGTAVTT_L    Monitor
B. Select MGTVCCAUX_L  Monitor
0. Return to Previous Menu
```

Read the selected INA226 registers1

```
VCU1287 System Controller v1.0
    - RAIL INA226 Menu -
-----------------------------
1. Get SHUNT         Register
2. Get BUS           Register
3. Get POWER         Register
4. Get CURRENT       Register
5. Get CALIBRATION   Register
6. Get MASK_ENABLE   Register
7. Get ALERT_LIMIT   Register
8. Get CONFIGURATION Register
9. Get DIE ID        Register
0. Return to Previous Menu
```

Set the selected INA226 registers

```
VCU1287 System Controller v1.0
    -  RAIL INA226 Menu -
-----------------------------
1. Set CALIBRATION   Register
2. Set MASK_ENABLE   Register
3. Set ALERT_LIMIT   Register
4. Set CONFIGURATION Register
0. Return to Previous Menu
```

FPGA Mezzanine Card (FMC)

The VCU1287 board provides three FPGA mezzanine card (FMC) ANSI/VITA 57.1 expansion interfaces. All FMC mezzanine cards must host an IIC EEPROM that can be read out through the FMC menu. A raw hexadecimal display and a formatted version of the FMC EEPROM data are provided through the FMC menu. The VITA 57.1 standard identifies the data fields of the intelligent platform management interface (IPMI) specification used for the FMC EEPROM. The VCU1287 board system controller supports the programmable clock resources on these FMC modules:

IMPORTANT: *These FMC modules are not included.*

- FMC XM101 LVDS QSE card
- FMC XM104 MGT serial connectivity card
- FMC XM105 debug card
- FMC XM107 loopback card

These mezzanine cards can be attached to JA2 (callout 28), J3A (callout 29), or J4A (callout 30) of the VCU1287 expansion ports. Table D-2 shows the accessible clock resources on each FMC module.

Table D-2: **FMC Module Clock Resources**

Xilinx FMC Module/Board	Clock Source #1	Clock Source #2
XM101	Si570	SI570
XM104	Si570	Si5638
XM105	Si570	n/a
XM107	Si570	n/a

FMC Menu Options

```
VCU1287 System Controller v1.0

     - FMC Menu -

-----------------------------

1. Set FMC XMxxx CLOCKS

2. Read FMC1 IIC EEPROM

3. Read FMC2 IIC EEPROM

4. Read FMC3 IIC EEPROM

0. Return to Main Menu
```

Identify the FMC module types and the FMC connecter number. The subsequent examples use FMC-XM107 connected to FMC1.

Option 1: Set FMC XMxxx CLOCKS

```
VCU1287 System Controller v1.0
      - FMC Clock Menu -
-----------------------------
1. Set FMC XM101 Clocks
2. Set FMC XM104 Clocks
3. Set FMC XM105 Clocks
4. Set FMC XM107 Clocks
0. Return to FMC Menu
```

Set FMC XM107 Clocks

```
VCU1287 System Controller v1.0
      - XM107 Menu -
-----------------------------
1. Set FMC1 Si570   Frequency
2. Set FMC2 Si570   Frequency
3. Set FMC3 Si570   Frequency
0. Return to FMC Clock Menu
```

Set FMC1 Si570 Frequency

(The returned values include diagnostic information)

```
FMC1 card present
board_area_offset = 008
board_area_format_version = 0x01
board_area_length = 056
board_mfg_hdr_offset = 014
board_mfg_length = 010
ReadBuffer index = 026
ReadBuffer[i] = 58
ReadBuffer[i+1] = 4D
ReadBuffer[i+2] = 31
ReadBuffer[i+3] = 30
ReadBuffer[i+4] = 37
Enter the Si570 frequency (10-810MHz):
100
Freq:100.0000000000 HS_DIV=5 N1=10 DCO=5000.0 RFREQ=0x02BC7E566E
```

(The returned values include diagnostic information)

Option 2: Read FMC IIC EEPROM

If the FMC IIC EEPROM has been programmed, several data groupings are displayed:

```
ReadBuffer[000] - ReadBuffer[255] displays various value contents
Common Header
Board Area Info
MultiRecord Area
- OEM FMC Record
- DC Load Records (three groups)
- DC Output Records (three groups)
```

If the FMC IIC EEPROM has not been programmed, ReadBuffer[000] - ReadBuffer[255] displays buffer contents = `0xFF` and the Common Header reports “Invalid Format Version FF”.

GPIO Data Menu

The system controller continuously scans specific user-activated inputs and several onboard status signals. Positions 1-4 (ADDR3, ADDR2, ADDR1, ADDR0) of address DIP switch SW13 are monitored, as well as five user pushbuttons (SW5, SW6, SW10, SW11, SW12).

GPIO Menu Options

```
VCU1287 System Controller v1.0

    - GPIO Menu -

------------------------------

1. Get GPIO PL Data

2. Continuous Scan GPIO Readings

0. Return to Main Menu
```

Option 1: Get GPIO PL Data

The signals monitored with this option are currently not available in the VCU1287 board.

```
----------------------
FMC1_PRSNT = NO
FMC2_PRSNT = NO
PMBUS_CABLE_B = NO
FPGA_IIC_BUSY = YES
PMBUS_ALERT = YES
```

Option 2: Continuous Scan GPIO Readings

```
Press any Key to Return to GPIO Menu
```

When any of the address DIP SW13 poles 1-4 are changed, or a pushbutton pressed, the value beneath the switch position changes accordingly (showing a 0 or a 1).

```
SYS ADDR (SW13) (ADDR3, ADDR2, ADDR1, ADDR0)
0 0 0 0
Pushbuttons (SW11, SW12, SW5, SW6, SW10)
0 0 0 0 0
----------------------
FMC1_PRSNT = NO
FMC2_PRSNT = NO
PMBUS_CABLE_B = NO
FPGA_IIC_BUSY = YES
PMBUS_ALERT = YES
```

Board EEPROM Data Menu

The VCU1287 includes a QSPI memory device (N25Q128A) that is used to store the system controller firmware as well as additional test information

```
VCU1287 System Controller v1.0

    - EEPROM Menu -

------------------------------

1. Read Board EEPROM Data

0. Return to Main Menu
```

Option 1: Read Board EEPROM Data Options

```
Board Name: VCU1287
Board Revision: 1.0
 Serial Number:
 Test Revision:
     Test Date:
     Test Time:
     Test Name    -    Status
-------------------------------
```

FPGA CONFIG Menu

The system controller CONFIG menu is used to configure the VCU1287 UltraScale FPGA from an SD card (callout 8). One of sixteen bitstreams can be selected for use by the configuration engine by setting a binary encoded value on the system controller mode DIP switch SW13 (see System Controller Configuration DIP Switches) prior to board power up or when the system controller POR pushbutton (SW4) is pressed. The system controller CONFIG menu can also be used to select the SD card bitstream.

```
CONFIG Menu Options

VCU1287 System Controller v1.0

    - CONFIG Menu -

------------------------------

1. Configure UltraScale FPGA from SD Card

0. Return to Main Menu
```

Option 1: Configure UltraScale FPGA from SD Card

```
Enter a Bitstream number (0-15):
0
Info : xilinx.sys opened
Info : Opening rev_1/set0/config.def
Info : Configuration definition file "rev_1/set0/config.def" opened
Info : Clock divider is set to 2
Info : Configuration clock frequency is 25MHz
Info : Bitfile "rev_1/set0/vu095led.bit" opened
...10%...20%...30%...40%...50%...60%...70%...80%...90%...100%
Configuration completed successfully
```

Option 0: Return to Main Menu

This option returns to the menu level above.

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

Solution Centers

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

References

The most up to date information related to the VCU1287 board and its documentation is available on these websites:

VCU1287 Characterization Kit

VCU1287 Characterization Kit – Master Answer Record (Xilinx AR66056)

These documents provide supplemental material useful with this guide:

1. *UltraScale Architecture and Product Overview* (UG890)
2. *UltraScale Architecture System Monitor User Guide* (UG580)
3. *Vivado Design Suite User Guide: Using Constraints* (UG903)
4. *HW-CLK-101-SCLK2 SuperClock-2 Module User Guide* (UG770)

For additional documents associated with Xilinx devices, design tools, intellectual property, boards, and kits see the Xilinx documentation website.

The following websites provide supplemental material useful with this guide:

5. Information about the power system components used in the VCU1287 board is available from the Maxim Integrated website.
6. Samtec, Inc.: www.samtec.com.
7. Texas Instruments: http://www.ti.com/lit/ds/symlink/ina226.pdf.

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