

Low-Voltage Single-Supply, SPDT Analog Switch in SC-70

DESCRIPTION

The DG4599 is a cost effective upgrade to other types of 4599 low-voltage, single-pole/double-throw analog switches available in the industry today.

Combining low power, high speed, low on-resistance and small physical size, the DG4599 is ideal for portable and battery powered applications.

The DG4599 is built on Vishay Siliconix's low voltage CMOS process. An epitaxial layer prevents latchup. Break-before-make is guaranteed for DG4599.

Each switch conducts equally well in both directions when on, and blocks up to the power supply level when off.

FEATURES

- 6-Pin SC-70 Package
- 60 Ω Max. (26 Typ.) On-Resistance
- 2 Ω Typ. R_{ON} Flatness
- Fast Switching: $t_{ON} = 30$ ns (Max.)
 $t_{OFF} = 25$ ns (Max.)
- 2.25 V to 5.5 V Single Supply Operation
- Break-Before-Make Switching
- TTL/CMOS-Logic Compatible



RoHS*
COMPLIANT

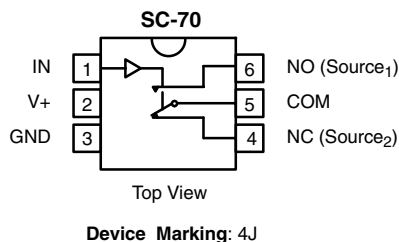
BENEFITS

- Reduced Power Consumption
- Simple Logic Interface
- High Accuracy
- Reduce Board Space

APPLICATIONS

- Battery-Operated Equipment
- Audio and Video Signal Routing
- Cellular Phones
- Low-Voltage Data-Acquisition Systems
- Sample-and-Hold Circuits
- Communications Systems

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



TRUTH TABLE

Logic	NC	NO
0	ON	OFF
1	OFF	ON

Logic "0" ≤ 0.8 V

Logic "1" ≥ 2.4 V

ORDERING INFORMATION

Temp Range	Package	Part Number
- 40 to 85 $^{\circ}$ C	SC70-6	DG4599DL-T1 DG4599DL-T1-E3

* Pb containing terminations are not RoHS compliant, exemptions may apply



ABSOLUTE MAXIMUM RATINGS			
Parameter		Limit	Unit
Referenced V+ to GND		- 0.3 to + 6	V
IN, COM, NC, NO ^a		- 0.3 to (V+ + 0.3)	
Continuous Current (Any Terminal)		± 50	mA
Peak Current (Pulsed at 1 ms, 10 % duty cycle)		± 200	
Storage Temperature (D Suffix)		- 65 to 125	°C
Power Dissipation (Packages) ^b	6-Pin SO70 ^c	250	mW

Notes:

- a. Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- b. All leads welded or soldered to PC Board.
- c. Derate 6.5 mW/°C above 25 °C.

SPECIFICATIONS (V+ = 5 V)							
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 5 V, ± 10 %, V _{IN} = 0.8 or 2.4 V ^e	Temp ^a	Limits - 40 to 85 °C			Unit
				Min ^b	Typ ^c	Max ^b	
Analog Switch							
Analog Signal Range ^d	V _{NO} , V _{NC} V _{COM}		Full	0		V+	V
Drain-Source On-Resistance	r _{DS(on)}	V+ = 4.5 V, V _D = 3 V, I _S = 10 mA	Room Full		7 10	60 65	Ω
r _{DS(on)} Flatness ^d	r _{DS(on)} Flatness	V+ = 2.5 V	Room		2		
Switch Off Leakage Current	I _{S(off)}	V+ = 5.5 V V _S = 1 V/4.5 V, V _D = 4.5 V/1 V	Room Full			1.0 4.0	nA
	I _{D(off)}		Room Full				
Channel-On Leakage Current	I _{D(on)}	V+ = 5.5 V, V _S = V _D = 1 V/4.5 V	Room Full			1.0 4.5	
Digital Control							
Input High Voltage	V _{INH}		Full	2.4			V
Input Low Voltage	V _{INL}		Full			0.8	
Input Capacitance	C _{in}		Full		3		pF
Input Current	I _{INL} or I _{INH}	V _{IN} = 0 or V+	Full	- 1		1	μA
Dynamic Characteristics							
Turn-On Time ^d	t _{ON}	V _D or V _S = 3 V, R _L = 300 Ω, C _L = 35 pF Figures 1 and 2	Room Full		9	30 40	ns
Turn-Off Time ^d	t _{OFF}		Room Full		5	25 30	
Break-Before-Make Time ^d	t _d		Room	1	4		
Charge Injection ^d	Q _{INJ}	C _L = 1 nF, V _S = 0 V V _{GEN} = 0 V, R _{GEN} = 0 Ω, Figure 3	Room		5	10	pC
Off-Isolation ^d	OIRR	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz	Room		- 73		dB
Crosstalk ^d	X _{TALK}		Room		- 70		
Source-Off Capacitance ^d	C _{S(off)}	V _{IN} = 0 or V+, f = 1 MHz	Room		7		pF
Channel-On Capacitance ^d	C _{D(on)}		Room		20		
Drain-to-Source Capacitance ^d	C _{DS(off)}		Room		20		
Power Supply							
Power Supply Range	V+			4.5		5.5	V
Power Supply Current	I+	V _{IN} = 0 or V+			0.01	1.0	μA
Power Consumption	P _C						5.5



SPECIFICATIONS (V+ = 3 V)							
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 3 V, ± 10 %, VIN = 0.4 or 2.0 V ^e	Temp ^a	Limits - 40 to 85 °C			Unit
				Min ^b	Typ ^c	Max ^b	
Analog Switch							
Analog Signal Range ^d	V _{NO} , V _{NC} V _{COM}		Full	0		V+	V
Drain-Source On-Resistance ^d	r _{DS(on)}	V+ = 2.7 V, V _D = 1.5 V, I _S = 10 mA	Room Full		15 19	95 105	Ω
r _{DS(on)} Flatness ^d	r _{DS(on)} Flatness	V _S = 0 to V+, I _S = 10 mA	Room		7.5		
Digital Control							
Input High Voltage	V _{INH}		Full	2			V
Input Low Voltage	V _{INL}		Full			0.8	
Input Current	I _{INL} or I _{INH}	V _{IN} = 0 or V+	Full	- 1		1	μA
Dynamic Characteristics							
Turn-On Time ^d	t _{ON}	V _D or V _S = 2.0 V, R _L = 300 Ω, C _L = 35 pF Figures 1 and 2	Room Full		12	45 55	ns
Turn-Off Time ^d	t _{OFF}		Room Full		6	35 40	
Break-Before-Make Time ^d	t _d		Room	1	7		
Charge Injection ^d	Q _{INJ}	C _L = 1 nF, V _{GEN} = 0 V, V _S = 0 V R _{GEN} = 0 Ω, Figure 3	Room		5	10	pC
Power Supply							
Power Supply Range	V+			2.7		3.3	V
Power Supply Current	I+	V _{IN} = 0 or V+			0.01	1.0	μA
Power Consumption	P _C						3.3



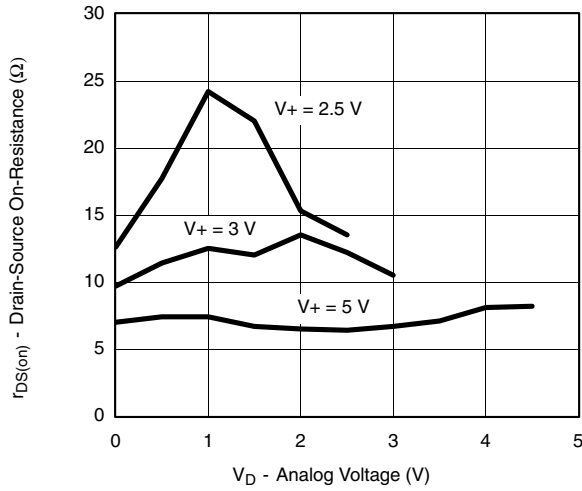
SPECIFICATIONS (V+ = 2.5 V)							
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 2.5 V, ± 10 %, VIN = 0.4 or 2.0 V ^e	Temp ^a	Limits - 40 to 85 °C			Unit
				Min ^b	Typ ^c	Max ^b	
Analog Switch							
Analog Signal Range ^d	V _{NO} , V _{NC} V _{COM}		Full	0		V+	V
Drain-Source On-Resistance	r _{DS(on)}	V+ = 2.25 V, V _D = 1.0 V, I _S = 10 mA	Room Full ^d		26 29	110 120	Ω
r _{DS(on)} Flatness ^d	r _{DS(on)} Flatness	V+ = 2.5 V	Room		10		
Digital Control							
Input High Voltage	V _{INH}		Full	2			V
Input Low Voltage	V _{INL}		Full			0.4	
Input Current	I _{INL} or I _{INH}	V _{IN} = 0 or V+	Full	- 1		1	μA
Dynamic Characteristics							
Turn-On Time	t _{ON}	V _D or V _S = 1.5 V, R _L = 300 Ω, C _L = 35 pF Figures 1 and 2	Room Full ^d		16	50 60	ns
Turn-Off Time	t _{OFF}		Room Full ^d		7	35 45	
Break-Before-Make Time	t _d		Room	1	12		
Power Supply							
Power Supply Range	V+			2.25		2.75	V
Power Supply Current ^d	I+	V _{IN} = 0 or V+			0.01	1.0	μA
Power Consumption	P _C						2.75

Notes:

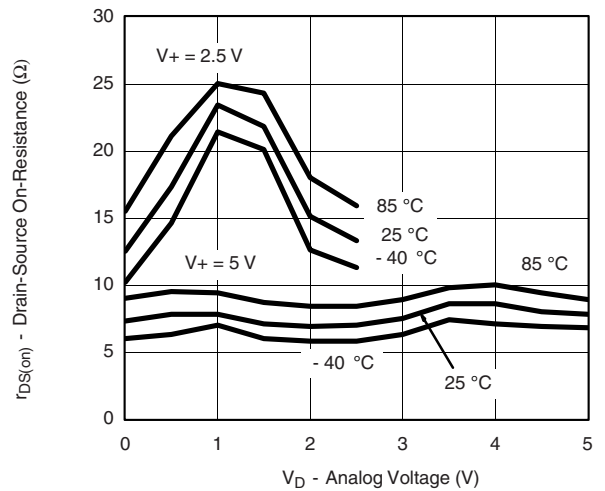
- a. Room = 25 °C, Full = as determined by the operating suffix.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Typical values are for design aid only, not guaranteed nor subject to production testing.
- d. Guarantee by design, nor subjected to production test.
- e. V_{IN} = input voltage to perform proper function.
- f. Guaranteed by 5 V leakage testing, not production tested.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

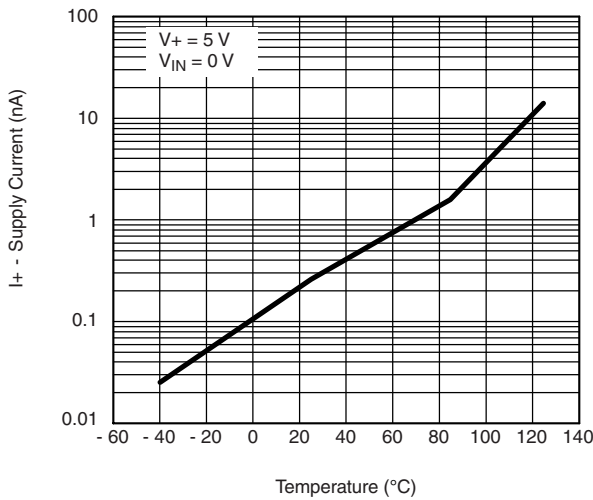
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



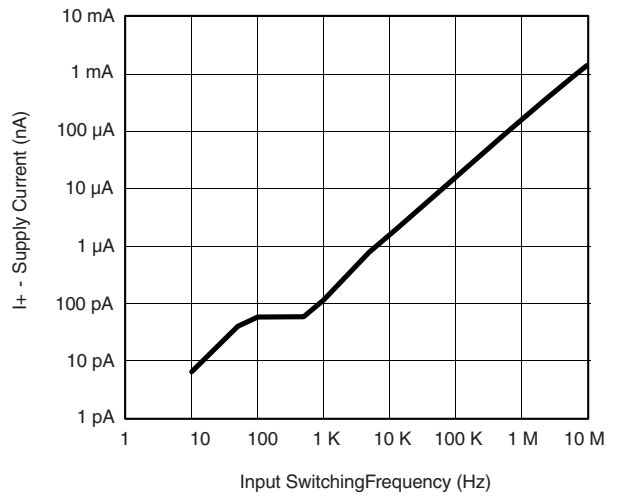
$r_{DS(on)}$ vs. Analog and Power Voltage



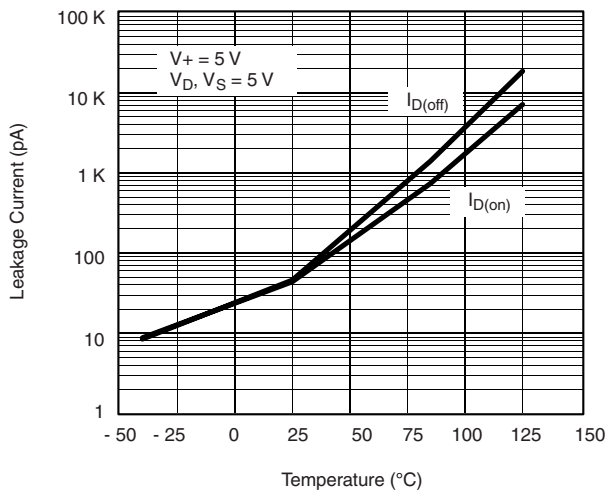
$r_{DS(on)}$ vs. Analog Voltage and Temperature



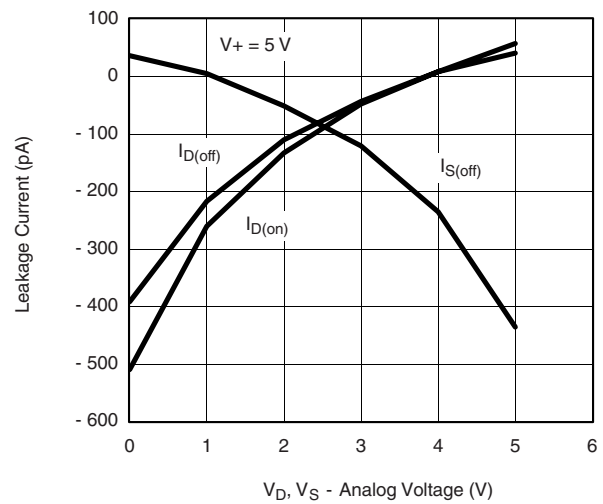
Supply Current vs. Temperature



Supply Current vs. Input Switching Frequency

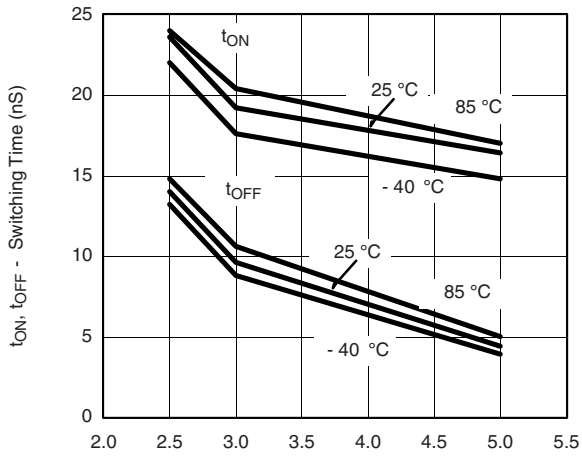


Leakage Current vs. Temperature

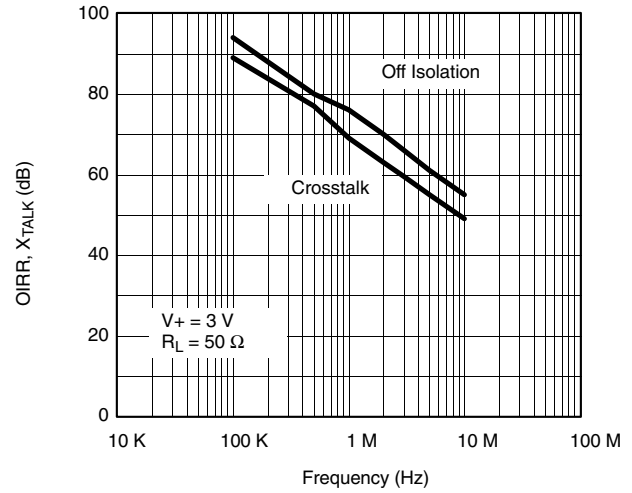


Leakage vs. Analog Voltage

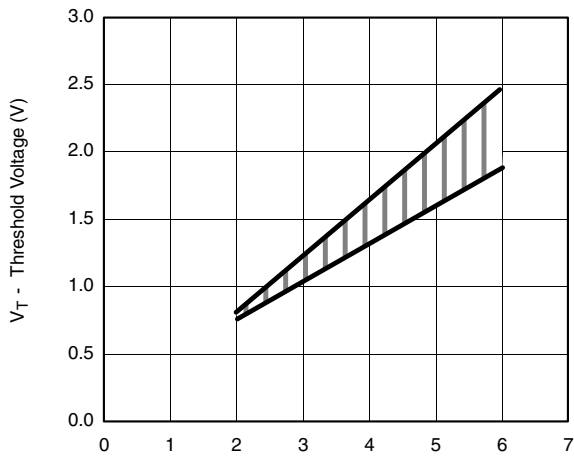
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



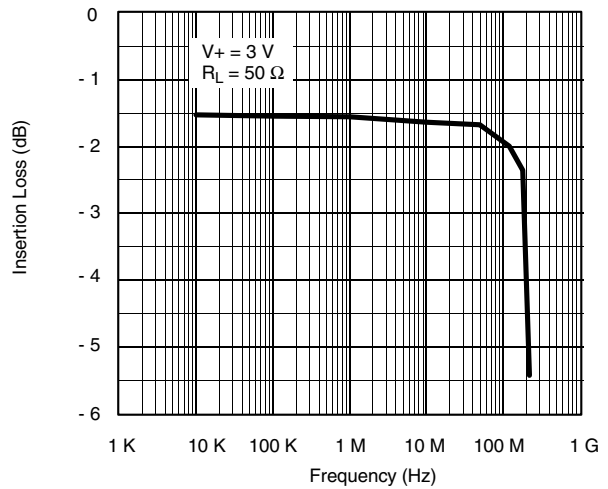
V+ - Supply Voltage (V)
Switching Time vs. Temperature and Supply Voltage



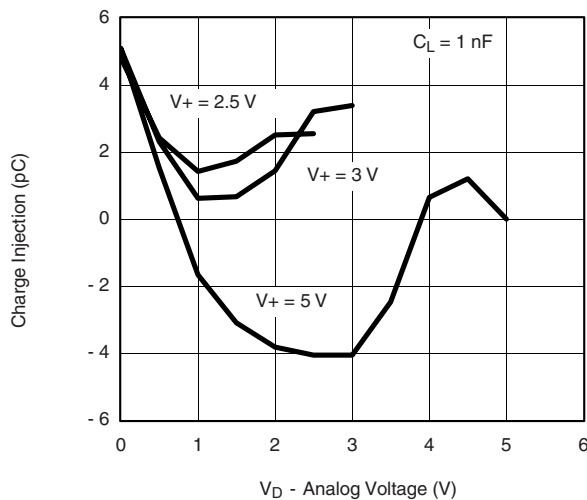
Crosstalk and Off Isolation vs. Frequency



V+ - Supply Voltage (V)
Input Switching Threshold vs. Supply Voltage

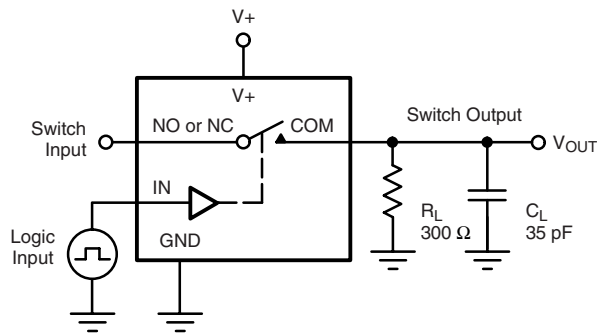


Insertion Loss vs. Frequency



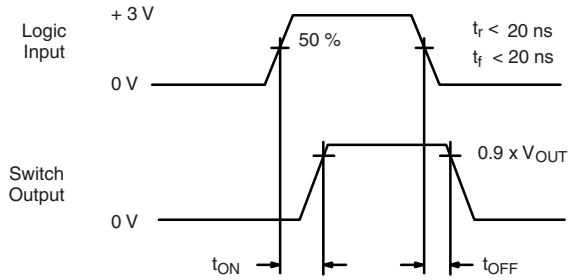
Charge Injection vs. Analog Voltage

TEST CIRCUITS



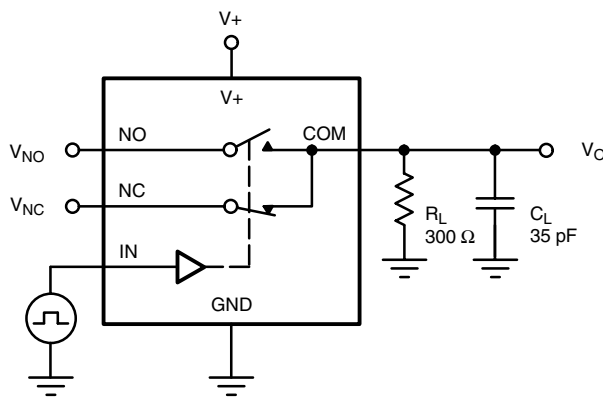
C_L (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM} \left(\frac{R_L}{R_L + R_{ON}} \right)$$



Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

Figure 1. Switching Time



C_L (includes fixture and stray capacitance)

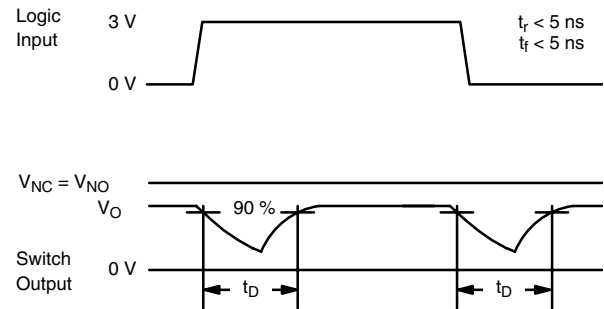
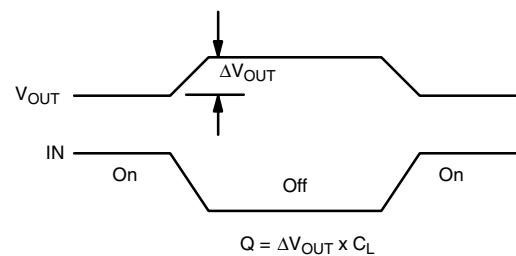
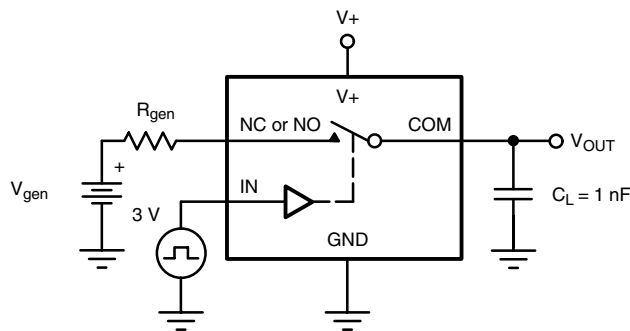


Figure 2. Break-Before-Make Interval



IN depends on switch configuration: input polarity determined by sense of switch.

Figure 3. Charge Injection

TEST CIRCUITS

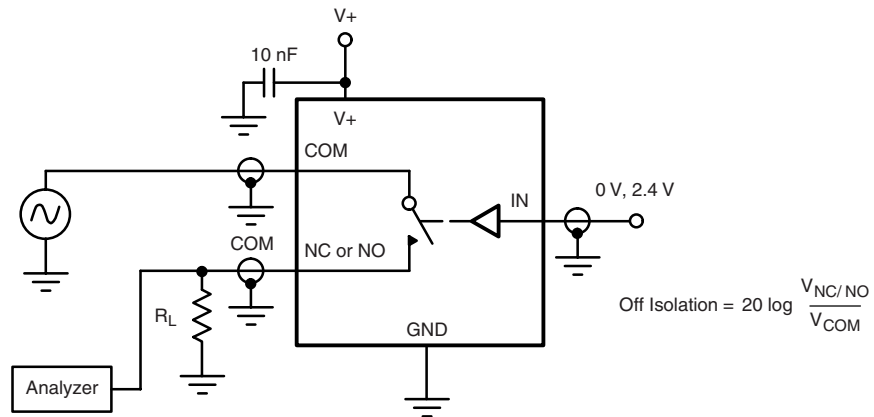


Figure 4. Off-Isolation

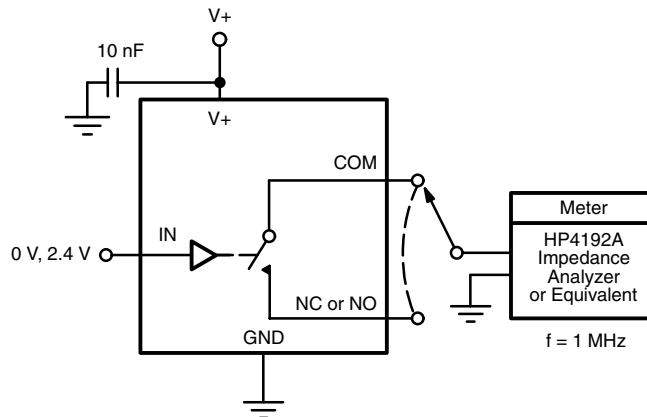


Figure 5. Channel Off/On Capacitance

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