

NTR3A052PZ

Power MOSFET

–20 V, –3.6 A, Single P–Channel
SOT–23 Package

Features

- Leading –20 V Trench for Low $R_{DS(on)}$
- –1.8 V Rated for Low Voltage Gate Drive
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Power Load Switch

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DS}	–20	V
Gate-to-Source Voltage	V_{GS}	± 8	V
Continuous Drain Current (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	I_D –3.3 A
		$T_A = 70^\circ\text{C}$	
	$t \leq 5\text{ s}$	$T_A = 25^\circ\text{C}$	
		$T_A = 70^\circ\text{C}$	
Power Dissipation (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	P_D 0.72 W
	$t \leq 5\text{ s}$		
Continuous Drain Current (Note 2)	Steady State	$T_A = 25^\circ\text{C}$	I_D –2.5 A
		$T_A = 70^\circ\text{C}$	
Power Dissipation (Note 2)		$T_A = 25^\circ\text{C}$	P_D 0.42 W
Pulsed Drain Current	$t_p = 10\text{ }\mu\text{s}$	I_{DM} –13	A
Operating Junction and Storage Temperature	T_J, T_{STG}	–55 to 150	$^\circ\text{C}$
Source Current (Body Diode)	I_S	–1.3	A
Lead Temperature for Soldering Purposes (1/8 in from case for 10 s)	T_L	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	174	$^\circ\text{C/W}$
Junction-to-Ambient – $t \leq 5\text{ s}$ (Note 1)	$R_{\theta JA}$	145	
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	300	

1. Surface-mounted on FR4 board using 1 in sq. pad size (Cu area = 727 mm sq., 1 oz).
2. Surface-mounted on FR4 board using minimum pad size (Cu area = 3.8 mm sq., 1 oz).

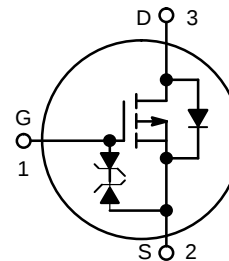


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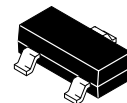
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$V_{(BR)DS}$	$R_{DS(on)}$ Max	I_D MAX
–20 V	47 m Ω @ –4.5 V	–3.6 A
	63 m Ω @ –2.5 V	
	100 m Ω @ –1.8 V	

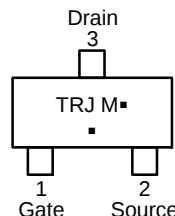
P–Channel MOSFET



MARKING DIAGRAM & PIN ASSIGNMENT



**SOT–23
CASE 318
STYLE 21**



TRJ = Specific Device Code
M = Date Code*
■ = Pb–Free Package

(Note: Microdot may be in either location)

*Date Code orientation may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping†
NTR3A052PZT1G	SOT–23 (Pb–Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NTR3A052PZ

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-20			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = -250\text{ }\mu\text{A}$, ref to 25°C		16		mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = -20\text{ V}$	$T_J = 25^\circ\text{C}$		-1	μA
			$T_J = 125^\circ\text{C}$		-100	μA
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 8\text{ V}$			± 10	μA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = -250\text{ }\mu\text{A}$	-0.4		-1.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			3.3		mV/ $^\circ\text{C}$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = -4.5\text{ V}, I_D = -3.5\text{ A}$		33	47	m Ω
		$V_{GS} = -2.5\text{ V}, I_D = -3.0\text{ A}$		41	63	
		$V_{GS} = -1.8\text{ V}, I_D = -2.0\text{ A}$		54	100	
		$V_{GS} = -1.5\text{ V}, I_D = -0.5\text{ A}$		69		
Forward Transconductance	g_{FS}	$V_{DS} = -5\text{ V}, I_D = -3.5\text{ A}$		16		S

CHARGES AND CAPACITANCES

Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = -4\text{ V}$		1243		pF
Output Capacitance	C_{oss}			194		
Reverse Transfer Capacitance	C_{rss}			158		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -4.5\text{ V}, V_{DS} = -4\text{ V}, I_D = -3.5\text{ A}$		11.9		nC
Threshold Gate Charge	$Q_{G(TH)}$			0.7		
Gate-to-Source Charge	Q_{GS}			1.7		
Gate-to-Drain Charge	Q_{GD}			2.6		

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = -4.5\text{ V}, V_{DS} = -4\text{ V}, I_D = -1.2\text{ A}, R_G = 6.0\text{ }\Omega$		8.0		ns
Rise Time	t_r			15		
Turn-Off Delay Time	$t_{d(off)}$			38		
Fall Time	t_f			42		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V},$ $I_S = -1.2\text{ A}$	$T_J = 25^{\circ}\text{C}$		-0.7	-1.2	V
			$T_J = 125^{\circ}\text{C}$		-0.6		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, dI_{SD}/dt = 100\text{ A}/\mu\text{s},$ $I_S = -1.2\text{ A}$		18		ns	
Charge Time	t_a			8.0			
Discharge Time	t_b			10			
Reverse Recovery Charge	Q_{RR}				6.9		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: pulse width $\leq 300\text{ ms}$, duty cycle $\leq 2\%$.

4. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

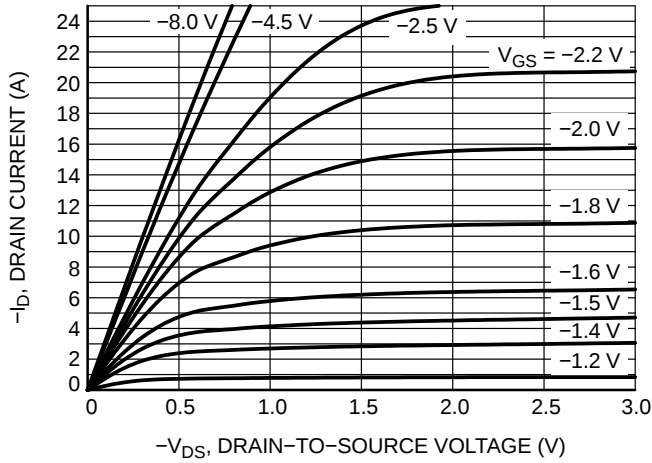


Figure 1. On-Region Characteristics

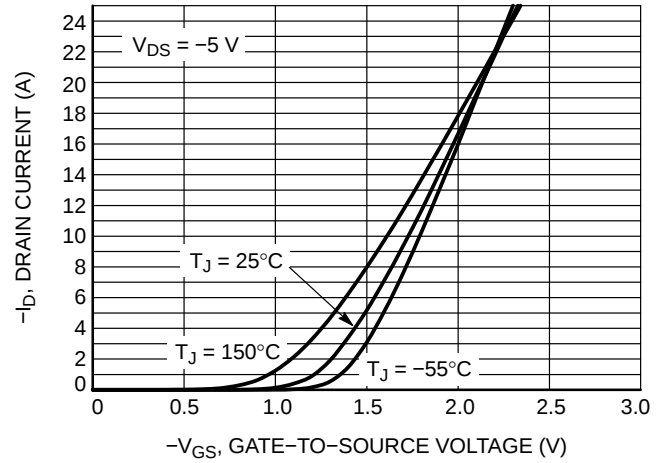


Figure 2. Transfer Characteristics

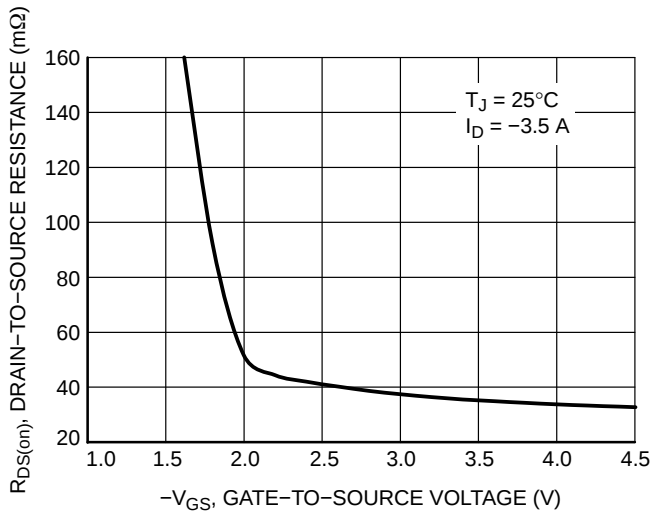


Figure 3. On-Resistance vs. Gate-to-Source Voltage

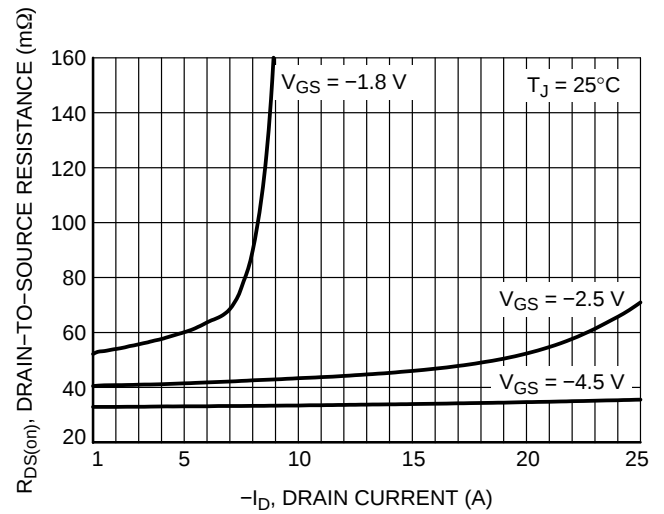


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

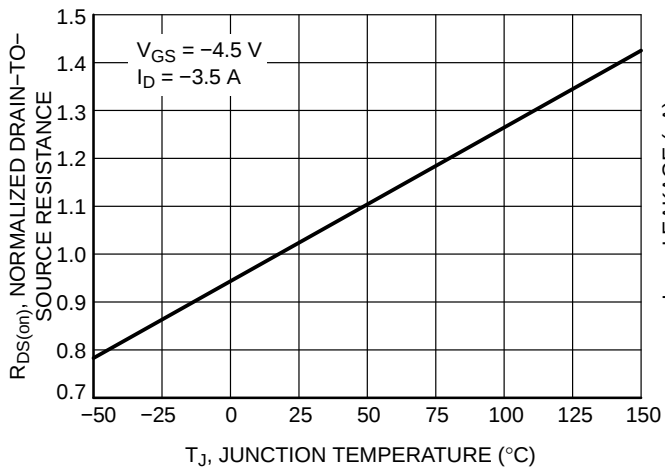


Figure 5. On-Resistance Variation with Temperature

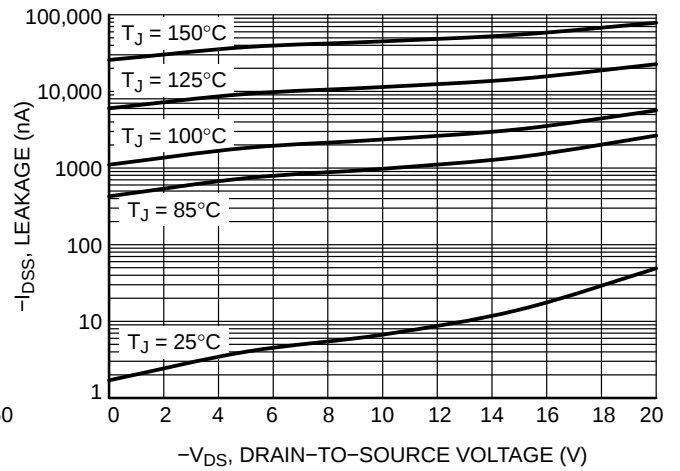


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

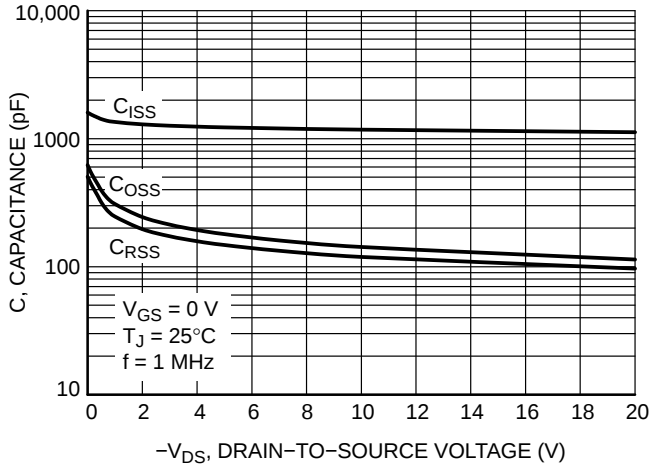


Figure 7. Capacitance Variation

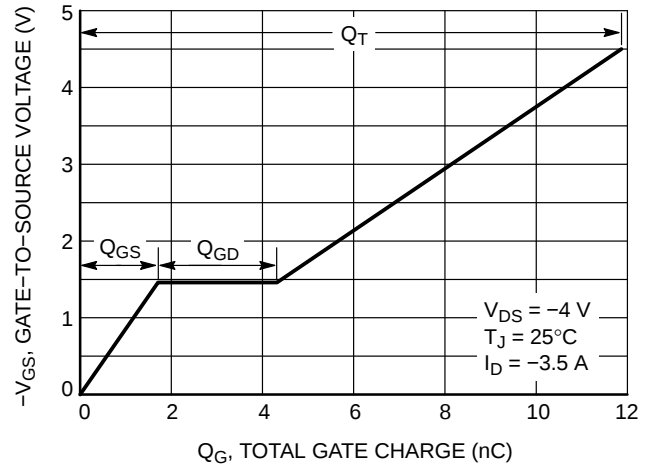


Figure 8. Gate-to-Source vs. Total Charge

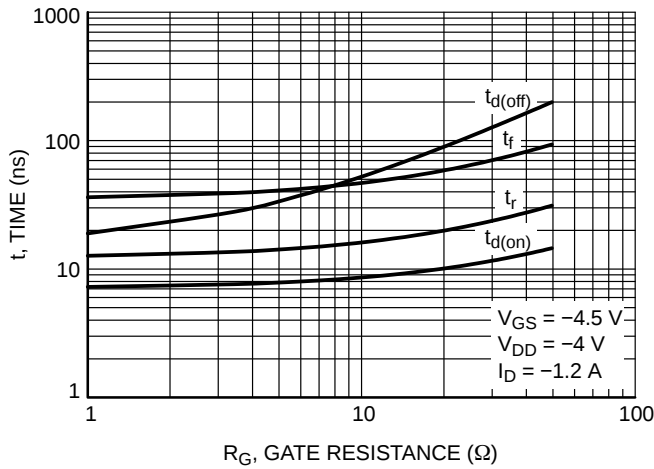


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

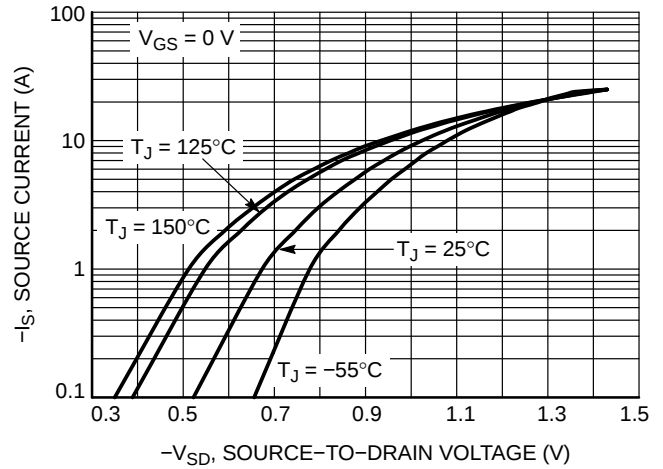


Figure 10. Diode Forward Voltage vs. Current

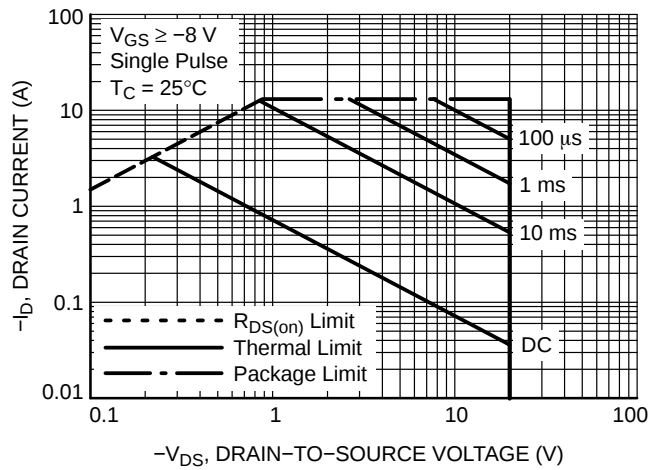


Figure 11. Maximum Rated Forward Biased Safe Operating Area

TYPICAL CHARACTERISTICS

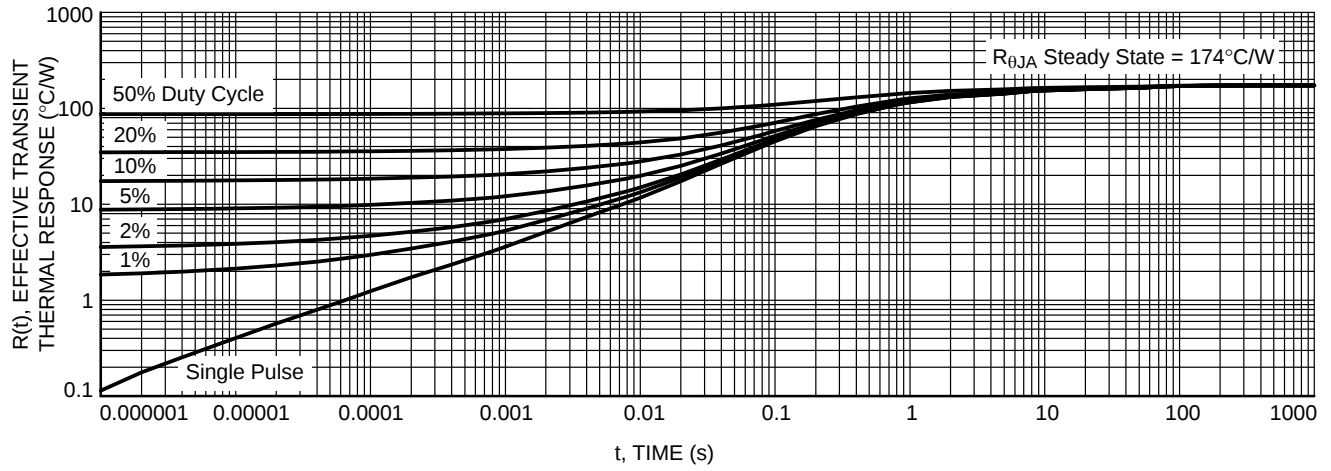
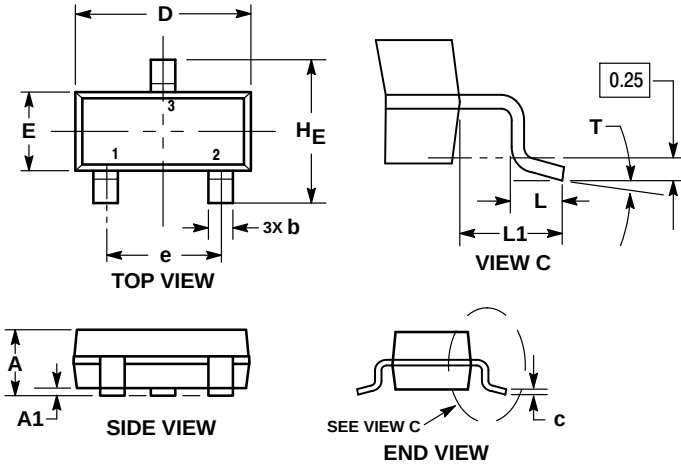


Figure 12. Thermal Impedance (Junction-to-Ambient)

NTR3A052PZ

PACKAGE DIMENSIONS

SOT-23 (TO-236) CASE 318-08 ISSUE AR



NOTES:

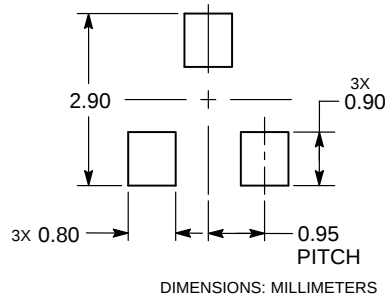
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1.00	1.11	0.035	0.039	0.044
A1	0.01	0.06	0.10	0.000	0.002	0.004
b	0.37	0.44	0.50	0.015	0.017	0.020
c	0.08	0.14	0.20	0.003	0.006	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.080
L	0.30	0.43	0.55	0.012	0.017	0.022
L1	0.35	0.54	0.69	0.014	0.021	0.027
H _E	2.10	2.40	2.64	0.083	0.094	0.104
T	0°	---	10°	0°	---	10°

STYLE 21:

1. GATE
2. SOURCE
3. DRAIN

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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