

SN74F574 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

SDFS005A – D3034, SEPTEMBER 1987 – REVISED OCTOBER 1993

- Eight D-Type Flip-Flops in a Single Package
- 3-State Bus-Driving True Outputs
- Full Parallel Access for Loading
- Buffered Control Inputs
- Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs

description

This 8-bit flip-flop features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

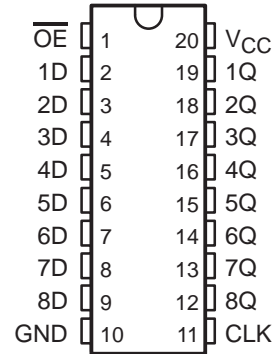
The eight flip-flops of the SN74F574 are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the Q outputs will be set to the logic levels that were set up at the data (D) inputs.

A buffered output enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output enable (\overline{OE}) does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74F574 is characterized for operation from 0°C to 70°C.

DW OR N PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each flip-flop)

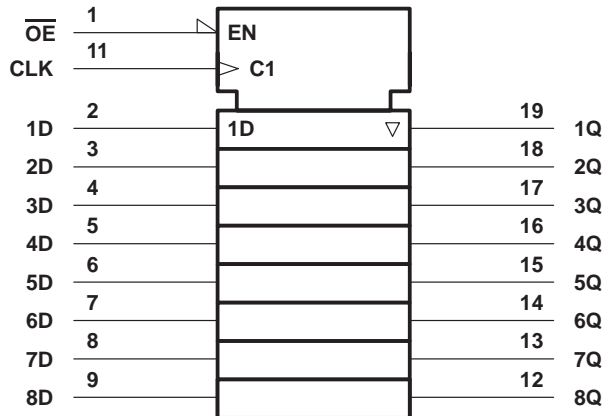
| INPUTS | | | OUTPUT |
|-----------------|-----|---|--------|
| \overline{OE} | CLK | D | Q |
| L | ↑ | H | H |
| L | ↑ | L | L |
| L | L | X | Q_0 |
| H | X | X | Z |

SN74F574

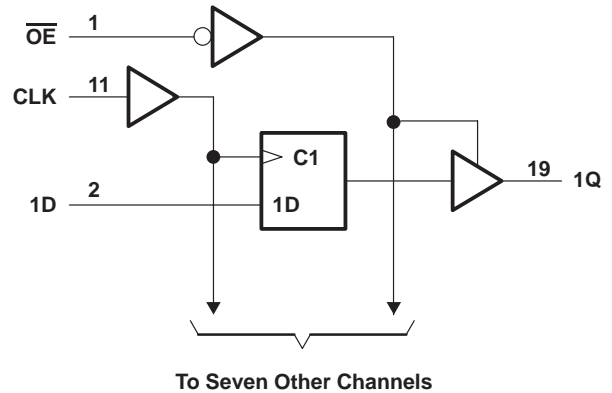
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logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

| | |
|--|--------------------|
| Supply voltage range, V_{CC} | -0.5 V to 7 V |
| Input voltage range, V_I (see Note 1) | -1.2 V to 7 V |
| Input current range | -30 mA to 5 mA |
| Voltage range applied to any output in the disabled or power-off state | -0.5 V to 5.5 V |
| Voltage range applied to any output in the high state | -0.5 V to V_{CC} |
| Current into any output in the low state | 48 mA |
| Operating free-air temperature range | 0°C to 70°C |
| Storage temperature range | -65°C to 150°C |

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input-voltage ratings may be exceeded provided the input-current ratings are observed.

recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|----------|--------------------------------|-----|-----|-----|------|
| V_{CC} | Supply voltage | 4.5 | 5 | 5.5 | V |
| V_{IH} | High-level input voltage | 2 | | | V |
| V_{IL} | Low-level input voltage | | | 0.8 | V |
| I_{IK} | Input clamp current | | | -18 | mA |
| I_{OH} | High-level output current | | | -3 | mA |
| I_{OL} | Low-level output current | | | 24 | mA |
| T_A | Operating free-air temperature | 0 | | 70 | °C |

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|-------------------|----------------------------|--|-----|------|------|---------------|
| V_{IK} | $V_{CC} = 4.5\text{ V}$, | $I_I = -18\text{ mA}$ | | | -1.2 | V |
| V_{OH} | $V_{CC} = 4.5\text{ V}$ | $I_{OH} = -1\text{ mA}$ | 2.5 | 3.4 | | V |
| | | $I_{OH} = -3\text{ mA}$ | 2.4 | 3.3 | | |
| | $V_{CC} = 4.75\text{ V}$, | $I_{OH} = -1\text{ mA to } -3\text{ mA}$ | 2.7 | | | |
| V_{OL} | $V_{CC} = 4.5\text{ V}$, | $I_{OL} = 24\text{ mA}$ | | 0.35 | 0.5 | V |
| I_{OZH} | $V_{CC} = 5.5\text{ V}$, | $V_O = 2.7\text{ V}$ | | | 50 | μA |
| I_{OZL} | $V_{CC} = 5.5\text{ V}$, | $V_O = 0.5\text{ V}$ | | | -50 | μA |
| I_I | $V_{CC} = 5.5\text{ V}$, | $V_I = 7\text{ V}$ | | | 0.1 | mA |
| I_{IH} | $V_{CC} = 5.5\text{ V}$, | $V_I = 2.7\text{ V}$ | | | 20 | μA |
| I_{IL} | $V_{CC} = 5.5\text{ V}$, | $V_I = 0.5\text{ V}$ | | | -0.6 | mA |
| I_{OS}^\ddagger | $V_{CC} = 5.5\text{ V}$, | $V_O = 0$ | -60 | | -150 | mA |
| I_{CCZ} | $V_{CC} = 5.5\text{ V}$, | See Note 2 | | 55 | 86 | mA |

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: I_{CCZ} is measured with \overline{OE} at 4.5 V and all other inputs grounded.

timing requirements

| | | $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ | | $V_{CC} = 4.5\text{ V to } 5.5\text{ V}$, $T_A = \text{MIN to MAX}^\S$ | | UNIT |
|--------------------|------------------------|---|-----|--|-----|------|
| | | MIN | MAX | MIN | MAX | |
| f_{clock} | Clock frequency | 0 | 100 | 0 | 100 | MHz |
| t_w | Pulse duration | CLK high | 7 | 7 | | ns |
| | | CLK low | 6 | 6 | | |
| t_{su} | Setup time before CLK↑ | Data high | 2 | 2 | | ns |
| | | Data low | 2 | 2 | | |
| t_h | Hold time after CLK↑ | Data high | 2 | 2 | | ns |
| | | Data low | 2 | 2 | | |

switching characteristics (see Note 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $R_L = 500\ \Omega$, $T_A = 25^\circ\text{C}$ | | | $V_{CC} = 4.5\text{ V to } 5.5\text{ V}$, $C_L = 50\text{ pF}$, $R_L = 500\ \Omega$, $T_A = \text{MIN to MAX}^\S$ | | UNIT |
|------------------|-----------------|----------------|--|-----|------|---|------|------|
| | | | MIN | TYP | MAX | MIN | MAX | |
| f_{max} | | | 100 | | | 100 | | MHz |
| t_{PLH} | CLK | Any Q | 3.2 | 6.1 | 8.5 | 3.2 | 10 | ns |
| t_{PHL} | | | 3.2 | 6.1 | 8.5 | 3.2 | 10 | |
| t_{PZH} | \overline{OE} | Any Q | 1.2 | 8.6 | 11.5 | 1.2 | 12.5 | ns |
| t_{PZL} | | | 1.2 | 4.9 | 7.5 | 1.2 | 8.5 | |
| t_{PHZ} | \overline{OE} | Any Q | 1.2 | 4.9 | 7 | 1.2 | 8 | ns |
| t_{PLZ} | | | 1.2 | 3.9 | 5.5 | 1.2 | 6.5 | |

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 3: Load circuits and waveforms are shown in Section 1.



PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| SN74F574DW | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74F574DWE4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74F574DWG4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74F574DWR | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74F574DWRE4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74F574DWRG4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74F574N | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN74F574NE4 | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN74F574NSR | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74F574NSRE4 | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74F574NSRG4 | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

TAPE AND REEL INFORMATION

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74F574DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.0 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74F574NSR | SO | NS | 20 | 2000 | 330.0 | 24.4 | 8.2 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74F574DWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74F574NSR | SO | NS | 20 | 2000 | 367.0 | 367.0 | 45.0 |

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G20)

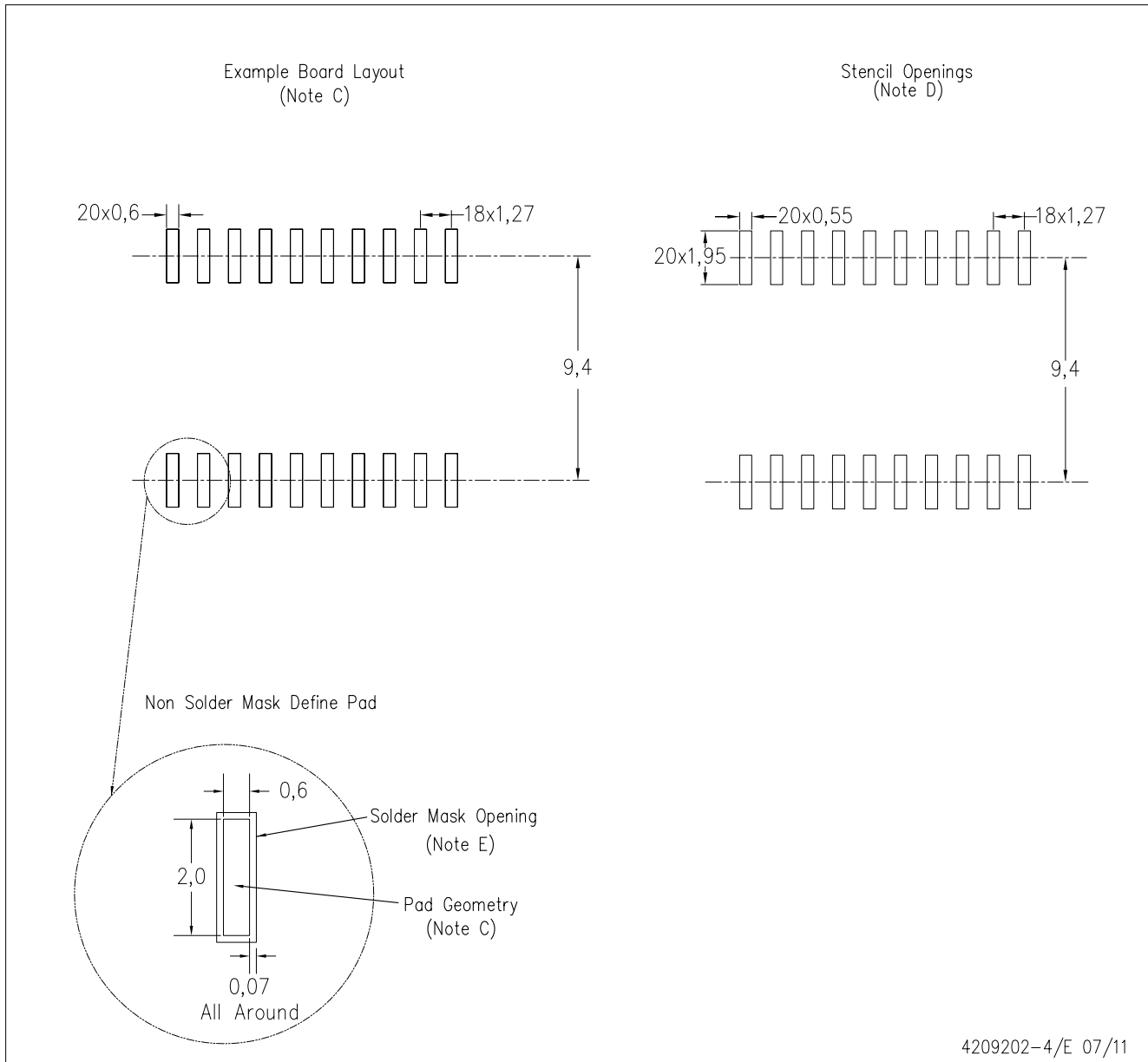
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-013 variation AC.

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



4209202-4/E 07/11

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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