



BUK965R8-100E

N-channel TrenchMOS logic level FET

28 July 2016

Product data sheet

1. General description

Logic level N-channel MOSFET in a SOT404 package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

2. Features and benefits

- AEC Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True logic level gate with $V_{gs(th)}$ rating of greater than 0.5V at 175 °C

3. Applications

- 12V, 24V and 48V Automotive systems
- Motors, lamps and solenoid control
- Start-Stop micro-hybrid applications
- Transmission control
- Ultra high performance power switching

4. Quick reference data

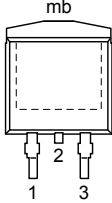
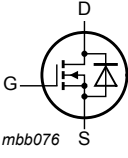
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$		-	-	100	V
I_D	drain current	$V_{GS} = 5\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	[1]	-	-	120	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1		-	-	349	W
Static characteristics							
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 5\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; Fig. 11		-	4.62	5.8	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	$V_{GS} = 5\text{ V}$; $I_D = 25\text{ A}$; $V_{DS} = 80\text{ V}$; Fig. 13 ; Fig. 14		-	51	-	nC

[1] Continuous current is limited by package.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 D2PAK (SOT404)	 mbb076
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK965R8-100E	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK965R8-100E	BUK965R8-100E

8. Limiting values

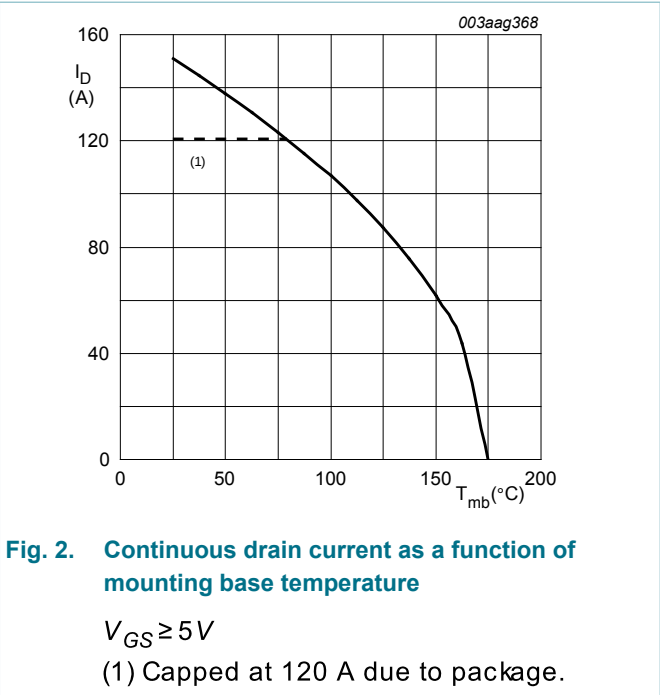
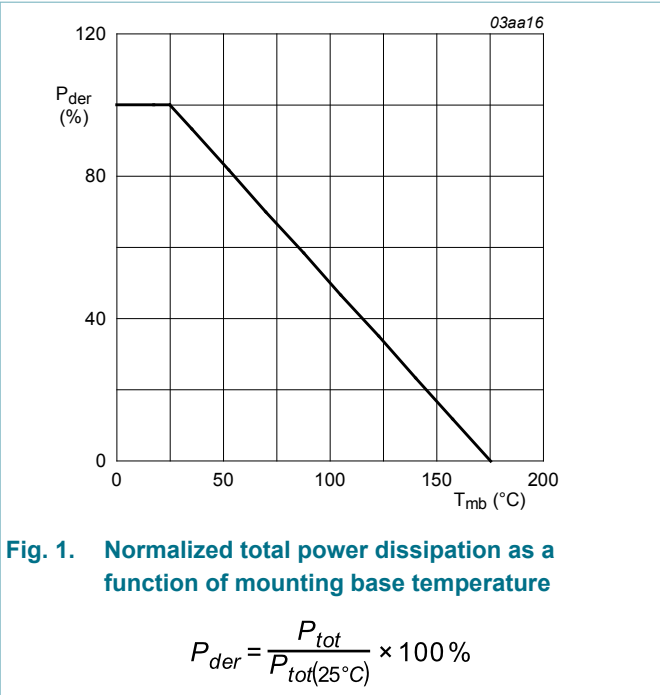
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$		-	100	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$		-	100	V
V_{GS}	gate-source voltage	$T_j \leq 175\text{ °C}$; DC		-10	10	V
		$T_j \leq 175\text{ °C}$; Pulsed	[1][2]	-15	15	V
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1		-	349	W
I_D	drain current	$T_{mb} = 25\text{ °C}$; $V_{GS} = 5\text{ V}$; Fig. 2	[3]	-	120	A
		$T_{mb} = 100\text{ °C}$; $V_{GS} = 5\text{ V}$; Fig. 2		-	105	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; Fig. 3		-	591	A
T_{stg}	storage temperature			-55	175	°C

Symbol	Parameter	Conditions		Min	Max	Unit
T _j	junction temperature			-55	175	°C
Source-drain diode						
I _S	source current	T _{mb} = 25 °C	[3]	-	120	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C		-	591	A
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 120 A; V _{sup} ≤ 100 V; R _{GS} = 50 Ω; V _{GS} = 5 V; T _{j(init)} = 25 °C; unclamped; Fig. 4	[4][5]	-	385	mJ

- [1] Accumulated pulse duration up to 50 hours delivers zero defect ppm
- [2] Significantly longer life times are achieved by lowering T_j and or V_{GS}
- [3] Continuous current is limited by package.
- [4] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [5] Refer to application note AN10273 for further information.



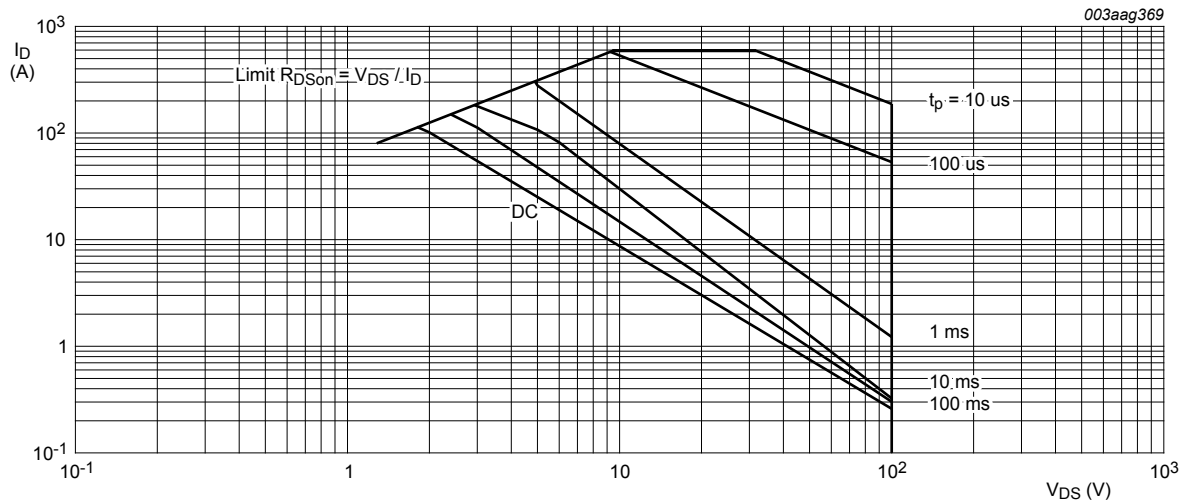


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25^{\circ}C$; I_{DM} is a single pulse

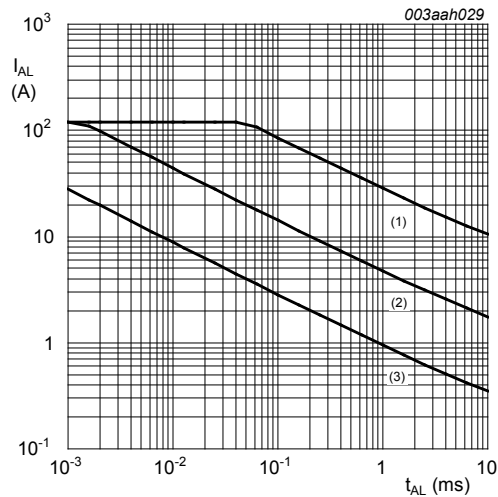


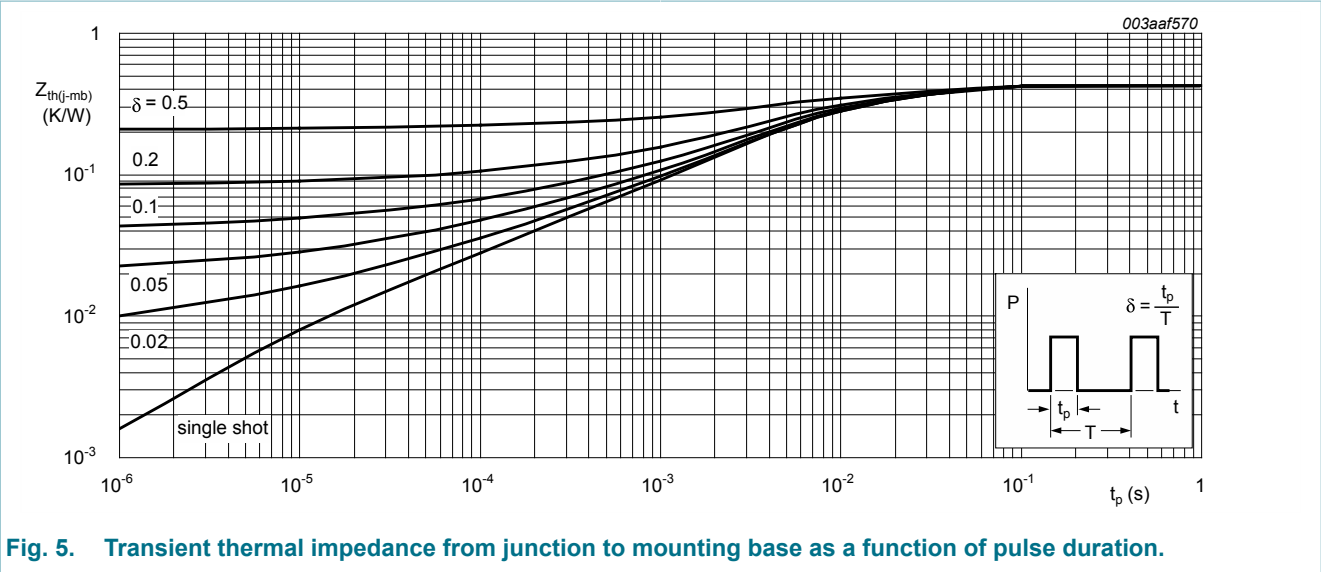
Fig. 4. Single-pulse and repetitive avalanche rating; avalanche current as a function of avalanche time

(1) $T_{j(init)} = 25^{\circ}C$; (2) $T_{j(init)} = 150^{\circ}C$; (3) Repetitive Avalanche

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	-	0.43	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint ; mounted on a printed-circuit board	-	50	-	K/W



10. Characteristics

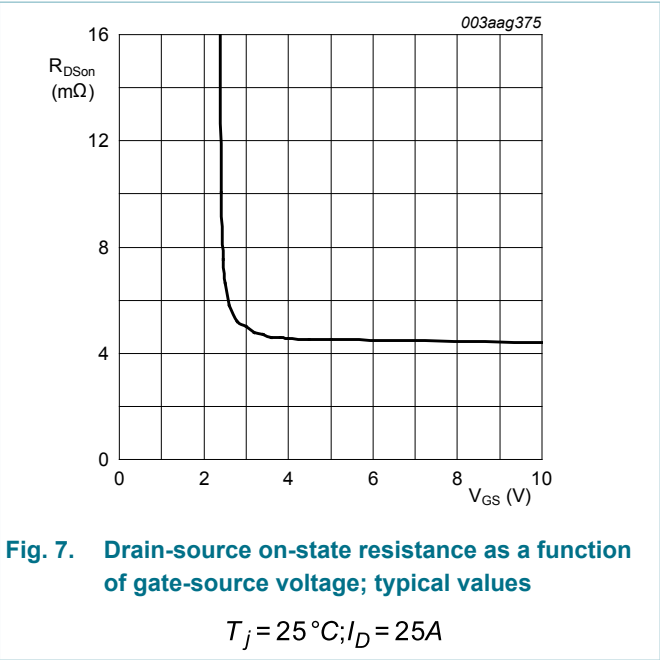
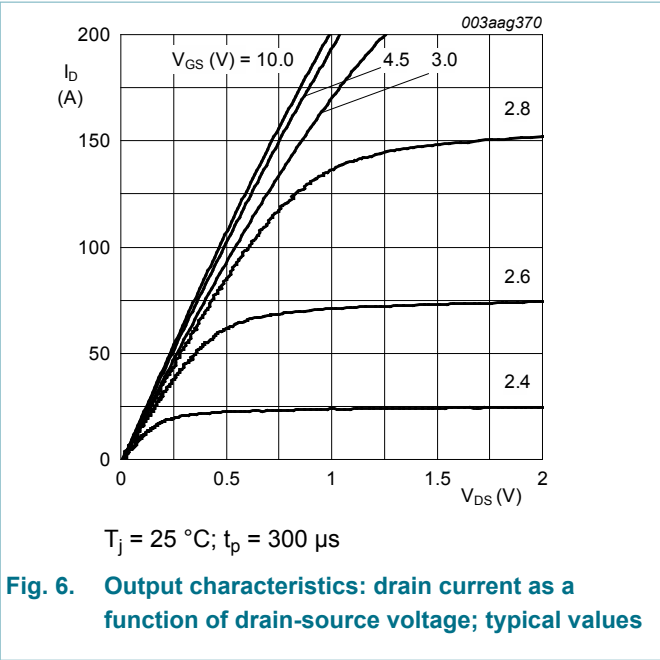
Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _J = 25 °C		100	-	-	V
		I _D = 250 μA; V _{GS} = 0 V; T _J = -55 °C		90	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; T _J = 25 °C; Fig. 9 ; Fig. 10		1.4	1.7	2.1	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _J = -55 °C; Fig. 9		-	-	2.45	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _J = 175 °C; Fig. 9		0.5	-	-	V
I _{DSS}	drain leakage current	V _{DS} = 100 V; V _{GS} = 0 V; T _J = 25 °C		-	0.05	1	μA
		V _{DS} = 100 V; V _{GS} = 0 V; T _J = 175 °C		-	-	500	μA
I _{GSS}	gate leakage current	V _{GS} = 10 V; V _{DS} = 0 V; T _J = 25 °C		-	2	100	nA
		V _{GS} = -10 V; V _{DS} = 0 V; T _J = 25 °C		-	2	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 5 V; I _D = 25 A; T _J = 25 °C; Fig. 11		-	4.62	5.8	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _J = 25 °C; Fig. 11		-	4.45	5.6	mΩ
		V _{GS} = 5 V; I _D = 25 A; T _J = 175 °C; Fig. 12 ; Fig. 11		-	-	16	mΩ
Dynamic characteristics							
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 80 V; V _{GS} = 5 V; Fig. 13 ; Fig. 14		-	133	-	nC
Q _{GS}	gate-source charge			-	23	-	nC

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Q_{GD}	gate-drain charge			-	51	-	nC
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V}; f = 1\text{ MHz};$ $T_j = 25\text{ }^{\circ}\text{C};$ Fig. 15		-	13100	17460	pF
C_{oss}	output capacitance			-	725	870	pF
C_{rss}	reverse transfer capacitance			-	450	620	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 80\text{ V}; R_L = 3.2\text{ }\Omega; V_{GS} = 5\text{ V};$ $R_{G(ext)} = 5\text{ }\Omega$		-	81	-	ns
t_r	rise time			-	168	-	ns
$t_{d(off)}$	turn-off delay time			-	237	-	ns
t_f	fall time			-	148	-	ns
L_D	internal drain inductance	from upper edge of drain mounting base to center of die		-	2.5	-	nH
L_S	internal source inductance	from source lead to source bonding pad		-	7.5	-	nH

Source-drain diode

V_{SD}	source-drain voltage	$I_S = 25\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^{\circ}\text{C};$ Fig. 16		-	0.77	1.2	V
t_{rr}	reverse recovery time	$I_S = 20\text{ A}; dI_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V};$ $V_{DS} = 25\text{ V}$		-	70	-	ns
Q_r	recovered charge			-	202	-	nC



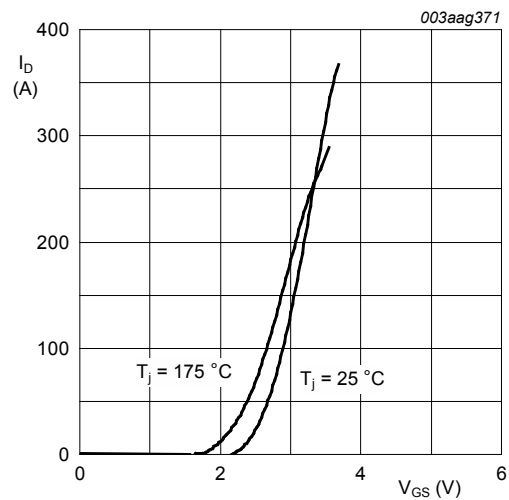


Fig. 8. Transfer characteristics: drain current as a function of gate-source voltage; typical values

$V_{DS} = 12\text{ V}$

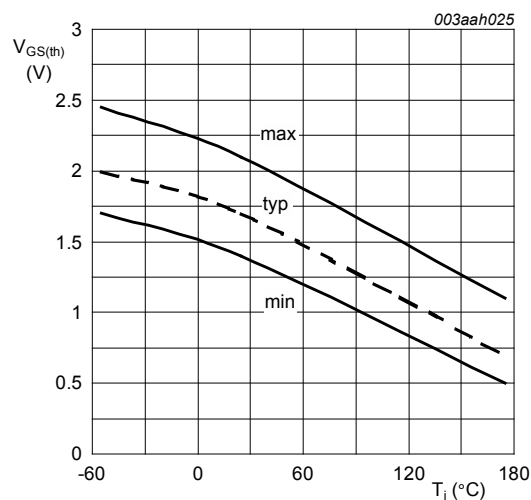


Fig. 9. Gate-source threshold voltage as a function of junction temperature

$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

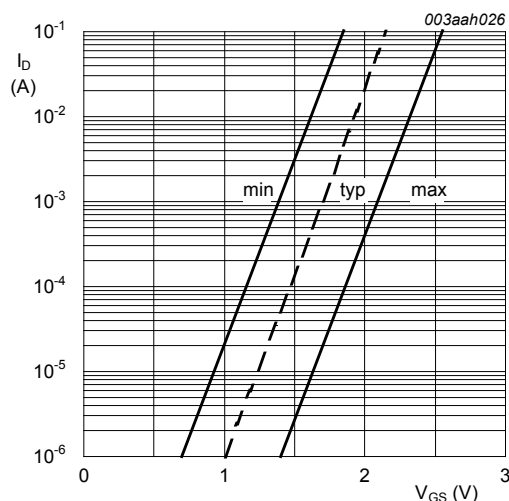


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

$T_J = 25\text{ °C}; V_{DS} = 5\text{ V}$

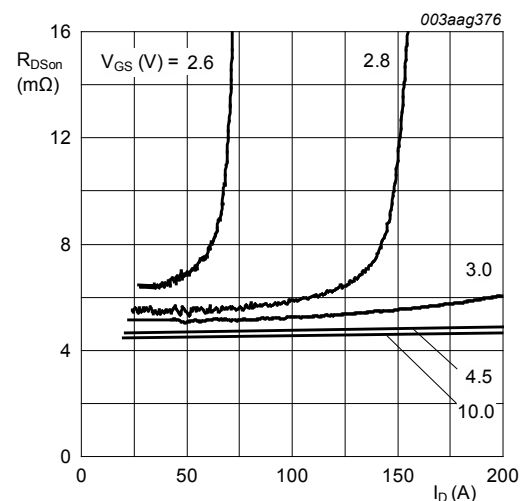


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

$T_J = 25\text{ °C}; t_p = 300\text{ }\mu\text{s}$

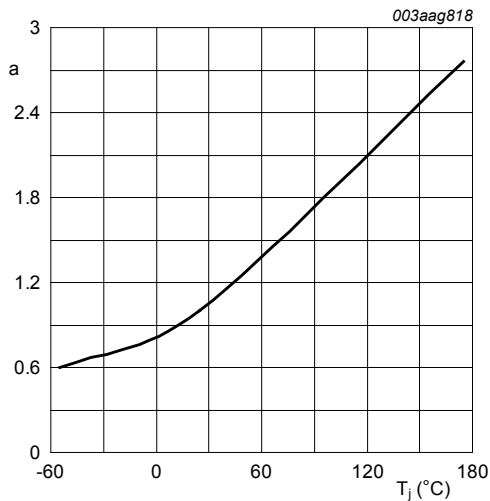


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon}(25\text{ }^{\circ}\text{C})}$$

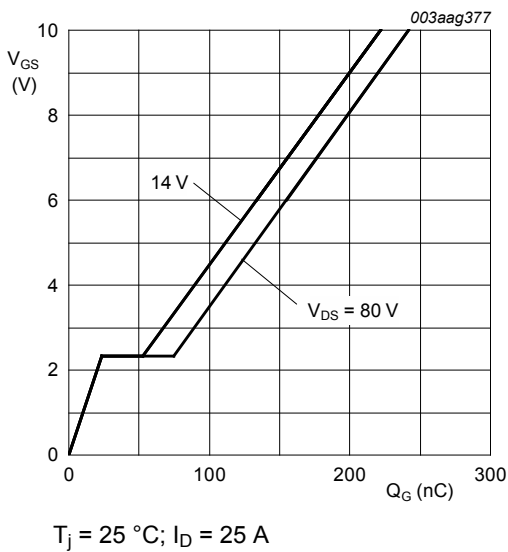


Fig. 14. Gate-source voltage as a function of gate charge; typical values

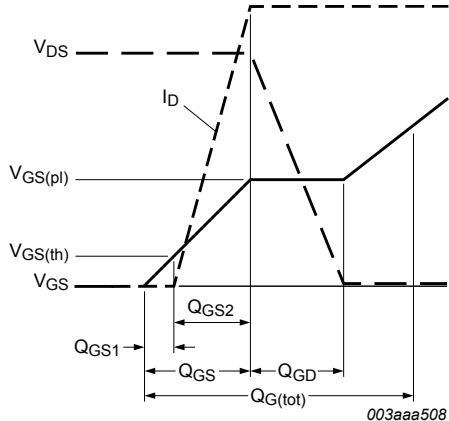


Fig. 13. Gate charge waveform definitions

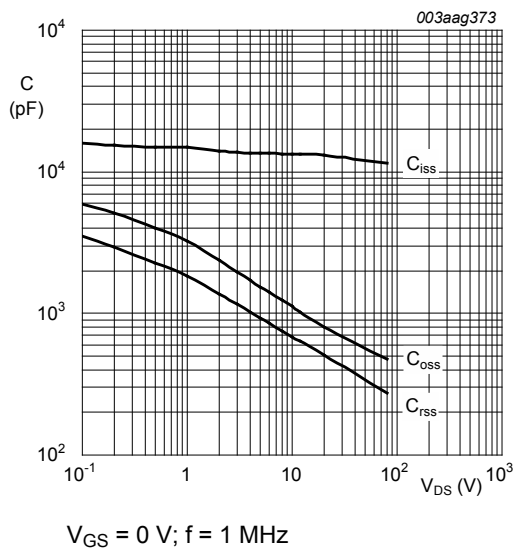
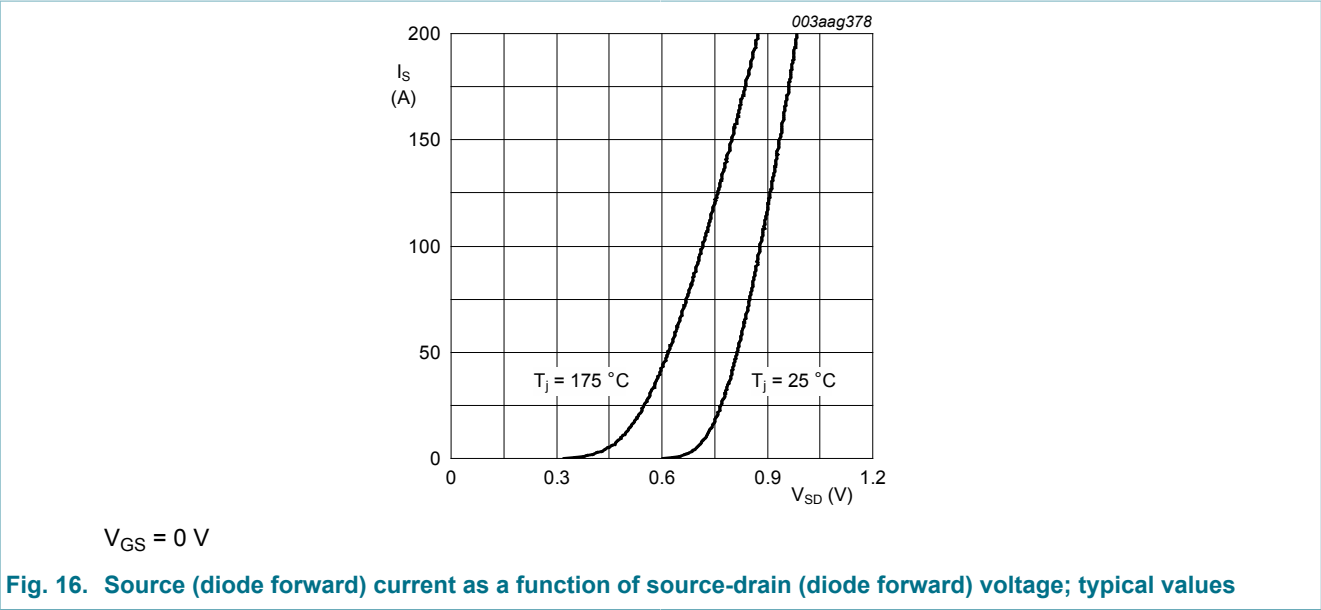


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



11. Package outline

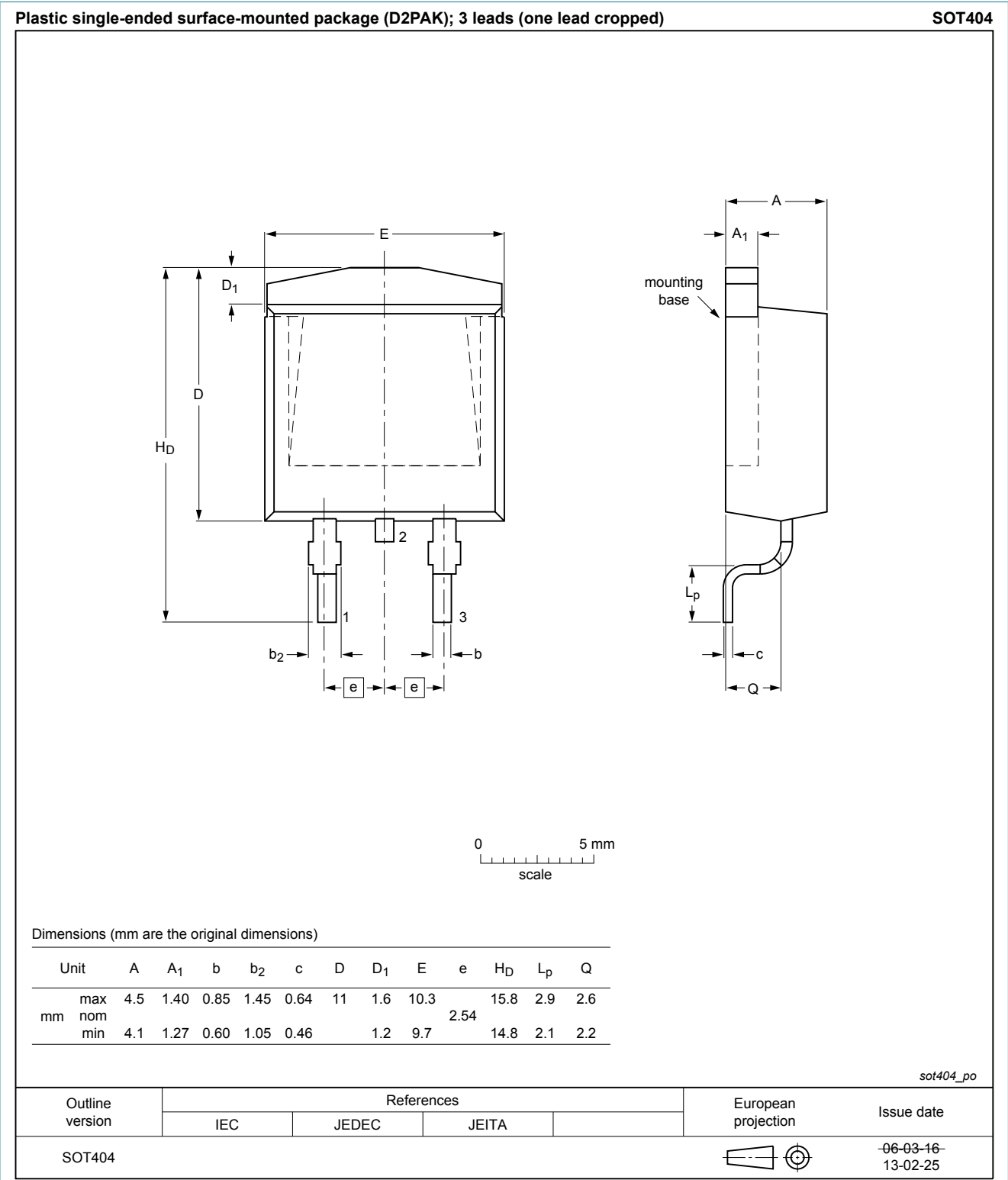


Fig. 17. Package outline D2PAK (SOT404)

12. Legal information

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Document status [1][2]	Product status [3]	Definition
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Date of release: 28 July 2016



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