# EFM8 Universal Bee 2 MCU
# EFM8UB2 Data Sheet

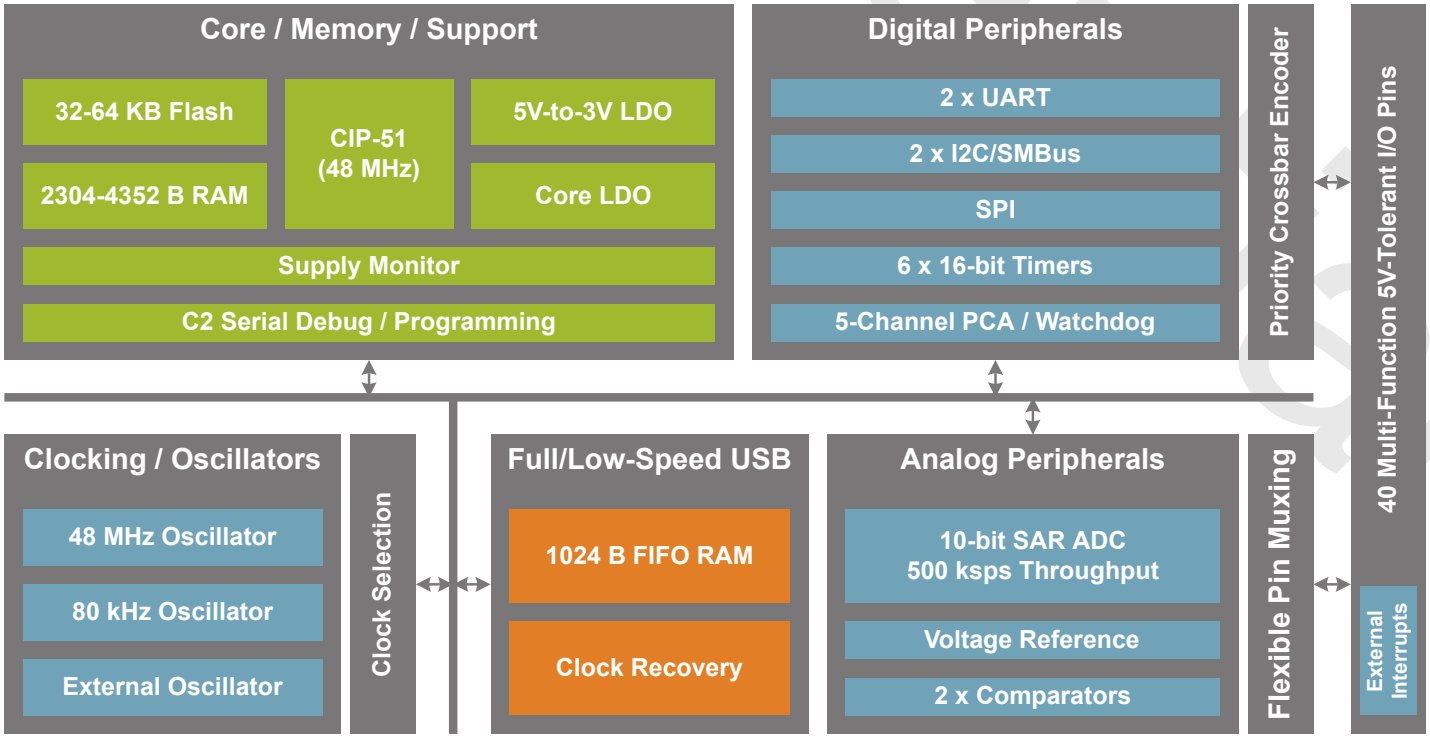
The EFM8UB2, part of the Universal Bee family of MCUs, is the world's most integrated mixed-signal 8-bit microcontroller with USB. Combining a high precision oscillator, clock recovery circuit, and integrated transceiver, the EFM8UB2 requires no external component for any full speed USB applications.

The EFM8UB2 has a fully-differential 10-bit ADC, precision oscillators, comparators, temperature sensor and voltage reference. The priority Crossbar enables the EFM8UB2 devices to operate in small packages by assigning only the desired peripherals to pins in a pre-defined order to eliminate pin conflicts. The EFM8UB2 creates its own class of high value and efficient USB controller with 64 or 32 kB flash sizes coupled with up to 4352-byte RAM. The EFM8UB2 is available in 32-pin QFN as well as hand solderable 48-pin TQFP and 32-pin LQFP packages.

For more details on the peripherals available on the device, see the System Overview chapter.

**KEY FEATURES**

- Pipelined 8-bit 8051 MCU Core with 48 MHz maximum operating frequency
- Crystal-less full speed/low speed USB 2.0 compliant controller with 1 kB buffer memory
- One single-ended and differential 10-bit ADC and two analog comparators
- Internal 48 MHz oscillator with ±0.25% accuracy with USB clock recovery supports crystal-free USB and UART operation
- 2 UARTs, SPI, 2 SMBus/I2C serial communications





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# 1. Electrical Specifications

## 1.1 Electrical Characteristics

All electrical parameters in all tables are specified under the conditions listed in Table 1.1 Recommended Operating Conditions on page 1, unless stated otherwise.

**Table 1.1. Recommended Operating Conditions**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Operating Supply Voltage on VDD | $V_{DD}$ | | 2.7[2] | 3.3 | 3.6 | V |
| Operating Supply Voltage on VREGIN | $V_{REGIN}$ | | 2.7 | — | 5.25 | V |
| System Clock Frequency | $f_{SYSCLK}$ | | 0 | — | 48 | MHz |
| Operating Ambient Temperature | $T_A$ | | -40 | — | 85 | °C |

**Note:**
1. All voltages with respect to GND
2. The USB specification requires 3.0 V minimum supply voltage.

**Table 1.2. Power Consumption**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Digital Core Supply Current | | | | | | |
| Normal Mode-Full speed with code executing from flash | $I_{DD}$ | $F_{SYSCLK}$ = 48 MHz[2] | — | 12 | 14 | mA |
| | | $F_{SYSCLK}$ = 24 MHz[2] | — | 7 | 8 | mA |
| | | $F_{SYSCLK}$ = 80 kHz[3] | — | 280 | — | µA |
| Idle Mode—Core halted with peripherals running | $I_{DD}$ | $F_{SYSCLK}$ = 48 MHz[2] | — | 6.5 | 8 | mA |
| | | $F_{SYSCLK}$ = 24 MHz[2] | — | 3.5 | 5 | mA |
| | | $F_{SYSCLK}$ = 80 kHz[3] | — | 220 | — | µA |
| Suspend Mode-Core halted and high frequency clocks stopped, Supply monitor off. Regulators in low-power mode. | $I_{DD}$ | LFO Running | — | 105 | — | µA |
| | | LFO Stopped | — | 100 | — | µA |
| Stop Mode—Core halted and all clocks stopped, Regulators in low-power mode, Supply monitor off. | $I_{DD}$ | | — | 100 | — | µA |
| Shutdown Mode—Core halted and all clocks stopped,Regulators Off, Supply monitor off. | $I_{DD}$ | | — | 0.25 | — | µA |
| Analog Peripheral Supply Currents | | | | | | |
| High-Frequency Oscillator 0 | $I_{HFOSC0}$ | Operating at 48 MHz, $T_A$ = 25 °C | — | 900 | — | µA |
| Low-Frequency Oscillator | $I_{LFOSC}$ | Operating at 80 kHz, $T_A$ = 25 °C | — | 5 | — | µA |
| ADC0 Supply Current | $I_{ADC}$ | Operating at 500 ksps $V_{DD}$ = 3.0 V | — | 750 | 1000 | µA |

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| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| On-chip Precision Reference | $I_{VREFP}$ | | — | 75 | — | µA |
| Temperature Sensor | $I_{TSENSE}$ | | — | 35 | — | µA |
| Comparator 0 (CMP0, CMP1) | $I_{CMP}$ | CPMD = 11 | — | 1 | — | µA |
| | | CPMD = 10 | — | 4 | — | µA |
| | | CPMD = 01 | — | 10 | — | µA |
| | | CPMD = 00 | — | 20 | — | µA |
| Voltage Supply Monitor (VMON0) | $I_{VMON}$ | | — | 15 | 50 | µA |
| Regulator Bias Currents | $I_{VREG}$ | Both Regulators in Normal Mode | — | 200 | — | µA |
| | | Both Regulators in Low Power Mode | — | 100 | — | µA |
| | | 5 V Regulator Off, Internal LDO in Low Power Mode | — | 150 | — | µA |
| USB (USB0) Full-Speed | $I_{USB}$ | Active | — | 8 | — | mA |

**Note:**
1. Currents are additive. For example, where $I_{DD}$ is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
2. Includes supply current from regulators, supply monitor, and High Frequency Oscillator.
3. Includes supply current from regulators, supply monitor, and Low Frequency Oscillator.

**Table 1.3. Reset and Supply Monitor**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| VDD Supply Monitor Threshold | $V_{VDDM}$ | | 2.60 | 2.65 | 2.70 | V |
| VDD Ramp Time | $t_{RMP}$ | Time to $V_{DD}$ > 2.7 V | — | — | 3 | ms |
| Reset Delay from non-POR source | $t_{RST}$ | Time between release of reset source and code execution | — | — | 250 | µs |
| RST Low Time to Generate Reset | $t_{RSTL}$ | | 15 | — | — | µs |
| Missing Clock Detector Response Time (final rising edge to reset) | $t_{MCD}$ | $F_{SYSCLK}$ >1 MHz | 80 | 580 | 800 | µs |
| VDD Supply Monitor Turn-On Time | $t_{MON}$ | | — | — | 100 | µs |

**Table 1.4. Flash Memory**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Write Time[1] | $t_{WRITE}$ | One Byte | 10 | 15 | 20 | µs |
| Erase Time[1] | $t_{ERASE}$ | One Page | 10 | 15 | 22.5 | ms |
| $V_{DD}$ Voltage During Programming[2] | $V_{PROG}$ | | 2.7 | — | 3.6 | V |
| Endurance (Write/Erase Cycles) | $N_{WE}$ | | 10k | 100k | — | Cycles |

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| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|

**Note:**

1. Does not include sequencing time before and after the write/erase operation, which may be multiple SYSCLK cycles.
2. Flash can be safely programmed at any voltage above the supply monitor threshold ($V_{VDDM}$).
3. Data Retention Information is published in the Quarterly Quality and Reliability Report.

**Table 1.5. Internal Oscillators**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| High Frequency Oscillator 0 (48 MHz) | | | | | | |
| Oscillator Frequency | $f_{HFOSC0}$ | Full Temperature and Supply Range | 47.3 | 48 | 48.7 | MHz |
| Power Supply Sensitivity | $PSS_{HFOSC0}$ | $T_A$ = 25 °C | — | 110 | — | ppm/V |
| Temperature Sensitivity | $TS_{HFOSC0}$ | $V_{DD}$ = 3.0 V | — | 25 | — | ppm/°C |
| Low Frequency Oscillator (80 kHz) | | | | | | |
| Oscillator Frequency | $f_{LFOSC}$ | Full Temperature and Supply Range | 75 | 80 | 85 | kHz |
| Power Supply Sensitivity | $PSS_{LFOSC}$ | $T_A$ = 25 °C | — | 0.05 | — | %/V |
| Temperature Sensitivity | $TS_{LFOSC}$ | $V_{DD}$ = 3.0 V | — | 65 | — | ppm/°C |

**Table 1.6. Crystal Oscillator**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Crystal Frequency | $f_{XTAL}$ | | 0.02 | — | 30 | MHz |

**Table 1.7. External Clock Input**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| External Input CMOS Clock Frequency (at EXTCLK pin) | $f_{CMOS}$ | | 0 | — | 48 | MHz |

**Table 1.8. ADC**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Resolution | $N_{bits}$ | | | 10 | | Bits |
| Throughput Rate | $f_S$ | | — | — | 500 | ksps |
| Tracking Time | $t_{TRK}$ | | 300 | — | — | ns |
| SAR Clock Frequency | $f_{SAR}$ | | — | — | 8.33 | MHz |
| Conversion Time | $t_{CNV}$ | 10-Bit Conversion, | 13 | — | — | Clocks |
| Sample/Hold Capacitor | $C_{SAR}$ | | — | 30 | — | pF |
| Input Mux Impedance | $R_{MUX}$ | | — | 5 | — | kΩ |
| Voltage Reference Range | $V_{REF}$ | | 1 | — | $V_{DD}$ | V |

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| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input Voltage Range[1] | $V_{IN}$ | Single-Ended (AIN+ - GND) | 0 | — | $V_{REF}$ | V |
| | | Differential (AIN+ - AIN-) | $-V_{REF}$ | — | $V_{REF}$ | V |
| Power Supply Rejection Ratio | $PSRR_{ADC}$ | | — | 70 | — | dB |
| DC Performance, VREF = 2.4 V | | | | | | |
| Integral Nonlinearity | INL | | — | ±0.5 | ±1 | LSB |
| Differential Nonlinearity (Guaranteed Monotonic) | DNL | | — | ±0.5 | ±1 | LSB |
| Offset Error | $E_{OFF}$ | | -2 | 0 | 2 | LSB |
| Offset Temperature Coefficient | $TC_{OFF}$ | | — | 0.005 | — | LSB/°C |
| Slope Error | $E_M$ | | — | -0.2 | ±0.5 | % |
| Dynamic Performance 10 kHz Sine Wave Input 1dB below full scale, VREF = 2.4 V | | | | | | |
| Signal-to-Noise | SNR | | 55 | 58 | — | dB |
| Signal-to-Noise Plus Distortion | SNDR | | 55 | 58 | — | dB |
| Total Harmonic Distortion (Up to 5th Harmonic) | THD | | — | -73 | — | dB |
| Spurious-Free Dynamic Range | SFDR | | — | 78 | — | dB |

**Note:**
1. Absolute input pin voltage is limited by the VDD and GND supply pins.

**Table 1.9. Voltage Reference**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| On-chip Precision Reference | | | | | | |
| Output Voltage | $V_{REFP}$ | T = 25 °C | 2.38 | 2.42 | 2.46 | V |
| Turn-on Time, settling to 0.5 LSB | $t_{VREFP}$ | 4.7 µF tantalum + 0.1 µF ceramic bypass on VREF pin | — | 3 | — | ms |
| | | 0.1 µF ceramic bypass on VREF pin | — | 100 | — | µs |
| Load Regulation | $LR_{VREFP}$ | Load = 0 to 200 µA to GND | — | 360 | — | µV / µA |
| Short-circuit current | $ISC_{VREFP}$ | | — | — | 8 | mA |
| Power Supply Rejection | $PSRR_{VREFP}$ | | — | 140 | — | ppm/V |
| External Reference | | | | | | |
| Input Current | $I_{EXTREF}$ | Sample Rate = 500 ksps; VREF = 3.0 V | — | 9 | — | µA |

**Table 1.10. Temperature Sensor**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Offset | $V_{OFF}$ | $T_A$ = 0 °C | — | 764 | — | mV |
| Offset Error1 | $E_{OFF}$ | $T_A$ = 0 °C | — | 15 | — | mV |

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| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Slope | M | | — | 2.87 | — | mV/°C |
| Slope Error1 | $E_M$ | | — | 120 | — | µV/°C |
| Linearity | | | — | 0.5 | — | °C |
| Turn-on Time | | | — | 1.8 | — | µs |

**Note:**
1. Represents one standard deviation from the mean.

**Table 1.11. 5V Voltage Regulator**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input Voltage Range[1] | $V_{REGIN}$ | | 2.7 | — | 5.25 | V |
| Output Voltage on VDD[2] | $V_{REGOUT}$ | Output Current = 1 to 100 mA | 3.0 | 3.3 | 3.6 | V |
| Output Current[2] | $I_{REGOUT}$ | | — | — | 100 | mA |

**Note:**
1. Input range specified for regulation. When an external regulator is used, VREGIN should be tied to VDD.
2. Output current is total regulator output, including any current required by the device.

**Table 1.12. Comparators**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Response Time, CPMD = 00 (Highest Speed) | $t_{RESP0}$ | +100 mV Differential | — | 100 | — | ns |
| | | -100 mV Differential | — | 250 | — | ns |
| Response Time, CPMD = 11 (Lowest Power) | $t_{RESP3}$ | +100 mV Differential | — | 1.05 | — | µs |
| | | -100 mV Differential | — | 5.2 | — | µs |
| Positive Hysteresis Mode 0 (CPMD = 00) | $HYS_{CP+}$ | CPHYP = 00 | — | 0.4 | — | mV |
| | | CPHYP = 01 | — | 8 | — | mV |
| | | CPHYP = 10 | — | 16 | — | mV |
| | | CPHYP = 11 | — | 32 | — | mV |
| Negative Hysteresis Mode 0 (CPMD = 00) | $HYS_{CP-}$ | CPHYN = 00 | — | -0.4 | — | mV |
| | | CPHYN = 01 | — | -8 | — | mV |
| | | CPHYN = 10 | — | -16 | — | mV |
| | | CPHYN = 11 | — | -32 | — | mV |
| Positive Hysteresis Mode 1 (CPMD = 01) | $HYS_{CP+}$ | CPHYP = 00 | — | 0.5 | — | mV |
| | | CPHYP = 01 | — | 6 | — | mV |
| | | CPHYP = 10 | — | 12 | — | mV |
| | | CPHYP = 11 | — | 24 | — | mV |

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| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Negative Hysteresis Mode 1 (CPMD = 01) | $HYS_{CP-}$ | CPHYN = 00 | — | -0.5 | — | mV |
| | | CPHYN = 01 | — | -6 | — | mV |
| | | CPHYN = 10 | — | -12 | — | mV |
| | | CPHYN = 11 | — | -24 | — | mV |
| Positive Hysteresis Mode 2 (CPMD = 10) | $HYS_{CP+}$ | CPHYP = 00 | — | 0.7 | — | mV |
| | | CPHYP = 01 | — | 4.5 | — | mV |
| | | CPHYP = 10 | — | 9 | — | mV |
| | | CPHYP = 11 | — | 18 | — | mV |
| Negative Hysteresis Mode 2 (CPMD = 10) | $HYS_{CP-}$ | CPHYN = 00 | — | -0.6 | — | mV |
| | | CPHYN = 01 | — | -4.5 | — | mV |
| | | CPHYN = 10 | — | -9 | — | mV |
| | | CPHYN = 11 | — | -18 | — | mV |
| Positive Hysteresis Mode 3 (CPMD = 11) | $HYS_{CP+}$ | CPHYP = 00 | — | 1.5 | — | mV |
| | | CPHYP = 01 | — | 4 | — | mV |
| | | CPHYP = 10 | — | 8 | — | mV |
| | | CPHYP = 11 | — | 16 | — | mV |
| Negative Hysteresis Mode 3 (CPMD = 11) | $HYS_{CP-}$ | CPHYN = 00 | — | -1.5 | — | mV |
| | | CPHYN = 01 | — | -4 | — | mV |
| | | CPHYN = 10 | — | -8 | — | mV |
| | | CPHYN = 11 | — | -16 | — | mV |
| Input Range (CP+ or CP-) | $V_{IN}$ | | -0.25 | — | $V_{DD}$+0.25 | V |
| Input Pin Capacitance | $C_{CP}$ | | — | 7.5 | — | pF |
| Common-Mode Rejection Ratio | $CMRR_{CP}$ | | — | 60 | — | dB |
| Power Supply Rejection Ratio | $PSRR_{CP}$ | | — | 60 | — | dB |
| Input Offset Voltage | $V_{OFF}$ | $T_A$ = 25 °C | -10 | 0 | 10 | mV |

**Table 1.13. Port I/O**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -3 mA | $V_{DD}$ - 0.7 | — | — | V |
| | | $I_{OH}$ = -10 µA | $V_{DD}$ - 0.1 | — | — | V |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 8.5 mA | — | — | 0.6 | V |
| | | $I_{OL}$ = 10 µA | — | — | 0.1 | V |
| Input High Voltage | $V_{IH}$ | | 2.0 | — | — | V |
| Input Low Voltage | $V_{IL}$ | | — | — | 0.8 | V |
| Pin Capacitance | $C_{IO}$ | | — | 7 | — | pF |
| Weak Pull-Up Current ($V_{IN}$ = 0 V) | $I_{PU}$ | $V_{DD}$ = 3.6 | -50 | -15 | — | µA |

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| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input Leakage (Pullups off or Analog) | $I_{LK}$ | GND < $V_{IN}$ < $V_{DD}$ | -1 | — | 1 | µA |
| Input Leakage Current with $V_{IN}$ above $V_{DD}$ | $I_{LK}$ | $V_{DD}$ < $V_{IN}$ < $V_{DD}$+2.0 V | 0 | 5 | 150 | µA |

**Table 1.14. USB Transceiver**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Transmitter | | | | | | |
| Output High Voltage | $V_{OH}$ | $V_{DD}$ ≥3.0V | 2.8 | — | — | V |
| Output Low Voltage | $V_{OL}$ | $V_{DD}$ ≥3.0V | — | — | 0.8 | V |
| Output Crossover Point | $V_{CRS}$ | | 1.3 | — | 2.0 | V |
| Output Impedance | $Z_{DRV}$ | Driving High<br>Driving Low | —<br>— | 38<br>38 | —<br>— | Ω |
| Pull-up Resistance | $R_{PU}$ | Full Speed (D+ Pull-up)<br>Low Speed (D- Pull-up) | 1.425 | 1.5 | 1.575 | kΩ |
| Output Rise Time | $T_R$ | Low Speed | 75 | — | 300 | ns |
| | | Full Speed | 4 | — | 20 | ns |
| Output Fall Time | $T_F$ | Low Speed | 75 | — | 300 | ns |
| | | Full Speed | 4 | — | 20 | ns |
| Receiver | | | | | | V |
| Differential Input Sensitivity | $V_{DI}$ | \| (D+) - (D-) \| | 0.2 | — | — | V |
| Differential Input Common Mode Range | $V_{CM}$ | | 0.8 | — | 2.5 | V |
| Input Leakage Current | $I_L$ | Pullups Disabled | — | <1.0 | — | µA |
| Refer to the USB Specification for timing diagrams and symbol definitions. | | | | | | |

## 1.2 Thermal Conditions

**Table 1.15. Thermal Conditions**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Thermal Resistance | $_{JA}$ | TQFP48 Packages | | 60 | | °C/W |
| | | LQFP32 Packages | | 80 | | °C/W |
| | | QFN32 Packages | | 28 | | °C/W |

**Note:**
1. Thermal resistance assumes a multi-layer PCB with any exposed pad soldered to a PCB pad.

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### 1.3 Absolute Maximum Ratings

Stresses above those listed in Table 1.16 Absolute Maximum Ratings on page 8 may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at http://www.silabs.com/support/quality/pages/default.aspx.

**Table 1.16. Absolute Maximum Ratings**

| Parameter | Symbol | Test Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Ambient Temperature Under Bias | $T_{BIAS}$ | | -55 | 125 | °C |
| Storage Temperature | $T_{STG}$ | | -65 | 150 | °C |
| Voltage on VDD | $V_{DD}$ | | GND-0.3 | 4.2 | V |
| Voltage on VREGIN | $V_{REGIN}$ | | GND-0.3 | 5.8 | V |
| Voltage on I/O, RSTb, or VBUS pins | $V_{IN}$ | $V_{DD}$ > 2.2 V | GND-0.3 | 5.8 | V |
| | | $V_{DD}$ < 2.2 V | GND-0.3 | $V_{DD}$+3.6 | V |
| Total Current Sunk into Supply Pin | $I_{VDD}$ | | | 500 | mA |
| Total Current Sourced out of Ground Pin | $I_{GND}$ | | 500 | | mA |
| Current Sourced or Sunk by any I/O Pin or RSTb | $I_{IO}$ | | -100 | 100 | mA |

**Note:**
1. Exposure to maximum rating conditions for extended periods may affect device reliability.

### 1.4 Typical Performance Curves

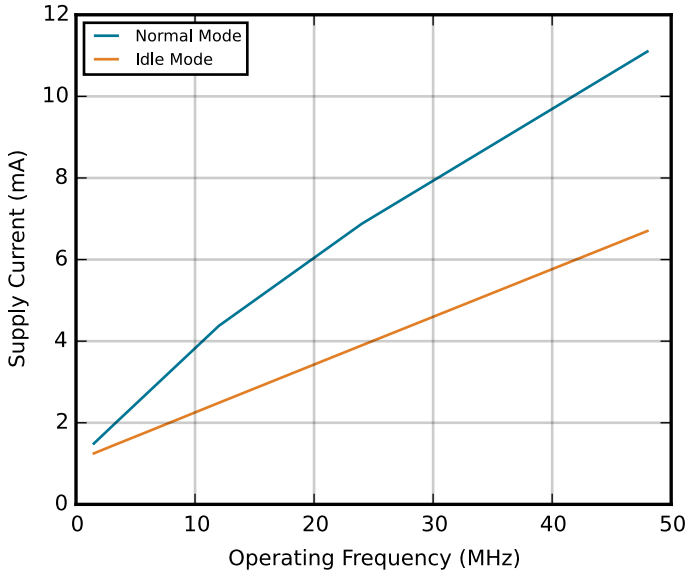


**Figure 1.1. Typical Operating Supply Current using HFOSC0**

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# 2. System Overview

## 2.1 Introduction

The EFM8UB2 device family is a fully integrated, mixed-signal system-on-a-chip family of MCUs. Highlighted features are listed below.

- Core:
  - Pipelined CIP-51 Core
  - Fully compatible with standard 8051 instruction set
  - 70% of instructions execute in 1-2 clock cycles
  - 48 MHz maximum operating frequency
- Memory:
  - Up to 64 KB flash memory, in-system re-programmable from firmware.
  - Up to 4352 bytes RAM (including 256 bytes standard 8051 RAM and 4096 bytes on-chip XRAM)
- Power:
  - Internal LDO regulator for CPU core voltage
  - Internal 5-to-3.3 V LDO allows direct connection to USB supply net
  - Power-on reset circuit and brownout detectors
- I/O: Up to 40 total multifunction I/O pins:
  - Flexible peripheral crossbar for peripheral routing
  - 10 mA source, 25 mA sink allows direct drive of LEDs
- Clock Sources:
  - Internal 48 MHz precision oscillator ( ±1.5% accuracy without USB clock recovery, ±0.25% accuracy with USB clock recovery)
  - Internal 80 kHz low-frequency oscillator
  - External crystal, RC, C, and CMOS clock options
- Timers/Counters and PWM:
  - 5-channel Programmable Counter Array (PCA) supporting PWM, capture/compare, and frequency output modes with watchdog timer function
  - 6 x 16-bit general-purpose timers
- Communications and Digital Peripherals:
  - Universal Serial Bus (USB) Function Controller with eight flexible endpoint pipes, integrated transceiver, and 1 KB FIFO RAM
  - 2 x UART
  - SPI™ Master / Slave
  - 2 x SMBus™/I2C™ Master / Slave
  - External Memory Interface (EMIF)
- Analog:
  - 10-Bit Analog-to-Digital Converter (ADC0)
  - 2 x Low-current analog comparators
- On-Chip, Non-Intrusive Debugging
  - Full memory and register inspection
  - Four hardware breakpoints, single-stepping

With on-chip power-on reset, voltage supply monitor, watchdog timer, and clock oscillator, the EFM8UB2 devices are truly standalone system-on-a-chip solutions. The flash memory is reprogrammable in-circuit, providing non-volatile data storage and allowing field upgrades of the firmware. The on-chip debugging interface (C2) allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, and run and halt commands. All analog and digital peripherals are fully functional while debugging. Each device is specified for 2.65 to 3.6 V operation and is available in 32-pin QFN, 32-pin LQFP, or 48-pin TQFP packages. All package options are lead-free and RoHS compliant.

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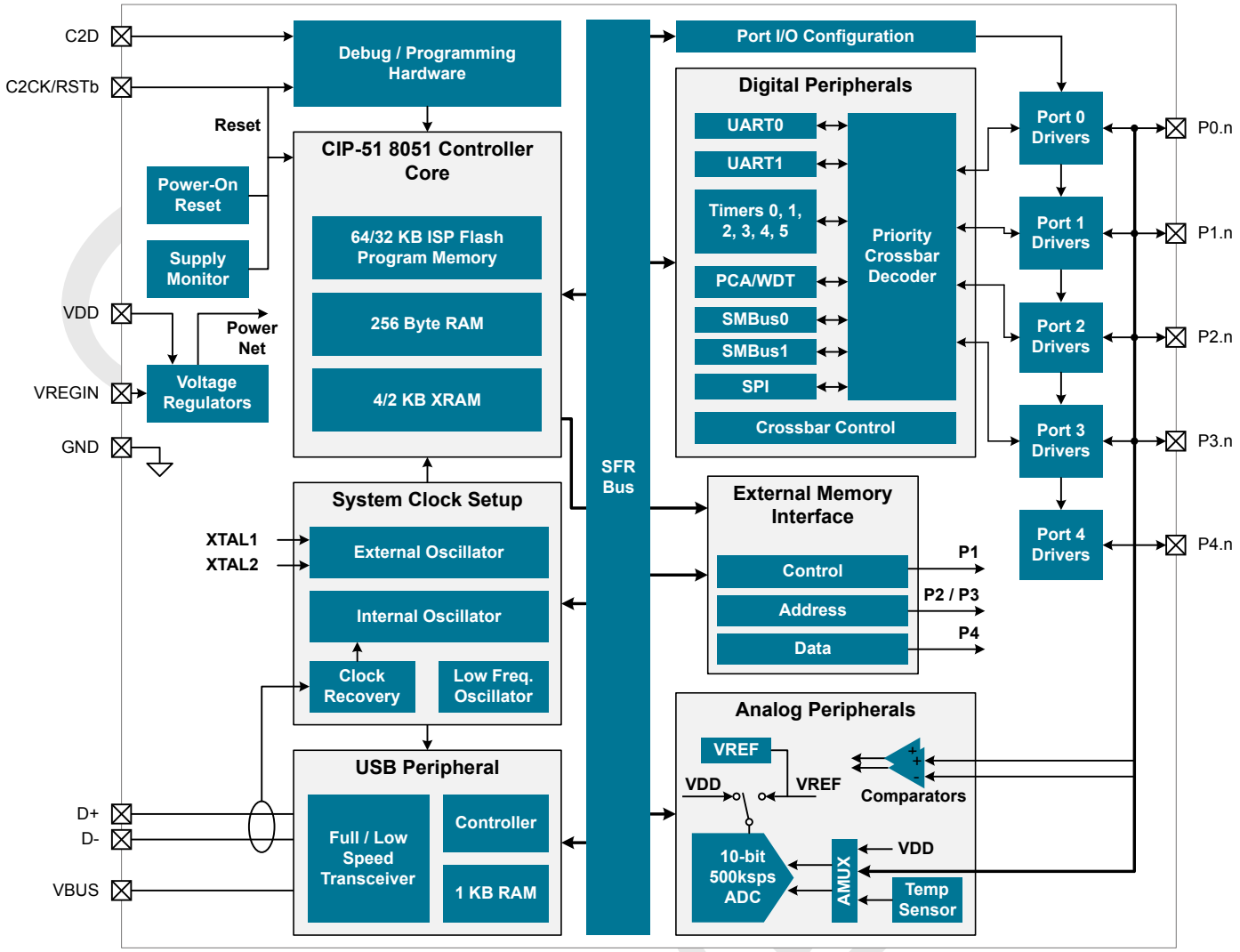


**Figure 2.1. Detailed EFM8UB2 Block Diagram**

### 2.2 Power

All internal circuitry draws power from the VDD supply pin. Circuits with external connections (I/O pins, analog muxes) are powered directly from the VDD supply voltage, while most of the internal circuitry is supplied by an on-chip LDO regulator. Control over the device power can be achieved by enabling/disabling individual peripherals as needed. Each analog peripheral can be disabled when not in use and placed in low power mode. Digital peripherals, such as timers and serial buses, have their clocks gated off and draw little power when they are not in use.

**Table 2.1. Power Modes**

| Power Mode | Details | Mode Entry | Wake-Up Sources |
|---|---|---|---|
| Normal | Core and all peripherals clocked and fully operational | — | — |
| Idle | • Core halted<br>• All peripherals clocked and fully operational<br>• Code resumes execution on wake event | Set IDLE bit in PCON0 | Any interrupt |
| Suspend | • Core and peripheral clocks halted<br>• Code resumes execution on wake event | 1. Switch SYSCLK to HFOSC0<br>2. Set SUSPEND bit in HFO0CN | USB0 Bus Activity |
| Shutdown | • All internal power nets shut down<br>• 5V regulator remains active (if enabled)<br>• Pins retain state<br>• Exit on pin or power-on reset | 1. Set STOPCF bit in REG01CN<br>2. Set STOP bit in PCON0 | • RSTb pin reset<br>• Power-on reset |

### 2.3 I/O

Digital and analog resources are externally available on the device's multi-purpose I/O pins. Port pins P0.0-P3.7 can be defined as general-purpose I/O (GPIO), assigned to one of the internal digital resources through the crossbar or dedicated channels, or assigned to an analog function. Port pins P4.0-P4.7 can be used as GPIO. P3.0 on some packages is shared with the C2 Interface Data signal (C2D).

- Up to 40 multi-functions I/O pins, supporting digital and analog functions.
- Flexible priority crossbar decoder for digital peripheral assignment.
- Two direct-pin interrupt sources with dedicated interrupt vectors (INT0 and INT1) available on P0 pins.

### 2.4 Clocking

The CPU core and peripheral subsystem may be clocked by both internal and external oscillator resources. By default, the system clock comes up running from the 48 MHz oscillator divided by 4, then divided by 8 (1.5 MHz).

- Provides clock to core and peripherals.
- 48 MHz internal oscillator (HFOSC0), accurate to ±1.5% over supply and temperature corners: accurate to +/- 0.25% when using USB clock recovery.
- 80 kHz low-frequency oscillator (LFOSC0).
- External RC, C, CMOS, and high-frequency crystal clock options (EXTCLK).
- Internal oscillator has clock divider with eight settings for flexible clock scaling: 1, 2, 4, or 8.

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## 2.5 Counters/Timers and PWM

### Programmable Counter Array (PCA0)

The programmable counter array (PCA) provides multiple channels of enhanced timer and PWM functionality while requiring less CPU intervention than standard counter/timers. The PCA consists of a dedicated 16-bit counter/timer and one 16-bit capture/compare module for each channel. The counter/timer is driven by a programmable timebase that has flexible external and internal clocking options. Each capture/compare module may be configured to operate independently in one of five modes: Edge-Triggered Capture, Software Timer, High-Speed Output, Frequency Output, or Pulse-Width Modulated (PWM) Output. Each capture/compare module has its own associated I/O line (CEXn) which is routed through the crossbar to port I/O when enabled.

- 16-bit time base.
- Programmable clock divisor and clock source selection.
- Five independently-configurable channels.
- 8- or 16-bit PWM modes (edge-aligned operation).
- Frequency output mode.
- Capture on rising, falling or any edge.
- Compare function for arbitrary waveform generation.
- Software timer (internal compare) mode.
- Integrated watchdog timer.

### Timers (Timer 0, Timer 1, Timer 2, Timer 3, Timer 4, and Timer 5)

Several counter/timers are included in the device: two are 16-bit counter/timers compatible with those found in the standard 8051, and the rest are 16-bit auto-reload timers for timing peripherals or for general purpose use. These timers can be used to measure time intervals, count external events and generate periodic interrupt requests. Timer 0 and Timer 1 are nearly identical and have four primary modes of operation. The other timers offer both 16-bit and split 8-bit timer functionality with auto-reload capabilities.

Timer 0 and Timer 1 include the following features:

- Standard 8051 timers, supporting backwards-compatibility with firmware and hardware.
- Clock sources include SYSCLK, SYSCLK divided by 12, 4, or 48, the External Clock divided by 8, or an external pin.
- 8-bit auto-reload counter/timer mode
- 13-bit counter/timer mode
- 16-bit counter/timer mode
- Dual 8-bit counter/timer mode (Timer 0).

Timer 2, Timer 3, Timer 4, and Timer 5 are 16-bit timers including the following features:

- Clock sources include SYSCLK, SYSCLK divided by 12, or the External Clock divided by 8.
- 16-bit auto-reload timer mode
- Dual 8-bit auto-reload timer mode
- USB start-of-frame or falling edge of LFOSC0 capture (Timer 2 and Timer 3)

### Watchdog Timer (WDT0)

The device includes a programmable watchdog timer (WDT) integrated within the PCA0 peripheral. A WDT overflow forces the MCU into the reset state. To prevent the reset, the WDT must be restarted by application software before overflow. If the system experiences a software or hardware malfunction preventing the software from restarting the WDT, the WDT overflows and causes a reset. Following a reset, the WDT is automatically enabled and running with the default maximum time interval. If needed, the WDT can be disabled by system software. The state of the RSTb pin is unaffected by this reset.

The Watchdog Timer integrated in the PCA0 peripheral has the following features:

- Programmable timeout interval
- Runs from the selected PCA clock source
- Automatically enabled after any system reset

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## 2.6 Communications and Other Digital Peripherals

**Universal Serial Bus (USB0)**

The USB0 module provides Full/Low Speed function for USB peripheral implementations. The USB function controller (USB0) consists of a Serial Interface Engine (SIE), USB transceiver (including matching resistors and configurable pull-up resistors), 1 kB FIFO block, and clock recovery mechanism for crystal-less operation. No external components are required. The USB0 module is Universal Serial Bus Specification 2.0 compliant.

The USB0 module includes the following features:

- Full and Low Speed functionality.
- Implements 4 bidirectional endpoints.
- USB 2.0 compliant USB peripheral support (no host capability).
- Direct module access to 1 kB of RAM for FIFO memory.
- Clock recovery to meet USB clocking requirements with no external components.

**Universal Asynchronous Receiver/Transmitter (UART0)**

UART0 is an asynchronous, full duplex serial port offering modes 1 and 3 of the standard 8051 UART. Enhanced baud rate support allows a wide range of clock sources to generate standard baud rates. Received data buffering allows UART0 to start reception of a second incoming data byte before software has finished reading the previous data byte.

The UART module provides the following features:

- Asynchronous transmissions and receptions
- Baud rates up to SYSCLK / 2 (transmit) or SYSCLK / 8 (receive)
- 8- or 9-bit data
- Automatic start and stop generation

**Universal Asynchronous Receiver/Transmitter (UART1)**

UART1 is an asynchronous, full duplex serial port offering a variety of data formatting options. A dedicated baud rate generator with a 16-bit timer and selectable prescaler is included, which can generate a wide range of baud rates. A received data FIFO allows UART1 to receive multiple bytes before data is lost and an overflow occurs.

UART1 provides the following features:

- Asynchronous transmissions and receptions.
- Dedicated baud rate generator supports baud rates up to SYSCLK/16.
- 5, 6, 7, 8, or 9 bit data.
- Automatic start and stop generation.
- Automatic parity generation and checking.
- Three byte FIFO on receive.

**Serial Peripheral Interface (SPI0)**

The serial peripheral interface (SPI) module provides access to a flexible, full-duplex synchronous serial bus. The SPI can operate as a master or slave device in both 3-wire or 4-wire modes, and supports multiple masters and slaves on a single SPI bus. The slave-select (NSS) signal can be configured as an input to select the SPI in slave mode, or to disable master mode operation in a multi-master environment, avoiding contention on the SPI bus when more than one master attempts simultaneous data transfers. NSS can also be configured as a firmware-controlled chip-select output in master mode, or disabled to reduce the number of pins required. Additional general purpose port I/O pins can be used to select multiple slave devices in master mode.

The SPI module includes the following features:

- Supports 3- or 4-wire operation in master or slave modes.
- Supports external clock frequencies up to SYSCLK / 2 in master mode and SYSCLK / 10 in slave mode.
- Support for four clock phase and polarity options.
- 8-bit dedicated clock clock rate generator.
- Support for multiple masters on the same data lines.

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**System Management Bus / I2C (SMBus0, SMBus1)**

The SMBus I/O interface is a two-wire, bi-directional serial bus. The SMBus is compliant with the System Management Bus Specification, version 1.1, and compatible with the $I^2C$ serial bus.

The SMBus modules include the following features:

- Standard (up to 100 kbps) and Fast (400 kbps) transfer speeds.
- Support for master, slave, and multi-master modes.
- Hardware synchronization and arbitration for multi-master mode.
- Clock low extending (clock stretching) to interface with faster masters.
- Hardware support for 7-bit slave and general call address recognition.
- Firmware support for 10-bit slave address decoding.
- Ability to inhibit all slave states.
- Programmable data setup/hold times.

**External Memory Interface (EMIF0)**

The External Memory Interface (EMIF) enables access of off-chip memories and memory-mapped devices connected to the GPIO ports. The external memory space may be accessed using the external move instruction (MOVX) with the target address specified in either 8-bit or 16-bit formats.

- Supports multiplexed memory access.
- Four external memory modes:
  - Internal only.
  - Split mode without bank select.
  - Split mode with bank select.
  - External only
- Configurable ALE (address latch enable) timing.
- Configurable address setup and hold times.
- Configurable write and read pulse widths.

## 2.7 Analog

**10-Bit Analog-to-Digital Converter (ADC0)**

The ADC is a successive-approximation-register (SAR) ADC with 10-bit differential and single-ended modes, integrated track-and hold and a programmable window detector. The ADC is fully configurable under software control via several registers. The ADC may be configured to measure different signals using the analog multiplexer. The voltage reference for the ADC is selectable between internal and external reference sources.

- Up to 32 external inputs.
- Differential or Single-ended 10-bit operation.
- Supports an output update rate of 500 ksps samples per second.
- Asynchronous hardware conversion trigger, selectable between software, external I/O and internal timer sources.
- Output data window comparator allows automatic range checking.
- Two tracking mode options with programmable tracking time.
- Conversion complete and window compare interrupts supported.
- Flexible output data formatting.
- Voltage reference selectable from external reference pin, on-chip precision reference (driven externally on reference pin), or VDD supply.
- Integrated temperature sensor.

**Low Current Comparators (CMP0, CMP1)**

An analog comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. External input connections to device I/O pins and internal connections are available through separate multiplexers on the positive and negative inputs. Hysteresis, response time, and current consumption may be programmed to suit the specific needs of the application.

The comparator module includes the following features:

- Up to 5 external positive inputs.
- Up to 5 external negative inputs.
- Synchronous and asynchronous outputs can be routed to pins via crossbar.
- Programmable hysteresis between 0 and +/-20 mV.
- Programmable response time.
- Interrupts generated on rising, falling, or both edges.

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### 2.8 Reset Sources

Reset circuitry allows the controller to be easily placed in a predefined default condition. On entry to this reset state, the following occur:

- The core halts program execution.
- Module registers are initialized to their defined reset values unless the bits reset only with a power-on reset.
- External port pins are forced to a known state.
- Interrupts and timers are disabled.

All registers are reset to the predefined values noted in the register descriptions unless the bits only reset with a power-on reset. The contents of RAM are unaffected during a reset; any previously stored data is preserved as long as power is not lost. The Port I/O latches are reset to 1 in open-drain mode. Weak pullups are enabled during and after the reset. For VDD Supply Monitor and power-on resets, the RSTb pin is driven low until the device exits the reset state. On exit from the reset state, the program counter (PC) is reset, and the system clock defaults to an internal oscillator. The Watchdog Timer is enabled, and program execution begins at location 0x0000.

Reset sources on the device include:

- Power-on reset
- External reset pin
- Comparator reset
- Software-triggered reset
- Supply monitor reset (monitors VDD supply)
- Watchdog timer reset
- Missing clock detector reset
- Flash error reset
- USB reset

### 2.9 Debugging

The EFM8UB2 devices include an on-chip Silicon Labs 2-Wire (C2) debug interface to allow flash programming and in-system debugging with the production part installed in the end application. The C2 interface uses a clock signal (C2CK) and a bi-directional C2 data signal (C2D) to transfer information between the device and a host system. See the C2 Interface Specification for details on the C2 protocol.

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# 3. Ordering Information

All EFM8UB2 family members have the following features:

- CIP-51 Core running up to 48 MHz
- Two Internal Oscillators (48 MHz and 80 kHz)
- USB Full/Low speed Function Controller
- 5 V-In, 3.3 V-Out Regulator
- 2 SMBus/I2C Interfaces
- SPI
- 2 UARTs
- 5-Channel Programmable Counter Array (PWM, Clock Generation, Capture/Compare)
- 6 16-bit Timers
- 2 Analog Comparators
- 10-bit Differential Analog-to-Digital Converter with integrated multiplexer and temperature sensor

In addition to these features, each part number in the EFM8UB2 family has a set of features that vary across the product line. The product selection guide shows the features available on each family member.

**Table 3.1. Product Selection Guide**

| Ordering Part Number | Flash Memory (kB) | RAM (Bytes) | Digital Port I/Os (Total) | ADC0 Channels | Comparator 0 Inputs | Comparator 1 Inputs | Crystal Oscillator | External Memory Inferface | Pb-free (RoHS Compliant) | Temperature Range | Package |
|---|---|---|---|---|---|---|---|---|---|---|---|
| EFM8UB20F64G-A-TQFP48 | 64 | 4352 | 40 | 32 | 5 | 5 | Yes | Yes | Yes | -40 to +85 °C | TQFP48 |
| EFM8UB20F64G-A-LQFP32 | 64 | 4352 | 25 | 20 | 5 | 4 | — | — | Yes | -40 to +85 °C | LQFP32 |
| EFM8UB20F64G-A-QFN32 | 64 | 4352 | 25 | 20 | 5 | 4 | — | — | Yes | -40 to +85 °C | QFN32 |
| EFM8UB20F32G-A-TQFP48 | 32 | 2304 | 40 | 32 | 5 | 5 | Yes | Yes | Yes | -40 to +85 °C | TQFP48 |
| EFM8UB20F32G-A-LQFP32 | 32 | 2304 | 25 | 20 | 5 | 4 | — | — | Yes | -40 to +85 °C | LQFP32 |
| EFM8UB20F32G-A-QFN32 | 32 | 2304 | 25 | 20 | 5 | 4 | — | — | Yes | -40 to +85 °C | QFN32 |

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# 4. Pin Definitions

## 4.1 EFM8UB2x-TQFP48 Pin Definitions

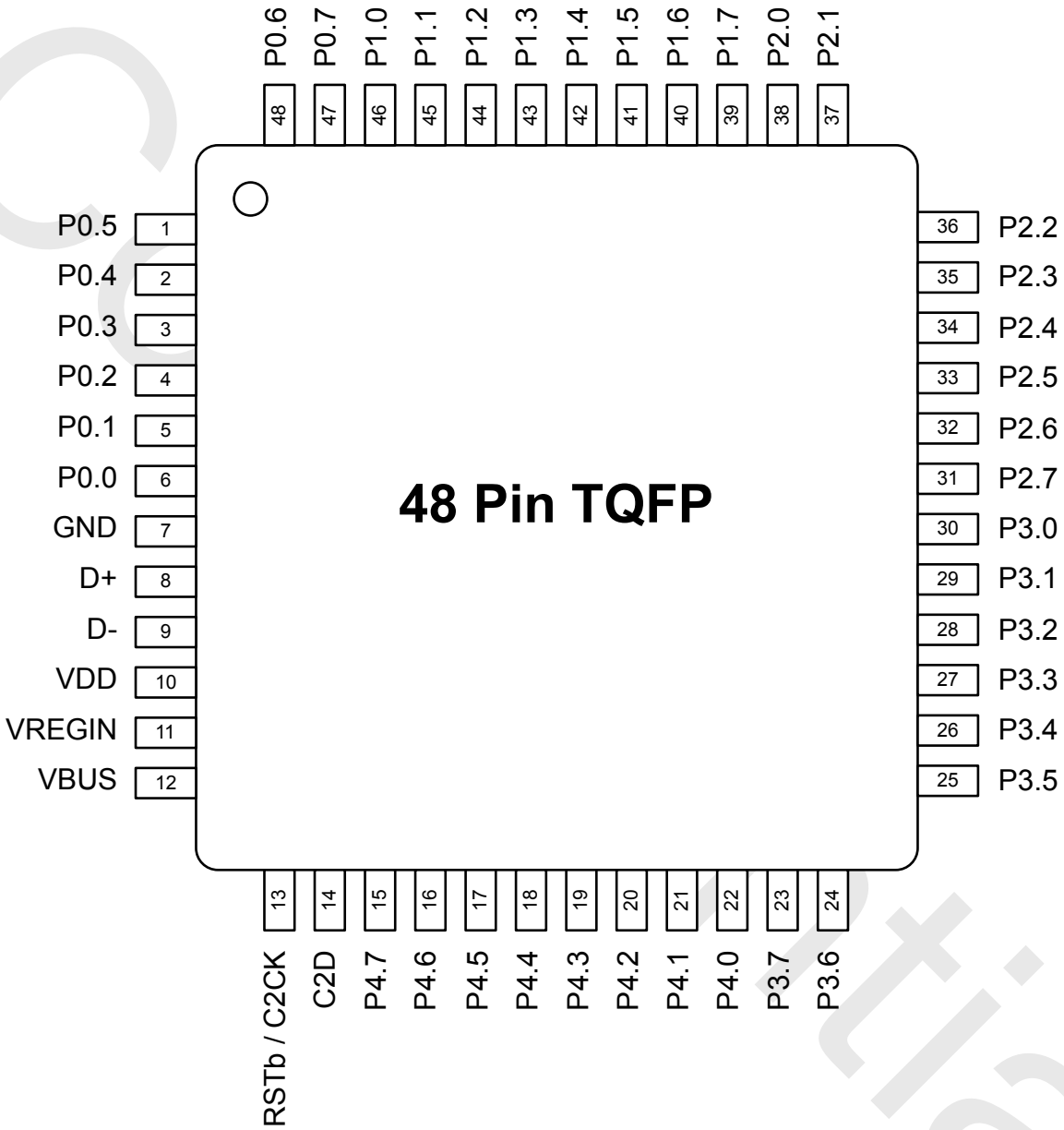


**Figure 4.1. EFM8UB2x-TQFP48 Pinout**

**Table 4.1. Pin Definitions for EFM8UB2x-TQFP48**

| Pin Number | Pin Name | Description | Crossbar Capability | Additional Digital Functions | Analog Functions |
|---|---|---|---|---|---|
| 1 | P0.5 | Multifunction I/O | Yes | UART0_RX<br>INT0.5<br>INT1.5 | |
| 2 | P0.4 | Multifunction I/O | Yes | UART0_TX<br>INT0.4<br>INT1.4 | ADC0P.18<br>ADC0N.18<br>CMP0N.4 |
| 3 | P0.3 | Multifunction I/O | Yes | INT0.3<br>INT1.3 | ADC0P.17<br>ADC0N.17<br>CMP0P.4 |
| 4 | P0.2 | Multifunction I/O | Yes | INT0.2<br>INT1.2 | |
| 5 | P0.1 | Multifunction I/O | Yes | INT0.1<br>INT1.1 | |
| 6 | P0.0 | Multifunction I/O | Yes | INT0.0<br>INT1.0 | |
| 7 | GND | Ground | | | |
| 8 | D+ | USB Data Positive | | | |
| 9 | D- | USB Data Negative | | | |
| 10 | VDD | Supply Power Input /<br>5V Regulator Output | | | |
| 11 | VREGIN | 5V Regulator Input | | | |
| 12 | VBUS | USB VBUS Sense Input | | VBUS | |
| 13 | RST /<br>C2CK | Active-low Reset /<br>C2 Debug Clock | | | |
| 14 | C2D | C2 Debug Data | | | |
| 15 | P4.7 | Multifunction I/O | | EMIF_D7<br>EMIF_AD7m | ADC0P.34<br>ADC0N.34 |
| 16 | P4.6 | Multifunction I/O | | EMIF_D6<br>EMIF_AD6m | ADC0P.15<br>ADC0N.15<br>CMP1N.3 |
| 17 | P4.5 | Multifunction I/O | | EMIF_D5<br>EMIF_AD5m | ADC0P.14<br>ADC0N.14<br>CMP1P.3 |
| 18 | P4.4 | Multifunction I/O | | EMIF_D4<br>EMIF_AD4m | ADC0P.13<br>ADC0N.13<br>CMP0N.3 |
| 19 | P4.3 | Multifunction I/O | | EMIF_D3<br>EMIF_AD3m | ADC0P.12<br>ADC0N.12<br>CMP0P.3 |

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| Pin Number | Pin Name | Description | Crossbar Capability | Additional Digital Functions | Analog Functions |
|---|---|---|---|---|---|
| 20 | P4.2 | Multifunction I/O | | EMIF_D2<br>EMIF_AD2m | ADC0P.33<br>ADC0N.33 |
| 21 | P4.1 | Multifunction I/O | | EMIF_D1<br>EMIF_AD1m | ADC0P.32<br>ADC0N.32 |
| 22 | P4.0 | Multifunction I/O | | EMIF_D0<br>EMIF_AD0m | ADC0P.11<br>ADC0N.11<br>CMP1N.2 |
| 23 | P3.7 | Multifunction I/O | Yes | EMIF_A7<br>EMIF_A15m | ADC0P.10<br>ADC0N.10<br>CMP1P.2 |
| 24 | P3.6 | Multifunction I/O | Yes | EMIF_A6<br>EMIF_A14m | ADC0P.29<br>ADC0N.29 |
| 25 | P3.5 | Multifunction I/O | Yes | EMIF_A5<br>EMIF_A13m | ADC0P.9<br>ADC0N.9<br>CMP0N.2 |
| 26 | P3.4 | Multifunction I/O | Yes | EMIF_A4<br>EMIF_A12m | ADC0P.8<br>ADC0N.8<br>CMP0P.2 |
| 27 | P3.3 | Multifunction I/O | Yes | EMIF_A3<br>EMIF_A11m | ADC0P.28<br>ADC0N.28 |
| 28 | P3.2 | Multifunction I/O | Yes | EMIF_A2<br>EMIF_A10m | ADC0P.27<br>ADC0N.27 |
| 29 | P3.1 | Multifunction I/O | Yes | EMIF_A1<br>EMIF_A9m | ADC0P.7<br>ADC0N.7<br>CMP1N.1 |
| 30 | P3.0 | Multifunction I/O | Yes | EMIF_A0<br>EMIF_A8m | ADC0P.6<br>ADC0N.6<br>CMP1P.1 |
| 31 | P2.7 | Multifunction I/O | Yes | EMIF_A15 | ADC0P.26<br>ADC0N.26 |
| 32 | P2.6 | Multifunction I/O | Yes | EMIF_A14 | ADC0P.5<br>ADC0N.5<br>CMP0N.1 |
| 33 | P2.5 | Multifunction I/O | Yes | EMIF_A13 | ADC0P.4<br>ADC0N.4<br>CMP0P.1 |
| 34 | P2.4 | Multifunction I/O | Yes | EMIF_A12 | ADC0P.25<br>ADC0N.25 |
| 35 | P2.3 | Multifunction I/O | Yes | EMIF_A11 | ADC0P.3<br>ADC0N.3<br>CMP1N.0 |
| 36 | P2.2 | Multifunction I/O | Yes | EMIF_A10 | ADC0P.2<br>ADC0N.2<br>CMP1P.0 |

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| Pin Number | Pin Name | Description | Crossbar Capability | Additional Digital Functions | Analog Functions |
|---|---|---|---|---|---|
| 37 | P2.1 | Multifunction I/O | Yes | EMIF_A9 | ADC0P.1<br>ADC0N.1<br>CMP0N.0 |
| 38 | P2.0 | Multifunction I/O | Yes | EMIF_A8 | ADC0P.0<br>ADC0N.0<br>CMP0P.0 |
| 39 | P1.7 | Multifunction I/O | Yes | EMIF_WRb | ADC0P.24<br>ADC0N.24 |
| 40 | P1.6 | Multifunction I/O | Yes | EMIF_RDb | ADC0P.23<br>ADC0N.23 |
| 41 | P1.5 | Multifunction I/O | Yes | | VREF |
| 42 | P1.4 | Multifunction I/O | Yes | CNVSTR | |
| 43 | P1.3 | Multifunction I/O | Yes | EMIF_ALEm | ADC0P.22<br>ADC0N.22 |
| 44 | P1.2 | Multifunction I/O | Yes | | ADC0P.20<br>ADC0N.20<br>CMP1N.4 |
| 45 | P1.1 | Multifunction I/O | Yes | | ADC0P.19<br>ADC0N.19<br>CMP1P.4 |
| 46 | P1.0 | Multifunction I/O | Yes | | ADC0P.21<br>ADC0N.21 |
| 47 | P0.7 | Multifunction I/O | Yes | XTAL2<br>EXTCLK<br>INT0.7<br>INT1.7 | |
| 48 | P0.6 | Multifunction I/O | Yes | XTAL1<br>INT0.6<br>INT1.6 | |

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### 4.2 EFM8UB2x-LQFP32 Pin Definitions

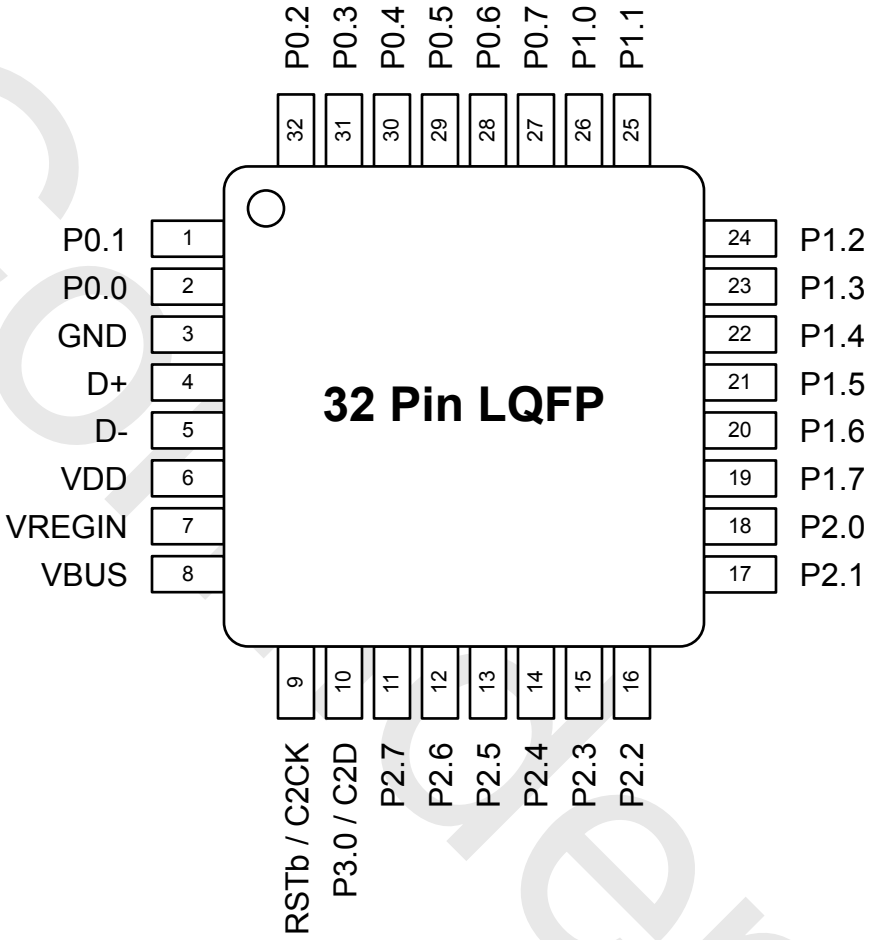


**Figure 4.2. EFM8UB2x-LQFP32 Pinout**

**Table 4.2. Pin Definitions for EFM8UB2x-LQFP32**

| Pin Number | Pin Name | Description | Crossbar Capability | Additional Digital Functions | Analog Functions |
|---|---|---|---|---|---|
| 1 | P0.1 | Multifunction I/O | Yes | INT0.1<br>INT1.1 | ADC0P.18<br>ADC0N.18<br>CMP0N.4 |
| 2 | P0.0 | Multifunction I/O | Yes | INT0.0<br>INT1.0 | ADC0P.17<br>ADC0N.17<br>CMP0P.4 |
| 3 | GND | Ground | | | |
| 4 | D+ | USB Data Positive | | | |
| 5 | D- | USB Data Negative | | | |

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| Pin Number | Pin Name | Description | Crossbar Capability | Additional Digital Functions | Analog Functions |
|---|---|---|---|---|---|
| 6 | VDD | Supply Power Input / 5V Regulator Output | | | |
| 7 | VREGIN | 5V Regulator Input | | | |
| 8 | VBUS | USB VBUS Sense Input | | VBUS | |
| 9 | RST / C2CK | Active-low Reset / C2 Debug Clock | | | |
| 10 | P3.0 / C2D | Multifunction I/O / C2 Debug Data | Yes | | ADC0P.16<br>ADC0N.16 |
| 11 | P2.7 | Multifunction I/O | Yes | | ADC0P.15<br>ADC0N.15 |
| 12 | P2.6 | Multifunction I/O | Yes | | ADC0P.14<br>ADC0N.14 |
| 13 | P2.5 | Multifunction I/O | Yes | | ADC0P.13<br>ADC0N.13<br>CMP0N.3 |
| 14 | P2.4 | Multifunction I/O | Yes | | ADC0P.12<br>ADC0N.12<br>CMP0P.3 |
| 15 | P2.3 | Multifunction I/O | Yes | | ADC0P.11<br>ADC0N.11<br>CMP1N.2 |
| 16 | P2.2 | Multifunction I/O | Yes | | ADC0P.10<br>ADC0N.10<br>CMP1P.2 |
| 17 | P2.1 | Multifunction I/O | Yes | | ADC0P.9<br>ADC0N.9<br>CMP0N.2 |
| 18 | P2.0 | Multifunction I/O | Yes | | ADC0P.8<br>ADC0N.8<br>CMP0P.2 |
| 19 | P1.7 | Multifunction I/O | Yes | | ADC0P.7<br>ADC0N.7<br>CMP1N.1 |
| 20 | P1.6 | Multifunction I/O | Yes | | ADC0P.6<br>ADC0N.6<br>CMP1P.1 |
| 21 | P1.5 | Multifunction I/O | Yes | | ADC0P.5<br>ADC0N.5<br>CMP0N.1 |
| 22 | P1.4 | Multifunction I/O | Yes | | ADC0P.4<br>ADC0N.4<br>CMP0P.1 |

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| Pin Number | Pin Name | Description | Crossbar Capability | Additional Digital Functions | Analog Functions |
|---|---|---|---|---|---|
| 23 | P1.3 | Multifunction I/O | Yes | | ADC0P.3<br>ADC0N.3<br>CMP1N.0 |
| 24 | P1.2 | Multifunction I/O | Yes | | ADC0P.2<br>ADC0N.2<br>CMP1P.0 |
| 25 | P1.1 | Multifunction I/O | Yes | | ADC0P.1<br>ADC0N.1<br>CMP0N.0 |
| 26 | P1.0 | Multifunction I/O | Yes | | ADC0P.0<br>ADC0N.0<br>CMP0P.0 |
| 27 | P0.7 | Multifunction I/O | Yes | INT0.7<br>INT1.7 | VREF |
| 28 | P0.6 | Multifunction I/O | Yes | CNVSTR<br>INT0.6<br>INT1.6 | |
| 29 | P0.5 | Multifunction I/O | Yes | INT0.5<br>INT1.5<br>UART0_RX | ADC0P.20<br>ADC0N.20<br>CMP1N.4 |
| 30 | P0.4 | Multifunction I/O | Yes | INT0.4<br>INT1.4<br>UART0_TX | ADC0P.19<br>ADC0N.19<br>CMP1P.4 |
| 31 | P0.3 | Multifunction I/O | Yes | EXTCLK<br>INT0.3<br>INT1.3 | |
| 32 | P0.2 | Multifunction I/O | Yes | INT0.2<br>INT1.2 | |

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### 4.3 EFM8UB2x-QFN32 Pin Definitions

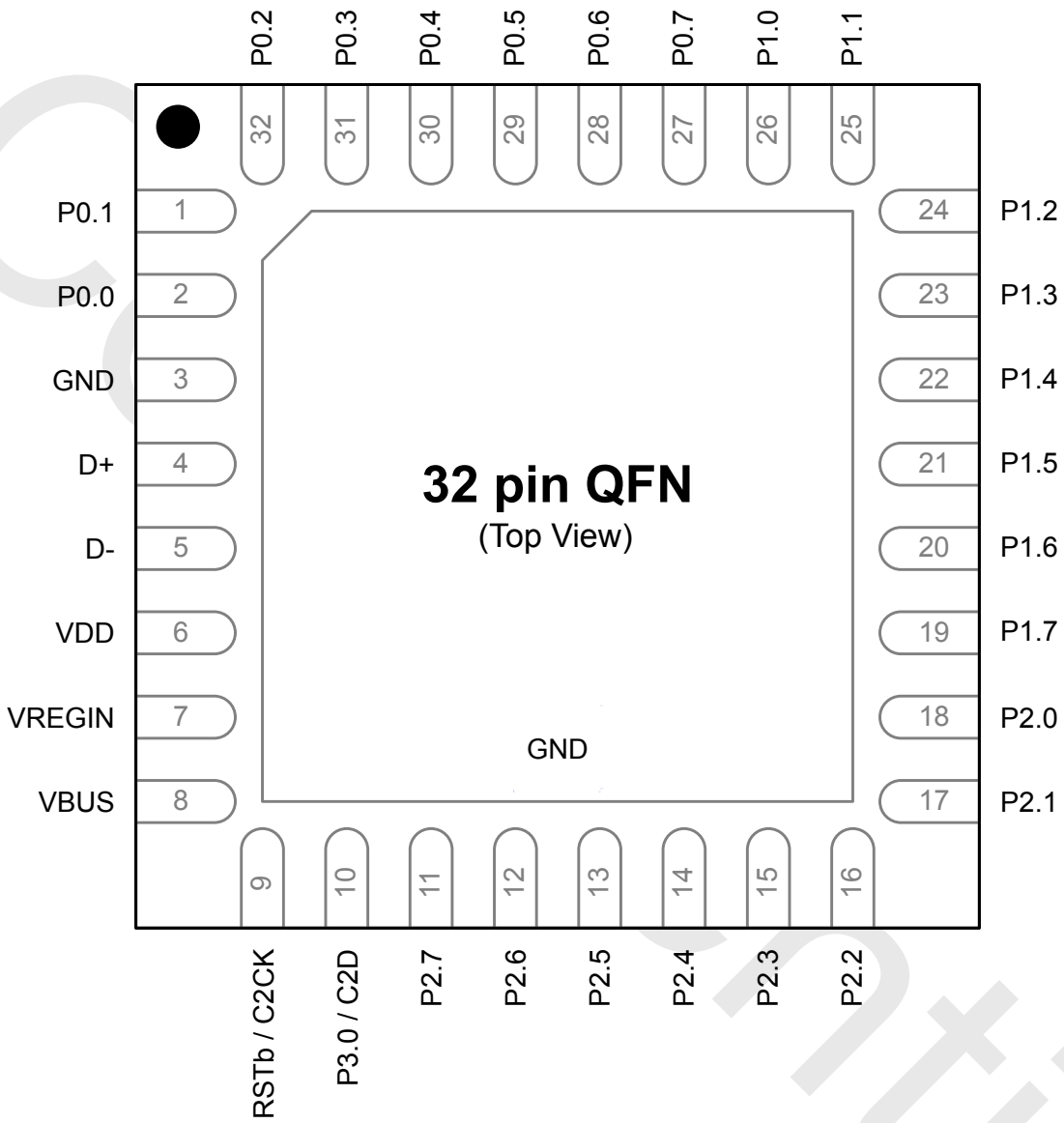


**Figure 4.3. EFM8UB2x-QFN32 Pinout**

**Table 4.3. Pin Definitions for EFM8UB2x-QFN32**

| Pin Number | Pin Name | Description | Crossbar Capability | Additional Digital Functions | Analog Functions |
|---|---|---|---|---|---|
| 1 | P0.1 | Multifunction I/O | Yes | INT0.1<br>INT1.1 | ADC0P.18<br>ADC0N.18<br>CMP0N.4 |

| Pin Number | Pin Name | Description | Crossbar Capability | Additional Digital Functions | Analog Functions |
|---|---|---|---|---|---|
| 2 | P0.0 | Multifunction I/O | Yes | INT0.0<br>INT1.0 | ADC0P.17<br>ADC0N.17<br>CMP0P.4 |
| 3 | GND | Ground | | | |
| 4 | D+ | USB Data Positive | | | |
| 5 | D- | USB Data Negative | | | |
| 6 | VDD | Supply Power Input /<br>5V Regulator Output | | | |
| 7 | VREGIN | 5V Regulator Input | | | |
| 8 | VBUS | USB VBUS Sense Input | | VBUS | |
| 9 | RST /<br>C2CK | Active-low Reset /<br>C2 Debug Clock | | | |
| 10 | P3.0 /<br>C2D | Multifunction I/O /<br>C2 Debug Data | Yes | | ADC0P.16<br>ADC0N.16 |
| 11 | P2.7 | Multifunction I/O | Yes | | ADC0P.15<br>ADC0N.15 |
| 12 | P2.6 | Multifunction I/O | Yes | | ADC0P.14<br>ADC0N.14 |
| 13 | P2.5 | Multifunction I/O | Yes | | ADC0P.13<br>ADC0N.13<br>CMP0N.3 |
| 14 | P2.4 | Multifunction I/O | Yes | | ADC0P.12<br>ADC0N.12<br>CMP0P.3 |
| 15 | P2.3 | Multifunction I/O | Yes | | ADC0P.11<br>ADC0N.11<br>CMP1N.2 |
| 16 | P2.2 | Multifunction I/O | Yes | | ADC0P.10<br>ADC0N.10<br>CMP1P.2 |
| 17 | P2.1 | Multifunction I/O | Yes | | ADC0P.9<br>ADC0N.9<br>CMP0N.2 |
| 18 | P2.0 | Multifunction I/O | Yes | | ADC0P.8<br>ADC0N.8<br>CMP0P.2 |
| 19 | P1.7 | Multifunction I/O | Yes | | ADC0P.7<br>ADC0N.7<br>CMP1N.1 |
| 20 | P1.6 | Multifunction I/O | Yes | | ADC0P.6<br>ADC0N.6<br>CMP1P.1 |

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| Pin Number | Pin Name | Description | Crossbar Capability | Additional Digital Functions | Analog Functions |
|---|---|---|---|---|---|
| 21 | P1.5 | Multifunction I/O | Yes | | ADC0P.5<br>ADC0N.5<br>CMP0N.1 |
| 22 | P1.4 | Multifunction I/O | Yes | | ADC0P.4<br>ADC0N.4<br>CMP0P.1 |
| 23 | P1.3 | Multifunction I/O | Yes | | ADC0P.3<br>ADC0N.3<br>CMP1N.0 |
| 24 | P1.2 | Multifunction I/O | Yes | | ADC0P.2<br>ADC0N.2<br>CMP1P.0 |
| 25 | P1.1 | Multifunction I/O | Yes | | ADC0P.1<br>ADC0N.1<br>CMP0N.0 |
| 26 | P1.0 | Multifunction I/O | Yes | | ADC0P.0<br>ADC0N.0<br>CMP0P.0 |
| 27 | P0.7 | Multifunction I/O | Yes | INT0.7<br>INT1.7 | VREF |
| 28 | P0.6 | Multifunction I/O | Yes | CNVSTR<br>INT0.6<br>INT1.6 | |
| 29 | P0.5 | Multifunction I/O | Yes | INT0.5<br>INT1.5<br>UART0_RX | ADC0P.20<br>ADC0N.20<br>CMP1N.4 |
| 30 | P0.4 | Multifunction I/O | Yes | INT0.4<br>INT1.4<br>UART0_TX | ADC0P.19<br>ADC0N.19<br>CMP1P.4 |
| 31 | P0.3 | Multifunction I/O | Yes | EXTCLK<br>INT0.3<br>INT1.3 | |
| 32 | P0.2 | Multifunction I/O | Yes | INT0.2<br>INT1.2 | |
| Center | GND | Ground | | | |

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# 5. TQFP48 Package Specifications

## 5.1 TQFP48 Package Dimensions

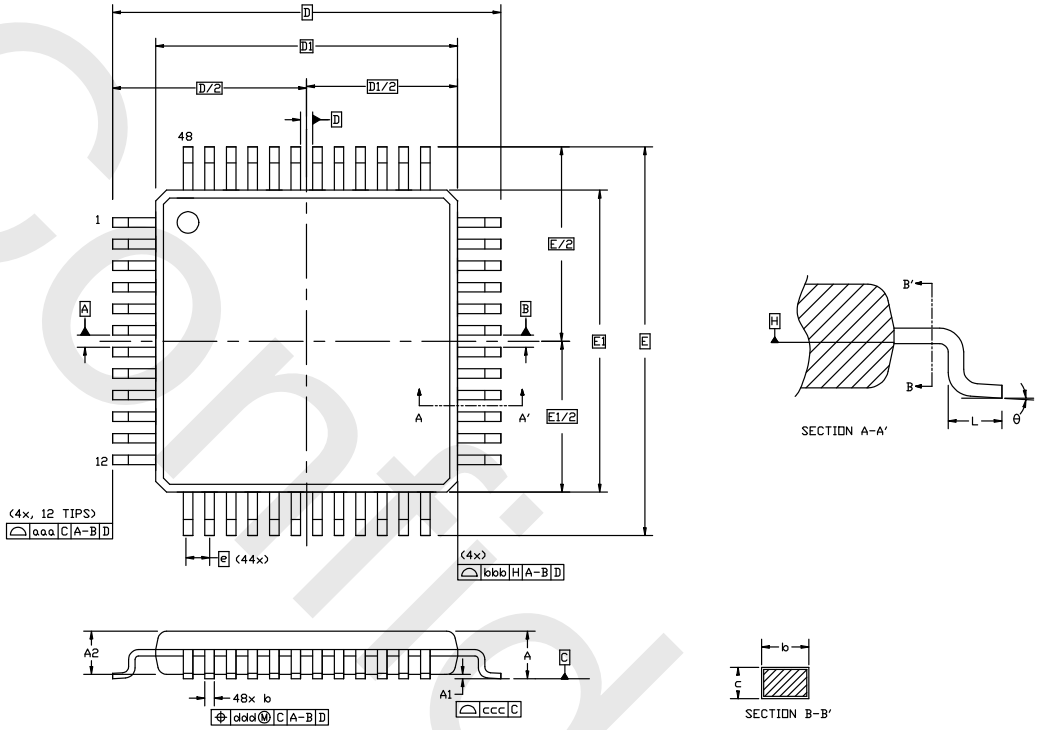


**Figure 5.1. TQFP48 Package Drawing**

**Table 5.1. TQFP48 Package Dimensions**

| Dimension | Min | Typ | Max |
|---|---|---|---|
| A | — | — | 1.20 |
| A1 | 0.05 | — | 0.15 |
| A2 | 0.95 | 1.00 | 1.05 |
| b | 0.17 | 0.22 | 0.27 |
| D | | 9.00 BSC | |
| D1 | | 7.00 BSC | |
| e | | 0.50 BSC | |
| E | | 9.00 BSC | |
| E1 | | 7.00 BSC | |
| L | 0.45 | 0.60 | 0.75 |
| aaa | | 0.20 | |
| bbb | | 0.20 | |

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| Dimension | Min | Typ | Max |
|---|---|---|---|
| ccc | | 0.08 | |
| ddd | | 0.08 | |
| theta | 0° | 3.5° | 7° |

**Note:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MS-026, variation ABC.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

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### 5.2 TQFP48 PCB Land Pattern

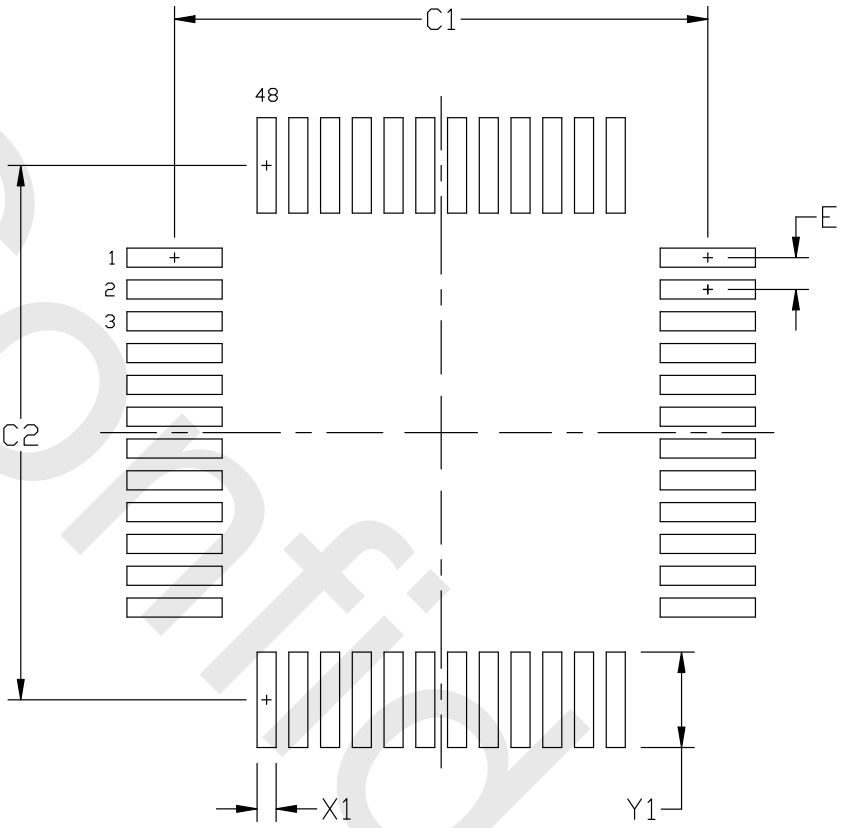


**Figure 5.2. TQFP48 PCB Land Pattern Drawing**

**Table 5.2. TQFP48 PCB Land Pattern Dimensions**

| Dimension | Min | Max |
|---|---|---|
| C1 | 8.30 | 8.40 |
| C2 | 8.30 | 8.40 |
| E | 0.50 BSC | |
| X1 | 0.20 | 0.30 |
| Y1 | 1.40 | 1.50 |

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| Dimension | Min | Max |
|---|---|---|

**Note:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A No-Clean, Type-3 solder paste is recommended.
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

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# 6. LQFP32 Package Specifications

## 6.1 LQFP32 Package Dimensions

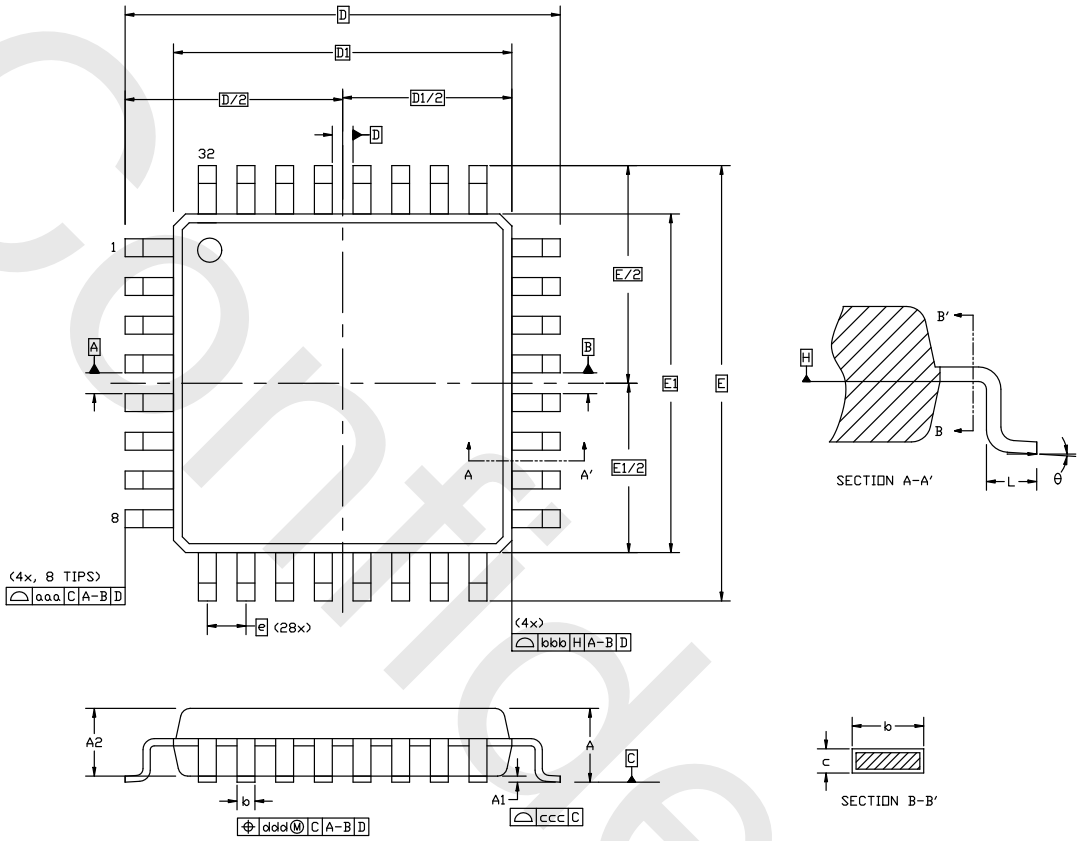


**Figure 6.1. LQFP32 Package Drawing**

**Table 6.1. LQFP32 Package Dimensions**

| Dimension | Min | Typ | Max |
|---|---|---|---|
| A | — | — | 1.60 |
| A1 | 0.05 | — | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| b | 0.30 | 0.37 | 0.45 |
| D | | 9.00 BSC | |
| D1 | | 7.00 BSC | |
| e | | 0.80 BSC | |
| E | | 9.00 BSC | |
| E1 | | 7.00 BSC | |
| L | 0.45 | 0.60 | 0.75 |
| aaa | | 0.20 | |

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| Dimension | Min | Typ | Max |
|---|---|---|---|
| bbb | | 0.20 | |
| ccc | | 0.10 | |
| ddd | | 0.20 | |
| theta | 0° | 3.5° | 7° |

**Note:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MS-026, variation BBA.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

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### 6.2 LQFP32 PCB Land Pattern

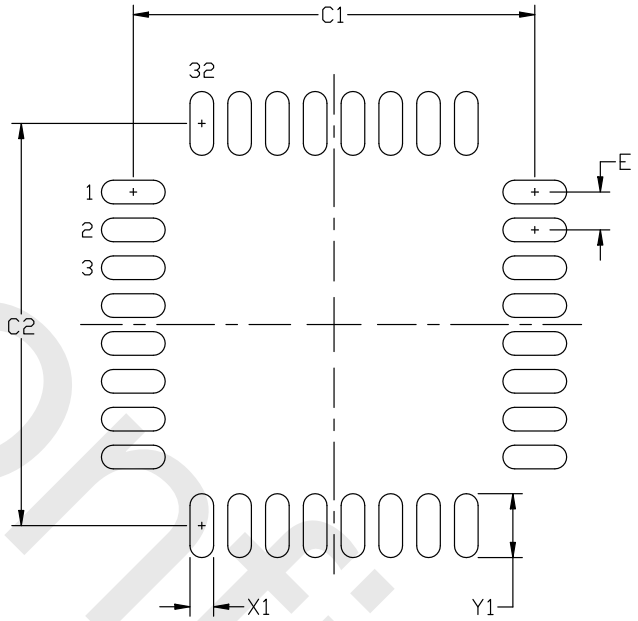


**Figure 6.2. LQFP32 PCB Land Pattern Drawing**

**Table 6.2. LQFP32 PCB Land Pattern Dimensions**

| Dimension | Min | Max |
|---|---|---|
| C1 | 8.40 | 8.50 |
| C2 | 8.40 | 8.50 |
| E | 0.80 BSC | |
| X1 | 0.40 | 0.50 |
| Y1 | 1.25 | 1.35 |

**Note:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A No-Clean, Type-3 solder paste is recommended.
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

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# 7. QFN32 Package Specifications

## 7.1 QFN32 Package Dimensions

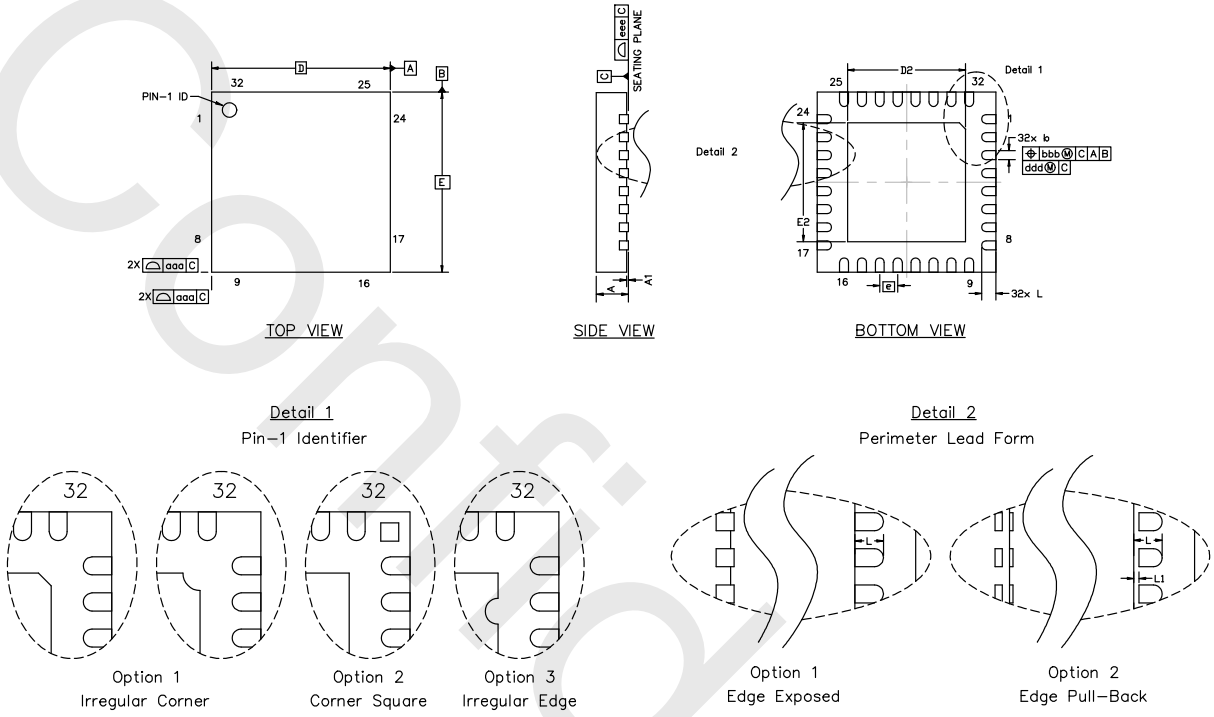


**Figure 7.1. QFN32 Package Drawing**

**Table 7.1. QFN32 Package Dimensions**

| Dimension | Min | Typ | Max |
|---|---|---|---|
| A | 0.80 | 0.85 | 0.90 |
| A1 | 0.00 | 0.02 | 0.05 |
| b | 0.18 | 0.25 | 0.30 |
| D | | 5.00 BSC | |
| D2 | 3.20 | 3.30 | 3.40 |
| e | | 0.50 BSC | |
| E | | 5.00 BSC | |
| E2 | 3.20 | 3.30 | 3.40 |
| L | 0.30 | 0.40 | 0.50 |
| L1 | 0.00 | — | 0.15 |
| aaa | — | — | 0.15 |
| bbb | — | — | 0.10 |

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| Dimension | Min | Typ | Max |
|---|---|---|---|
| ddd | — | — | 0.05 |
| eee | — | — | 0.08 |

**Note:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Solid State Outline MO-220, variation VHHD except for custom features D2, E2, and L which are toleranced per supplier designation.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

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### 7.2 QFN32 PCB Land Pattern

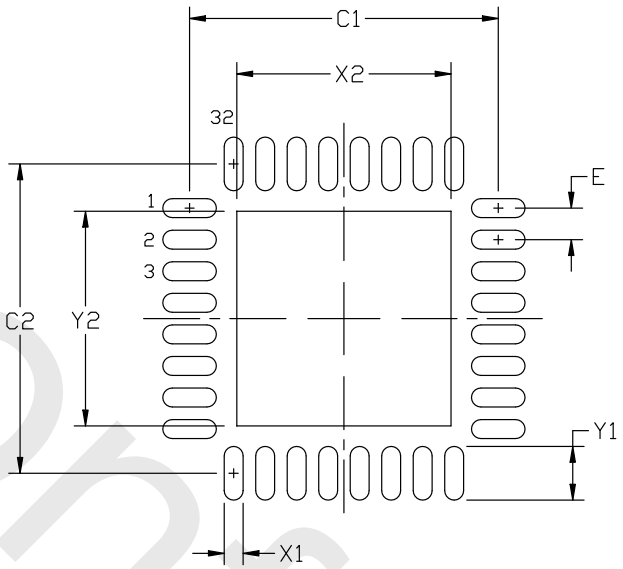


**Figure 7.2. QFN32 PCB Land Pattern Drawing**

**Table 7.2. QFN32 PCB Land Pattern Dimensions**

| Dimension | Min | Max |
|---|---|---|
| C1 | 4.80 | 4.90 |
| C2 | 4.80 | 4.90 |
| E | 0.50 BSC | |
| X1 | 0.20 | 0.30 |
| X2 | 3.20 | 3.40 |
| Y1 | 0.75 | 0.85 |
| Y2 | 3.20 | 3.40 |

**Note:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A 3 x 3 array of 1.0 mm x 1.0 mm openings on a 1.2 mm pitch should be used for the center pad.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

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