SST26WF016B/ SST26WF016BA

1.8V Serial Quad I/O (SQI) Flash Memory

Features

- Single Voltage Read and Write Operations
  - 1.65-1.95V
- Serial Interface Architecture
  - Nibble-wide multiplexed I/O's with SPI-like serial command structure
    - Mode 0 and Mode 3
  - x1/x2/x4 Serial Peripheral Interface (SPI) Protocol
- High Speed Clock Frequency
  - 104 MHz max
- Burst Modes
  - Continuous linear burst
  - 8/16/32/64 Byte linear burst with wrap-around
- Superior Reliability
  - Endurance: 100,000 Cycles (min)
  - Greater than 100 years Data Retention
- Low Power Consumption:
  - Active Read current: 15 mA (typical @ 104 MHz)
  - Standby current: 10 µA (typical)
  - Deep Power-Down current: 2.5 µA (typical)
- Page-Program
  - 256 Bytes per page in x1 or x4 mode
- End-of-Write Detection
  - Software polling the BUSY bit in status register
- Flexible Erase Capability
  - Uniform 4 KByte sectors
  - Four 8 KByte top and bottom parameter overlay blocks
  - One 32 KByte top and bottom overlay block
  - Uniform 64 KByte overlay blocks
- Write-Suspend
  - Suspend Program or Erase operation to access another block/sector
- Software Reset (RST) mode
- Software Write Protection
  - Individual Block-Locking
    - 64 KByte blocks, two 32 KByte blocks, and eight 8 KByte parameter blocks
- Security ID
  - One-Time Programmable (OTP) 2 KByte, Secure ID
    - 64 bit unique, factory pre-programmed identifier
    - User-programmable area
- Temperature Range
  - Industrial: -40°C to +85°C
- Packages Available
  - 8-contact WDFN (6mm x 5mm)
  - 8-lead SOIC (150 mil)
  - 8-ball XFBGA (Z-Scale™)
- All devices are RoHS compliant

Product Description

The Serial Quad I/O™ (SQI™) family of flash-memory devices features a six-wire, 4-bit I/O interface that allows for low-power, high-performance operation in a low pin-count package. SST26WF016B/016BA also support full command-set compatibility to traditional Serial Peripheral Interface (SPI) protocol. System designs using SQI flash devices occupy less board space and ultimately lower system costs.

All members of the 26 Series, SQI family are manufactured with SST proprietary, high-performance CMOS SuperFlash® technology. The split-gate cell design and thick-oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches.

The SST26WF016B/SST26WF016BA significantly improves performance and reliability, while lowering power consumption. This device writes (Program or Erase) with a single power supply of 1.65-1.95V. The total energy consumed is a function of the applied voltage, current, and time of application. Since for any given voltage range, the SuperFlash technology uses less current to program and has a shorter erase time, the total energy consumed during any Erase or Program operation is less than alternative flash memory technologies.

SST26WF016B/016BA is offered in 8-contact WDFN (6 mm x 5 mm), 8-lead SOIC (150 mil), and 8-ball XFBGA (Z-Scale™) packages. See Figure 2-1 for pin assignments.

Two configurations are available upon order: SST26WF016B default at power-up has the WP# and Hold# pins enabled and SST26WF016BA default at power-up has the WP# and Hold# pins disabled.

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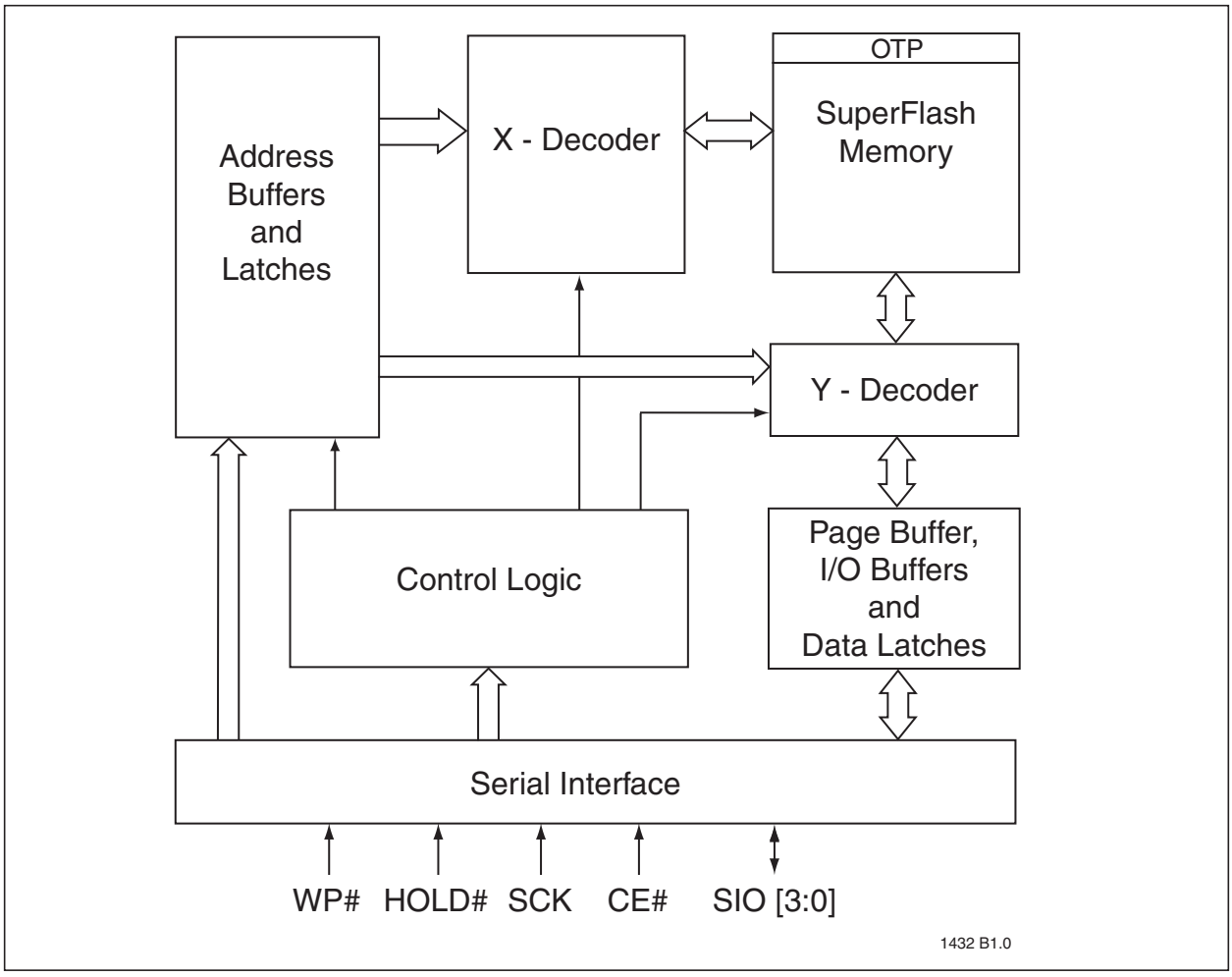
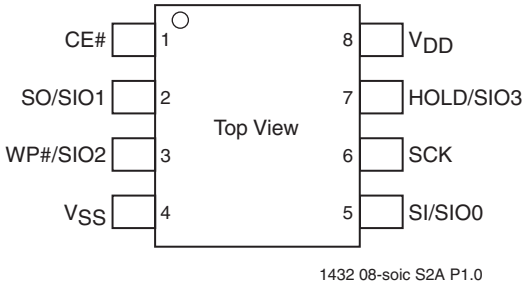
1.0 BLOCK DIAGRAM

FIGURE 1-1: FUNCTIONAL BLOCK DIAGRAM

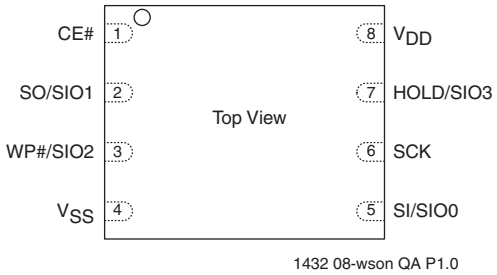


2.0 PIN DESCRIPTION

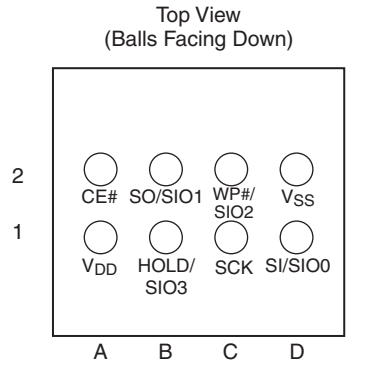
FIGURE 2-1: PIN DESCRIPTION FOR 8-LEAD SOIC, 8-CONTACT WDFN, AND 8-BALL XFBGA



8-Lead SOIC



8-Contact WDFN



8-Ball XFBGA

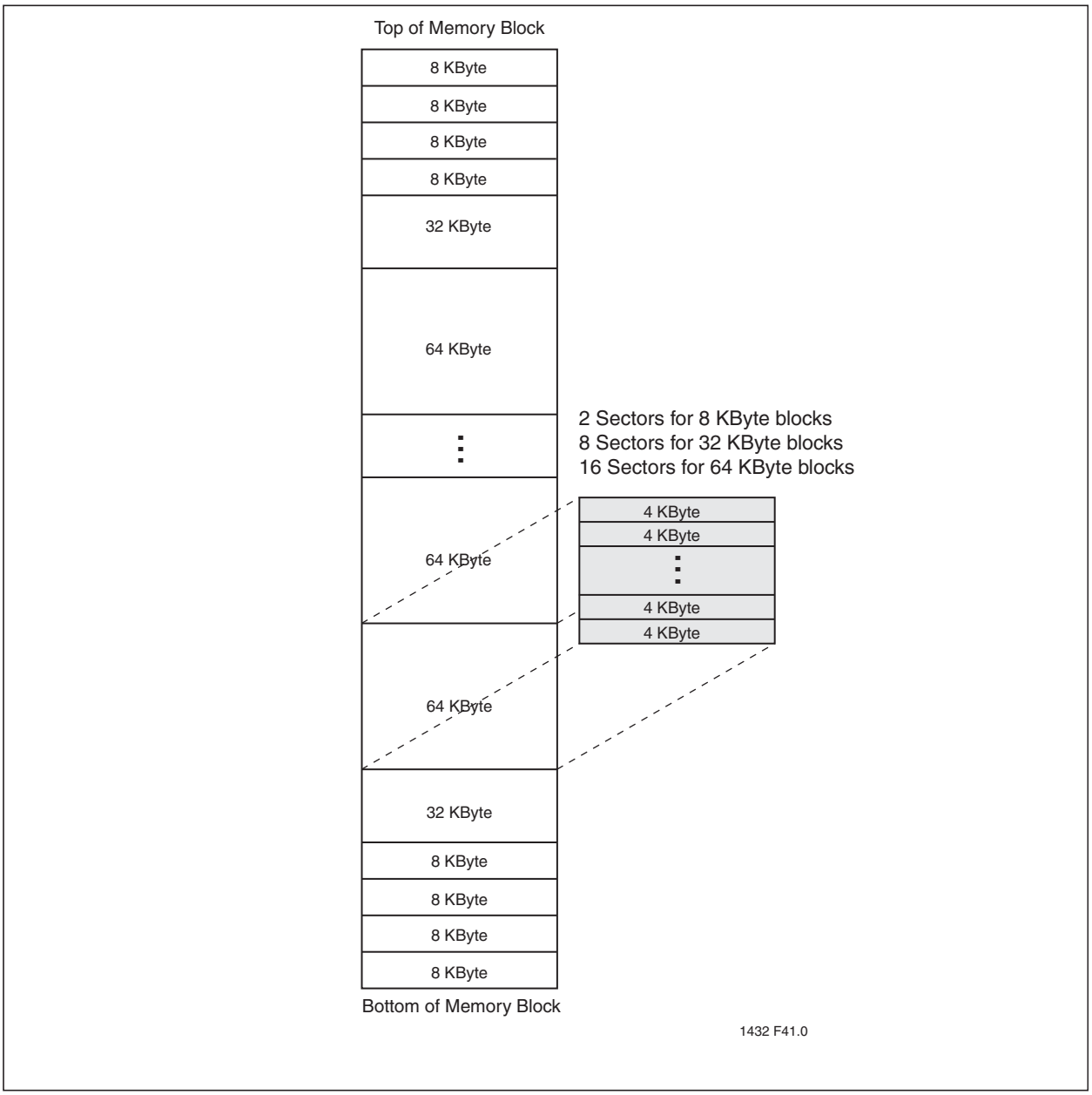
TABLE 2-1: PIN DESCRIPTION

Symbol	Pin Name	Functions
SCK	Serial Clock	To provide the timing of the serial interface. Commands, addresses, or input data are latched on the rising edge of the clock input, while output data is shifted out on the falling edge of the clock input.
SIO[3:0]	Serial Data Input/Output	To transfer commands, addresses, or data serially into the device or data out of the device. Inputs are latched on the rising edge of the serial clock. Data is shifted out on the falling edge of the serial clock. The Enable Quad I/O (EQIO) command instruction configures these pins for Quad I/O mode.
SI	Serial Data Input for SPI mode	To transfer commands, addresses or data serially into the device. Inputs are latched on the rising edge of the serial clock. SI is the default state after a power on reset.
SO	Serial Data Output for SPI mode	To transfer data serially out of the device. Data is shifted out on the falling edge of the serial clock. SO is the default state after a power on reset.
CE#	Chip Enable	The device is enabled by a high to low transition on CE#. CE# must remain low for the duration of any command sequence; or in the case of Write operations, for the command/data input sequence.
WP#	Write Protect	The WP# pin is used in conjunction with the WPEN and IOC bits in the configuration register to prohibit Write operations to the Block-Protection register. This pin only works in SPI, single-bit and dual-bit Read mode.
HOLD#	Hold	Temporarily stops serial communication with the SPI Flash memory while the device is selected. This pin only works in SPI, single-bit and dual-bit Read mode. This pin must be tied high when not in use.
V_{DD}	Power Supply	To provide power supply voltage.
V_{SS}	Ground	

3.0 MEMORY ORGANIZATION

The SST26WF016B/016BA SQI memory array is organized in uniform, 4 KByte erasable sectors with the following erasable blocks: eight 8 KByte parameter, two 32 KByte overlay, and thirty 64 KByte overlay blocks. See Figure 3-1.

FIGURE 3-1: MEMORY MAP



4.0 DEVICE OPERATION

The SST26WF016B/016BA support both Serial Peripheral Interface (SPI) bus protocol and a 4-bit multiplexed SQI bus protocol. To provide backward compatibility to traditional SPI Serial Flash devices, the device's initial state after a power-on reset is SPI mode which supports multi-I/O (x1/x2/x4) Read/Write commands. A command instruction configures the device to SQI mode. The dataflow in the SQI mode is similar to the SPI mode, except it uses four multiplexed I/O signals for command, address, and data sequence.

SQI Flash Memory supports both Mode 0 (0,0) and Mode 3 (1,1) bus operations. The difference between the two modes is the state of the SCK signal when the bus master is in stand-by mode and no data is being transferred. The SCK signal is low for Mode 0 and SCK signal is high for Mode 3. For both modes, the Serial Data I/O (SIO[3:0]) is sampled at the rising edge of the SCK clock signal for input, and driven after the falling edge of the SCK clock signal for output. The traditional SPI protocol uses separate input (SI) and output (SO) data signals as shown in Figure 4-1. The SQI protocol uses four multiplexed signals, SIO[3:0], for both data in and data out, as shown in Figure 4-2. This means the SQI protocol quadruples the traditional bus transfer speed at the same clock frequency, without the need for more pins on the package.

FIGURE 4-1: SPI PROTOCOL (TRADITIONAL 25 SERIES SPI DEVICE)

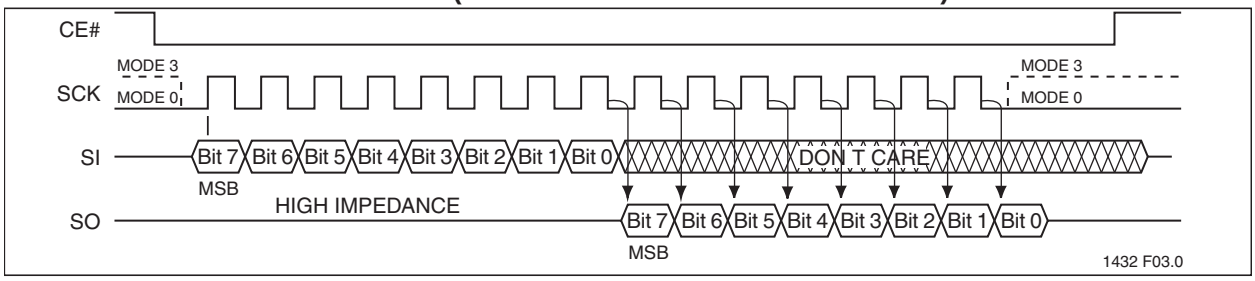
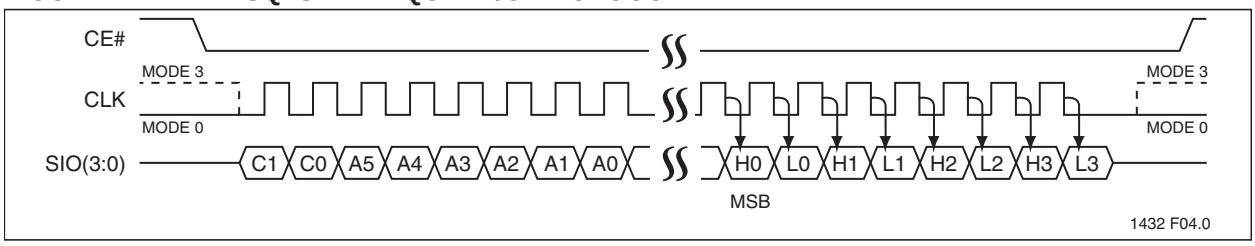


FIGURE 4-2: SQI SERIAL QUAD I/O PROTOCOL



4.1 Device Protection

The SST26WF016B/016BA offers a flexible memory protection scheme that allows the protection state of each individual block to be controlled separately. In addition, the Write-Protection Lock-Down register prevents any change of the lock status during device operation. To avoid inadvertent writes during power-up, the device is write-protected by default after a power-on reset cycle. A Global Block-Protection Unlock command offers a single command cycle that unlocks the entire memory array for faster manufacturing throughput.

For extra protection, there is an additional non-volatile register that can permanently write-protect the Block-Protection register bits for each individual block. Each of the corresponding lock-down bits are one time programmable (OTP)—once written, they cannot be erased. Data that had been previously programmed into these blocks cannot be altered by programming or erase and is not reversible

4.1.1 INDIVIDUAL BLOCK PROTECTION

The SST26WF016B/016BA has a Block-Protection register which provides a software mechanism to write-lock the individual memory blocks and write-lock, and/or read-lock, the individual parameter blocks. The Block-Protection register is 48 bits wide: two bits each for the eight 8 KByte parameter blocks (write-lock and read-lock), and one bit each for the remaining 32 KByte and 64 KByte overlay blocks (write-lock). See Table 5-6 for address range protected per register bit.

Each bit in the Block-Protection register (BPR) can be written to a '1' (protected) or '0' (unprotected). For the parameter blocks, the most significant bit is for read-lock, and the least significant bit is for write-lock. Read-locking the parameter blocks provides additional security for sensitive data after retrieval (e.g., after initial boot). If a block is read-locked all reads to the block return data 00H.

The Write Block-Protection Register command is a two-cycle command which requires that Write-Enable (WREN) is executed prior to the Write Block-Protection

Register command. The Global Block-Protection Unlock command clears all write protection bits in the Block-Protection register.

4.1.2 WRITE-PROTECTION LOCK-DOWN (VOLATILE)

To prevent changes to the Block-Protection register, use the Lock-Down Block-Protection Register (LBPR) command to enable Write-Protection Lock-Down. Once Write-Protection Lock-Down is enabled, the Block-Protection register can not be changed. To avoid inadvertent lock down, the WREN command must be executed prior to the LBPR command.

To reset Write-Protection Lock-Down, performing a power cycle on the device is required. The Write-Protection Lock-Down status may be read from the Status register.

4.1.3 WRITE-LOCK LOCK-DOWN (NON-VOLATILE)

The non-Volatile Write-Lock Lock-Down register is an alternate register that permanently prevents changes to the block-protect bits. The non-Volatile Write-Lock Lock-Down register (nVWLDR) is 40 bits wide per device: one bit each for the eight 8-KByte parameter blocks, and one bit each for the remaining 32 KByte and 64 KByte overlay blocks. See Table 5-6 for address range protected per register bit.

Writing ‘1’ to any or all of the nVWLDR bits disables the change mechanism for the corresponding Write-Lock bit in the BPR, and permanently sets this bit to a ‘1’ (protected) state. After this change, both bits will be set to ‘1’, regardless of the data entered in subsequent writes to either the nVWLDR or the BPR. Subsequent writes to the nVWLDR can only alter available locations that have not been previously written to a ‘1’. This method provides write-protection for the corresponding memory-array block by protecting it from future program or erase operations.

Writing a ‘0’ in any location in the nVWLDR has no effect on either the nVWLDR or the corresponding Write-Lock bit in the BPR.

Note that if the Block-Protection register had been previously locked down, see “ Write-Protection Lock-Down (Volatile)”, the device must be power cycled before using the nVWLDR. If the Block-Protection register is locked down and the Write nVWLDR command is accessed, the command will be ignored.

4.2 Hardware Write Protection

The hardware Write Protection pin (WP#) is used in conjunction with the WPEN and IOC bits in the configuration register to prohibit write operations to the Block-Protection and Configuration registers. The WP# pin function only works in SPI single-bit and dual-bit read mode when the IOC bit in the configuration register is set to ‘0’.

The WP# pin function is disabled when the WPEN bit in the configuration register is ‘0’. This allows installation of the SST26WF016B/016BA in a system with a grounded WP# pin while still enabling Write to the Block-Protection register. The Lock-Down function of the Block-Protection Register supersedes the WP# pin, see Table 4-1 for Write Protection Lock-Down states.

The factory default setting at power-up of the WPEN bit is ‘0’, disabling the Write Protect function of the WP# after power-up. WPEN is a non-volatile bit; once the bit is set to ‘1’, the Write Protect function of the WP# pin continues to be enabled after power-up. The WP# pin only protects the Block-Protection Register and Configuration Register from changes. Therefore, if the WP# pin is set to low before or after a Program or Erase command, or while an internal Write is in progress, it will have no effect on the Write command.

The IOC bit takes priority over the WPEN bit in the configuration register. When the IOC bit is ‘1’, the function of the WP# pin is disabled and the WPEN bit serves no function. When the IOC bit is ‘0’ and WPEN is ‘1’, setting the WP# pin active low prohibits Write operations to the Block Protection Register.

TABLE 4-1: WRITE PROTECTION LOCK-DOWN STATES

WP#	IOC	WPEN	WPLD	Execute WBPR Instruction	Configuration Register
L	0	1	1	Not Allowed	Protected
L	0	0	1	Not Allowed	Writable
L	0	1	0	Not Allowed	Protected
L	0[1]	0[2]	0	Allowed	Writable
H	0	X	1	Not Allowed	Writable
H	0	X	0	Allowed	Writable
X	1	X	1	Not Allowed	Writable
X	1[3]	0[2]	0	Allowed	Writable

1. Default at power-up Register settings for SST26WF016B
2. Factory default setting is ‘0’. This is a non-volatile bit; default at power-up is the value set prior to power-down.
3. Default at power-up Register settings for SST26WF016BA

4.3 Security ID

SST26WF016B/016BA offers a 2 KByte Security ID (Sec ID) feature. The Security ID space is divided into two parts – one factory-programmed, 64-bit segment and one user-programmable segment. The factory-programmed segment is programmed during manufacturing with a unique number and cannot be changed. The user-programmable segment is left unprogrammed for the customer to program as desired.

Use the Program Security ID (PSID) command to program the Security ID using the address shown in Table 5-5. The Security ID can be locked using the Lockout Security ID (LSID) command. This prevents any future write operations to the Security ID.

The factory-programmed portion of the Security ID can't be programmed by the user; neither the factory-programmed nor user-programmable areas can be erased.

4.4 Hold Operation

The HOLD# pin pauses active serial sequences without resetting the clocking sequence. **This pin is active after every power up and only operates during SPI single-bit and dual-bit modes**. Two factory configurations are available: SST26WF016B ships with the IOC bit set to '0' and the HOLD# pin function enabled; SST26WF016BA ships with the IOC bit set to '1' and the HOLD# pin function disabled. The HOLD# pin is always disabled in SQI mode and only works in SPI single-bit and dual-bit read mode.

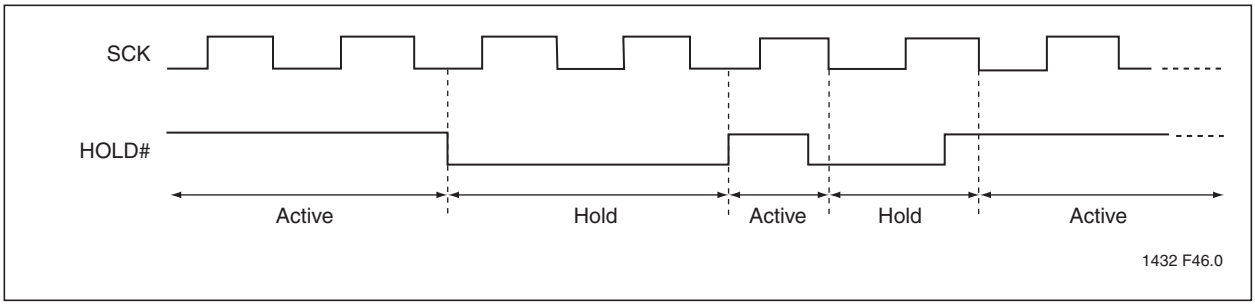
To activate the Hold mode, CE# must be in active low state. The Hold mode begins when the SCK active low state coincides with the falling edge of the HOLD# signal. The Hold mode ends when the HOLD# signal's rising edge coincides with the SCK active low state.

If the falling edge of the HOLD# signal does not coincide with the SCK active low state, then the device enters Hold mode when the SCK next reaches the active low state. Similarly, if the rising edge of the HOLD# signal does not coincide with the SCK active low state, then the device exits Hold mode when the SCK next reaches the active low state. See Figure 4-3.

Once the device enters Hold mode, SO will be in high impedance state while SI and SCK can be V_{IL} or V_{IH}.

If CE# is driven active high during a Hold condition, it resets the internal logic of the device. As long as HOLD# signal is low, the memory remains in the Hold condition. To resume communication with the device, HOLD# must be driven active high, and CE# must be driven active low.

FIGURE 4-3: HOLD CONDITION WAVEFORM.



4.5 Status Register

The Status register is a read-only register that provides the following status information: whether the flash memory array is available for any Read or Write operation, if the device is write-enabled, whether an erase or program operation is suspended, and if the Block-Protection register and/or Security ID are locked down. During an internal Erase or Program operation, the Status register may be read to determine the completion of an operation in progress. Table 4-2 describes the function of each bit in the Status register.

TABLE 4-2: STATUS REGISTER

Bit	Name	Function	Default at Power-up	Read/Write (R/W)
0	BUSY	Write operation status 1 = Internal Write operation is in progress 0 = No internal Write operation is in progress	0	R
1	WEL	Write-Enable Latch status 1 = Device is write-enabled 0 = Device is not write-enabled	0	R
2	WSE	Write Suspend-Erase status 1 = Erase suspended 0 = Erase is not suspended	0	R
3	WSP	Write Suspend-Program status 1 = Program suspended 0 = Program is not suspended	0	R
4	WPLD	Write Protection Lock-Down status 1 = Write Protection Lock-Down enabled 0 = Write Protection Lock-Down disabled	0	R
5	SEC[1]	Security ID status 1 = Security ID space locked 0 = Security ID space not locked	0[1]	R
6	RES	Reserved for future use	0	R
7	BUSY	Write operation status 1 = Internal Write operation is in progress 0 = No internal Write operation is in progress	0	R

1. The Security ID status will always be ‘1’ at power-up after a successful execution of the Lockout Security ID instruction, otherwise default at power-up is ‘0’.

4.5.1 WRITE-ENABLE LATCH (WEL)

The Write-Enable Latch (WEL) bit indicates the status of the internal memory’s Write-Enable Latch. If the WEL bit is set to ‘1’, the device is write enabled. If the bit is set to ‘0’ (reset), the device is not write enabled and does not accept any memory Program or Erase, Protection Register Write, or Lock-Down commands. The Write-Enable Latch bit is automatically reset under the following conditions:

- Power-up
- Reset
- Write-Disable (WRDI) instruction
- Page-Program instruction completion
- Sector-Erase instruction completion
- Block-Erase instruction completion
- Chip-Erase instruction completion
- Write-Block-Protection register instruction
- Lock-Down Block-Protection register instruction
- Program Security ID instruction completion
- Lockout Security ID instruction completion
- Write-Suspend instruction
- SPI Quad Page Program
- Write Status Register

4.5.2 WRITE SUSPEND ERASE STATUS (WSE)

The Write Suspend-Erase status (WSE) indicates when an Erase operation has been suspended. The WSE bit is ‘1’ after the host issues a suspend command during an Erase operation. Once the suspended Erase resumes, the WSE bit is reset to ‘0’.

4.5.3 WRITE SUSPEND PROGRAM STATUS (WSP)

The Write Suspend-Program status (WSP) bit indicates when a Program operation has been suspended. The WSP is '1' after the host issues a suspend command during the Program operation. Once the suspended Program resumes, the WSP bit is reset to '0'.

4.5.4 WRITE PROTECTION LOCK-DOWN STATUS (WPLD)

The Write Protection Lock-Down status (WPLD) bit indicates when the Block-Protection register is locked-down to prevent changes to the protection settings. The WPLD is '1' after the host issues a Lock-Down Block-Protection command. After a power cycle, the WPLD bit is reset to '0'.

4.5.5 SECURITY ID STATUS (SEC)

The Security ID Status (SEC) bit indicates when the Security ID space is locked to prevent a Write command. The SEC is '1' after the host issues a Lockout SID command. Once the host issues a Lockout SID command, the SEC bit can never be reset to '0.'

4.5.6 BUSY

The Busy bit determines whether there is an internal Erase or Program operation in progress. If the BUSY bit is '1', the device is busy with an internal Erase or Program operation. If the bit is '0', no Erase or Program operation is in progress.

4.5.7 CONFIGURATION REGISTER

The Configuration register is a Read/Write register that stores a variety of configuration information. See Table 4-3 for the function of each bit in the register.

TABLE 4-3: CONFIGURATION REGISTER

Bit	Name	Function	Default at Power-up	Read/Write (R/W)
0	RES	Reserved	0	R
1	IOC	I/O Configuration for SPI Mode 1 = WP# and HOLD# pins disabled 0 = WP# and HOLD# pins enabled	0[1]	R/W
2	RES	Reserved	0	R
3	BPNV	Block-Protection Volatility State 1 = No memory block has been permanently locked 0 = Any block has been permanently locked	1	R
4	RES	Reserved	0	R
5	RES	Reserved	0	R
6	RES	Reserved	0	R
7	WPEN	Write-Protection Pin (WP#) Enable 1 = WP# enabled 0 = WP# disabled	0[2]	R/W

1. SST26WF016B default at Power-up is '0'
   SST26WF016BA default at Power-up is '1'
2. Factory default setting. This is a non-volatile bit; default at power-up will be the setting prior to power-down.

4.5.8 I/O CONFIGURATION (IOC)

The I/O Configuration (IOC) bit re-configures the I/O pins. The IOC bit is set by writing a ‘1’ to Bit 1 of the Configuration register. When IOC bit is ‘0’ the WP# pin and HOLD# pin are enabled (SPI or Dual Configuration setup). When IOC bit is set to ‘1’ the SIO2 pin and SIO3 pin are enabled (SPI Quad I/O Configuration setup). The IOC bit must be set to ‘1’ before issuing the following SPI commands: SQOR (6BH), SQIOR (EBH), RBSPI (ECH), and SPI Quad page program (32H). Without setting the IOC bit to ‘1’, those SPI commands are not valid. The I/O configuration bit does not apply when in SQI mode. The default at power-up for SST26WF016B is ‘0’ and for SST26WF016BA is ‘1’.

4.5.9 BLOCK-PROTECTION VOLATILITY STATE (BPNV)

The Block-Protection Volatility State bit indicates whether any block has been permanently locked with the non-Volatile Write-Lock Lock-Down register (nVWLDR). When no bits in the nVWLDR have been set (the default state from the factory) the BPNV bit is `1'; when one or more bits in the nVWLDR are set to `1' the BPNV bit will also be `0' from that point forward, even after power-up.

4.5.10 WRITE-PROTECT ENABLE (WPEN)

The Write-Protect Enable (WPEN) bit is a non-volatile bit that enables the WP# pin.

The Write-Protect (WP#) pin and the Write-Protect Enable (WPEN) bit control the programmable hardware write-protect feature. Setting the WP# pin to low, and the WPEN bit to ‘1’, enables Hardware write-protection. To disable Hardware write protection, set either the WP# pin to high or the WPEN bit to ‘0’. There is latency associated with writing to the WPEN bit. Poll the BUSY bit in the Status register, or wait T_{WPEN}, for the completion of the internal, self-timed Write operation. When the chip is hardware write protected, only Write operations to Block-Protection and Configuration registers are disabled. See “Hardware Write Protection” on page 8 and Table 4-1 for more information about the functionality of the WPEN bit.

5.0 INSTRUCTIONS

Instructions are used to read, write (erase and program), and configure the SST26WF016B/016BA. The complete list of the instructions is provided in Table 5-1.

TABLE 5-1: DEVICE OPERATION INSTRUCTIONS FOR SST26WF016B/016BA (1 OF 2)

Instruction	Description	Command Cycle[1]	Mode		Address Cycle(s)[2, 3]	Dummy Cycle(s)[3]	Data Cycle(s)[3]	Max Freq
			SPI	SQI				
Configuration								
NOP	No Operation	00H	X	X	0	0	0	104 MHz
RSTEN	Reset Enable	66H	X	X	0	0	0	
RST[4]	Reset Memory	99H	X	X	0	0	0	
EQIO	Enable Quad I/O	38H	X		0	0	0	
RSTQIO[5]	Reset Quad I/O	FFH	X	X	0	0	0	
RDSR	Read Status Register	05H	X		0	0	1 to ∞	
				X	0	1	1 to ∞	
WRSR	Write Status Register	01H	X	X	0	0	2	
RDCR	Read Configuration Register	35H	X		0	0	1 to ∞	
				X	0	1	1 to ∞	
Read								
Read	Read Memory	03H	X		3	0	1 to ∞	40 MHz
High-Speed Read	Read Memory at Higher Speed	0BH		X	3	3	1 to ∞	104 MHz
			X		3	1	1 to ∞	
SQOR[6]	SPI Quad Output Read	6BH	X		3	1	1 to ∞	
SQIOR[7]	SPI Quad I/O Read	EBH	X		3	3	1 to ∞	
SDOR[8]	SPI Dual Output Read	3BH	X		3	1	1 to ∞	
SDIOR[9]	SPI Dual I/O Read	BBH	X		3	1	1 to ∞	80 MHz
SB	Set Burst Length	C0H	X	X	0	0	1	104 MHz
RBSQI	SQI nB Burst with Wrap	0CH		X	3	3	n to ∞	
RBSPI[7]	SPI nB Burst with Wrap	ECH	X		3	3	n to ∞	
Identification								
JEDEC-ID	JEDEC-ID Read	9FH	X		0	0	3 to ∞	104 MHz
Quad J-ID	Quad I/O J-ID Read	AFH		X	0	1	3 to ∞	
SFDP	Serial Flash Discoverable Parameters	5AH	X		3	1	1 to ∞	
Write								
WREN	Write Enable	06H	X	X	0	0	0	104 MHz
WRDI	Write Disable	04H	X	X	0	0	0	
SE[10]	Erase 4 KBytes of Memory Array	20H	X	X	3	0	0	
BE[11]	Erase 64, 32 or 8 KBytes of Memory Array	D8H	X	X	3	0	0	
CE	Erase Full Array	C7H	X	X	0	0	0	
PP	Page Program	02H	X	X	3	0	1 to 256	

TABLE 5-1: DEVICE OPERATION INSTRUCTIONS FOR SST26WF016B/016BA (CONTINUED) (2

Instruction	Description	Command Cycle[1]	Mode		Address Cycle(s)[2, 3]	Dummy Cycle(s)[3]	Data Cycle(s)[3]	Max Freq
			SPI	SQI				
SPI Quad PP[6]	SQI Quad Page Program	32H	X		3	0	1 to 256	104 MHz
WRSU	Suspends Program/ Erase	B0H	X	X	0	0	0	
WRRE	Resumes Program/ Erase	30H	X	X	0	0	0	
Protection								
RBPR	Read Block-Protection Register	72H	X		0	0	1 to 6	104 MHz
				X	0	1	1 to 6	
WBPR	Write Block-Protection Register	42H	X	X	0	0	1 to 6	
LBPR	Lock Down Block-Protection Register	8DH	X	X	0	0	0	
nVWLDR	non-Volatile Write Lock-Down Register	E8H	X	X	0	0	1 to 6	
ULBPR	Global Block Protection Unlock	98H	X	X	0	0	0	
RSID	Read Security ID	88H	X		2	1	1 to 2048	
				X	2	3	1 to 2048	
PSID	Program User Security ID area	A5H	X	X	2	0	1 to 256	
LSID	Lockout Security ID Programming	85H	X	X	0	0	0	
Power Saving								
DPD	Deep Power-down Mode	B9H	X	X	0	0	0	104 MHz
RDPD	Release from Deep Power-down and Read ID	ABH	X	X	3	0	1 to ∞	

0

1. Command cycle is two clock periods in SQI mode and eight clock periods in SPI mode.
2. Address bits above the most significant bit of each density can be V_{IL} or V_{IH}.
3. Address, Dummy/Mode bits, and Data cycles are two clock periods in SQI and eight clock periods in SPI mode.
4. RST command only executed if RSTEN command is executed first. Any intervening command will disable Reset.
5. Device accepts eight-clock command in SPI mode, or two-clock command in SQI mode.
6. Data cycles are two clock periods. IOC bit must be set to '1' before issuing the command.
7. Address, Dummy/Mode bits, and data cycles are two clock periods. IOC bit must be set to '1' before issuing the command.
8. Data cycles are four clock periods.
9. Address, Dummy/Mode bits, and Data cycles are four clock periods.
10. Sector Addresses: Use A_{MS} - A_{12}, remaining address are don't care, but must be set to V_{IL} or V_{IH}.
11. Blocks are 64 KByte, 32 KByte, or 8KByte, depending on location. Block Erase Address: A_{MS} - A_{16} for 64 KByte; A_{MS} - A_{15} for 32 KByte; A_{MS} - A_{13} for 8 KByte. Remaining addresses are don't care, but must be set to V_{IL} or V_{IH}.

5.1 No Operation (NOP)

The No Operation command only cancels a Reset Enable command. NOP has no impact on any other command.

5.2 Reset-Enable (RSTEN) and Reset (RST)

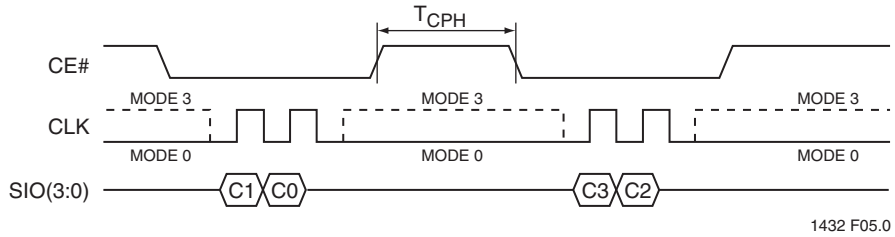
The Reset operation is used as a system (software) reset that puts the device in normal operating Ready mode. This operation consists of two commands: Reset-Enable (RSTEN) followed by Reset (RST).

To reset the SST26WF016B/016BA, the host drives CE# low, sends the Reset-Enable command (66H), and drives CE# high. Next, the host drives CE# low again, sends the Reset command (99H), and drives CE# high, see Figure 5-1.

The Reset operation requires the Reset-Enable command followed by the Reset command. Any command other than the Reset command after the Reset-Enable command will disable the Reset-Enable.

Once the Reset-Enable and Reset commands are successfully executed, the device returns to normal operation Read mode and then does the following: resets the protocol to SPI mode, resets the burst length to 8 Bytes, clears all the bits, except for bit 4 (WPLD) and bit 5 (SEC), in the Status register to their default states, and clears bit 1 (IOC) in the configuration register to its default state. A device reset during an active Program or Erase operation aborts the operation, which can cause the data of the targeted address range to be corrupted or lost. Depending on the prior operation, the reset timing may vary. Recovery from a Write operation requires more latency time than recovery from other operations. See Table 6-9 on page 45 for Rest timing parameters.

FIGURE 5-1: RESET SEQUENCE



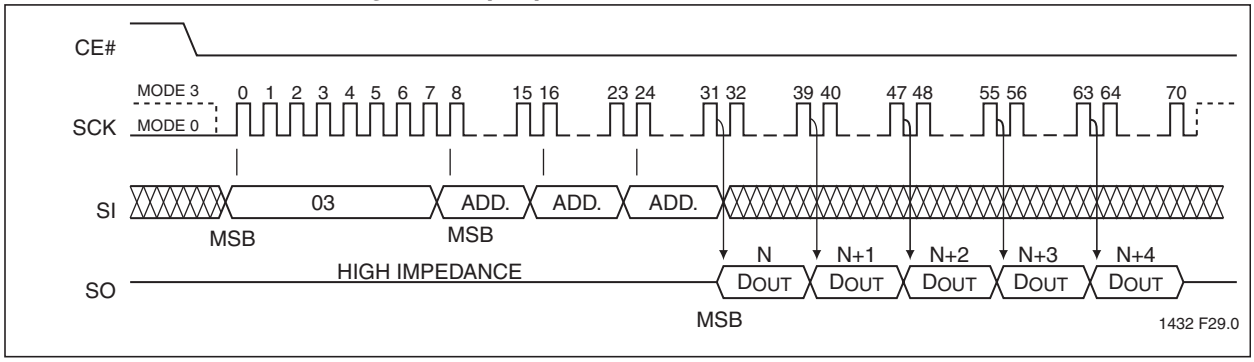
Note: C[1:0] = 66H; C[3:2] = 99H

5.3 Read (40 MHz)

The Read instruction, 03H, is supported in SPI bus protocol only with clock frequencies up to 40 MHz. This command is not supported in SQI bus protocol. The device outputs the data starting from the specified address location, then continuously streams the data output through all addresses until terminated by a low-to-high transition on CE#. The internal address pointer will automatically increment until the highest memory address is reached. Once the highest memory address is reached, the address pointer will automatically return to the beginning (wrap-around) of the address space.

Initiate the Read instruction by executing an 8-bit command, 03H, followed by address bits A[23:0]. CE# must remain active low for the duration of the Read cycle. See Figure 5-2 for Read Sequence.

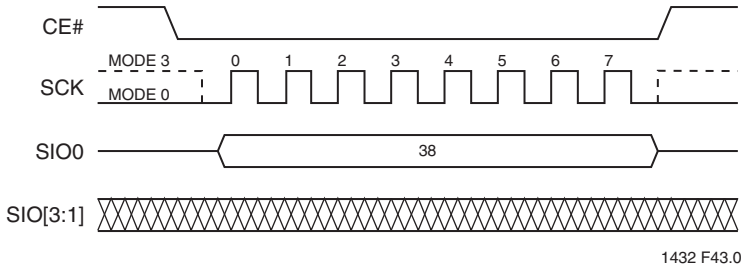
FIGURE 5-2: READ SEQUENCE (SPI)



5.4 Enable Quad I/O (EQIO)

The Enable Quad I/O (EQIO) instruction, 38H, enables the flash device for SQI bus operation. Upon completion of the instruction, all instructions thereafter are expected to be 4-bit multiplexed input/output (SQI mode) until a power cycle or a “Reset Quad I/O instruction” is executed. See Figure 5-3.

FIGURE 5-3: ENABLE QUAD I/O SEQUENCE



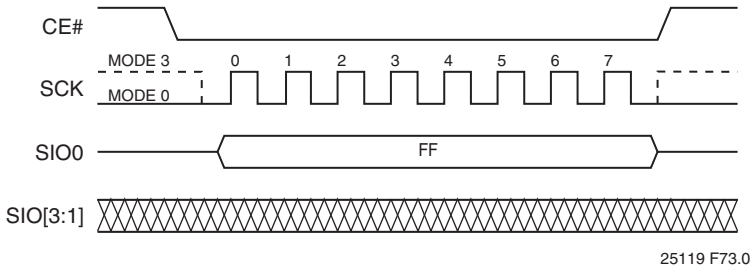
Note: SIO[3:1] must be driven V_{IH}

5.5 Reset Quad I/O (RSTQIO)

The Reset Quad I/O instruction, FFH, resets the device to 1-bit SPI protocol operation or exits the Set Mode configuration during a read sequence. This command allows the flash device to return to the default I/O state (SPI) without a power cycle, and executes in either 1-bit or 4-bit mode. If the device is in the Set Mode configuration, while in SQI High-Speed Read mode, the RSTQIO command will only return the device to a state where it can accept new SQI command instruction. An additional RSTQIO is required to reset the device to SPI mode.

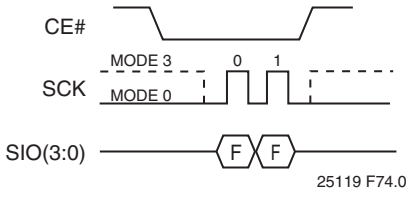
To execute a Reset Quad I/O operation, the host drives CE# low, sends the Reset Quad I/O command cycle (FFH) then, drives CE# high. Execute the instruction in either SPI (8 clocks) or SQI (2 clocks) command cycles. For SPI, SIO[3:1] are don’t care for this command, but should be driven to V_{IH} or V_{IL}. See Figures 5-4 and 5-5.

FIGURE 5-4: RESET QUAD I/O SEQUENCE (SPI)



Note: SIO[3:1] must be driven V_{IH}

FIGURE 5-5: RESET QUAD I/O SEQUENCE (SQI)

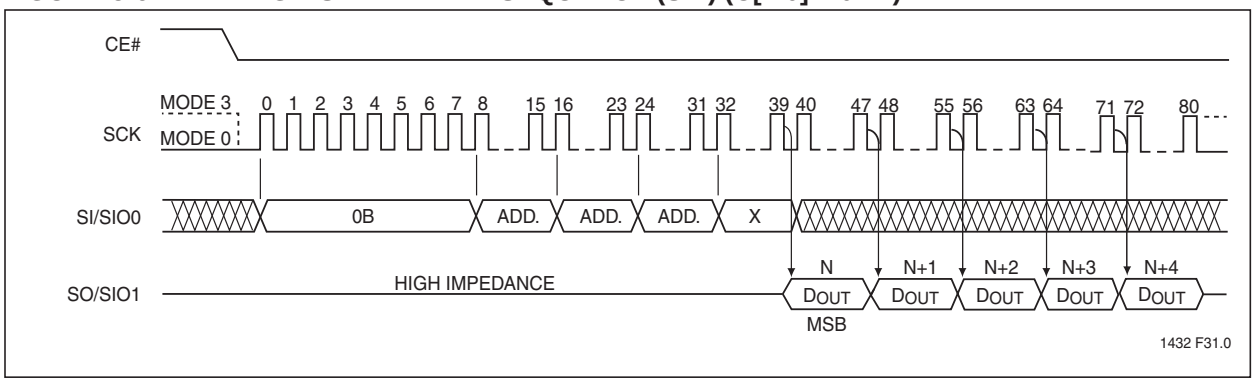


5.6 High-Speed Read (104 MHz)

The High-Speed Read instruction, 0BH, is supported in both SPI bus protocol and SQI protocol. On power-up, the device is set to use SPI.

Initiate High-Speed Read by executing an 8-bit command, 0BH, followed by address bits A[23-0] and a dummy byte. CE# must remain active low for the duration of the High-Speed Read cycle. See Figure 5-6 for the High-Speed Read sequence for SPI bus protocol.

FIGURE 5-6: HIGH-SPEED READ SEQUENCE (SPI) (C[1:0] = 0BH)



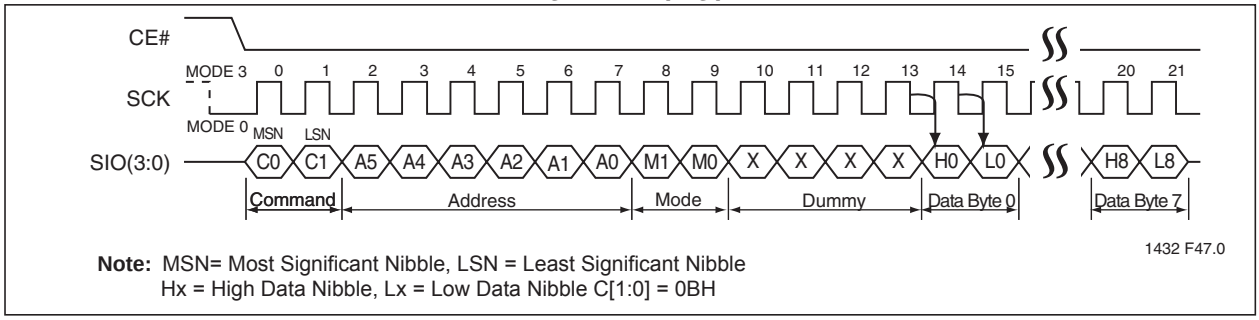
In SQI protocol, the host drives CE# low then send the Read command cycle command, 0BH, followed by three address cycles, a Set Mode Configuration cycle, and two dummy cycles. Each cycle is two nibbles (clocks) long, most significant nibble first.

After the dummy cycles, the device outputs data on the falling edge of the SCK signal starting from the specified address location. The device continually streams data output through all addresses until terminated by a low-to-high transition on CE#. The internal address pointer automatically increments until the highest memory address is reached, at which point the address pointer returns to address location 000000H. During this operation, blocks that are Read-locked will output data 00H.

The Set Mode Configuration bit M[7:0] indicates if the next instruction cycle is another SQI High-Speed Read command. When M[7:0] = AXH, the device expects the next continuous instruction to be another Read command, 0BH, and does not require the op-code to be entered again. The host may initiate the next Read cycle by driving CE# low, then sending the four-bits input for address A[23:0], followed by the Set Mode configuration bits M[7:0], and two dummy cycles. After the two dummy cycles, the device outputs the data starting from the specified address location. There are no restrictions on address location access.

When M[7:0] is any value other than AXH, the device expects the next instruction initiated to be a command instruction. To reset/exit the Set Mode configuration, execute the Reset Quad I/O command, FFH. While in the Set Mode configuration, the RSTQIO command will only return the device to a state where it can accept new SQI command instruction. An additional RSTQIO is required to reset the device to SPI mode. See Figure 5-10 for the SPI Quad I/O Mode Read sequence when M[7:0] = AXH.

FIGURE 5-7: HIGH-SPEED READ SEQUENCE (SQI)



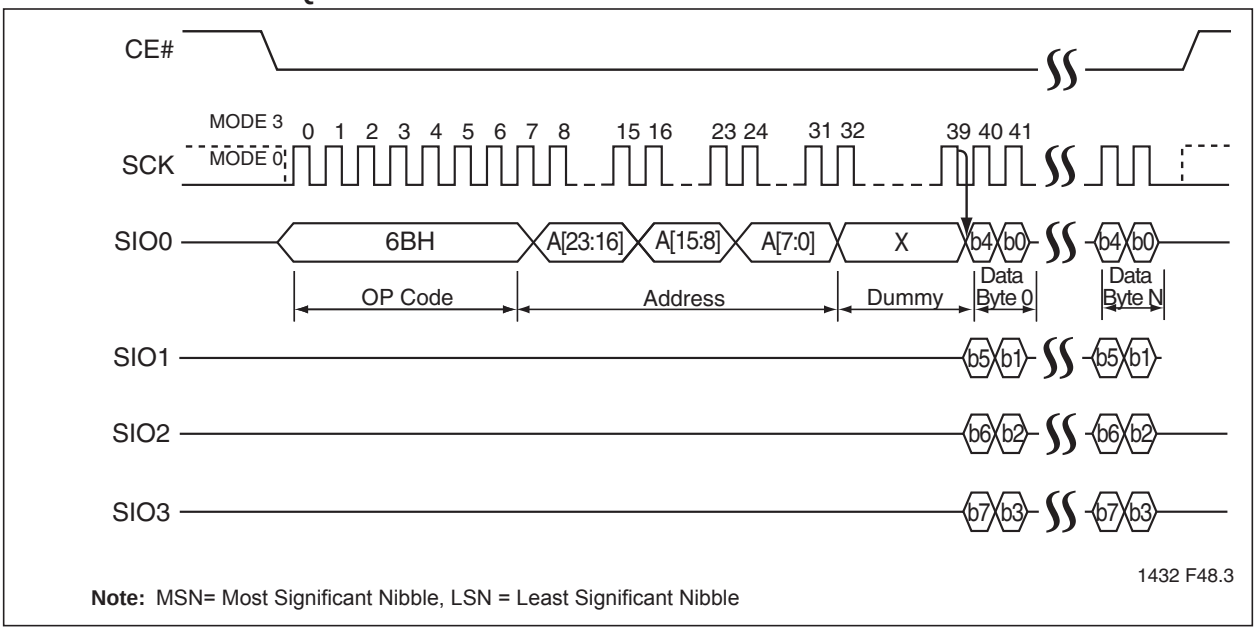
Note: MSN= Most Significant Nibble, LSN = Least Significant Nibble
Hx = High Data Nibble, Lx = Low Data Nibble C[1:0] = 0BH

5.7 SPI Quad-Output Read

The SPI Quad-Output Read instruction supports up to 104 MHz frequency. SST26WF016B requires the IOC bit in the configuration register to be set to ‘1’ prior to executing the command. Initiate SPI Quad-Output Read by executing an 8-bit command, 6BH, followed by address bits A[23-0] and a dummy byte. CE# must remain active low for the duration of the SPI Quad Mode Read. See Figure 5-8 for the SPI Quad Output Read sequence.

Following the dummy byte, the device outputs data from SIO[3:0] starting from the specified address location. The device continually streams data output through all addresses until terminated by a low-to-high transition on CE#. The internal address pointer automatically increments until the highest memory address is reached, at which point the address pointer returns to the beginning of the address space.

FIGURE 5-8: SPI QUAD OUTPUT READ



Note: MSN= Most Significant Nibble, LSN = Least Significant Nibble

5.8 SPI Quad I/O Read

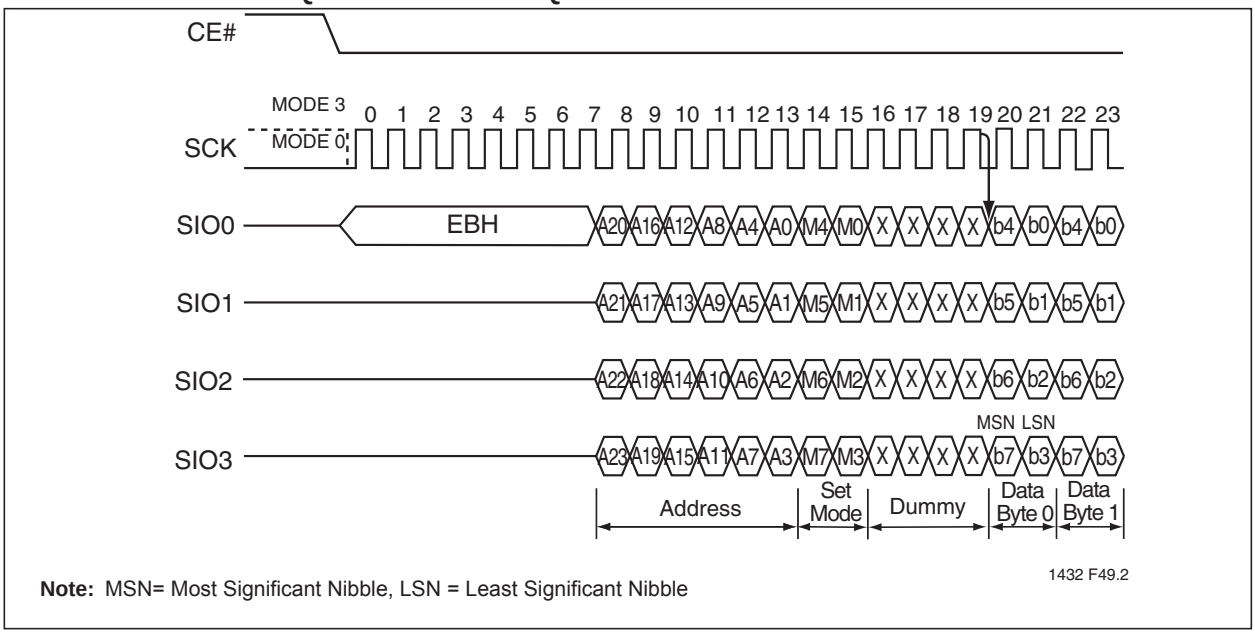
The SPI Quad I/O Read (SQIOR) instruction supports up to 104 MHz frequency. SST26WF016B requires the IOC bit in the configuration register to be set to '1' prior to executing the command. Initiate SQIOR by executing an 8-bit command, EBH. The device then switches to 4-bit I/O mode for address bits A[23-0], followed by the Set Mode configuration bits M[7:0], and two dummy bytes.CE# must remain active low for the duration of the SPI Quad I/O Read. See Figure 5-9 for the SPI Quad I/O Read sequence.

Following the dummy bytes, the device outputs data from the specified address location. The device continually streams data output through all addresses until terminated by a low-to-high transition on CE#. The internal address pointer automatically increments until the highest memory address is reached, at which point the address pointer returns to the beginning of the address space.

The Set Mode Configuration bit M[7:0] indicates if the next instruction cycle is another SPI Quad I/O Read command. When M[7:0] = AXH, the device expects the next continuous instruction to be another Read command, EBH, and does not require the op-code to be entered again. The host may set the next SQIOR cycle by driving CE# low, then sending the four-bit wide input for address A[23:0], followed by the Set Mode configuration bits M[7:0], and two dummy cycles. After the two dummy cycles, the device outputs the data starting from the specified address location. There are no restrictions on address location access.

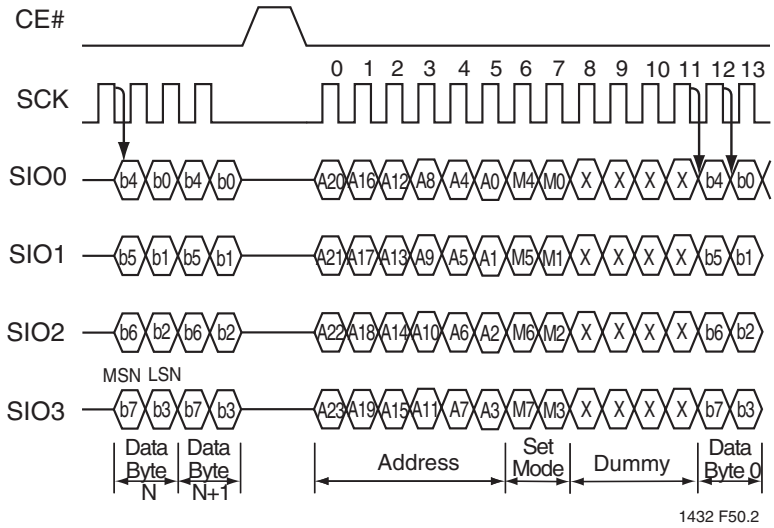
When M[7:0] is any value other than AXH, the device expects the next instruction initiated to be a command instruction. To reset/exit the Set Mode configuration, execute the Reset Quad I/O command, FFH. See Figure 5-10 for the SPI Quad I/O Mode Read sequence when M[7:0] = AXH.

FIGURE 5-9: SPI QUAD I/O READ SEQUENCE



Note: MSN= Most Significant Nibble, LSN = Least Significant Nibble

FIGURE 5-10: BACK-TO-BACK SPI QUAD I/O READ SEQUENCES WHEN M[7:0] = AXH



Note: MSN= Most Significant Nibble, LSN = Least Significant Nibble

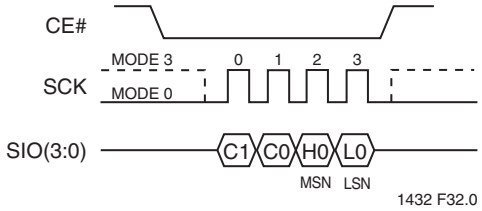
5.9 Set Burst

The Set Burst command specifies the number of bytes to be output during a Read Burst command before the device wraps around. It supports both SPI and SQI protocols. To set the burst length the host drives CE# low, sends the Set Burst command cycle (C0H) and one data cycle, then drives CE# high. After power-up or reset, the burst length is set to eight Bytes (00H). See Table 5-2 for burst length data and Figures 5-11 and 5-12 for the sequences.

TABLE 5-2: BURST LENGTH DATA

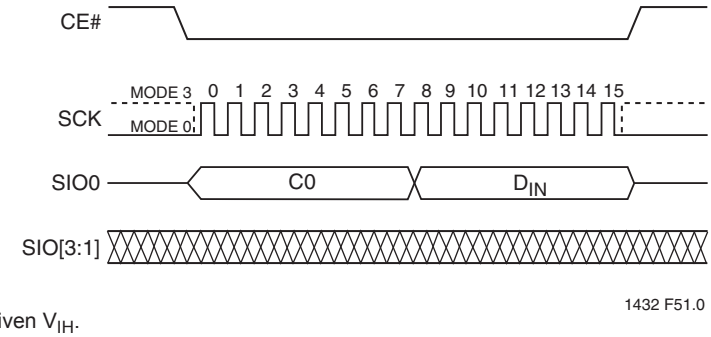
Burst Length	High Nibble (H0)	Low Nibble (L0)
8 Bytes	0h	0h
16 Bytes	0h	1h
32 Bytes	0h	2h
64 Bytes	0h	3h

FIGURE 5-11: SET BURST LENGTH SEQUENCE (SQI)



Note: MSN = Most Significant Nibble, LSN = Least Significant Nibble, C[1:0] = C0H

FIGURE 5-12: SET BURST LENGTH SEQUENCE (SPI)



Note: SIO[3:1] must be driven V_{IH}.

5.10 SQI Read Burst with Wrap (RBSQI)

SQI Read Burst with wrap is similar to High Speed Read in SQI mode, except data will output continuously within the burst length until a low-to-high transition on CE#. To execute a SQI Read Burst operation, drive CE# low then send the Read Burst command cycle (0CH), followed by three address cycles, and then three dummy cycles. Each cycle is two nibbles (clocks) long, most significant nibble first.

After the dummy cycles, the device outputs data on the falling edge of the SCK signal starting from the specified address location. The data output stream is continuous through all addresses until terminated by a low-to-high transition on CE#.

During RBSQI, the internal address pointer automatically increments until the last byte of the burst is reached, then it wraps around to the first byte of the burst. All bursts are aligned to addresses within the burst length, see Table 5-3. For example, if the burst length is eight Bytes, and the start address is 06h, the burst sequence would be: 06h, 07h, 00h, 01h, 02h, 03h, 04h, 05h, 06h, etc. The pattern repeats until the command is terminated by a low-to-high transition on CE#.

During this operation, blocks that are Read-locked will output data 00H.

5.11 SPI Read Burst with Wrap (RBSPI)

SPI Read Burst with Wrap (RBSPI) is similar to SPI Quad I/O Read except the data will output continuously within the burst length until a low-to-high transition on CE#. To execute a SPI Read Burst with Wrap operation, drive CE# low, then send the Read Burst command cycle (ECH), followed by three address cycles, and then three dummy cycles.

After the dummy cycle, the device outputs data on the falling edge of the SCK signal starting from the specified address location. The data output stream is continuous through all addresses until terminated by a low-to-high transition on CE#.

During RBSPI, the internal address pointer automatically increments until the last byte of the burst is reached, then it wraps around to the first byte of the burst. All bursts are aligned to addresses within the burst length, see Table 5-3. For example, if the burst length is eight Bytes, and the start address is 06h, the burst sequence would be: 06h, 07h, 00h, 01h, 02h, 03h, 04h, 05h, 06h, etc. The pattern repeats until the command is terminated by a low-to-high transition on CE#.

During this operation, blocks that are Read-locked will output data 00H.

TABLE 5-3: BURST ADDRESS RANGES

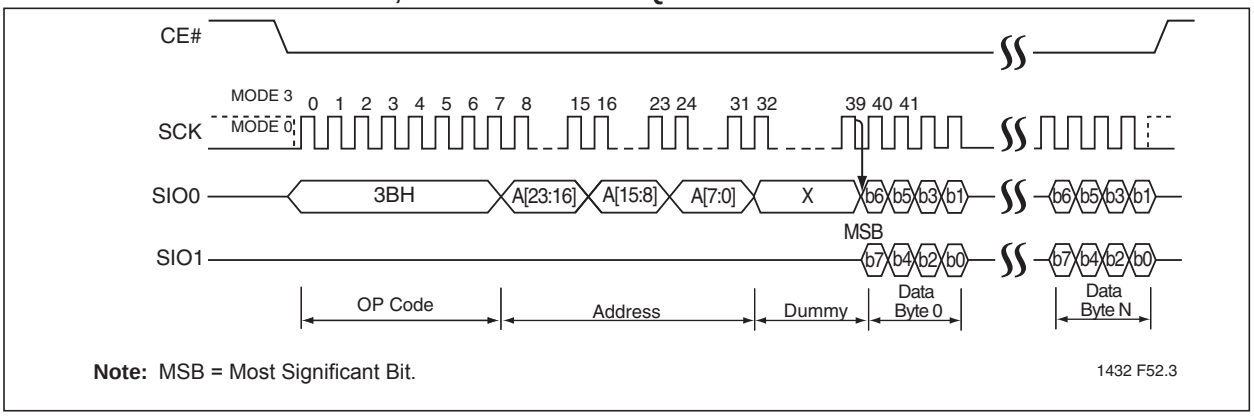
Burst Length	Burst Address Ranges
8 Bytes	00-07H, 08-0FH, 10-17H, 18-1FH...
16 Bytes	00-0FH, 10-1FH, 20-2FH, 30-3FH...
32 Bytes	00-1FH, 20-3FH, 40-5FH, 60-7FH...
64 Bytes	00-3FH, 40-7FH, 80-BFH, C0-FFH

5.12 SPI Dual-Output Read

The SPI Dual-Output Read instruction supports up to 104 MHz frequency. Initiate SPI Dual-Output Read by executing an 8-bit command, 3BH, followed by address bits A[23-0] and a dummy byte. CE# must remain active low for the duration of the SPI Dual-Output Read operation. See Figure 5-13 for the SPI Quad Output Read sequence.

Following the dummy byte, the SST26WF016B/SST26WF016BA outputs data from SIO[1:0] starting from the specified address location. The device continually streams data output through all addresses until terminated by a low-to-high transition on CE#. The internal address pointer automatically increments until the highest memory address is reached, at which point the address pointer returns to the beginning of the address space.

FIGURE 5-13: FAST READ, DUAL-OUTPUT SEQUENCE



Note: MSB = Most Significant Bit.

5.13 SPI Dual I/O Read

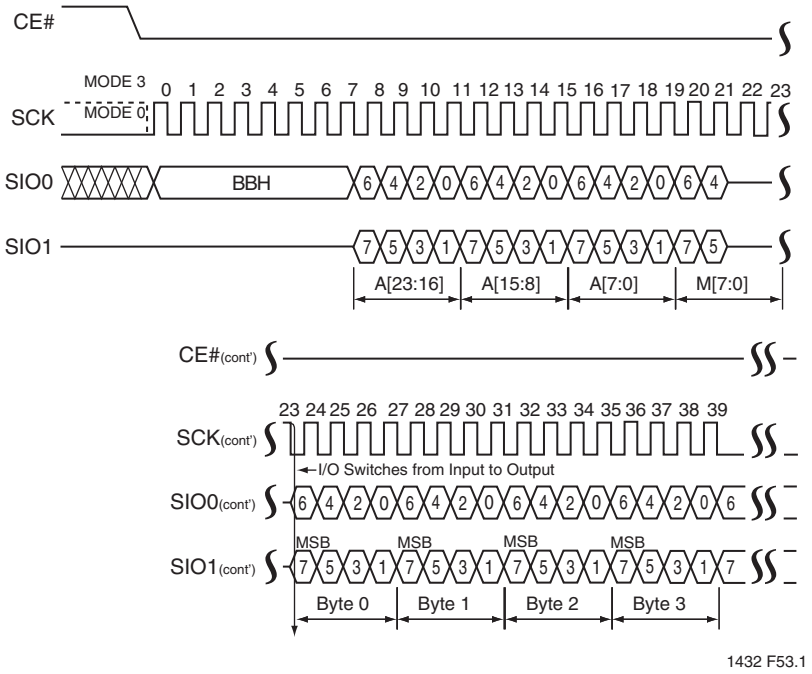
The SPI Dual I/O Read (SDIOR) instruction supports up to 80 MHz frequency. Initiate SDIOR by executing an 8-bit command, BBH. The device then switches to 2-bit I/O mode for address bits A[23-0], followed by the Set Mode configuration bits M[7:0], and two dummy bytes.CE# must remain active low for the duration of the SPI Dual I/O Read. See Figure 5-14 for the SPI Dual I/O Read sequence.

Following the dummy bytes, the SST26WF016B/SST26WF016BA outputs data from the specified address location. The device continually streams data output through all addresses until terminated by a low-to-high transition on CE#. The internal address pointer automatically increments until the highest memory address is reached, at which point the address pointer returns to the beginning of the address space.

The Set Mode Configuration bit M[7:0] indicates if the next instruction cycle is another SPI Dual I/O Read command. When M[7:0] = AXH, the device expects the next continuous instruction to be another SDIOR command, BBH, and does not require the op-code to be entered again. The host may set the next SDIOR cycle by driving CE# low, then sending the two-bit wide input for address A[23:0], followed by the Set Mode configuration bits M[7:0], and two dummy cycles. After the two dummy cycles, the device outputs the data starting from the specified address location. There are no restrictions on address location access.

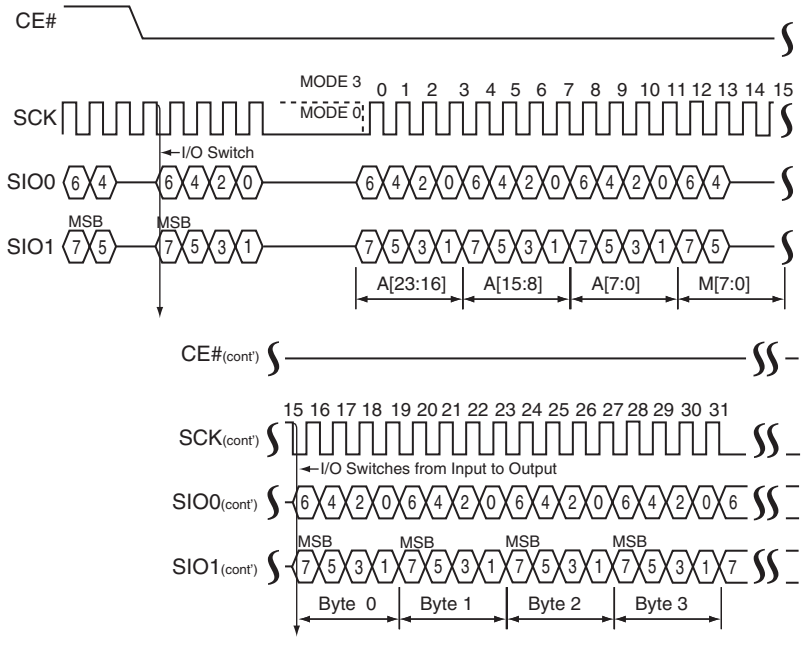
When M[7:0] is any value other than AXH, the device expects the next instruction initiated to be a command instruction. To reset/exit the Set Mode configuration, execute the Reset Quad I/O command, FFH. See Figure 5-15 for the SPI Dual I/O Read sequence when M[7:0] = AXH.

FIGURE 5-14: SPI DUAL I/O READ SEQUENCE



Note: MSN= Most Significant Nibble, LSN = Least Significant Nibble

FIGURE 5-15: BACK-TO-BACK SPI DUAL I/O READ SEQUENCES WHEN M[7:0] = AXH



Note: MSN= Most Significant Nibble, LSN = Least Significant Nibble

5.14 JEDEC-ID Read (SPI Protocol)

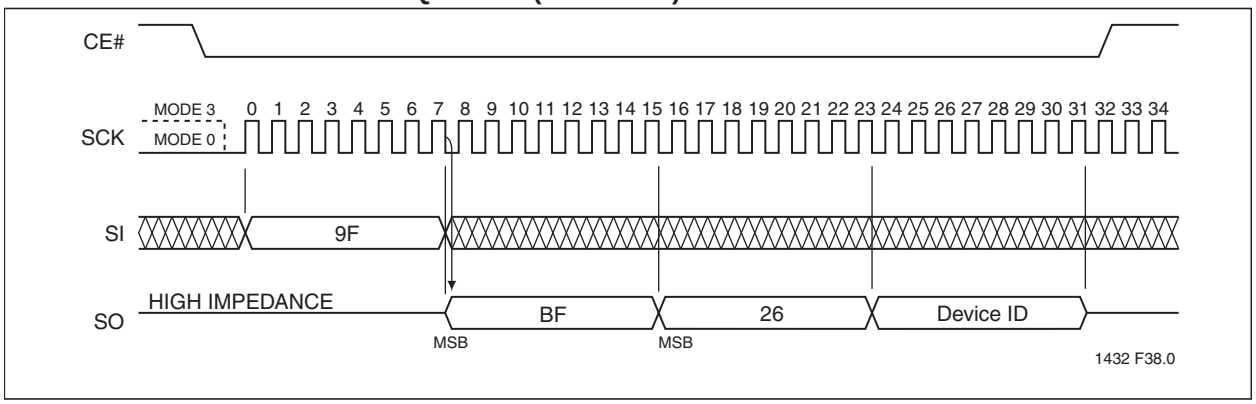
Using traditional SPI protocol, the JEDEC-ID Read instruction identifies the device as SST26WF016B/016BA and the manufacturer as SST. To execute a JECEC-ID operation the host drives CE# low then sends the JEDEC-ID command cycle (9FH).

Immediately following the command cycle, SST26WF016B/016BA outputs data on the falling edge of the SCK signal. The data output stream is continuous until terminated by a low-to-high transition on CE#. The device outputs three bytes of data: manufacturer, device type, and device ID, see Table 5-4. See Figure 5-16 for instruction sequence.

TABLE 5-4: DEVICE ID DATA OUTPUT

Product	Manufacturer ID (Byte 1)	Device ID	
		Device Type (Byte 2)	Device ID (Byte 3)
SST26WF016B/ SST26WF016BA	BFH	26H	51H

FIGURE 5-16: JEDEC-ID SEQUENCE (SPI MODE)

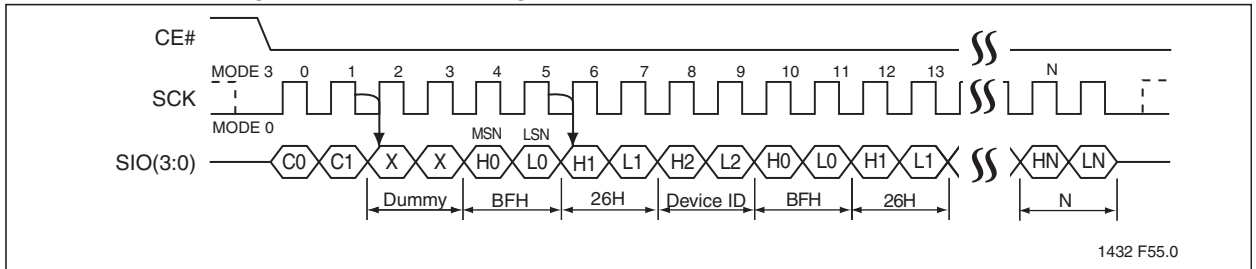


5.15 Read Quad J-ID Read (SQI Protocol)

The Read Quad J-ID Read instruction identifies the device as SST26WF016B/016BA and manufacturer as SST. To execute a Quad J-ID operation the host drives CE# low and then sends the Quad J-ID command cycle (AFH). Each cycle is two nibbles (clocks) long, most significant nibble first.

Immediately following the command cycle, and one dummy cycle, SST26WF016B/016BA outputs data on the falling edge of the SCK signal. The data output stream is continuous until terminated by a low-to-high transition of CE#. The device outputs three bytes of data: manufacturer, device type, and device ID, see Table 5-4. See Figure 5-17 for instruction sequence.

FIGURE 5-17: QUAD J-ID READ SEQUENCE



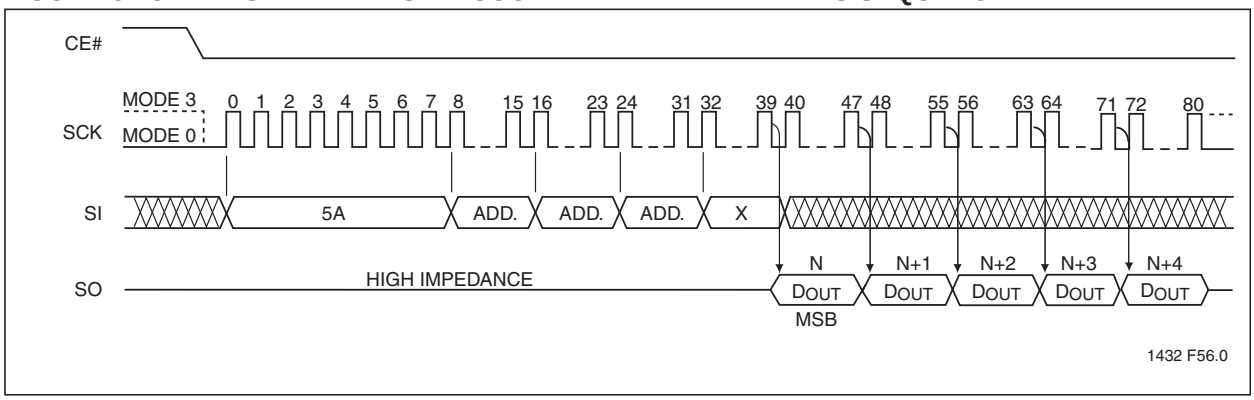
Note: MSN = Most significant Nibble; LSN= Least Significant Nibble, C[1:0]=AFH

5.16 Serial Flash Discoverable Parameters (SFDP)

The Serial Flash Discoverable Parameters (SFDP) contain information describing the characteristics of the device. This allows device-independent, JEDEC ID-independent, and forward/backward compatible software support for all future Serial Flash device families. See Table 9-1 on page 54 for address and data values.

Initiate SFDP by executing an 8-bit command, 5AH, followed by address bits A[23-0] and a dummy byte. CE# must remain active low for the duration of the SFDP cycle. For the SFDP sequence, see Figure 5-18.

FIGURE 5-18: SERIAL FLASH DISCOVERABLE PARAMETERS SEQUENCE

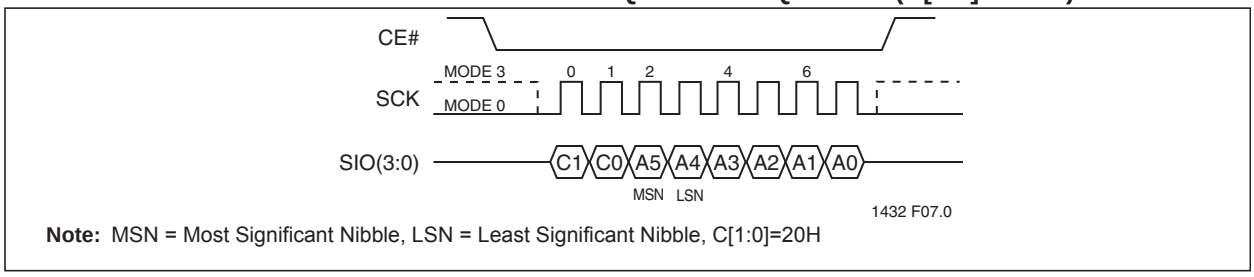


5.17 Sector-Erase

The Sector-Erase instruction clears all bits in the selected 4 KByte sector to '1,' but it does not change a protected memory area. Prior to any write operation, the Write-Enable (WREN) instruction must be executed.

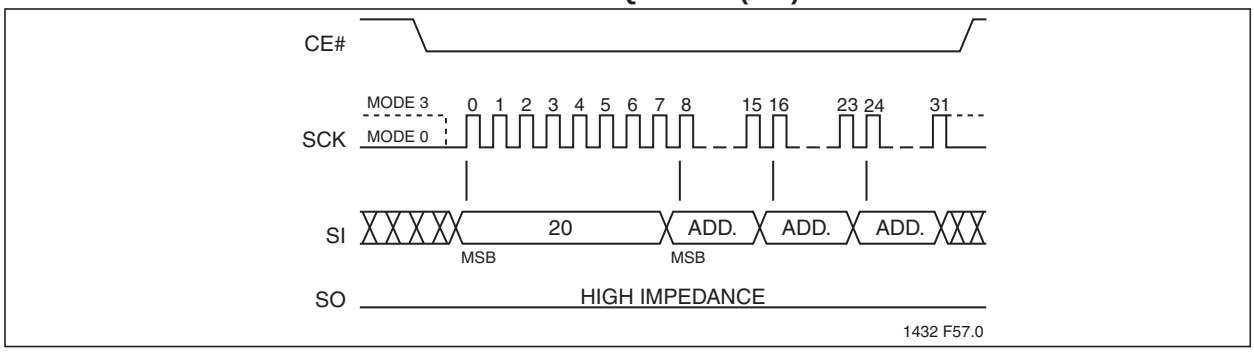
To execute a Sector-Erase operation, the host drives CE# low, then sends the Sector Erase command cycle (20H) and three address cycles, and then drives CE# high. Address bits [A_{MS}:A_{12}] (A_{MS} = Most Significant Address) determine the sector address (SA_X); the remaining address bits can be V_{IL} or V_{IH}. To identify the completion of the internal, self-timed, Write operation, poll the BUSY bit in the Status register, or wait T_{SE}. See Figures 5-19 and 5-20 for the Sector-Erase sequence.

FIGURE 5-19: 4 KBYTE SECTOR-ERASE SEQUENCE– SQI MODE (C[1:0] = 20 H)



Note: MSN = Most Significant Nibble, LSN = Least Significant Nibble, C[1:0]=20H

FIGURE 5-20: 4 KBYTE SECTOR-ERASE SEQUENCE (SPI)

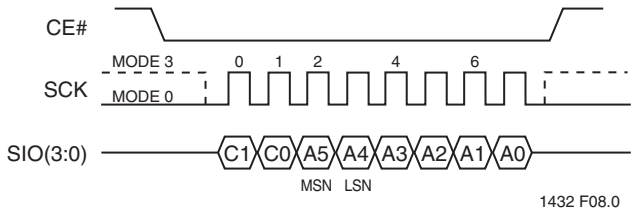


5.18 Block-Erase

The Block-Erase instruction clears all bits in the selected block to '1'. Block sizes can be 8 KByte, 32 KByte or 64 KByte depending on address, see Figure 3-1, Memory Map, for details. A Block-Erase instruction applied to a protected memory area will be ignored. Prior to any write operation, execute the WREN instruction. Keep CE# active low for the duration of any command sequence.

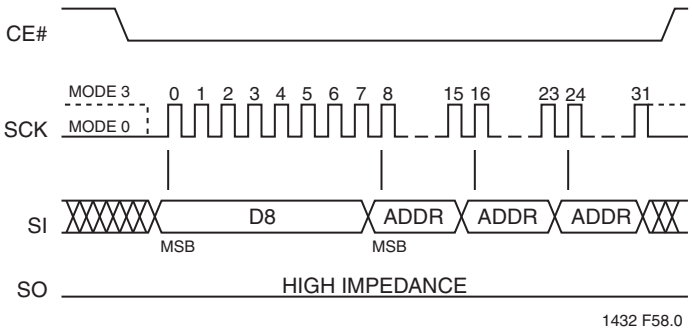
To execute a Block-Erase operation, the host drives CE# low then sends the Block-Erase command cycle (D8H), three address cycles, then drives CE# high. Address bits A_{MS}-A_{13} determine the block address (BA_X); the remaining address bits can be V_{IL} or V_{IH}. For 32 KByte blocks, A_{14}:A_{13} can be V_{IL} or V_{IH}; for 64 KByte blocks, A_{15}:A_{13} can be V_{IL} or V_{IH}. Poll the BUSY bit in the Status register, or wait T_{BE}, for the completion of the internal, self-timed, Block-Erase operation. See Figures 5-21 and 5-22 for the Block-Erase sequence.

FIGURE 5-21: BLOCK-ERASE SEQUENCE (SQI)



Note: MSN = Most Significant Nibble,
LSN = Least Significant Nibble
C[1:0] = D8H

FIGURE 5-22: BLOCK-ERASE SEQUENCE (SPI)

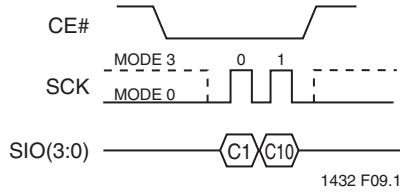


5.19 Chip-Erase

The Chip-Erase instruction clears all bits in the device to '1.' The Chip-Erase instruction is ignored if any of the memory area is protected. Prior to any write operation, execute the WREN instruction.

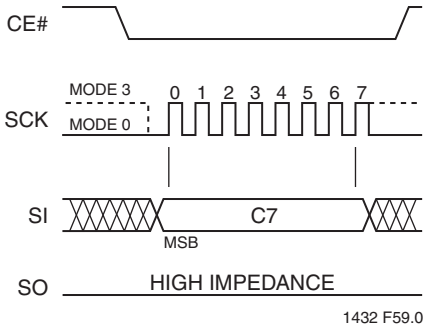
To execute a Chip-Erase operation, the host drives CE# low, sends the Chip-Erase command cycle (C7H), then drives CE# high. Poll the BUSY bit in the Status register, or wait $T_{SCE,}$ for the completion of the internal, self-timed, Write operation. See Figures 5-23 and 5-24 for the Chip Erase sequence.

FIGURE 5-23: CHIP-ERASE SEQUENCE (SQI)



Note: C[1:0] = C7H

FIGURE 5-24: CHIP-ERASE SEQUENCE (SPI)



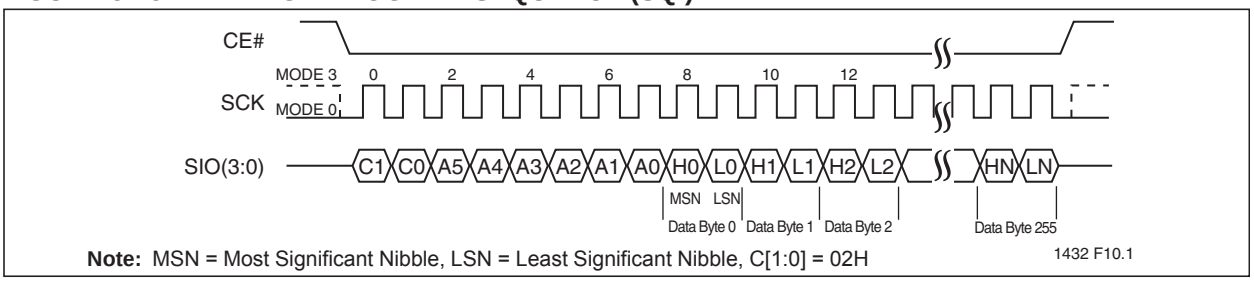
5.20 Page-Program

The Page-Program instruction programs up to 256 Bytes of data in the memory, and supports both SPI and SQI protocols. The data for the selected page address must be in the erased state (FFH) before initiating the Page-Program operation. A Page-Program applied to a protected memory area will be ignored. Prior to the program operation, execute the WREN instruction.

To execute a Page-Program operation, the host drives CE# low then sends the Page Program command cycle (02H), three address cycles followed by the data to be programmed, then drives CE# high. The programmed data must be between 1 to 256 Bytes and in whole Byte increments; sending less than a full Byte will cause the partial Byte to be ignored. Poll the BUSY bit in the Status register, or wait T_{PP}, for the completion of the internal, self-timed, Block-Erase operation. See Figures 5-25 and 5-26 for the Page-Program sequence.

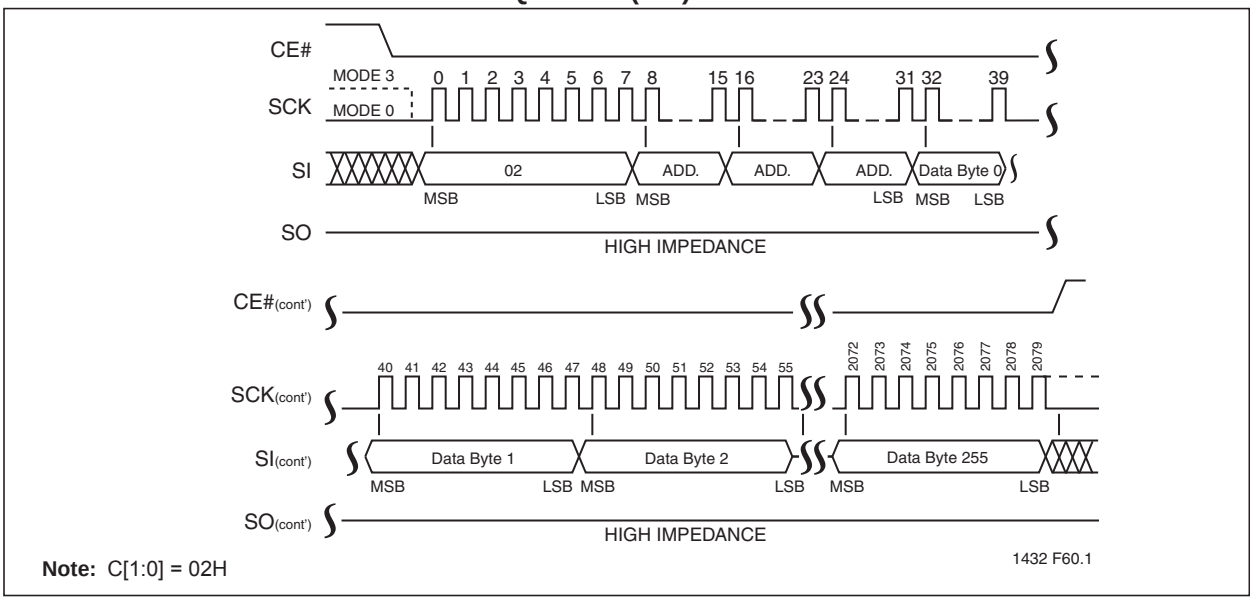
When executing Page-Program, the memory range for the SST26WF016B/016BA is divided into 256 Byte page boundaries. The device handles shifting of more than 256 Bytes of data by maintaining the last 256 Bytes of data as the correct data to be programmed. If the target address for the Page-Program instruction is not the beginning of the page boundary (A[7:0] are not all zero), and the number of bytes of data input exceeds or overlaps the end of the address of the page boundary, the excess data inputs wrap around and will be programmed at the start of that target page.

FIGURE 5-25: PAGE-PROGRAM SEQUENCE (SQI)



Note: MSN = Most Significant Nibble, LSN = Least Significant Nibble, C[1:0] = 02H

FIGURE 5-26: PAGE-PROGRAM SEQUENCE (SPI)



Note: C[1:0] = 02H

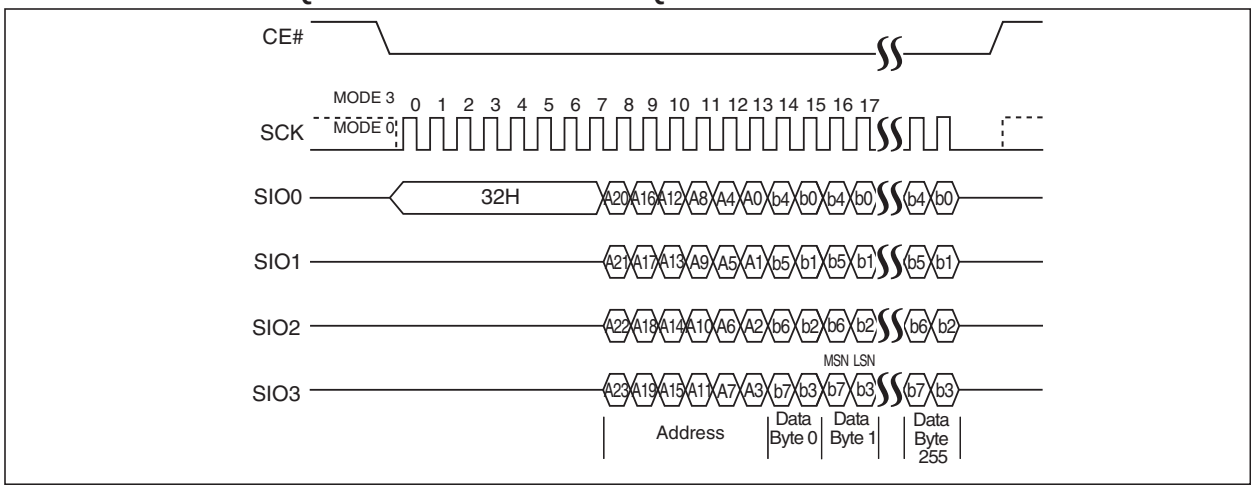
5.21 SPI Quad Page-Program

The SPI Quad Page-Program instruction programs up to 256 Bytes of data in the memory. The data for the selected page address must be in the erased state (FFH) before initiating the SPI Quad Page-Program operation. A SPI Quad Page-Program applied to a protected memory area will be ignored. SST26WF016B requires the ICO bit in the configuration register to be set to '1' prior to executing the command.Prior to the program operation, execute the WREN instruction.

To execute a SPI Quad Page-Program operation, the host drives CE# low then sends the SPI Quad Page-Program command cycle (32H), three address cycles followed by the data to be programmed, then drives CE# high. The programmed data must be between 1 to 256 Bytes and in whole Byte increments. The command cycle is eight clocks long, the address and data cycles are each two clocks long, most significant bit first. Poll the BUSY bit in the Status register, or wait $T_{PP,}$ for the completion of the internal, self-timed, Write operation.See Figure 5-27.

When executing SPI Quad Page-Program, the memory range for the SST26WF016B/016BA is divided into 256 Byte page boundaries. The device handles shifting of more than 256 Bytes of data by maintaining the last 256 Bytes of data as the correct data to be programmed. If the target address for the SPI Quad Page-Program instruction is not the beginning of the page boundary (A[7:0] are not all zero), and the of bytes of data input exceeds or overlaps the end of the address of the page boundary, the excess data inputs wrap around and will be programmed at the start of that target page.

FIGURE 5-27: SPI QUAD PAGE-PROGRAM SEQUENCE



5.22 Write-Suspend and Write-Resume

Write-Suspend allows the interruption of Sector-Erase, Block-Erase, SPI Quad Page-Program, or Page-Program operations in order to erase, program, or read data in another portion of memory. The original operation can be continued with the Write-Resume command. This operation is supported in both SQI and SPI protocols.

Only one write operation can be suspended at a time; if an operation is already suspended, the device will ignore the Write-Suspend command. Write-Suspend during Chip-Erase is ignored; Chip-Erase is not a valid command while a write is suspended. The Write-Resume command is ignored until any write operation (Program or Erase) initiated during the Write-Suspend is complete. The device requires a minimum of 500 µs between each Write-Suspend command.

5.23 Write-Suspend During Sector-Erase or Block-Erase

Issuing a Write-Suspend instruction during Sector-Erase or Block-Erase allows the host to program or read any sector that was not being erased. The device will ignore any programming commands pointing to the suspended sector(s). Any attempt to read from the suspended sector(s) will output unknown data because the Sector- or Block-Erase will be incomplete.

To execute a Write-Suspend operation, the host drives CE# low, sends the Write Suspend command cycle (B0H), then drives CE# high. The Status register indicates that the erase has been suspended by changing the WSE bit from '0' to '1,' but the device will not accept another command until it is ready. To determine when the device will accept a new command, poll the BUSY bit in the Status register or wait T_{WS}.

5.24 Write Suspend During Page Programming or SPI Quad Page Programming

Issuing a Write-Suspend instruction during Page Programming allows the host to erase or read any sector that is not being programmed. Erase commands pointing to the suspended sector(s) will be ignored. Any attempt to read from the suspended page will output unknown data because the program will be incomplete.

To execute a Write Suspend operation, the host drives CE# low, sends the Write Suspend command cycle (B0H), then drives CE# high. The Status register indicates that the programming has been suspended by changing the WSP bit from '0' to '1,' but the device will not accept another command until it is ready. To determine when the device will accept a new command, poll the BUSY bit in the Status register or wait T_{WS}.

5.25 Write-Resume

Write-Resume restarts a Write command that was suspended, and changes the suspend status bit in the Status register (WSE or WSP) back to '0'.

To execute a Write-Resume operation, the host drives CE# low, sends the Write Resume command cycle (30H), then drives CE# high. To determine if the internal, self-timed Write operation completed, poll the BUSY bit in the Status register, or wait the specified time T_{SE}, T_{BE} or T_{PP} for Sector-Erase, Block-Erase, or Page-Programming, respectively. The total write time before suspend and after resume will not exceed the uninterrupted write times T_{SE}, T_{BE} or T_{PP}.

5.26 Read Security ID

The Read Security ID operation is supported in both SPI and SQI modes. To execute a Read Security ID (SID) operation in SPI mode, the host drives CE# low, sends the Read Security ID command cycle (88H), two address cycles, and then one dummy cycle. To execute a Read Security ID operation in SQI mode, the host drives CE# low and then sends the Read Security ID command, two address cycles, and three dummy cycles.

After the dummy cycles, the device outputs data on the falling edge of the SCK signal, starting from the specified address location. The data output stream is continuous through all SID addresses until terminated by a low-to-high transition on CE#. See Table 5-5 for the Security ID address range.

5.27 Program Security ID

The Program Security ID instruction programs one to 2040 Bytes of data in the user-programmable, Security ID space. This Security ID space is one-time programmable (OTP). The device ignores a Program Security ID instruction pointing to an invalid or protected address, see Table 5-5. Prior to the program operation, execute WREN.

To execute a Program SID operation, the host drives CE# low, sends the Program Security ID command cycle (A5H), two address cycles, the data to be programmed, then drives CE# high. The programmed data must be between 1 to 256 Bytes and in whole Byte increments.

The device handles shifting of more than 256 Bytes of data by maintaining the last 256 Bytes of data as the correct data to be programmed. If the target address for the Program Security ID instruction is not the beginning of the page boundary, and the number of data input exceeds or overlaps the end of the address of the page boundary, the excess data inputs wrap around and will be programmed at the start of that target page.

The Program Security ID operation is supported in both SPI and SQI mode. To determine the completion of the internal, self-timed Program SID operation, poll the BUSY bit in the software status register, or wait T_{PSID} for the completion of the internal self-timed Program Security ID operation.

TABLE 5-5: PROGRAM SECURITY ID

Program Security ID	Address Range
Unique ID Pre-Programmed at factory	0000 – 0007H
User Programmable	0008H – 07FFH

5.28 Lockout Security ID

The Lockout Security ID instruction prevents any future changes to the Security ID, and is supported in both SPI and SQI modes. Prior to the operation, execute WREN.

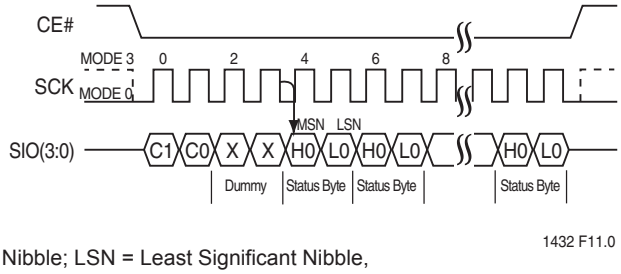
To execute a Lockout SID, the host drives CE# low, sends the Lockout Security ID command cycle (85H), then drives CE# high. Poll the BUSY bit in the software status register, or wait T_{PSID}, for the completion of the Lockout Security ID operation.

5.29 Read-Status Register (RDSR) and Read-Configuration Register (RDCR)

The Read-Status Register (RDSR) and Read Configuration Register (RDCR) commands output the contents of the Status and Configuration registers. These commands function in both SPI and SQI modes. The Status register may be read at any time, even during a Write operation. When a Write is in progress, poll the BUSY bit before sending any new commands to assure that the new commands are properly received by the device.

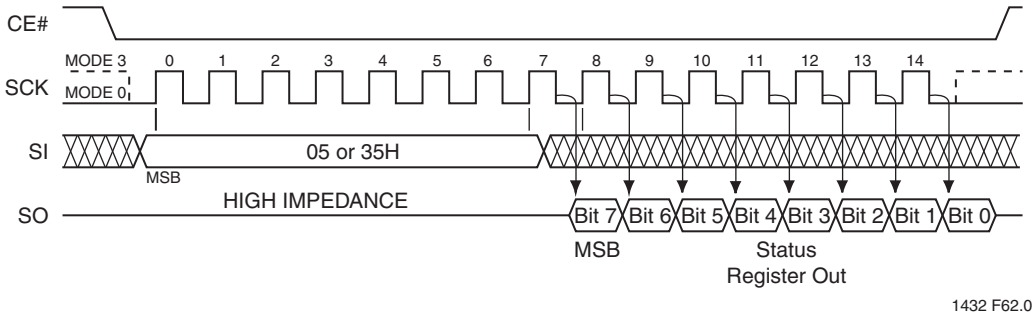
To Read the Status or Configuration registers, the host drives CE# low, then sends the Read-Status-Register command cycle (05H) or the Read Configuration Register command (35H). A dummy cycle is required in SQI mode. Immediately after the command cycle, the device outputs data on the falling edge of the SCK signal. The data output stream continues until terminated by a low-to-high transition on CE#. See Figures 5-28 and 5-29 for the RDSR instruction sequence.

FIGURE 5-28: READ-STATUS-REGISTER AND READ CONFIGURATION REGISTER SEQUENCE (SQI)



Note: MSN = Most Significant Nibble; LSN = Least Significant Nibble, C[1‘:0]=05H or 35H

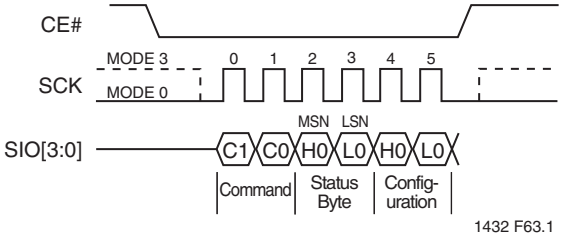
FIGURE 5-29: READ-STATUS-REGISTER AND READ CONFIGURATION REGISTER SEQUENCE (SPI)



5.30 Write-Status Register (WRSR)

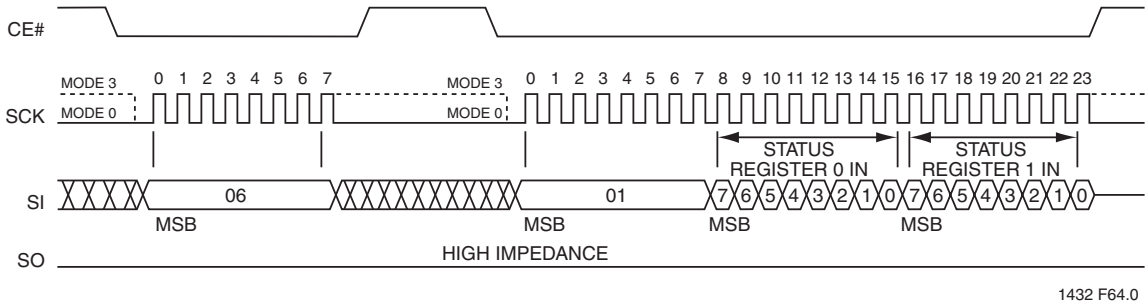
The Write-Status Register (WRSR) command writes new values to the Status register. To execute a Write-Status Register operation, the host drives CE# low, then sends the Write-Status Register command cycle (01H), two cycles of data, and then drives CE# high. The first cycle of data points to the Status register, the second points to the Configuration register. See Figures 5-30 and 5-31.

FIGURE 5-30: WRITE-STATUS-REGISTER AND WRITE CONFIGURATION REGISTER SEQUENCE (SQI)



Note: MSN = Most Significant Nibble; LSN = Least Significant Nibble, XX = Don't Care, C[1:0]=01H

FIGURE 5-31: WRITE-STATUS-REGISTER AND WRITE CONFIGURATION REGISTER SEQUENCE (SPI)



Note: XX = Don't Care

5.31 Write-Enable (WREN)

The Write Enable (WREN) instruction sets the Write-Enable-Latch bit in the Status register to '1,' allowing Write operations to occur. The WREN instruction must be executed prior to any of the following operations: Sector Erase, Block Erase, Chip Erase, Page Program, Program Security ID, Lockout Security ID, Write Block-Protection Register, Lock-Down Block-Protection Register, and Non-Volatile Write-Lock Lock-Down Register, SPI Quad Page Program, and Write Status Register. To execute a Write Enable the host drives CE# low then sends the Write Enable command cycle (06H) then drives CE# high. See Figures 5-32 and 5-33 for the WREN instruction sequence. See Figures 5-32 and 5-33 for the WREN instruction sequence.

FIGURE 5-32: WRITE-ENABLE SEQUENCE (SQI)

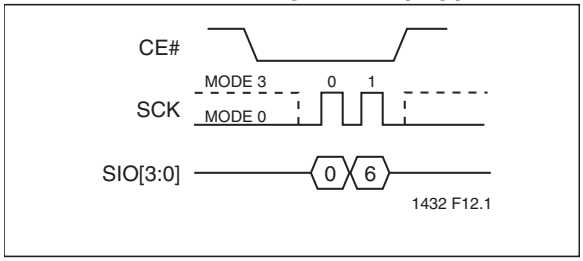
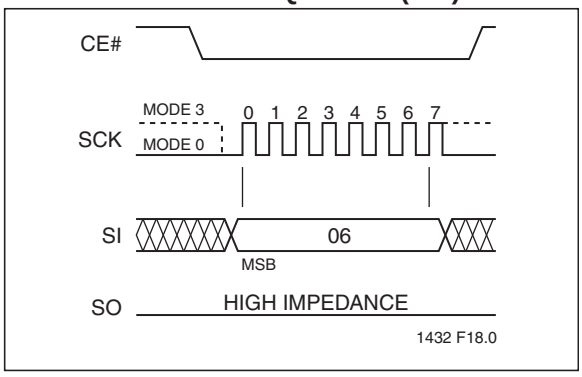


FIGURE 5-33: WRITE-ENABLE SEQUENCE (SPI)



5.32 Write-Disable (WRDI)

The Write-Disable (WRDI) instruction sets the Write-Enable-Latch bit in the Status register to '0,' preventing Write operations. The WRDI instruction is ignored during any internal write operations. Any Write operation started before executing WRDI will complete. Drive CE# high before executing WRDI.

To execute a Write-Disable, the host drives CE# low, sends the Write Disable command cycle (04H), then drives CE# high. See Figures 5-34 and 5-35.

FIGURE 5-34: WRITE-DISABLE (WRDI) SEQUENCE (SQI)

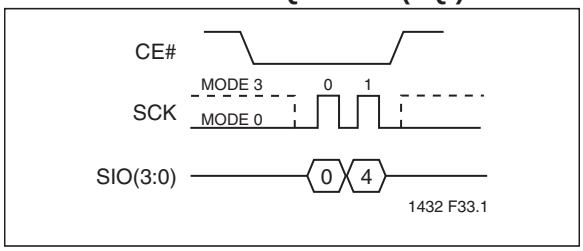
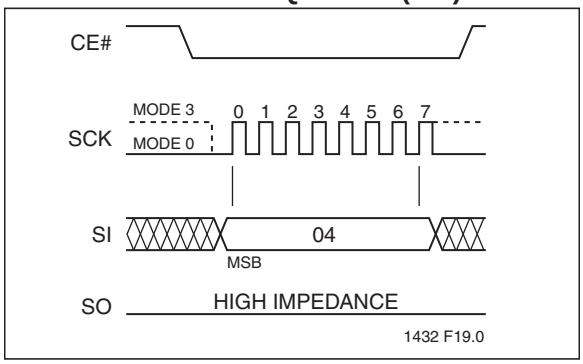


FIGURE 5-35: WRITE-DISABLE (WRDI) SEQUENCE (SPI)

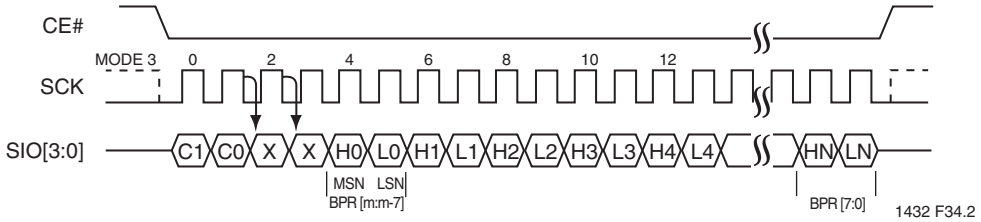


5.33 Read Block-Protection Register (RBPR)

The Read Block-Protection Register instruction outputs the Block-Protection register data which determines the protection status. To execute a Read Block-Protection Register operation, the host drives CE# low, and then sends the Read Block-Protection Register command cycle (72H). A dummy cycle is required in SQI mode.

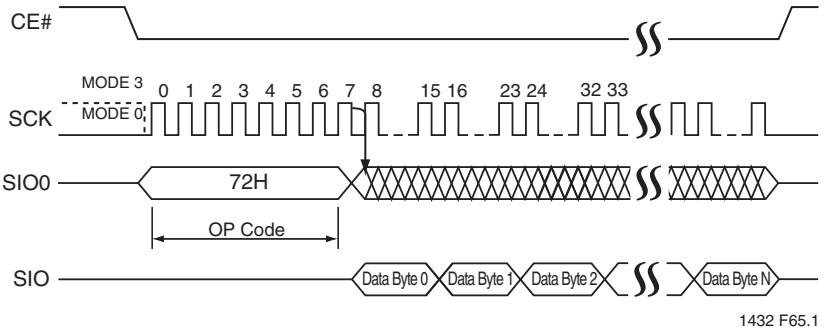
After the command cycle, the device outputs data on the falling edge of the SCK signal starting with the most significant nibble, see Table 5-6 for definitions of each bit in the Block-Protection register. The RBPR command does not wrap around. After all data has been output, the device will output 0H until terminated by a low-to-high transition on CE#. Figures 5-36 and 5-37.

FIGURE 5-36: READ BLOCK-PROTECTION REGISTER SEQUENCE (SQI)



Note: MSN = Most Significant Nibble, LSN = Least Significant Nibble
Block-Protection Register (BPR) m = 47 for SST26WF016B/016BA
C[1:0]=72H

FIGURE 5-37: READ BLOCK-PROTECTION REGISTER SEQUENCE (SPI)

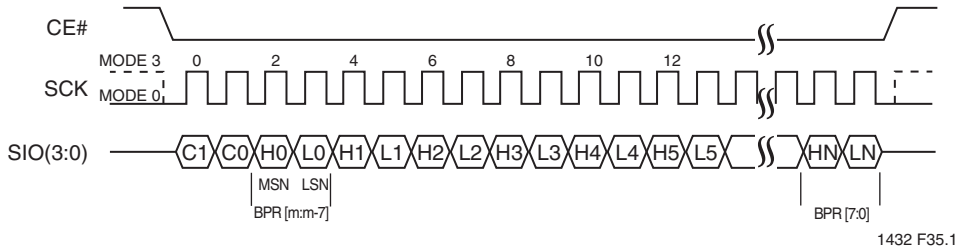


5.34 Write Block-Protection Register (WBPR)

The Write Block-Protection Register (WBPR) command changes the Block-Protection register data to indicate the protection status. Execute WREN before executing WBPR.

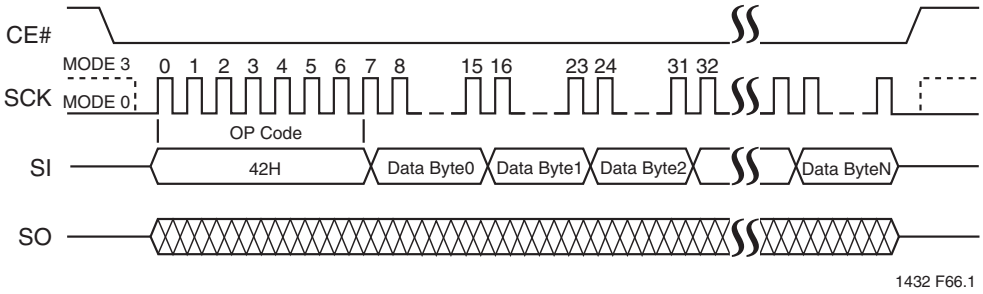
To execute a Write Block-Protection Register operation the host drives CE# low, sends the Write Block-Protection Register command cycle (42H), sends six cycles of data, and finally drives CE# high. Data input must be most significant nibble first. See Table 5-6 for definitions of each bit in the Block-Protection register. See Figures 5-38 and 5-39.

FIGURE 5-38: WRITE BLOCK-PROTECTION REGISTER SEQUENCE (SQI)



Note: MSN = Most Significant Nibble, LSN = Least Significant Nibble
Block-Protection Register (BPR) m = 47 for SST26WF016B/016BA
C[1:0]=42H

FIGURE 5-39: WRITE BLOCK-PROTECTION REGISTER SEQUENCE (SPI)



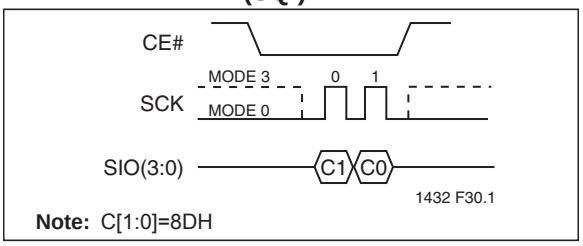
Note: C[1:0]=42H

5.35 Lock-Down Block-Protection Register (LBPR)

The Lock-Down Block-Protection Register instruction prevents changes to the Block-Protection register during device operation. Lock-Down resets after power cycling; this allows the Block-Protection register to be changed. Execute WREN before initiating the Lock-Down Block-Protection Register instruction.

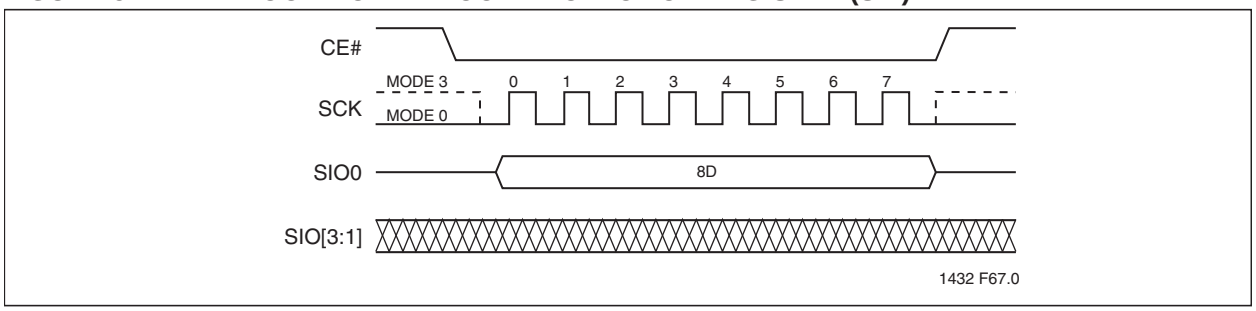
To execute a Lock-Down Block-Protection Register, the host drives CE# low, then sends the Lock-Down Block-Protection Register command cycle (8DH), then drives CE# high.

FIGURE 5-40: LOCK-DOWN BLOCK-PROTECTION REGISTER (SQI)



Note: C[1:0]=8DH

FIGURE 5-41: LOCK-DOWN BLOCK-PROTECTION REGISTER (SPI)



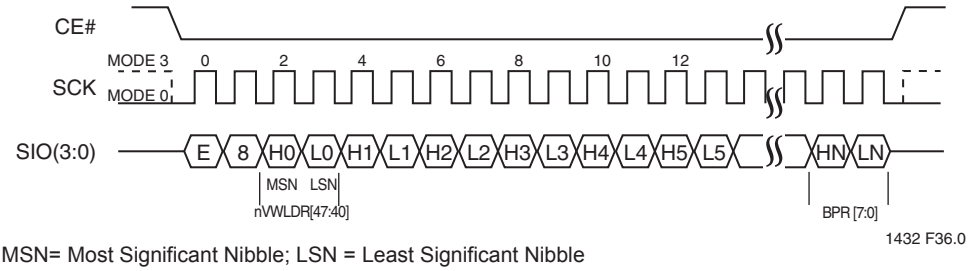
5.36 Non-Volatile Write-Lock Lock-Down Register (nVWLDR)

The Non-Volatile Write-Lock Lock-Down Register (nVWLDR) instruction controls the ability to change the Write-Lock bits in the Block-Protection register. Execute WREN before initiating the nVWLDR instruction.

To execute nVWLDR, the host drives CE# low, then sends the nVWLDR command cycle (E8H), followed by six cycles of data, and then drives CE# high.

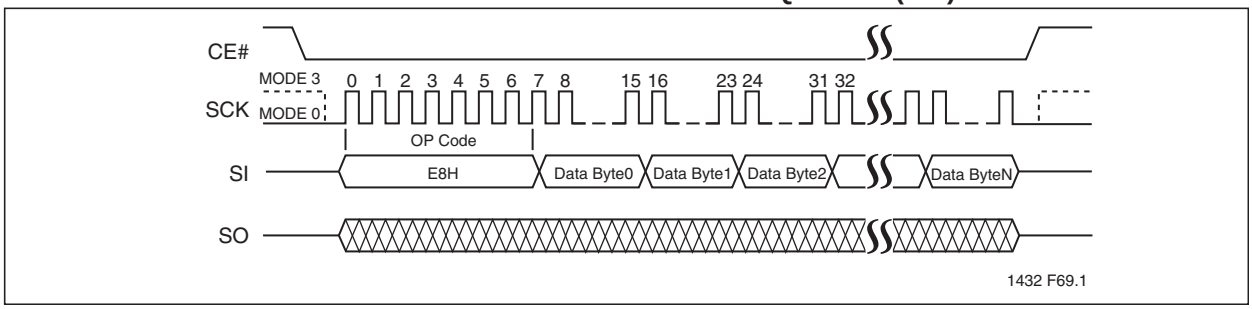
After CE# goes high, the non-volatile bits are programmed and the programming time-out must complete before any additional commands, other than Read Status Register, can be entered. Poll the BUSY bit in the Status register, or wait T_{PP}, for the completion of the internal, self-timed, Write operation. Data inputs must be most significant bit(s) first.

FIGURE 5-42: WRITE-LOCK LOCK-DOWN REGISTER SEQUENCE (SQI)



Note: MSN= Most Significant Nibble; LSN = Least Significant Nibble
Write-Lock Lock-Down Register (nVWLDR)

FIGURE 5-43: WRITE-LOCK LOCK-DOWN REGISTER SEQUENCE (SPI)

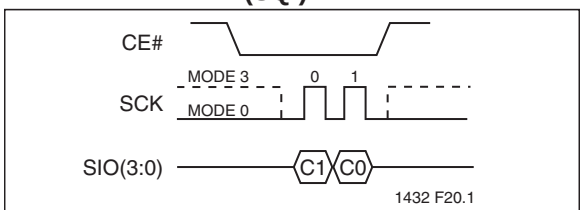


5.37 Global Block-Protection Unlock (ULBPR)

The Global Block-Protection Unlock (ULBPR) instruction clears all write-protection bits in the Block-Protection register, except for those bits that have been locked down with the nVWLDR command. Execute WREN before initiating the ULBPR instruction.

To execute a ULBPR instruction, the host drives CE# low, then sends the ULBPR command cycle (98H), and then drives CE# high.

FIGURE 5-44: GLOBAL BLOCK-PROTECTION UNLOCK (SQI)



Note: C[1:0]=98H

FIGURE 5-45: GLOBAL BLOCK-PROTECTION UNLOCK (SPI)

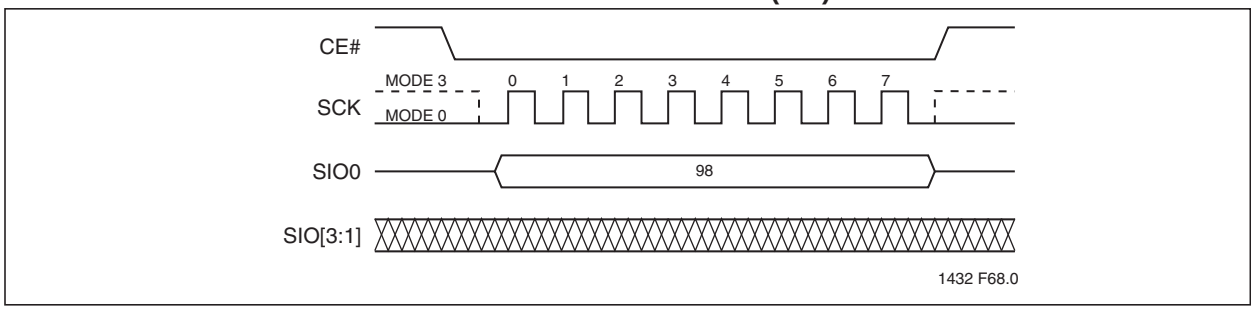


TABLE 5-6: BLOCK-PROTECTION REGISTER FOR SST26WF016B/SST26WF016BA (1 OF 2)[1]

BPR Bits		Address Range	Protected Block Size
Read Lock	Write Lock/nVWLDR[2]		
47	46	1FE000H - 1FFFFFH	8 KByte
45	44	1FC000H - 1FDFFFH	8 KByte
43	42	1FA000H - 1FBFFFH	8 KByte
41	40	1F8000H - 1F9FFFH	8 KByte
39	38	006000H - 007FFFH	8 KByte
37	36	004000H - 005FFFH	8 KByte
35	34	002000H - 003FFFH	8 KByte
33	32	000000H - 001FFFH	8 KByte
	31	1F0000H - 1F7FFFH	32 KByte
	30	008000H - 00FFFFH	32 KByte
	29	1E0000H - 1EFFFFH	64 KByte
	28	1D0000H -1DFFFFH	64 KByte
	27	1C0000H -1CFFFFH	64 KByte

TABLE 5-6: BLOCK-PROTECTION REGISTER FOR SST26WF016B/SST26WF016BA (2 OF 2)[1]

BPR Bits		Address Range	Protected Block Size
Read Lock	Write Lock/nVWLDR[2]		
	26	1B0000H - 1BFFFFH	64 KByte
	25	1A0000H - 1AFFFFH	64 KByte
	24	190000H - 19FFFFH	64 KByte
	23	180000H - 18FFFFH	64 KByte
	22	170000H - 17FFFFH	64 KByte
	21	160000H - 16FFFFH	64 KByte
	20	150000H - 15FFFFH	64 KByte
	19	140000H - 14FFFFH	64 KByte
	18	130000H - 13FFFFH	64 KByte
	17	120000H - 12FFFFH	64 KByte
	16	110000H - 11FFFFH	64 KByte
	15	100000H - 10FFFFH	64 KByte
	14	0F0000H - 0FFFFFH	64 KByte
	13	0E0000H - 0EFFFFH	64 KByte
	12	0D0000H - 0DFFFFH	64 KByte
	11	0C0000H - 0CFFFFH	64 KByte
	10	0B0000H - 0BFFFFH	64 KByte
	9	0A0000H - 0AFFFFH	64 KByte
	8	090000H - 09FFFFH	64 KByte
	7	080000H - 08FFFFH	64 KByte
	6	070000H - 07FFFFH	64 KByte
	5	060000H - 06FFFFH	64 KByte
	4	050000H - 05FFFFH	64 KByte
	3	040000H - 04FFFFH	64 KByte
	2	030000H - 03FFFFH	64 KByte
	1	020000H - 02FFFFH	64 KByte
	0	010000H - 01FFFFH	64 KByte

0

1. The default state after a power-on reset is write-protected BPR[47:0] = 5555 FFFF FFFF
2. nVWLDR bits are one-time-programmable. Once a WLLDR bit is set, the protection state of that particular block is permanently write-locked.

5.38 Deep Power-Down

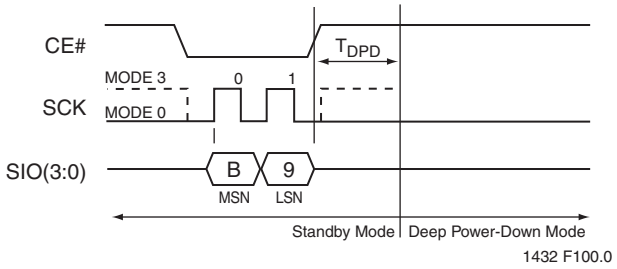
The Deep Power-down (DPD) instruction puts the device in the lowest power consumption mode–the Deep Power-down mode. The Deep Power-down instruction is ignored during an internal write operation. While the device is in Deep Power-down mode, all instructions will be ignored except for the Release Deep Power-down instruction.

Enter Deep Power-down mode by initiating the Deep Power-down (DPD) instruction (B9H) while driving CE# low. CE# must be driven high before executing the DPD instruction. After CE# is driven high, it requires a delay of T_{DPD} before the standby current I_{SB} is reduced to deep power-down current I_{DPD}. See Table 5-7 for Deep Power-down timing. If the device is busy performing an internal erase or program operation, initiating a Deep Power-down instruction will not placed the device in Deep Power-down mode. See Figures 5-46 and 5-47 for the DPD instruction sequence.

TABLE 5-7: DEEP POWER-DOWN

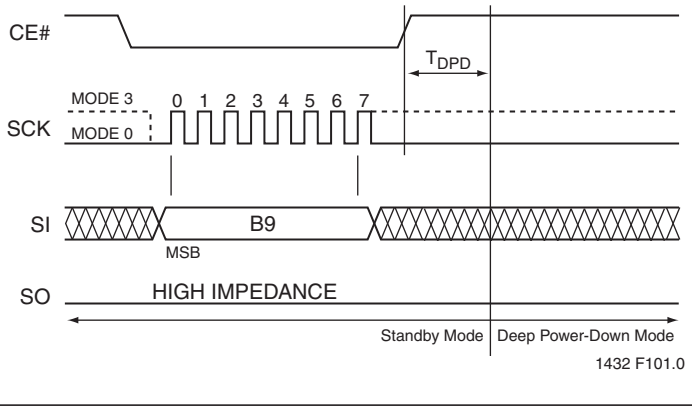
Symbol	Parameter	Min	Max	Units
TDPD	CE# High to Deep Power-down		3	µs
TSBR	CE# High to Standby Mode		10	µs

FIGURE 5-46: DEEP POWER-DOWN (DPD) SEQUENCE (SQI)



Note: MSN= Most Significant Nibble; LSN = Least Significant Nibble

FIGURE 5-47: DEEP POWER-DOWN (DPD) (SPI)

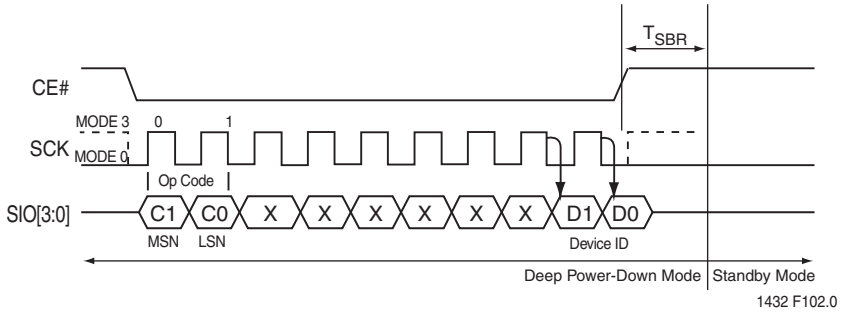


5.39 Release from Deep Power-Down and Read ID

Release from Deep Power-Down (RDPD) and Read ID instruction exits Deep Power-down mode. To exit Deep Power down mode, execute the RDPD. During this command, the host drives CE# low, then sends the Deep Power-Down command cycle (ABH), and then drives CE# high. The device will return to Standby mode and be ready for the next instruction after T_{SBR}.

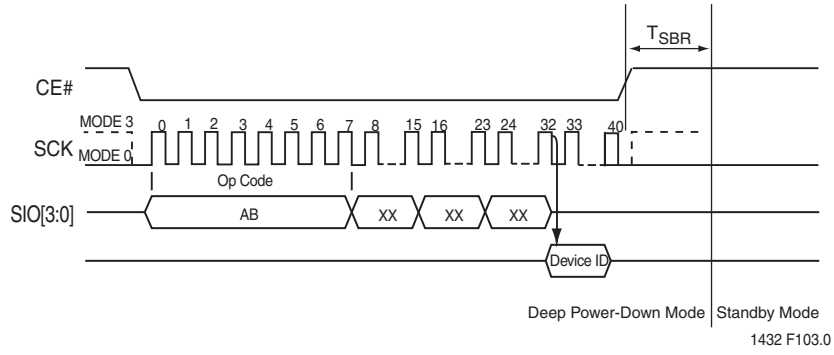
To execute RDPD and read the Device ID, the host drives CE# low then sends the Deep Power-Down command cycle (ABH), three dummy clock cycles, and then drives CE# high. The device outputs the Device ID on the falling edge of the SCK signal following the dummy cycles. The data output stream is continuous until terminated by a low-to-high transition on CE, and will return to Standby mode and be ready for the next instruction after T_{SBR}. See Figures 5-48 and 5-49 for the command sequence.

FIGURE 5-48: RELEASE FROM DEEP POWER-DOWN (RDPD) AND READ ID SEQUENCE (SQI)



Note: C[1:0]=ABH

FIGURE 5-49: RELEASE FROM DEEP POWER-DOWN (RDPD) AND READ ID SEQUENCE (SPI)



6.0 ELECTRICAL SPECIFICATIONS

Applied conditions greater than those listed under “Absolute Maximum Stress Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias. . . . . -55°C to +125°C
Storage Temperature . . . . . -65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential. . . . . -0.5V to V_{DD}+0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential . . . . . -2.0V to V_{DD}+2.0V
Package Power Dissipation Capability (T_A = 25°C) 1.0W
Surface Mount Solder Reflow Temperature . . . . . 260°C for 10 seconds
Output Short Circuit Current[1] . . . . . 50 mA

1. Output shorted for no more than one second. No more than one output shorted at a time.

TABLE 6-1: OPERATING RANGE

Range	Ambient Temp	V_{DD}
Industrial	-40°C to +85°C	1.65-1.95V

TABLE 6-2: AC CONDITIONS OF TEST[1]

Input Rise/Fall Time	Output Load
3ns	C_L = 30 pF

1. See Figure 6-7

6.1 Power-Up Specifications

All functionalities and DC specifications are specified for a V_{DD} ramp rate of greater than 1V per 100 ms (0V to 3.0V in less than 300 ms).

When V_{DD} drops from the operating voltage to below the minimum V_{DD} threshold at power-down, all operations are disabled and the device does not respond to commands. Data corruption may result if a power-down occurs while a Write-Registers, program, or erase operation is in progress. See Figure 6-2.

TABLE 6-3: RECOMMENDED SYSTEM POWER-UP/DOWN TIMINGS

Symbol	Parameter	Minimum	Max	Units	Condition
$T_{PU-READ}$[1]	V_{DD} Min to Read Operation	100		µs	
$T_{PU-WRITE}$[1]	V_{DD} Min to Write Operation	100		µs	
T_{PD}[1]	Power-down Duration	100		ms	
V_{OFF}	V_{DD} off time		0.3	V	0V recommended

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

FIGURE 6-1: POWER-UP TIMING DIAGRAM

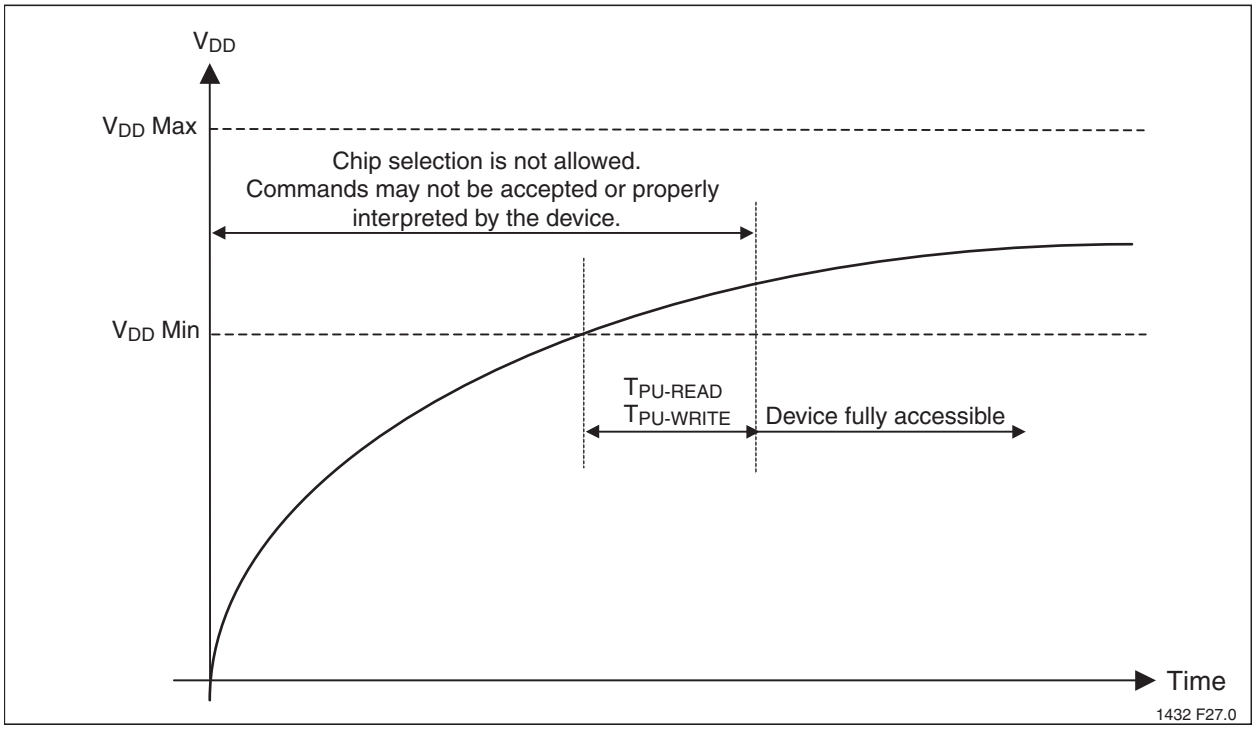
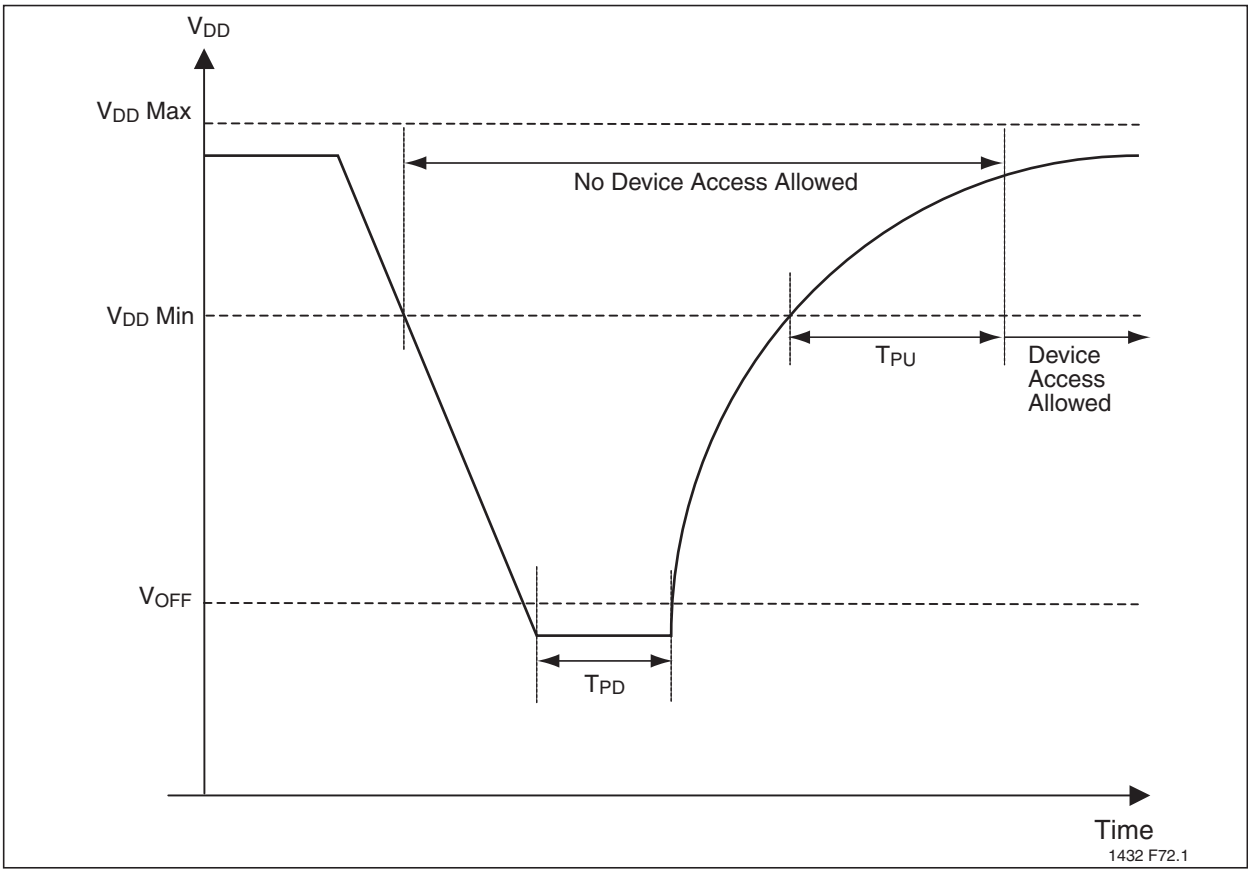


FIGURE 6-2: POWER-DOWN AND VOLTAGE DROP DIAGRAM



6.2 DC Characteristics

TABLE 6-4: DC OPERATING CHARACTERISTICS (V_{DD} = 1.65V–1.95V)

Symbol	Parameter	Limits				Test Conditions
		Min	Typ	Max	Units	
I_{DDR1}	Read Current		8	15	mA	V_{DD}=V_{DD} Max, CE#=0.1 V_{DD}/0.9 V_{DD}@40 MHz, SO=open
I_{DDR2}	Read Current			20	mA	V_{DD} = V_{DD} Max, CE#=0.1 V_{DD}/0.9 V_{DD}@104 MHz, SO=open
I_{DDW}	Program and Erase Current			25	mA	V_{DD} Max
I_{SB}	Standby Current		10	40	µA	CE#=V_{DD}, V_{IN}=V_{DD} or V_{SS}
I_{DPD}	Deep Power-down Current		2.5	5	µA	CE#=V_{DD}, V_{IN}=V_{DD} or V_{SS}
I_{LI}	Input Leakage Current			2	µA	V_{IN}=GND to V_{DD}, V_{DD}=V_{DD} Max
I_{LO}	Output Leakage Current			2	µA	V_{OUT}=GND to V_{DD}, V_{DD}=V_{DD} Max
V_{IL}	Input Low Voltage			0.3	V	V_{DD}=V_{DD} Min
V_{IH}	Input High Voltage	0.7 V_{DD}			V	V_{DD}=V_{DD} Max
V_{OL}	Output Low Voltage			0.2	V	I_{OL}=100 µA, V_{DD}=V_{DD} Min
V_{OH}	Output High Voltage	V_{DD}-0.2			V	I_{OH}=-100 µA, V_{DD}=V_{DD} Min

TABLE 6-5: CAPACITANCE (TA = 25°C, F=1 MHZ, OTHER PINS OPEN)

Parameter	Description	Test Condition	Maximum
C_{OUT}[1]	Output Pin Capacitance	V_{OUT} = 0V	8 pF
C_{IN}[1]	Input Capacitance	V_{IN} = 0V	6 pF

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 6-6: RELIABILITY CHARACTERISTICS

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}[1]	Endurance	100,000	Cycles	JEDEC Standard A117
T_{DR}[1]	Data Retention	100	Years	JEDEC Standard A103
I_{LTH}[1]	Latch Up	100 + I_{DD}	mA	JEDEC Standard 78

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 6-7: WRITE TIMING PARAMETERS (V_{DD} = 1.65V–1.95V)

Symbol	Parameter	Minimum	Maximum	Units
T_{SE}	Sector-Erase		25	ms
T_{BE}	Block-Erase		25	ms
T_{SCE}	Chip-Erase		50	ms
T_{PP}	Page-Program		1.5	ms
T_{PSID}	Program Security-ID		1.5	ms
T_{WS}	Write-Suspend Latency		25	µs
T_{Wpen}	Write-Protection Enable Bit Latency		25	ms

6.3 AC Characteristics

TABLE 6-8: AC OPERATING CHARACTERISTICS (V_{DD} = 1.65V–1.95V)

Symbol	Parameter	Limits - 40 MHz		Limits - 80 MHz		Limits - 104 MHz		Units
		Min	Max	Min	Max	Min	Max	
F_{CLK}	Serial Clock Frequency		40		80		104	MHz
T_{CLK}	Serial Clock Period		25		12.5		9.6	ns
T_{SCKH}	Serial Clock High Time	11		5.5		4.5		ns
T_{SCKL}	Serial Clock Low Time	11		5.5		4.5		ns
T_{SCKR}[1]	Serial Clock Rise Time (slew rate)	0.1		0.1		0.1		V/ns
T_{SCKF}[1]	Serial Clock Fall Time (slew rate)	0.1		0.1		0.1		V/ns
T_{CES}[2]	CE# Active Setup Time	8		5		5		ns
T_{CEH}[2]	CE# Active Hold Time	8		5		5		ns
T_{CHS}[2]	CE# Not Active Setup Time	8		5		5		ns
T_{CHH}[2]	CE# Not Active Hold Time	8		5		5		ns
T_{CPH}	CE# High Time	25		12.5		12		ns
T_{CHZ}	CE# High to High-Z Output		19		12.5		12	ns
T_{CLZ}	SCK Low to Low-Z Output	0		0		0		ns
T_{HLS}	HOLD# Low Setup Time	8		5		5		ns
T_{HHS}	HOLD# High Setup Time	8		5		5		ns
T_{HLH}	HOLD# Low Hold Time	8		5		5		ns
T_{HHH}	HOLD# High Hold Time	8		5		5		ns
T_{HZ}	HOLD# Low-to-High-Z Output		8		8		8	ns
T_{LZ}	HOLD# High-to-Low-Z Output		8		8		8	ns
T_{DS}	Data In Setup Time	3		3		3		ns
T_{DH}	Data In Hold Time	4		4		4		ns
T_{OH}	Output Hold from SCK Change	0		0		0		ns
T_V	Output Valid from SCK		8/5[3]		8/5[3]		8/5[3]	ns

1. Maximum Rise and Fall time may be limited by T_{SCKH} and T_{SCKL} requirements
2. Relative to SCK.
3. 30 pF/10 pF

FIGURE 6-3: HOLD TIMING DIAGRAM

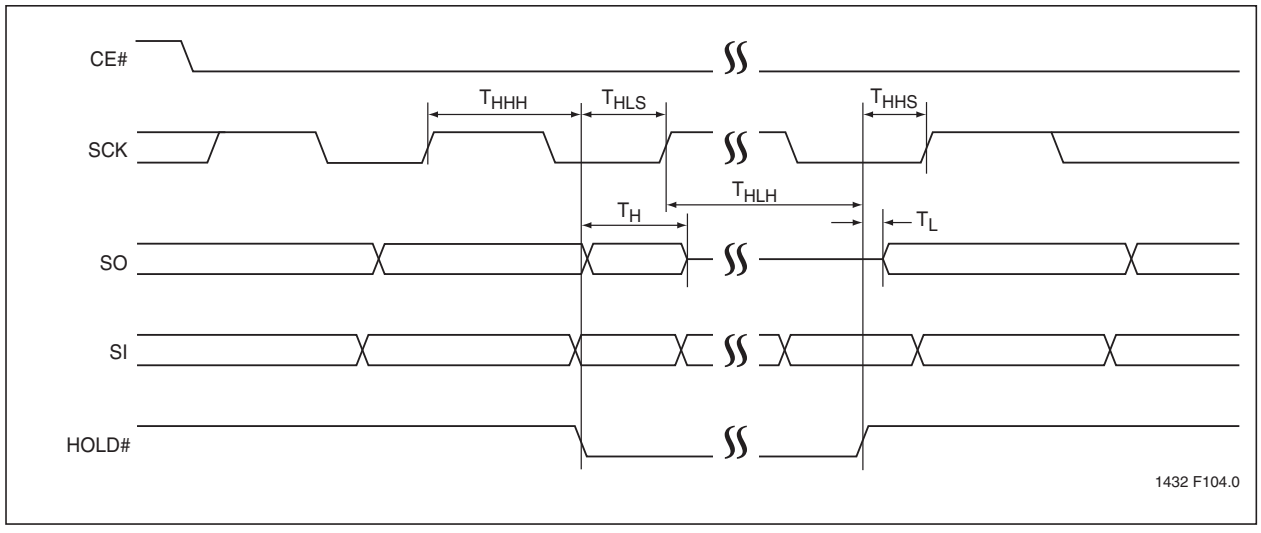


FIGURE 6-4: SERIAL INPUT TIMING DIAGRAM

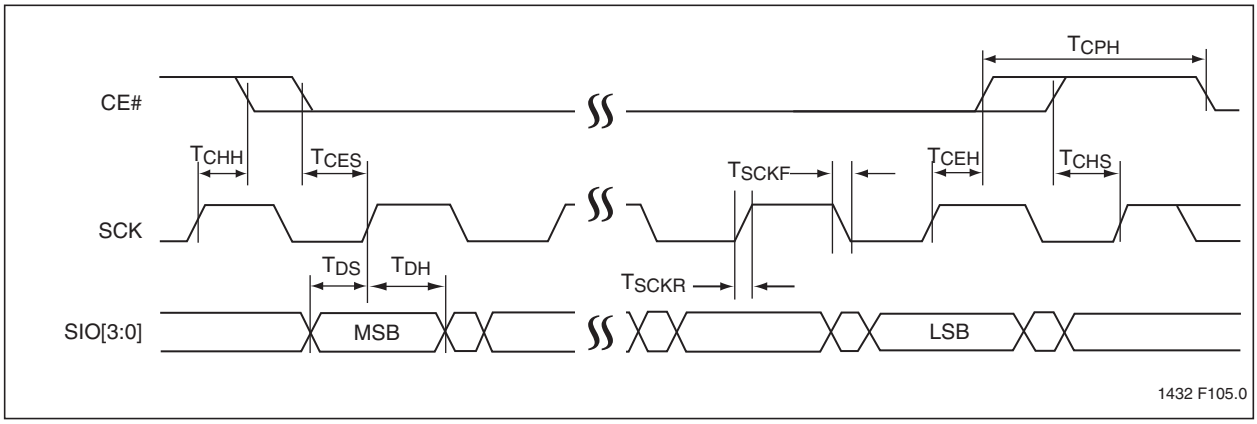


FIGURE 6-5: SERIAL OUTPUT TIMING DIAGRAM

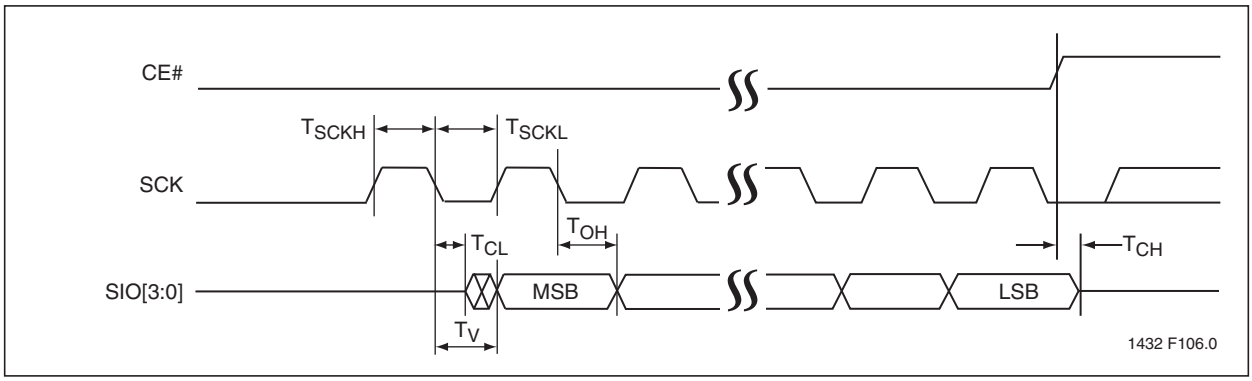
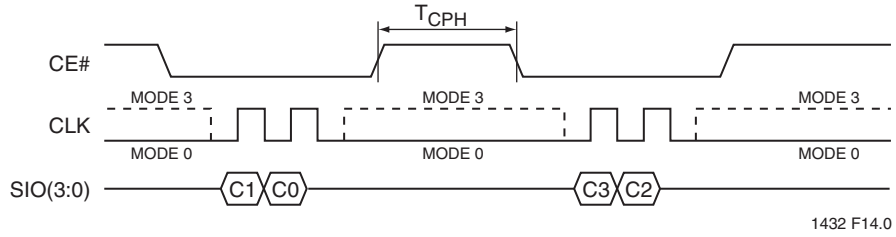


TABLE 6-9: RESET TIMING PARAMETERS

$T_{R(i)}$	Parameter	Minimum	Maximum	Units
$T_{R(o)}$	Reset to Read (non-data operation)		20	ns
$T_{R(p)}$	Reset Recovery from Program or Suspend		100	µs
$T_{R(e)}$	Reset Recovery from Erase		1	ms

FIGURE 6-6: RESET TIMING DIAGRAM



Note: C[1:0] = 66H; C[3:2] = 99H

FIGURE 6-7: AC INPUT/OUTPUT REFERENCE WAVEFORMS

1432 F28.0

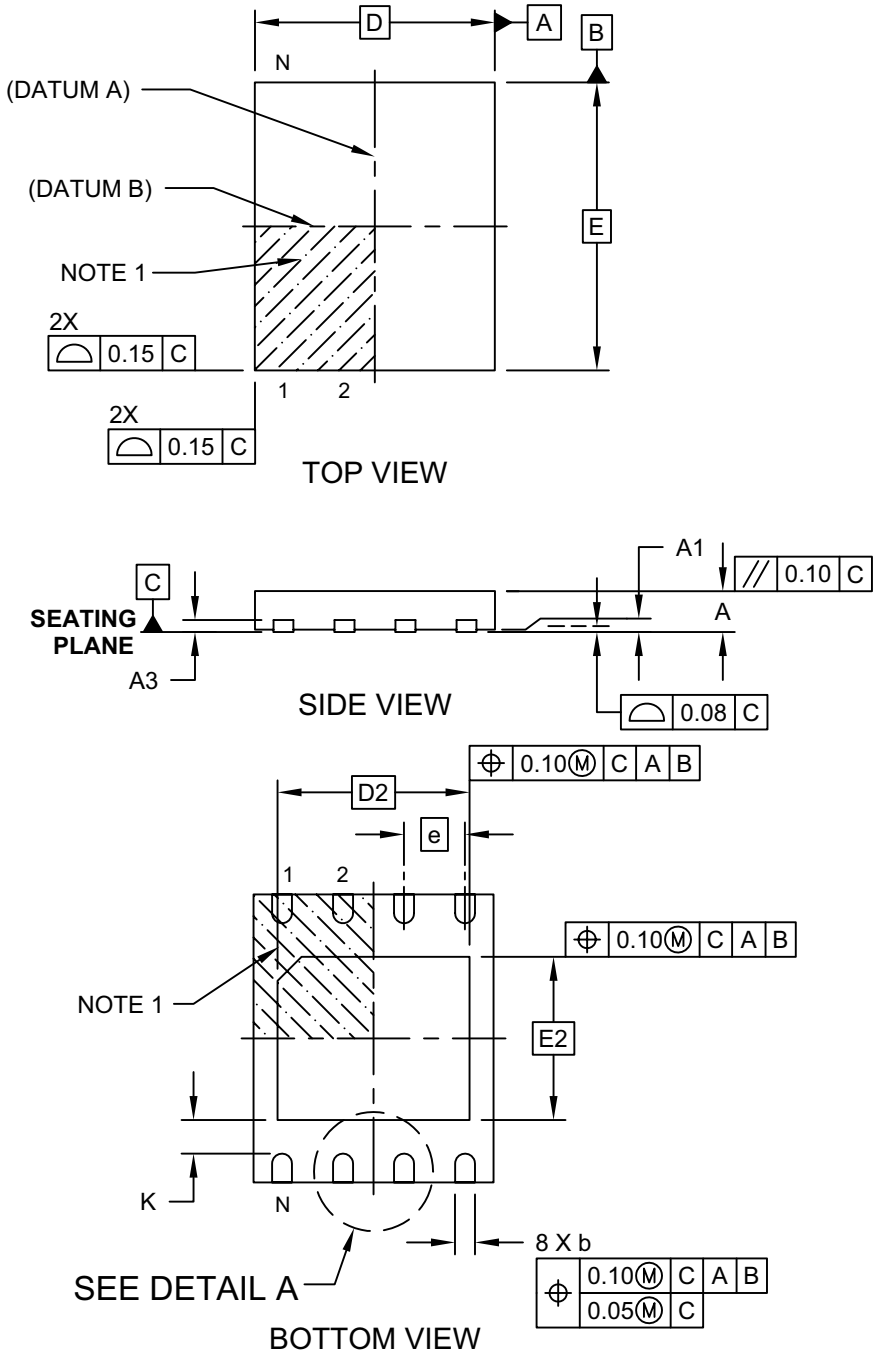
AC test inputs are driven at V_{IHT} ($0.9V_{DD}$) for a logic '1' and V_{ILT} ($0.1V_{DD}$) for a logic '0'. Measurement reference points for inputs and outputs are V_{HT} ($0.5V_{DD}$) and V_{LT} ($0.5V_{DD}$). Input rise and fall times (10% ↔ 90%) are <3 ns.

Note: V_{HT} - V_{HIGH} Test
V_{LT} - V_{LOW} Test
V_{IHT} - V_{INPUT} HIGH Test
V_{ILT} - V_{INPUT} LOW Test

7.0 PACKAGING DIAGRAMS

8-Lead Plastic Very, Very Thin Small Outline No-Lead (MF) - 5x6 mm Body [WDFN]

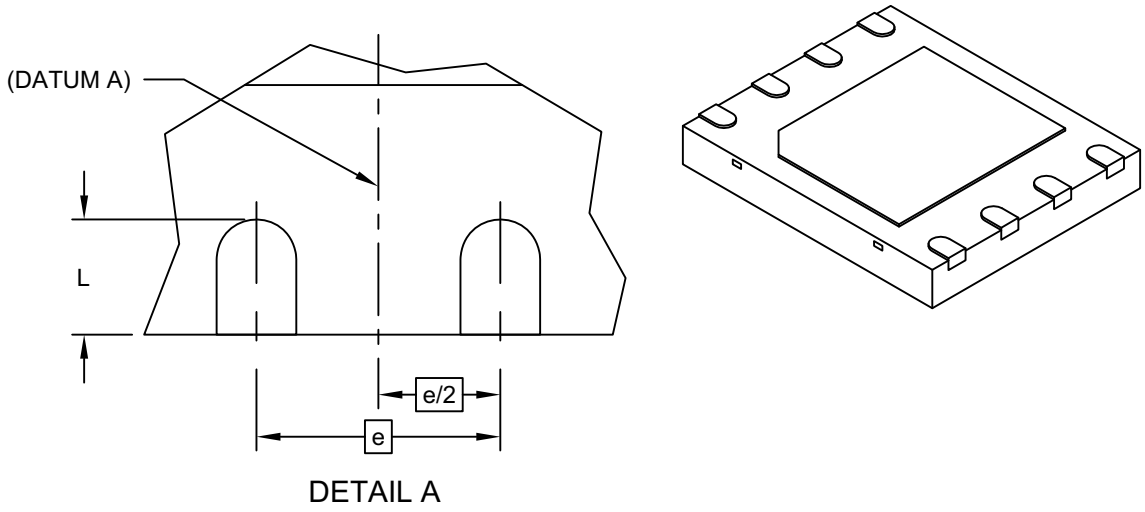
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-210B Sheet 1 of 2

8-Lead Plastic Very, Very Thin Small Outline No-Lead (MF) - 5x6 mm Body [WDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL A

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	0.70	0.75	0.80
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Width	D		5.00 BSC	
Exposed Pad Width	D2		4.00 BSC	
Overall Length	E		6.00 BSC	
Exposed Pad Length	E2		3.40 BSC	
Terminal Width	b	0.35	0.42	0.48
Terminal Length	L	0.50	0.60	0.70
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

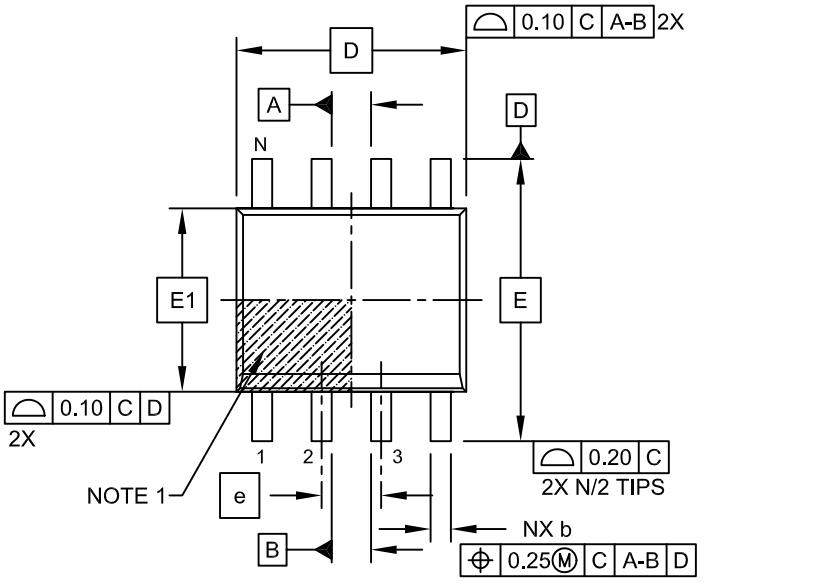
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

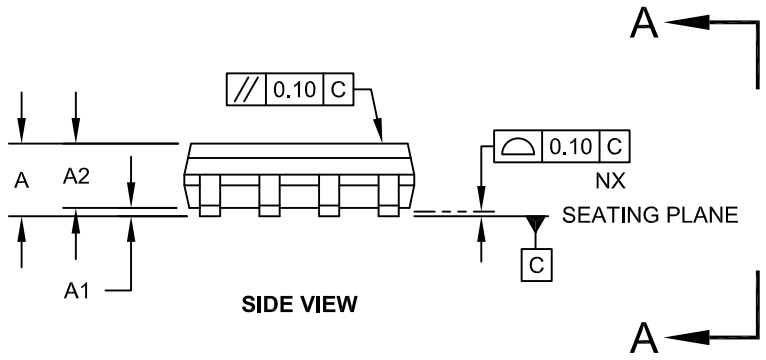
Microchip Technology Drawing C04-210B Sheet 2 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

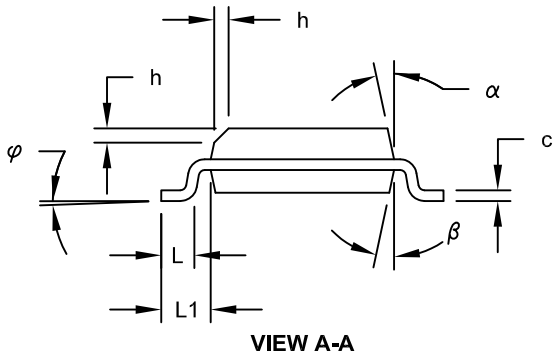
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

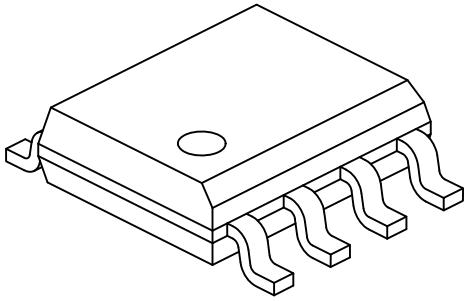


VIEW A-A

Microchip Technology Drawing No. C04-057C Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-057C Sheet 2 of 2

TABLE 7-1: REVISION HISTORY

Revision	Description	Date
A	• Initial release of data sheet	May 2012
B	• Updated document to new format • Revised CPNs to reflect the new package codes • Updated package drawings to the new format • Revised "Hardware Write Protection" on page 8, "Write-Suspend and Write-Resume" on page 29, and "Lock-Down Block-Protection Register (LBPR)" on page 36 • Updated "Power-Up Specifications" on page 41	Apr 2013
C	• Revised "Features" on page 1 • Minor updates to Figure 5-7 on page 17, Table 6-4 on page 43,and Figure 6-7 on page 46 • Updated "Product Identification System" on page 53 • Updated package description for MF package from WSON to WDFN	Sep 2013

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8.0 PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	–	XXX	X	/	XX
Device	Tape/Reel Indicator		Operating Frequency	Temperature		Package

Device:	SST26WF016B	= 16 Mbit, 2.7-3.6V, SQI Flash Memory WP#/Hold# pin Enable at power-up
	SST26WF016BA	= 16 Mbit, 2.7-3.6V, SQI Flash Memory WP#/Hold# pin Disable at power-up
Tape and Reel Flag:	T	= Tape and Reel
Operating Frequency:	104	= 104 MHz
Temperature:	I	= -40°C to +85°C
Package:	MF	= WDFN (6mm x 5mm Body), 8-contact
	SN	= SOIC (150 mil Body), 8-contact
	CS	= Z-Scale, XFBGA, 8-ball

Valid Combinations:

SST26WF016B-104I/MF
SST26WF016BT-104I/MF
SST26WF016BA-104I/MF
SST26WF016BAT-104I/MF
SST26WF016B-104I/SN
SST26WF016BT-104I/SN
SST26WF016BA-104I/SN
SST26WF016BAT-104I/SN
SST26WF016BT-104I/CS

TABLE 8-1: PART MARKING

Ordering Number	Marking On Part
SST26WF016B-104I/MF	26WF016B-I/MF
SST26WF016BA-104I/MF	26WF016B-I/MF
SST26WF016B-104I/SN	26WF016B-I/SN
SST26WF016BA-104I/SN	26WF016B-I/SN
SST26WF016BT-104I/CS	W16B

Note: Due to intellectual property concerns, the 8-ball XFBGA Z-Scale™ package drawing is not included in this data sheet. Please contact Microchip Sales for more information.

9.0 APPENDIX

TABLE 9-1: SERIAL FLASH DISCOVERABLE PARAMETER (SFDP) (1 OF 10)

Address	Bit Address	Data	Comments
SFDP Header			
SFDP Header: 1st DWORD			
00H	A7:A0	53H	**SFDP Signature** SFDP Signature=50444653H
01H	A15:A8	46H	
02H	A23:A16	44H	
03H	A31:A24	50H	
SFDP Header: 2nd DWORD			
04H	A7:A0	00H	**SFDP Minor Revision Number**
05H	A15:A8	01H	**SFDP Major Revision Number**
06H	A23:A16	02H	**Number of Parameter Headers (NPH)**
07H	A31:A24	FFH	**Unused**. Contains FFH and can not be changed.
Parameter Headers			
JEDEC Flash Parameter Header: 1st DWORD			
08H	A7:A0	00H	**ID Number**. When this field is set to 00H, it indicates a JEDEC-specified header. For vendor-specified headers, this field must be set to the vendor's manufacturer ID.
09H	A15:A8	00H	**Parameter Table Minor Revision Number** Minor revisions are either clarifications or changes that add parameters in existing Reserved locations. Minor revisions do NOT change overall structure of SFDP. Minor Revision starts at 00H.
0AH	A23:A16	01H	**Parameter Table Major Revision Number** Major revisions are changes that reorganize or add parameters to locations that are NOT currently Reserved. Major revisions would require code (BIOS/firmware) or hardware change to get previously defined discoverable parameters. Major Revision starts at 01H
0BH	A31:A24	09H	**Parameter Table Length** Number of DWORDs that are in the Parameter table
JEDEC Flash Parameter Header: 2nd DWORD			
0CH	A7:A0	30H	**Parameter Table Pointer (PTP)** A 24-bit address that specifies the start of this header's Parameter table in the SFDP structure. The address must be DWORD-aligned.
0DH	A15:A8	00H	
0EH	A23:A16	00H	
0FH	A31:A24	FFH	**Unused**. Contains FF and can not be changed.
JEDEC Flash Parameter Header: 3rd DWORD			
10H	A7:A0	00H	**ID Number**. When this field is set to 00H, it indicates a JEDEC-specified header. For vendor-specified headers, this field must be set to the vendor's manufacturer ID.
11H	A15:A8	FFH	**Parameter Table Minor Revision Number** Minor revisions are either clarifications or changes that add parameters in existing Reserved locations. Minor revisions do NOT change overall structure of SFDP. Minor Revision starts at 00H.

TABLE 9-1: SERIAL FLASH DISCOVERABLE PARAMETER (SFDP) (CONTINUED) (2 OF 10)

Address	Bit Address	Data	Comments
12H	A23:A16	FFH	**Parameter Table Major Revision Number** Major revisions are changes that reorganize or add parameters to locations that are NOT currently Reserved. Major revisions would require code (BIOS/firmware) or hardware change to get previously defined discoverable parameters. Major Revision starts at 01H
13H	A31:A24	00H	**Parameter Table Length** Number of DWORDs that are in the Parameter table
JEDEC Flash Parameter Header: 4th DWORD			
14H	A7:A0	FFH	**Parameter Table Pointer (PTP)** This 24-bit address specifies the start of this header's Parameter Table in the SFDP structure. The address must be DWORD-aligned.
15H	A15:A8	FFH	
16H	A23:A16	FFH	
17H	A31:A24	FFH	**Unused**. Contains FF can not be changed.
Microchip/SST (Vendor) Parameter Header: 5th DWORD			
18H	A7:A0	BFH	**ID Number** Manufacture ID (vendor specified header)
19H	A15:A8	00H	**Parameter Table Minor Revision Number**
1AH	A23:A16	01H	**Parameter Table major Revision Number,** Revision 1.0
1BH	A31:A24	18H	**Parameter Table Length,** 24 Double Words
SST (Vendor) Parameter Header: 6th DWORD			
1CH	A7:A0	00H	**Parameter Table Pointer (PTP)** This 24-bit address specifies the start of this header's Parameter Table in the SFDP structure. The address must be DWORD-aligned.
1DH	A15:A8	02H	
1EH	A23:A16	00H	
1FH	A31:A24	FFH	**Unused.** Contains FF can not be changed.
JEDEC Flash Parameter Table			
JEDEC Flash Parameter Table: 1st DWORD			
30H	A1:A0	FDH	**Block/Sector Erase Sizes** 00: Reserved **01: 4 KByte Erase** 10: Reserved 11: Use this setting only if the 4 Kilobyte erase is unavailable.
	A2		**Write Granularity** 0: Single-byte programmable devices or buffer programmable devices with buffer is less than 64 bytes (32 Words). **1: For buffer programmable devices when the buffer size is 64 bytes (32 Words) or larger.**
	A3		**Write Enable Instruction Required for Writing to Volatile Status Register** 0: Target flash has nonvolatile status bit. Write/Erase commands do not require status register to be written on every power on. **1: Target flash requires 0x00 to be written to the status register in order to allow write and Erase**
	A4		**Write Enable Opcode Select for Writing to Volatile Status Register** 0: 0x50. Enables a status register write when bit 3 is set to 1. **1: 0x06 Enables a status register write when bit 3 is set to 1**.
	A7:A5		**Unused**. Contains 111b and can not be changed
31H	A15:A8	20H	**4 KByte Erase Opcode**

TABLE 9-1: SERIAL FLASH DISCOVERABLE PARAMETER (SFDP) (CONTINUED) (3 OF 10)

Address	Bit Address	Data	Comments
32H	A16	F1H	Supports (1-1-2) Fast Read 0: (1-1-2) Fast Read NOT supported **1: (1-1-2) Fast Read supported**
	A18:A17		**Address Bytes** Number of bytes used in addressing flash array read, write and erase **00: 3-Byte only addressing** 01: 3- or 4-Byte addressing (e.g. defaults to 3-Byte mode; enters 4-Byte mode on command) 10: 4-Byte only addressing 11: Reserved
	A19		**Supports Double Transfer Rate (DTR) Clocking** Indicates the device supports some type of double transfer rate clocking. **0: DTR NOT supported** 1: DTR Clocking supported
	A20		**Supports (1-2-2) Fast Read** Device supports single input opcode, dual input address, and dual output data Fast Read. 0: (1-2-2) Fast Read NOT supported. **1: (1-2-2) Fast Read supported.**
	A21		**Supports (1-4-4) Fast Read** Device supports single input opcode, quad input address, and quad output data Fast Read 0: (1-4-4) Fast Read NOT supported. **1: (1-4-4) Fast Read supported.**
	A22		**Supports (1-1-4) Fast Read** Device supports single input opcode & address and quad output data Fast Read. 0: (1-1-4) Fast Read NOT supported. **1: (1-1-4) Fast Read supported.**
	A23		**Unused**. Contains ‘1’ can not be changed
33H	A31:A24	FFH	**Unused**. Contains FF can not be changed
JEDEC Flash Parameter Table: 2nd DWORD			
34H	A7:A0	FFH	**Flash Memory Density** SST26WF016B/016BA= 00FFFFFFH
35H	A15:A8	FFH	
36H	A23:A16	FFH	
37H	A31:A24	00H	
JEDEC Flash Parameter Table: 3rd DWORD			
38H	A4:A0	44H	**(1-4-4) Fast Read Number of Wait states (dummy clocks) needed before valid output** 00100b: 4 dummy clocks (16 dummy bits) are needed with a quad input address phase instruction
	A7:A5		**Quad Input Address Quad Output (1-4-4) Fast Read Number of Mode Bits** 010b: 2 dummy clocks (8 mode bits) are needed with a single input opcode, quad input address and quad output data Fast Read Instruction.
39H	A15:A8	EBH	**(1-4-4) Fast Read Opcode** Opcode for single input opcode, quad input address, and quad output data Fast Read.

TABLE 9-1: SERIAL FLASH DISCOVERABLE PARAMETER (SFDP) (CONTINUED) (4 OF 10)

Address	Bit Address	Data	Comments
3AH	A20:A16	08H	**(1-1-4) Fast Read Number of Wait states (dummy clocks) needed before valid output** 01000b: 8 dummy bits are needed with a single input opcode & address and quad output data Fast Read Instruction
	A23:A21		**(1-1-4) Fast Read Number of Mode Bits** 000b: No mode bits are needed with a single input opcode & address and quad output data Fast Read Instruction
3BH	A31:A24	6BH	**(1-1-4) Fast Read Opcode** Opcode for single input opcode & address and quad output data Fast Read.
JEDEC Flash Parameter Table: 4th DWORD			
3CH	A4:A0	08H	**(1-1-2) Fast Read Number of Wait states (dummy clocks) needed before valid output** 01000b: 8 dummy clocks are needed with a single input opcode, address and dual output data fast read instruction.
	A7:A5		**(1-1-2) Fast Read Number of Mode Bits** 000b: No mode bits are needed with a single input opcode & address and quad output data Fast Read Instruction
3DH	A15:A8	3BH	**(1-1-2) Fast Read Opcode** Opcode for single input opcode& address and dual output data Fast Read.
3EH	A20:A16	42H	**(1-2-2) Fast Read Number of Wait states (dummy clocks) needed before valid output** 00010b: 2 clocks of dummy cycle.
	A23:A21		**(1-2-2) Fast Read Number of Mode Bits (in clocks)** 010b: 2 clocks (4 bits) of mode bits are needed
3FH	A31:A24	BBH	**(1-2-2) Fast Read Opcode** Opcode for single input opcode, dual input address, and dual output data Fast Read.
JEDEC Flash Parameter Table: 5th DWORD			
40H	A0	FEH	**Supports (2-2-2) Fast Read** Device supports dual input opcode& address and dual output data Fast Read. **0: (2-2-2) Fast Read NOT supported.** 1: (2-2-2) Fast Read supported.
	A3:A1		Reserved. Bits default to all 1's.
	A4		**Supports (4-4-4) Fast Read** Device supports Quad input opcode & address and quad output data Fast Read. 0: (4-4-4) Fast Read NOT supported. **1: (4-4-4) Fast Read supported.**
	A7:A5		Reserved. Bits default to all 1's.
41H	A15:A8	FFH	Reserved. Bits default to all 1's.
42H	A23:A16	FFH	Reserved. Bits default to all 1's.
43H	A31:A24	FFH	Reserved. Bits default to all 1's.
JEDEC Flash Parameter Table: 6th DWORD			
44H	A7:A0	FFH	Reserved. Bits default to all 1's.
45H	A15:A8	FFH	Reserved. Bits default to all 1's.

TABLE 9-1: SERIAL FLASH DISCOVERABLE PARAMETER (SFDP) (CONTINUED) (5 OF 10)

Address	Bit Address	Data	Comments
46H	A20:A16	00H	**(2-2-2) Fast Read Number of Wait states (dummy clocks) needed before valid output** 00000b: No dummy bit is needed
	A23:A21		**(2-2-2) Fast Read Number of Mode Bits** 000b: No mode bits are needed
47H	A31:A24	FFH	**(2-2-2) Fast Read Opcode** Opcode for dual input opcode& address and dual output data Fast Read. (not supported)
JEDEC Flash Parameter Table: 7th DWORD			
48H	A7:A0	FFH	Reserved. Bits default to all 1's.
49H	A15:A8	FFH	Reserved. Bits default to all 1's.
4AH	A20:A16	44H	**(4-4-4) Fast Read Number of Wait states (dummy clocks) needed before valid output** 00100b: 4 clocks dummy are needed with a quad input opcode & address and quad output data Fast Read Instruction
	A23:A21		**(4-4-4) Fast Read Number of Mode Bits** 010b: 2 clocks mode bits are needed with a quad input opcode & address and quad output data Fast Read Instruction
4BH	A31:A24	0BH	**(4-4-4) Fast Read Opcode** Opcode for quad input opcode/address, quad output data Fast Read
JEDEC Flash Parameter Table: 8th DWORD			
4CH	A7:A0	0DH	**Sector Type 1 Size** 8 KByte, Sector/block size = 2^N bytes
4DH	A15:A8	D8H	**Sector Type 1 Opcode** Opcode used to erase the number of bytes specified by Sector Type 1 Size (bits 7-0).
4EH	A23:A16	0FH	**Sector Type 2 Size** 32 KByte, Sector/block size = 2^N bytes
4FH	A31:A24	D8H	**Sector Type 2 Opcode** Opcode used to erase the number of bytes specified by Sector Type 2 Size (bits23-16).
JEDEC Flash Parameter Table: 9th DWORD			
50H	A7:A0	10H	**Sector Type 3 Size** 64 KByte, Sector/block size = 2^N bytes
51H	A15:A8	D8H	**Sector Type 3 Opcode** Opcode used to erase the number of bytes specified by Sector Type 3 Size (bits7-0).
52H	A23:A16	00H	**Sector Type 4 Size** 0x00: this sector type does not exist
53H	A31:A24	00H	**Sector Type 4 Opcode** Opcode used to erase the number of bytes specified by Sector Type 4 Size (bits23-16) 0x00: this sector type does not exist
SST26WF016B/016BA (Vendor) Parameter Table			
SST26WF016B/016BA Identification			
200H	A7:A0	BFH	**Manufacturer ID**
201H	A15:A8	26H	**Memory Type**
202H	A23:A16	51H	**Device ID** SST26WF016B/016BA=51H
203H	A31:A24	FFH	**Reserved.** Bits default to all 1's.

TABLE 9-1: SERIAL FLASH DISCOVERABLE PARAMETER (SFDP) (CONTINUED) (6 OF 10)

Address	Bit Address	Data	Comments
SST26WF016B/016BA Interface			
204H	A2:A0	B9H	Interfaces Supported 000: SPI only **001: Power up default is SPI; Quad can be enabled/disabled** 010: Reserved : : 111: Reserved
	A3		**Supports Enable Quad** 0: not supported **1: supported**
	A6:A4		**Supports Hold#/Reset# Function** 000: Hold# 001: Reset# 010: HOLD/Reset# **011: Hold# & I/O when in SQI(4-4-4), 1-4-4 or 1-1-4 Read**
	A7		Supports Software Reset 0: not supported **1: supported**
205H	A8	DFH	Supports Quad Reset 0: not supported **1: supported**
	A10:A9		Reserved. Bits default to all 1's
	A13:A11		**Byte-Program or Page-Program (256 Bytes)** 011: Byte Program/Page Program in SPI and Quad Page Program once Quad is enabled
	A14		**Program-Erase Suspend Supported** 0: Not Supported **1: Program/Erase Suspend Supported**
	A15		**Deep Power-Down Mode Supported** 0: Not Supported **1: Deep Power-Down Mode Supported**
206H	A16	FDH	**OTP Capable (Security ID) Supported** 0: not supported **1: supported**
	A17		**Supports Block Group Protect** **0: not supported** 1: supported
	A18		**Supports Independent Block Protect** 0: not supported **1: supported**
	A19		**Supports Independent non Volatile Lock (Block or Sector becomes OTP)** 0: not supported **1: supported**
	A23:A20		Reserved. Bits default to all 1's.
207H	A31:A24	FFH	Reserved. Bits default to all 1's.
208H	A7:A0	65H	**V_{DD} Minimum Supply Voltage** 1.65V (F165H)
209H	A15:A8	F1H	

TABLE 9-1: SERIAL FLASH DISCOVERABLE PARAMETER (SFDP) (CONTINUED) (7 OF 10)

Address	Bit Address	Data	Comments
20AH	A23:A16	95H	**V_{DD} Maximum Supply Voltage** 1.95V (F195H)
20BH	A31:A24	F1H	
20CH	A7:A0	32H	**Typical time out for Byte-Program:** 50 µs Typical time out for Byte Program is in µs. Represented by conversion of the actual time from the decimal to hexadecimal number.
20DH	A15:A8	FFH	Reserved. Bits default to all 1's.
20EH	A23:A16	0AH	**Typ time out for page program**: 1.0ms (xxH*(0.1ms)
20FH	A31:A24	12H	**Typical time out for Sector-Erase/Block-Erase:** 18 ms Typical time out for Sector/Block-Erase is in ms. Represented by conversion of the actual time from the decimal to hexadecimal number.
210H	A7:A0	23H	**Typical time out for Chip-Erase:** 35 ms Typical time out for Chip-Erase is in ms. Represented by conversion of the actual time from the decimal to hexadecimal number.
211H	A15:A8	46H	**Max. time out for Byte-Program:** 70 µs Typical time out for Byte Program is in µs. Represented by conversion of the actual time from the decimal to hexadecimal number.
212H	A23:A16	FFH	Reserved. Bits default to all 1's.
213H	A31:A24	0FH	**Max time out for Page-Program:** 1.5ms. Typical time out for Page Program in xxH * (0.1ms) ms
214H	A7:A0	19H	**Max. time out for Sector Erase/Block Erase:** 25ms. Max time out for Sector/Block Erase in ms
215H	A15:A8	32H	**Max. time out for Chip Erase**: 50ms. Max time out for Chip Erase in ms.
216H	A23:A16	0FH	**Max. time out for Program Security ID:** 1.5 ms Max time out for Program Security ID in xxH*(0.1ms) ms
217H	A31:A24	19H	**Max. time for Write-Protection Bit Enable** Max time out for ms. Represented by conversion of the actual time from the decimal to hexadecimal number. (i.e. 25 ms = 19H)
218H	A23:A16	19H	**Max. time Write-Suspend Latency:** 25 µs Max time out for Write-Suspend Latency is in µs. Represented by conversion of the actual time from the decimal to hexadecimal number.)
219H	A31:A24	03H	**Max. time to Deep Power-Down:** 3 µs Represented by conversion of the actual time from the decimal to hexadecimal number. (i.e. 3 µs = 03H)
21AH	A23:A16	0AH	**Max. time out from Deep Power-Down mode to Standby mode:** 10 µs. Represented by conversion of the actual time from the decimal to hexadecimal number. (i.e. 10 µs = 0AH)
21BH	A31:A24	FFH	Reserved. Bits default to all 1's.
21CH	A23:A16	FFH	Reserved. Bits default to all 1's.
21DH	A31:A24	FFH	Reserved. Bits default to all 1's.
21EH	A23:A16	FFH	Reserved. Bits default to all 1's.
21FH	A31:A24	FFH	Reserved. Bits default to all 1's.
Supported Instructions			
220H	A7:A0	00H	No Operation
221H	A15:A8	66H	Reset Enable
222H	A23:A16	99H	Reset Memory
223H	A31:A24	38H	Enable Quad I/O
224H	A7:A0	FFH	Reset Quad I/O
225H	A15:A8	05H	Read Status Register

TABLE 9-1: SERIAL FLASH DISCOVERABLE PARAMETER (SFDP) (CONTINUED) (8 OF 10)

Address	Bit Address	Data	Comments
226H	A23:A16	01H	Write Status Register
227H	A31:A24	35H	Read Configuration Register
228H	A7:A0	06H	Write Enable
229H	A15:A8	04H	Write Disable
22AH	A23:A16	02H	Byte Program or Page Program
22BH	A31:A24	32H	SPI Quad Page Program
22CH	A7:A0	B0H	Suspends Program/Erase
22DH	A15:A8	30H	Resumes Program/Erase
22EH	A23:A16	72H	Read Block-Protection register
22FH	A31:A24	42H	Write Block Protection Register
230H	A7:A0	8DH	Lock Down Block Protection Register
231H	A15:A8	E8H	non-Volatile Write-Lock Down Register
232H	A23:A16	98H	Global Block Protection Unlock
233H	A31:A24	88H	Read Security ID
234H	A7:A0	A5H	Program User Security ID Area
235H	A15:A8	85H	Lockout Security ID Programming
236H	A23:A16	C0H	Set Burst Length
237H	A31:A24	9FH	JEDEC-ID
238H	A7:A0	AFH	Quad J-ID
239H	A15:A8	5AH	SFDP
23AH	A23:A16	B9H	Deep Power-Down Mode
23BH	A31:A24	ABH	**Release Deep Power-Down Mode**
23CH	A4:A0	06H	**(1-4-4) SPI nB Burst with Wrap Number of Wait states (dummy clocks) needed before valid output** 00110b**:** 6 clocks of dummy cycle
	A7:A5		**(1-4-4) SPI nB Burst with Wrap Number of Mode Bits** 000b: Set Mode bits are not supported
23DH	A15:A8	ECH	(1-4-4) SPI nB Burst with Wrap Opcode
23EH	A20:A16	06H	**(4-4-4) SQI nB Burst with Wrap Number of Wait states (dummy clocks) needed before valid output** 00110b: 6 clocks of dummy cycle
	A23:A21		**(4-4-4) SQI nB Burst with Wrap Number of Mode Bits** 000b: Set Mode bits are not supported
23FH	A31:A24	0CH	(4-4-4) SQI nB Burst with Wrap Opcode
240H	A4:A0	00H	**(1-1-1) Read Memory Number of Wait states (dummy clocks) needed before valid output** 00000b: Wait states/dummy clocks are not supported.
	A7:A5		**(1-1-1) Read Memory Number of Mode Bits** 000b: Mode bits are not supported,
241H	A15:A8	03H	(1-1-1) Read Memory Opcode
242H	A20:A16	08H	**(1-1-1) Read Memory at Higher Speed Number of Wait states (dummy clocks) needed before valid output** 01000: 8 clocks (8 bits) of dummy cycle
	A23:A21		**(1-1-1) Read Memory at Higher Speed Number of Mode Bits** 000b: Mode bits are not supported,
243H	A31:A24	0BH	(1-1-1) Read Memory at Higher Speed Opcode
244H	A7:A0	FFH	Reserved. Bits default to all 1's.

TABLE 9-1: SERIAL FLASH DISCOVERABLE PARAMETER (SFDP) (CONTINUED) (9 OF 10)

Address	Bit Address	Data	Comments
245H	A15:A8	FFH	Reserved. Bits default to all 1's.
246H	A23:A16	FFH	Reserved. Bits default to all 1's.
247H	A31:A24	FFH	Reserved. Bits default to all 1's.
Security ID			
248H	A7:A0	FFH	**Security ID size in bytes** Example: If the size is 2 KBytes, this field would be 07FFH
249H	A15:A8	07H	**Security ID Range** Unique ID (Pre-programmed at factory): 0000H - 0007H User Programmable: 0008H - 07FFH
24AH	A23:A16	FFH	Reserved. Bits default to all 1's.
24BH	A31:A24	FFH	Reserved. Bits default to all 1's.
Memory Organization/Block Protection Bit Mapping [1]			
24CH	A7:A0	01H	**Section 1: Sector Type Number:** Sector type in JEDEC Parameter Table (bottom, 8 KByte)
24DH	A15:A8	02H	**Section 1 Number of Sectors** Four of 8KB block (2^n)
24EH	A23:A16	FFH	**Section 1 Block Protection Bit Start** ((2^m) +1)+ c, c=FFH or -1, m= 5 for 16 Mb Address bits are Read Lock bit locations and Even Address bits are Write Lock bit locations. The most significant (left-most) bit indicates the sign of the integer; it is sometimes called the sign bit. If the sign bit is zero, then the number is greater than or equal to zero, or positive. If the sign bit is one then the number is less than zero or negative.
24FH	A31:A24	06H	**Section 1 (bottom) Block Protection Bit End** ((2^m) +1)+ c, c=06H or 6, m= 5 for 16 Mb Address bits are Read Lock bit locations and Even Address bits are Write Lock bit locations. The most significant (left-most) bit indicates the sign of the integer; it is sometimes called the sign bit. If the sign bit is zero, then the number is greater than or equal to zero, or positive. If the sign bit is one then the number is less than zero or negative.
250H	A7:A0	02H	**Section 2: Sector Type Number** Sector type in JEDEC Parameter Table (32KB Block)
251H	A15:A8	00H	**Section 2 Number of Sectors** One of 32KB Block (2^n, n=0)
252H	A23:A16	FDH	**Section 2 Block Protection Bit Start** ((2^m) +1)+ c, c=FDH or -3, m= 5 for 16 Mb The most significant (left-most) bit indicates the sign of the integer; it is sometimes called the sign bit. If the sign bit is zero, then the number is greater than or equal to zero, or positive. If the sign bit is one then the number is less than zero or negative.
253H	A31:A24	FDH	**Section 2 Block Protection Bit End** ((2^m) +1)+ c, c=FDH or -3, m= 5 for 16 Mb The most significant (left-most) bit indicates the sign of the integer; it is sometimes called the sign bit. If the sign bit is zero, then the number is greater than or equal to zero, or positive. If the sign bit is one then the number is less than zero or negative.
254H	A7:A0	03H	**Section 3: Sector Type Number** Sector type in JEDEC Parameter Table (64KB Block)

TABLE 9-1: SERIAL FLASH DISCOVERABLE PARAMETER (SFDP) (CONTINUED) (10 OF 10)

Address	Bit Address	Data	Comments
255H	A15:A8	05H	**Section 3 Number of Sectors** Thirty of 64KB Block (2^m-2, m= 5 for 16 Mb)
256H	A23:A16	00H	**Section 3 Block Protection Bit Start** Section 3 Block Protection Bit starts at 00H
257H	A31:A24	FCH	**Section 3 Block Protection Bit End** ((2^m) +1)+ c, c=FCH or -4, m= 5 for 16 Mb
258H	A7:A0	02H	**Section 4: Sector Type Number** Sector type in JEDEC Parameter Table (32KB Block)
259H	A15:A8	00H	**Section 4 Number of Sectors** One of 32KB Block (2^n, n=0)
25AH	A23:A16	FEH	**Section 4 Block Protection Bit Start** ((2^m) +1)+ c, c=FEH or -2, m= 5 for 16 Mb The most significant (left-most) bit indicates the sign of the integer; it is sometimes called the sign bit. If the sign bit is zero, then the number is greater than or equal to zero, or positive. If the sign bit is one then the number is less than zero or negative.
25BH	A31:A24	FEH	**Section 4 Block Protection Bit End** ((2^m) +1)+ c, c=FEH or -2, m= 5 for 16 Mb The most significant (left-most) bit indicates the sign of the integer; it is sometimes called the sign bit. If the sign bit is zero, then the number is greater than or equal to zero, or positive. If the sign bit is one then the number is less than zero or negative.
25CH	A7:A0	01H	**Section 5 Sector Type Number:** Sector type in JEDEC Parameter Table (top, 8 KByte)
25DH	A15:A8	02H	**Section 5 Number of Sectors** Four of 8KB block (2^n)
25EH	A23:A16	07H	**Section 5 Block Protection Bit Start** ((2^m) +1)+ c, c=07H or 7, m= 5 for 16 Mb Address bits are Read Lock bit locations and Even Address bits are Write Lock bit locations. The most significant (left-most) bit indicates the sign of the integer; it is sometimes called the sign bit. If the sign bit is zero, then the number is greater than or equal to zero, or positive. If the sign bit is one then the number is less than zero or negative.
25FH	A31:A24	0EH	**Section 5 (bottom) Block Protection Bit End** (((2^m) +1)+ c, c=0EH or 15, m= 5 for 16 Mb, Address bits are Read Lock bit locations and Even Address bits are Write Lock bit locations. The most significant (left-most) bit indicates the sign of the integer; it is sometimes called the sign bit. If the sign bit is zero, then the number is greater than or equal to zero, or positive. If the sign bit is one then the number is less than zero or negative.

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1. See “Mapping Guidance Details” for more detailed mapping information

9.1 Mapping Guidance Details

The SFDP Memory Organization/Block Protection Bit Mapping defines the memory organization including uniform sector/block sizes and different contiguous sectors/blocks sizes. In addition, this bit defines the number of these uniform and different sectors/blocks from address 000000H to the full range of Memory and the associated Block Locking Register bits of each sector/block.

Each major Section is defined as follows:

TABLE 9-2: SECTION DEFINITION

Major Section X	Section X: Sector Type Number
	Section X: Number of Sectors
	Section X: Block-Protection Register Bit Start Location
	Section X: Block-Protection Register Bit End Location

A Major Section consists of Sector Type Number, Number of Sector of this type, and the Block-Protection Bit Start/End locations. This is tied directly to JEDEC Flash Parameter Table Sector Size Type (in 7th DWORD and 8th DWORD section). Note that the contiguous 4KByte Sectors across the full memory range are not included on this section because they are not defined in the JEDEC Flash Parameter Table Sector Size Type section. Only the sectors/blocks that are dependently tied with the Block-Protection Register bits are defined. A major section is a partition of contiguous same-size sectors/blocks. There will be several Major Sections as you dissect across memory from 000000h to the full range. Similar sector/block size that re-appear may be defined as a different Major Section.

9.2 Sector Type Number

Sector Type Number is the sector/block size typed defined in JEDEC Flash Parameter Table: SFDP address locations 4CH, 4EH, and 50H. For SFDP address location 4CH, which is Sector Type 1, the size is represented by 01H; SFDP address location 4EH, Sector Type 2, size is represented by 02H; SFDP address location 50H, Sector Type 3, size is represented by 03H; and SFDP address location 52H, Sector Type 4, size is represented by 04H. Contiguous Same Sector Type # Size can re-emerge across the memory range and this Sector Type # will indicate that it is a separate/independent Major Section from the previous contiguous sectors/blocks.

9.3 Number of Sectors

Number of Sectors represents the number of contiguous sectors/blocks with similar size. A formula calculates the contiguous sectors/blocks with similar size. Given the sector/block size, type, and the number of sectors, the address range of these sectors/blocks can be determined along with specific Block Locking Register bits that control the read/write protection of each sectors/blocks.

9.4 Block-Protection Register Bit Start Location (BPSL)

Block-Protection Register Bit Start Location (BPSL) designates the start bit location in the Block-Protection Register where the first sector/block of this Major Section begins. If the value of BPSL is 00H, this location is the 0 bit location. If the value is other than 0, then this value is a constant value adder (c) for a given formula, **$(2^m + 1) + (c)$**. See “Memory Configuration”.

From the initial location, there will be a bit location for every increment by 1 until it reaches the Block Protection Register Bit End Location (BPEL). This number range from BPSL to BPEL will correspond to, and be equal to, the number of sectors/blocks on this Major Section.

9.5 Block Protection Register Bit End Location (BPEL)

Block Protection Register Bit End Location designates the end bit location in the Block Protection Register bit where the last sector/block of this Major Section ends. The value in this field is a constant value adder (c) for a given formula or equation, **$(2^m + 1) + (c)$**. See “Memory Configuration”

9.6 Memory Configuration

For the SST26WF016B/016BA family, the memory configuration is setup with different contiguous block sizes from bottom to the top of the memory. For example, starting from bottom of memory it has four 8KByte blocks, one 32KByte block, x number of 64KByte blocks depending on memory size, then one 32KByte block, and four 8KByte block on the top of memory. See Table 9-3.

TABLE 9-3: MEMORY BLOCK DIAGRAM REPRESENTATION

8 KByte Bottom Block (from 000000H)	Section 1: Sector Type 1
	Section 1: Number of Sectors
	Section 1: Block-Protection Register Bit Start Location
	Section 1: Block-Protection Register Bit End Location
32 KByte	Section 2: Sector Type Number
	Section 2: Number of Sectors
	Section 2: Block-Protection Register Bit Start Location
	Section 2: Block-Protection Register Bit End Location
64 KByte	Section 3: Sector Type Number
	Section 3: Number of Sectors
	Section 3: Block-Protection Register Bit Start Location
	Section 3: Block-Protection Register Bit End Location
32 KByte	Section 4: Sector Type Number
	Section 4: Number of Sectors
	Section 4: Block-Protection Register Bit Start Location
	Section 4: Block-Protection Register Bit End Location
8 KByte (Top Block)	Section 5: Sector Type Number
	Section 5: Number of Sectors
	Section 5: Block-Protection Register Bit Start Location
	Section 5: Block-Protection Register Bit End Location

Classifying these sector/block sizes via the Sector Type derived from JEDEC Flash Parameter Table: SFDP address locations 4CH, 4EH, and 50H is as follows:

- 8KByte Blocks are classified as Sector Type 1 (@4CH of SFDP)
- 32KByte Blocks are classified as Sector Type 2 (@4EH of SFDP)
- 64KByte Blocks are classified as Sector Type 3 (@50H of SFDP)

For the Number of Sectors associated with the contiguous sectors/blocks, a formula is used to determine the number of sectors/blocks of these Sector Types:

- 8KByte Block (Type 1) is calculated by 2n. n is a byte.
- 32KByte Block (Type 2) is calculated by 2n. n is a byte.
- 64KByte Block (Type 3) is calculated by (2m - 2). m can either be a 4, 5, 6, 7 or 8 depending on the memory size. This m field is going to be used for the 64KByte Block Section and will also be used for the Block Protection Register Bit Location formula.

m will have a constant value for specific densities and is defined as:

- 8Mbit = 4
- 16Mbit = 5
- 32Mbit = 6
- 64Mbit = 7
- 128Mbit = 8

Block Protect Register Start/End Bits are mapped in the SFDP by using the formula **$(2^m + 1) + (c)$**. “m” is a constant value that represents the different densities from 8Mbit to 128Mbit (used also in the formula calculating number of 64Kbyte Blocks above). The values that are going to be placed in the Block Protection Bit Start/End field table are the constant value adder (c) in the formula and are represented in two’s compliment except when the value is 00H. If the value is 00H, this location is the 0 bit location. If the value is other than 0, then this is a constant value adder (c) that will be used in the formula. The most significant (left most) bit indicates the sign of the integer; it is sometimes called the sign bit. If the sign bit is zero, then the number is greater than or equal to zero, or positive. If the sign bit is one, then the number is less than zero, or negative.

See Table 9-4 for an example of this formula.

TABLE 9-4: BPSL/BPEL EQUATION WITH ACTUAL CONSTANT ADDER DERIVED FROM THE FORMULA (2^M + 1) + (C)

Block Size	8 Mbit to 128 Mbit	Comments
8 KByte (Type 1) Bottom	BPSL = (2^m + 1) + FFH BPEL = (2^m + 1) + 04H	FFH = -1; 06H = 6 Odd address bits are Read-Lock bit locations and even address bits are Write-Lock bit locations.
32 KByte (Type 2)	BPSL = BPEL= (2^m + 1) + FDH	FDH= -3
64 KByte (Type 3)	BPSL = 00H BPEL = (2^m + 1) + FCH	00H is Block-Protection Register bit 0 location; FCH = -4
32 KByte (Type 2)	BPSL = BPEL= (2^m + 1) + FEH	FEH=-2
8 KByte (Type 1) Top	BPSL = (2^m + 1) + 07H BPEL = (2^m + 1) + 0EH	07H = 7; 0EH = 14 Odd address bits are Read-Lock bit locations and even address bits are Write-Lock bit locations.

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Printed on recycled paper.

ISBN:978-1-62077-495-3

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