

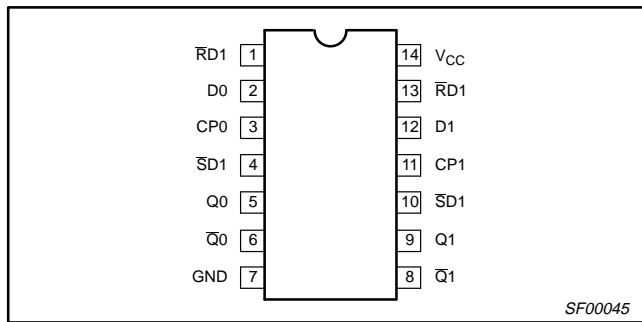
# Dual D-type flip-flop

# 74ABT74

## QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}\text{C};$ $\text{GND} = 0\text{V}$	TYPICAL	UNIT
$t_{PLH}$ $t_{PHL}$	Propagation delay CPn to Qn, $\bar{Q}$ n	$C_L = 50\text{pF};$ $V_{CC} = 5\text{V}$	3.0 2.5	ns
$t_{OSLH}$ $t_{OSHL}$	Output to Output skew		0.5	
$C_{IN}$	Input capacitance	$V_I = 0\text{V}$ or $V_{CC}$	3	pF
$I_{CC}$	Total supply current	Outputs disabled; $V_{CC} = 5.5\text{V}$	50	$\mu\text{A}$

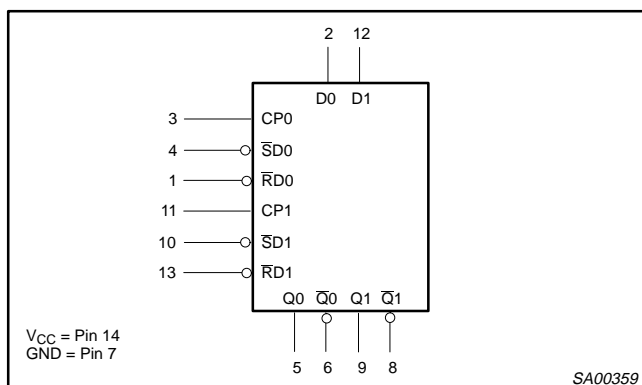
## PIN CONFIGURATION



## PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 2, 3, 4, 10, 11, 12, 13	$\bar{R}D_n, D_n, CP_n, \bar{S}D_n$	Data inputs
5, 6, 8, 9	$Q_n, \bar{Q}_n$	Data outputs
7	GND	Ground (0V)
14	$V_{CC}$	Positive supply voltage

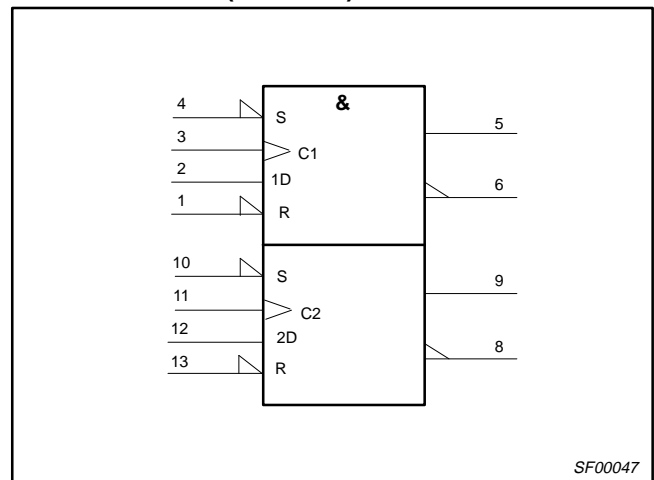
## LOGIC SYMBOL



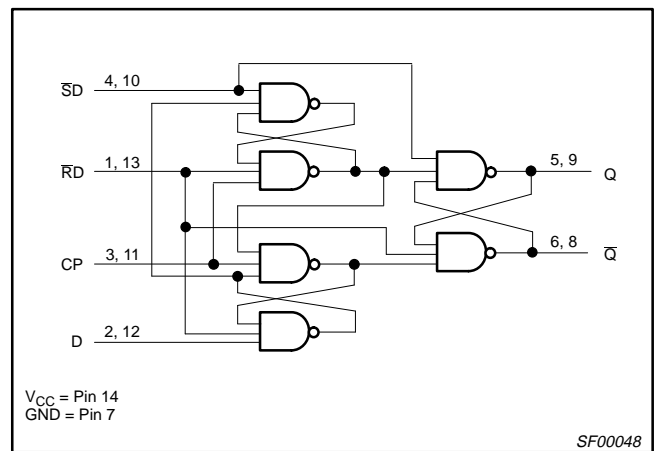
## DESCRIPTION

The 74ABT74 is a dual positive edge-triggered D-type flip-flop featuring individual data, clock, set, and reset inputs; also true and complementary outputs. Set ( $\bar{S}D$ ) and reset ( $\bar{R}D$ ) are asynchronous active low inputs and operate independently of the clock input. When set and reset are inactive (high), data at the D input is transferred to the Q and  $\bar{Q}$  outputs on the low-to-high transition of the clock. Data must be stable just one setup time prior to the low-to-high transition of the clock for predictable operation. Clock triggering occurs at a voltage level and is not directly related to the transition time of the positive-going pulse. Following the hold time interval, data at the D input may be changed without affecting the levels of the output.

## LOGIC SYMBOL (IEEE/IEC)



## LOGIC DIAGRAM



## ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
14-Pin Plastic DIP	-40°C to +85°C	74ABT74 N	74ABT74 N	SOT27-1
14-Pin plastic SO	-40°C to +85°C	74ABT74 D	74ABT74 D	SOT108-1
14-Pin Plastic SSOP Type II	-40°C to +85°C	74ABT74 DB	74ABT74 DB	SOT337-1
14-Pin Plastic TSSOP Type I	-40°C to +85°C	74ABT74 PW	74ABT74PW DH	SOT402-1

## Dual D-type flip-flop

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## FUNCTION TABLE

INPUTS				OUTPUTS		OPERATING MODE
$\overline{SD}$	$\overline{RD}$	CP	D	Q	$\overline{Q}$	
L	H	X	X	H	L	Asynchronous set
H	L	X	X	L	H	Asynchronous reset
L	L	X	X	H	H	Undetermined*
H	H	$\uparrow$	h	H	L	Load "1"
H	H	$\uparrow$	l	L	H	Load "0"
H	H	$\updownarrow$	X	NC	NC	Hold

## NOTES:

H = High voltage level

h = High voltage level one setup time prior to low-to-high clock transition

L = Low voltage level

l = Low voltage level one setup time prior to low-to-high clock transition

NC= No change from the previous setup

X = Don't care

 $\uparrow$  = Low-to-high clock transition $\updownarrow$  = Not low-to-high clock transition

\* = This setup is unstable and will change when either set or reset return to the high level.

ABSOLUTE MAXIMUM RATINGS<sup>1, 2</sup>

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
$V_{CC}$	DC supply voltage		-0.5 to +7.0	V
$I_{IK}$	DC input diode current	$V_I < 0$	-18	mA
$V_I$	DC input voltage <sup>3</sup>		-1.2 to +7.0	V
$I_{OK}$	DC output diode current	$V_O < 0$	-50	mA
$V_{OUT}$	DC output voltage <sup>3</sup>	output in Off or High state	-0.5 to +5.5	V
$I_{OUT}$	DC output current	output in Low state	40	mA
$T_{stg}$	Storage temperature range		-65 to 150	°C

## NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
$V_{CC}$	DC supply voltage	4.5	5.5	V
$V_I$	Input voltage	0	$V_{CC}$	V
$V_{IH}$	High-level input voltage	2.0		V
$V_{IL}$	Low-level input voltage		0.8	V
$I_{OH}$	High-level output current		-15	mA
$I_{OL}$	Low-level output current		20	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
$T_{amb}$	Operating free-air temperature range	-40	+85	°C

## Dual D-type flip-flop

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## DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T <sub>amb</sub> = +25°C			T <sub>amb</sub> = -40°C to +85°C		
			MIN	TYP	MAX	MIN	MAX	
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = 4.5V; I <sub>IK</sub> = -18mA		-0.9	-1.2		-1.2	V
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = 4.5V; I <sub>OH</sub> = -15mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>	2.5	2.9		2.5		V
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = 4.5V; I <sub>OL</sub> = 20mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>		0.35	0.5		0.5	V
I <sub>I</sub>	Input leakage current	V <sub>CC</sub> = 5.5V; V <sub>I</sub> = GND or 5.5V		±0.01	±1.0		±1.0	µA
I <sub>OFF</sub>	Power-off leakage current	V <sub>CC</sub> = 0.0V; V <sub>O</sub> or V <sub>I</sub> ≤ 4.5V		±5.0	±100		±100	µA
I <sub>CEX</sub>	Output High leakage current	V <sub>CC</sub> = 5.5V; V <sub>O</sub> = 5.5V; V <sub>I</sub> = GND or V <sub>CC</sub>		5.0	50		50	µA
I <sub>O</sub>	Output current <sup>1</sup>	V <sub>CC</sub> = 5.5V; V <sub>O</sub> = 2.5V	-50	-75	-180	-50	-180	mA
I <sub>CC</sub>	Quiescent supply current	V <sub>CC</sub> = 5.5V; V <sub>I</sub> = GND or V <sub>CC</sub>		2	50		50	µA
ΔI <sub>CC</sub>	Additional supply current per input pin <sup>2</sup>	V <sub>CC</sub> = 5.5V; One data input at 3.4V, other inputs at V <sub>CC</sub> or GND		0.25	500		500	µA

## NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- This is the increase in supply current for each input at 3.4V.
- For valid test results, data must not be loaded into the flip-flop or latch after applying the power.

## AC ELECTRICAL CHARACTERISTICS

GND = 0V; t<sub>R</sub> = t<sub>F</sub> = 2.5ns; C<sub>L</sub> = 50pF, R<sub>L</sub> = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T <sub>amb</sub> = +25°C V <sub>CC</sub> = +5.0V			T <sub>amb</sub> = -40°C to +85°C V <sub>CC</sub> = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
f <sub>MAX</sub>	Maximum clock frequency	1	180	250		150		MHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay CPn to Qn, Q̄n	1	1.0 1.0	3.0 2.5	4.2 3.5	1.0 1.0	4.7 4.0	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay Sn, Rn to Qn, Q̄n	3	1.0 1.0	3.4 2.9	4.9 4.5	1.0 1.0	6.2 5.2	ns
t <sub>OSHL</sub> t <sub>OSLH</sub> <sup>1</sup>	Output to Output skew An or Bn to Ȳn	4		0.5	0.6		0.6	ns

## NOTE:

- Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the the same direction, either HIGH-to-LOW (t<sub>OSHL</sub>) or LOW-to-HIGH (t<sub>OSLH</sub>); parameter guaranteed by design.

## AC SETUP REQUIREMENTS

GND = 0V; t<sub>R</sub> = t<sub>F</sub> = 2.5ns; C<sub>L</sub> = 50pF, R<sub>L</sub> = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			T <sub>amb</sub> = +25°C V <sub>CC</sub> = +5.0V		T <sub>amb</sub> = -40°C to +85°C V <sub>CC</sub> = +5.0V ±0.5V		
			MIN	TYP	MIN		
t <sub>SU</sub> (H) t <sub>SU</sub> (L)	Setup time, high or low Dn to CPn	1	2.6 2.4	1.4 1.4	2.6 2.4		ns
t <sub>H</sub> (H) t <sub>H</sub> (L)	Hold time, high or low Dn to CPn	1	0 0	-1.4 -1.4	0 0		ns
t <sub>W</sub> (H) t <sub>W</sub> (L)	CPn pulse width, high or low	1	1.7 1.7	1.0 1.0	2.1 2.1		ns
t <sub>W</sub> (L)	SDn, RDn pulse width, low	3	2.0	1.3	2.2		ns
t <sub>rec</sub>	Recovery time SDn, RDn to CPn	2	2.1	1.4	2.4		ns

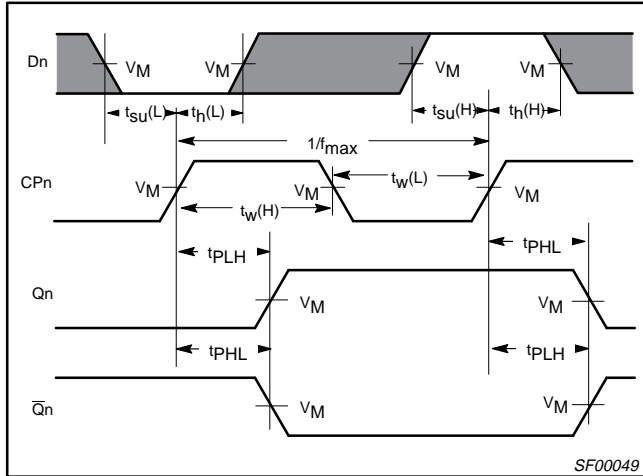
# Dual D-type flip-flop

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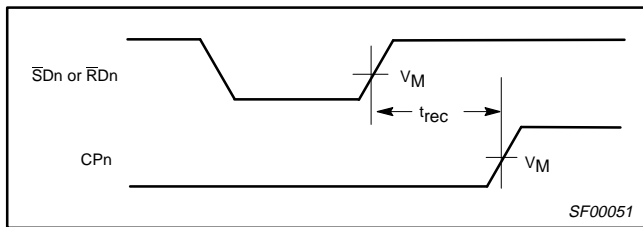
## AC WAVEFORMS

$V_M = 1.5V$ ,  $V_{IN} = GND$  to  $3.0V$

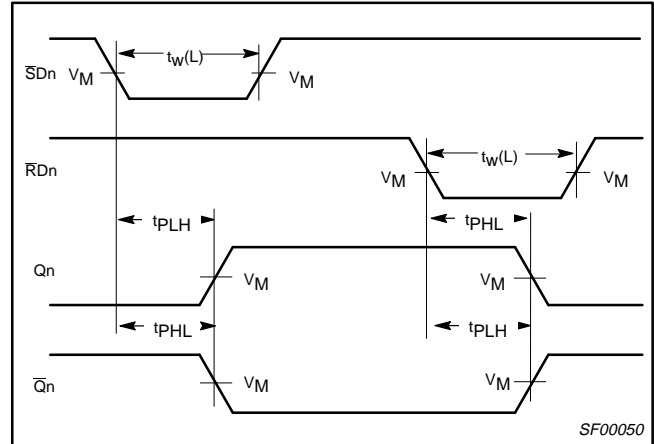
The shaded areas indicate when the input is permitted to change for predictable output performance



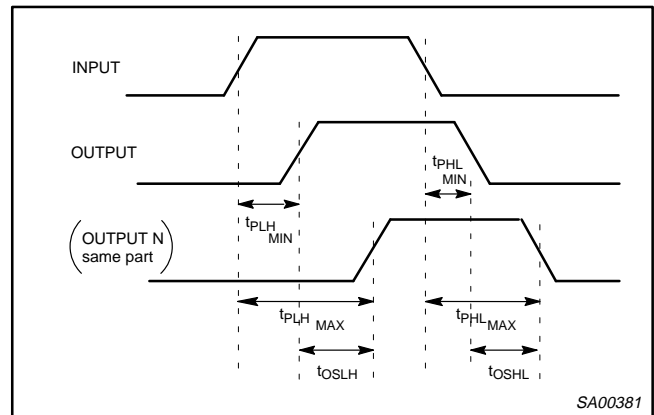
**Waveform 1. Propagation delay for data to output, data setup time and hold times, and clock width, and maximum clock frequency**



**Waveform 2. Recovery time for set or reset to clock**



**Waveform 3. Propagation delay for set and reset to output, set and reset pulse width**

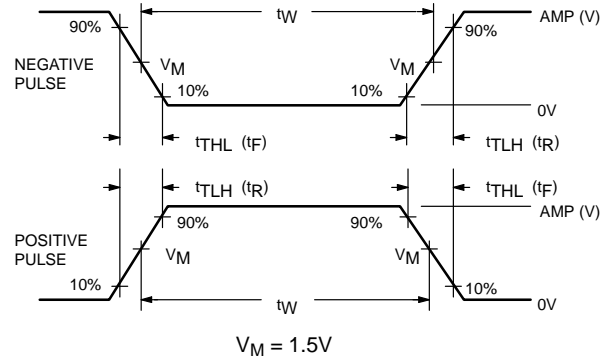
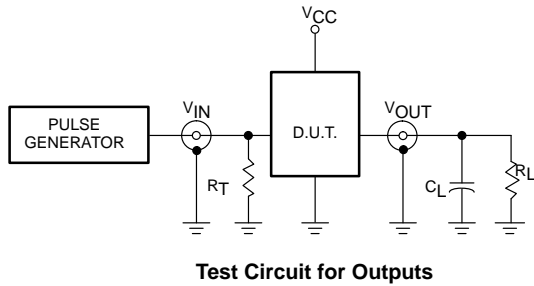


**Waveform 4. Common edge skew**

# Dual D-type flip-flop

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## TEST CIRCUIT AND WAVEFORMS



### DEFINITIONS

- $R_L$  = Load resistor; see AC CHARACTERISTICS for value.
- $C_L$  = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

### Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	$t_W$	$t_R$	$t_F$
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

SH00067



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