LC²MOS Complete, 12-Bit, 100 kHz, Sampling ADCs

AD7870/AD7875/AD7876

FEATURES

Complete monolithic 12-bit ADCs with
- **2 µs track-and-hold amplifier**
- **8 µs ADC**
- **On-chip reference**
- **Laser-trimmed clock**
- **Parallel, byte, and serial digital interface**

72 dB SNR at 10 kHz input frequency (AD7870, AD7875)
57 ns data access time
Low power: –60 mW typical
Variety of input ranges
- **±3 V for AD7870**
- **0 V to +5 V for AD7875**
- **±10 V for AD7876**

FUNCTIONAL BLOCK DIAGRAM

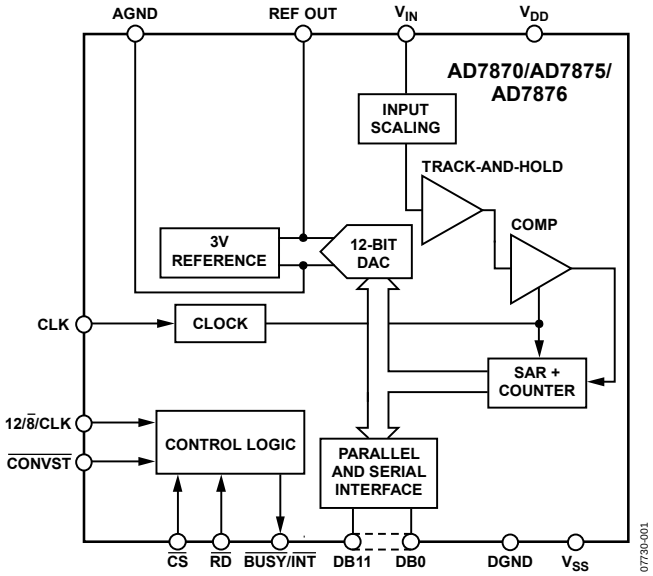

Figure 1.

GENERAL DESCRIPTION

The AD7870/AD7875/AD7876 are fast, complete, 12-bit analog-to-digital converters (ADCs). These converters consist of a track-and-hold amplifier, an 8 µs successive approximation ADC, a 3 V buried Zener reference, and versatile interface logic. The ADCs feature a self-contained internal clock which is laser trimmed to guarantee accurate control of conversion time. No external clock timing components are required; the on-chip clock may be overridden by an external clock if required.

The parts offer a choice of three data output formats: a single, parallel, 12-bit word; two 8-bit bytes or serial data. Fast bus access times and standard control inputs ensure easy interfacing to modern microprocessors and digital signal processors.

All parts operate from ±5 V power supplies. The AD7870 and AD7876 accept input signal ranges of ±3 V and ±10 V, respectively, while the AD7875 accepts a unipolar 0 V to +5 V input range. The parts can convert full power signals up to 50 kHz.

The AD7870/AD7875/AD7876 feature dc accuracy specifications, such as linearity, full-scale and offset error. In addition, the AD7870 and AD7875 are fully specified for dynamic performance parameters including distortion and signal-to-noise ratio.

The parts are available in a 24-pin, 0.3 inch-wide, plastic or hermetic dual-in-line package (DIP). The AD7870 and AD7875 are available in a 28-pin plastic leaded chip carrier (PLCC), while the AD7876 is available and in a 24-pin small outline (SOIC) package.

PRODUCT HIGHLIGHTS

1. Complete 12-bit ADC on a chip.
   The AD7870/AD7875/AD7876 provide all the functions necessary for analog-to-digital conversion and combine a 12-bit ADC with internal clock, track-and-hold amplifier and reference on a single chip.
2. Dynamic specifications for DSP users.
   The AD7870 and AD7875 are fully specified and tested for ac parameters, including signal-to-noise ratio, harmonic distortion and intermodulation distortion.
3. Fast microprocessor interface.
   Data access times of 57 ns make the parts compatible with modern 8-bit and 16-bit microprocessors and digital signal processors. Key digital timing parameters are tested and guaranteed over the full operating temperature range.

Rev. C
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REVISION HISTORY

2/09—Rev. B to Rev. C

Updated Format ... Universal
Reorganized Layout ... Universal
Deleted S Version ... Universal
Changes to Internal Clock Parameter, Table 1 and Added Endnote to Table 1 ... 4
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SPECIFICATIONS

V_{DD} = +5 V ± 5%, V_{SS} = −5 V ± 5%, AGND = DGND = 0 V, f_{CLK} = 2.5 MHz external, unless otherwise stated. All Specifications T_{min} to T_{max}, unless otherwise noted.

AD7870 SPECIFICATIONS

Table 1.

Parameter	ADN7870[1] J, A	K, B	L, C	T	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE[2]						
Signal-to-Noise Ratio[3] (SNR)						
@ +25°C	70	70	72	69	dB min	V_{IN} = 10 kHz sine wave, f_{SAMPLE} = 100 kHz
T_{MIN} to T_{MAX}	70	70	71	69	dB min	Typically 71.5 dB for 0 < V_{IN} < 50 kHz
Total Harmonic Distortion (THD)	−80	−80	−80	−78	dB max	V_{IN} = 10 kHz sine wave, f_{SAMPLE} = 100 kHz Typically −86 dB for 0 < V_{IN} < 50 kHz
Peak Harmonic or Spurious Noise	−80	−80	−80	−78	dB max	V_{IN} = 10 kHz, f_{SAMPLE} = 100 kHz Typically −86 dB for 0 < V_{IN} < 50 kHz
Intermodulation Distortion (IMD)						
Second Order Terms	−80	−80	−80	−78	dB max	fa = 9 kHz, fb = 9.5 kHz, f_{SAMPLE} = 50 kHz
Third Order Terms	−80	−80	−80	−78	dB max	fa = 9 kHz, fb = 9.5 kHz, f_{SAMPLE} = 50 kHz
Track-and-Hold Acquisition Time	2	2	2	2	µs max	
DC ACCURACY						
Resolution	12	12	12	12	Bits	
Minimum Resolution for which No Missing Codes are Guaranteed	12	12	12	12	Bits	
Integral Nonlinearity	±1/2	±1/2	±1/4	±1/2	LSB typ	
Integral Nonlinearity		±1	±1/2	±1	LSB max	
Differential Nonlinearity		±1	±1	±1	LSB max	
Bipolar Zero Error	±5	±5	±5	±5	LSB max	
Positive Full-Scale Error[4]	±5	±5	±5	±5	LSB max	
Negative Full-Scale Error[4]	±5	±5	±5	±5	LSB max	
ANALOG INPUT						
Input Voltage Range	±3	±3	±3	±3	V	
Input Current	±500	±500	±500	±500	µA max	
REFERENCE OUTPUT						
REF OUT @ +25°C	2.99	2.99	2.99	2.99	V min	
	3.01	3.01	3.01	3.01	V max	
REF OUT Tempco	±60	±60	±35	±35	ppm/°C max	
Reference Load Sensitivity (ΔREF OUT/ΔI)	±1	±1	±1	±1	mV max	Reference load current change (0 µA to 500 µA). Reference load should not be changed during conversion.
LOGIC INPUTS						
Input High Voltage, V_{INH}	2.4	2.4	2.4	2.4	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	±10	±10	µA max	V_{IN} = 0 V to V_{DD}
Input Current (12/$\overline{8}$/CLK Input Only)	±10	±10	±10	±10	µA max	V_{IN} = V_{SS} to V_{DD}
Input Capacitance, C_{IN}[5]	10	10	10	10	pF max	
LOGIC OUTPUTS						
Output High Voltage, V_{OH}	4.0	4.0	4.0	4.0	V min	I_{SOURCE} = 40 µA
Output Low Voltage, V_{OL}	0.4	0.4	0.4	0.4	V max	I_{SINK} = 1.6 mA
DB11 to DB0						
Floating-State Leakage Current	±10	±10	±10	±10	µA max	
Floating-State Output Capacitance[5]	15	15	15	15	pF max	

Parameter	ADN7870[1] J, A	K, B	L, C	T	Units	Test Conditions/Comments
CONVERSION TIME						
External Clock (f_{CLK} = 2.5 MHz)	8	8	8	8	µs max	
Internal Clock[6]	6.5/9	6.5/9	6.5/9	6.5/9	µs min/ µs max	
POWER REQUIREMENTS						
V_{DD}	+5	+5	+5	+5	V nom	±5% for specified performance
V_{SS}	−5	−5	−5	−5	V nom	±5% for specified performance
I_{DD}	13	13	13	13	mA max	Typically 8 mA
I_{SS}	6	6	6	6	mA max	Typically 4 mA
Power Dissipation	95	95	95	95	mW max	Typically 60 mW

[1] The temperature range for the J, K, and L versions is from 0°C to +70°C; for the A, B, and C versions is−40°C to +85°C; and for the T version is −55°C to +125°C.
[2] V_{IN} (p-p) = ±3 V.
[3] SNR calculation includes distortion and noise components.
[4] Measured with respect to internal reference and includes bipolar offset error.
[5] Sample tested @ +25°C to ensure compliance.
[6] Conversion time specification for the AD7870A device with internal clock used is 8 µs/10 µs minimum/maximum.

AD7875/AD7876 SPECIFICATIONS

Table 2.

Parameter	AD7875/AD7876[1] K, B	L, C	T	Units	Test Conditions/Comments
DC ACCURACY					
Resolution	12	12	12	Bits	
Min Resolution for which No Missing Codes Are Guaranteed	12	12	12	Bits	
Integral Nonlinearity @ +25°C	±1	±1/2	±1	LSB max	
T_{MIN} to T_{MAX} (AD7875 Only)	±1	±1	±1	LSB max	
T_{MIN} to T_{MAX} (AD7876 Only)	±1	±1/2	±1	LSB max	
Differential Nonlinearity	±1	±1	±1.5/−1.0	LSB max	
Unipolar Offset Error (AD7875 Only)	±5	±5	±5	LSB max	
Bipolar Zero Error (AD7876 Only)	±6	±2	±6	LSB max	
Full-Scale Error at +25°C[2]	±8	±8	±8	LSB max	Typical full-scale error is ±1 LSB
Full-Scale TC[2]	±60	±35	±60	ppm/°C max	Typical TC is ±20 ppm/°C
Track-and-Hold Acquisition Time	2	2	2	µs max	
DYNAMIC PERFORMANCE[3] (AD7875 ONLY)					
Signal-to-Noise Ratio[4] (SNR)					
@ +25°C	70	72	69	dB min	V_{IN} = 10 kHz sine wave, f_{SAMPLE} = 100 kHz
T_{MIN} to T_{MAX}	70	71	69	dB min	Typically 71.5 dB for 0 < V_{IN} < 50 kHz
Total Harmonic Distortion (THD)	−80	−80	−78	dB max	V_{IN} = 10 kHz sine wave, f_{SAMPLE} = 100 kHz Typically −86 dB for 0 < V_{IN} < 50 kHz
Peak Harmonic or Spurious Noise	−80	−80	−78	dB max	V_{IN} = 10 kHz, f_{SAMPLE} = 100 kHz Typically −86 dB for 0 < V_{IN} < 50 kHz
Intermodulation Distortion (IMD)					
Second Order Terms	−80	−80	−78	dB max	fa = 9 kHz, fb = 9.5 kHz, f_{SAMPLE} = 50 kHz
Third Order Terms	−80	−80	−78	dB max	fa = 9 kHz, fb = 9.5 kHz, f_{SAMPLE} = 50 kHz

Parameter	AD7875/AD7876[1] K, B	L, C	T	Units	Test Conditions/Comments
ANALOG INPUT					
AD7875 Input Voltage Range	0 to +5	0 to +5	0 to +5	V	
AD7875 Input Current	500	500	500	µA max	
AD7876 Input Voltage Range	±10	±10	±10	V	
AD7876 Input Current	±600	±600	±600	µA max	
REFERENCE OUTPUT					
REF OUT @ +25°C	2.99	2.99	2.99	V min	
	3.01	3.01	3.01	V max	
REF OUT Tempco	±60	±35	±60	ppm/°C max	Typical tempco Is ±20 ppm/°C
Reference Load Sensitivity (ΔREF OUT/ΔI)	−1	−1	−1	mV max	Reference load current change (0 µA to 500 µA). Reference load should not be changed during conversion.
LOGIC INPUTS					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	±10	µA max	V_{IN} = 0 V to V_{DD}
Input Current (12/$\overline{8}$/CLK Input Only)	±10	±10	±10	µA max	V_{IN} = V_{SS} to V_{DD}
Input Capacitance, C_{IN}[5]	10	10	10	pF max	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	4.0	4.0	4.0	V min	I_{SOURCE} = 40 mA
Output Low Voltage, V_{OL}	0.4	0.4	0.4	V max	I_{SINK} = 1.6 mA
DB11–DB0					
Floating-State Leakage Current	10	10	10	µA max	
Floating-State Output Capacitance[5]	15	15	15	pF max	
CONVERSION TIME					
External Clock (f_{CLK} = 2.5 MHz)	8	8	8	µs max	
Internal Clock	6.5/9	6.5/9	6.5/9	µs min/µs max	
POWER REQUIREMENTS	As per AD7870				Refer to the power requirements in Table 1.

[1] For the AD7875, the temperature range for the K and L versions is from 0°C to +70°C; for the B and C versions is–40°C to +85°C; and for the T version is –55°C to +125°C. For the AD7876, the temperature range for the B and C versions is from –40°C to +85°C and for the T version is–55°C to +125°C.
[2] Includes internal reference error and is calculated after unipolar offset error (AD7875) or bipolar zero error (AD7876) has been adjusted out. Full-scale error refers to both positive and negative full-scale error for the AD7876.
[3] Dynamic performance parameters are not tested on the AD7876, but these are typically the same as for the AD7875.
[4] SNR calculation includes distortion and noise components.
[5] Sample tested @ +25°C to ensure compliance.

TIMING CHARACTERISTICS

V_{DD} = +5 V ± 5%, V_{SS} = −5 V ± 5%, AGND = DGND = 0 V. See Figure 14, Figure 15, Figure 16, and Figure 17. Timing specifications are sample tested at 25°C to ensure compliance, unless otherwise noted. All input signals are specified with $t_r = t_f$ = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

Table 3.

Parameter[1]	Limit at T_{MIN}, T_{MAX} (J, K, L, A, B, C Versions)	Limit at T_{MIN}, T_{MAX} (T Version)	Units	Conditions/Comments
t_1	50	50	ns min	$\overline{CONVST}$ pulse width
t_2	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ setup time (Mode 1)
t_3[2]	60	75	ns min	$\overline{RD}$ pulse width
t_4	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ hold time (Mode 1)
t_5	70	70	ns max	$\overline{RD}$ to $\overline{INT}$ delay
t_6[2, 3]	57	70	ns max	Data access time after $\overline{RD}$
t_7[2, 4]	5	5	ns min	Bus relinquish time after $\overline{RD}$
	50	50	ns max	
t_8	0	0	ns min	HBEN to $\overline{RD}$ setup time
t_9	0	0	ns min	HBEN to $\overline{RD}$ hold time
t_{10}	100	100	ns min	$\overline{SSTRB}$ to SCLK falling edge setup time
t_{11}[5]	370	370	ns min	SCLK cycle time
t_{12}[6]	135	150	ns max	SCLK to valid data delay. C_L = 35 pF
t_{13}	20	20	ns min	SCLK rising edge to $\overline{SSTRB}$
	100	100	ns max	
t_{14}	10	10	ns min	Bus relinquish time after SCLK
	100	100	ns max	
t_{15}	60	60	ns min	$\overline{CS}$ to $\overline{RD}$ setup time (Mode 2)
t_{16}	120	120	ns max	$\overline{CS}$ to $\overline{BUSY}$ propagation delay
t_{17}	200	200	ns min	Data setup time prior to $\overline{BUSY}$
t_{18}	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ hold time (Mode 2)
t_{19}	0	0	ns min	HBEN to $\overline{CS}$ setup time
t_{20}	0	0	ns min	HBEN to $\overline{CS}$ hold time

[1] Serial timing is measured with a 4.7 kΩ pull-up resistor on SDATA and $\overline{SSTRB}$ and a 2 kΩ pull-up on SCLK. The capacitance on all three outputs is 35 pF.
[2] Timing specifications for t_3, t_6, and for the maximum limit at t_7 are 100% production tested.
[3] t_6 is measured with the load circuits of Figure 4 and defined as the time required for an output to cross 0.8 V or 2.4 V.
[4] t_7 is defined as the time required for the data lines to change 0.5 V when loaded with the circuits of Figure 5.
[5] SCLK mark/space ratio (measured from a voltage level of 1.6 V) is 40/60 to 60/40.
[6] SDATA will drive higher capacitive loads but this will add to t_{12} since it increases the external RC time constant (4.7 kΩ||C_L) and thus the time to reach 2.4 V.

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
V_{DD} to AGND	−0.3 V to +7 V
V_{SS} to AGND	+0.3 V to −7 V
AGND to DGND	−0.3 V to V_{DD} +0.3 V
V_{IN} to AGND	−15 V to +15 V
REF OUT to AGND	0 V to V_{DD}
Digital Inputs to DGND	−0.3 V to V_{DD} +0.3 V
Digital Outputs to DGND	−0.3 V to V_{DD} +0.3 V
Operating Temperature Range	
Commercial (J, K, L Versions–AD7870)	0°C to +70°C
Commercial (K, L Versions–AD7875)	0°C to +70°C
Industrial (A, B, C Versions–AD7870)	−25°C to +85°C
Industrial (B, C Versions–AD7875/AD7876)	−40°C to +85°C
Extended (T Version)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	+300°C
Power Dissipation (Any Package) to +75°C	450 mW
Derates above +75°C by	10 mW/°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

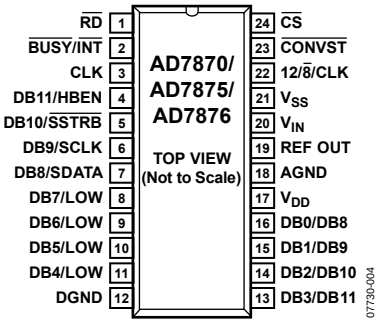


Figure 2. DIP and SOIC Pin Configuration

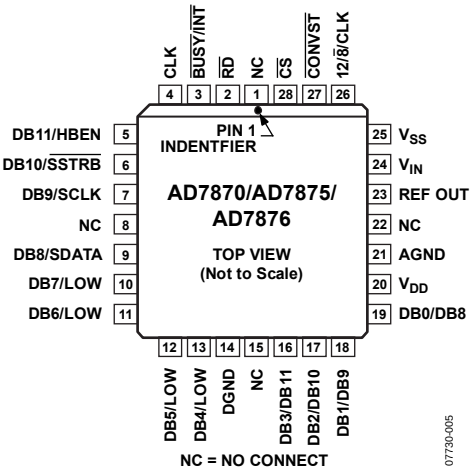


Figure 3. PLCC Pin Configuration

Table 5. Pin Function Descriptions

DIP and SOIC Pin No.	PLCC Pin No.	Mnemonic	Function
N/A	1, 8, 15, 22	NC	No Connect.
1	2	$\overline{RD}$	Read. Active low logic input. This input is used in conjunction with $\overline{CS}$ low to enable the data outputs.
2	3	$\overline{BUSY}/\overline{INT}$	Busy/Interrupt. Active low logic output indicating converter status. See Figure 14, Figure 15, Figure 16, and Figure 17.
3	4	CLK	Clock Input. An external TTL-compatible clock may be applied to this input pin. Alternatively, tying this pin to V_{SS} enables the internal laser-trimmed clock oscillator.
4	5	DB11/HBEN	Data Bit 11 (MSB)/High Byte Enable. The function of this pin is dependent on the state of the 12/$\overline{8}$/CLK input. When 12-bit parallel data is selected, this pin provides the DB11 output. When byte data is selected, this pin becomes the HBEN logic input. HBEN is used for 8-bit bus interfacing. When HBEN is low, DB7/LOW to DB0/DB8 become DB7 to DB0. With HBEN high, DB7/LOW to DB0/DB8 are used for the upper byte of data (see Table 6).
5	6	DB10/$\overline{SSTRB}$	Data Bit 10/Serial Strobe. When 12-bit parallel data is selected, this pin provides the DB10 output. $\overline{SSTRB}$ is an active low open-drain output that provides a strobe or framing pulse for serial data. An external 4.7 kΩ pull-up resistor is required on $\overline{SSTRB}$.
6	7	DB9/SCLK	Data Bit 9/Serial Clock. When 12-bit parallel data is selected, this pin provides the DB9 output. SCLK is the gated serial clock output derived from the internal or external ADC clock. If the 12/$\overline{8}$/CLK input is at −5 V, then SCLK runs continuously. If 12/$\overline{8}$/CLK is at 0 V, then SCLK is gated off after serial transmission is complete. SCLK is an open-drain output and requires an external 2 kΩ pull-up resistor.
7	9	DB8/SDATA	Data Bit 8/Serial Data. When 12-bit parallel data is selected, this pin provides the DB8 output. SDATA is an open-drain serial data output which is used with SCLK and $\overline{SSTRB}$ for serial data transfer. Serial data is valid on the falling edge of SCLK while $\overline{SSTRB}$ is low. An external 4.7 kΩ pull-up resistor is required on SDATA.
8 to11	10 to 13	DB7/LOW–DB4/LOW	Three-state data outputs controlled by $\overline{CS}$ and $\overline{RD}$. Their function depends on the 12/$\overline{8}$/CLK and HBEN inputs. With 12/$\overline{8}$/CLK high, they are always DB7–DB4. With 12/$\overline{8}$/CLK low or −5 V, their function is controlled by HBEN (see Table 6).
12	14	DGND	Digital Ground. Ground reference for digital circuitry.
13 to 16	16 to 19	DB3/DB11–DB0/DB8	Three-state data outputs which are controlled by $\overline{CS}$ and $\overline{RD}$. Their function depends on the 12/$\overline{8}$/CLK and HBEN inputs. With 12/$\overline{8}$/CLK high, they are always DB3–DB0. With 12/$\overline{8}$/CLK low or −5 V, their function is controlled by HBEN (see Table 6).
17	20	V_{DD}	Positive Supply, +5 V ± 5%.

DIP and SOIC Pin No.	PLCC Pin No.	Mnemonic	Function
18	21	AGND	Analog Ground. Ground reference for track-and-hold, reference and DAC.
19	23	REF OUT	Voltage Reference Output. The internal 3 V reference is provided at this pin. The external load capability is 500 µA.
20	24	V_{IN}	Analog Input. The analog input range is ±3 V for the AD7870, ±10 V for the AD7876, and 0 V to +5 V for the AD7875.
21	25	V_{SS}	Negative Supply, −5 V ± 5%.
22	26	12/$\overline{8}$/CLK	Three Function Input. Defines the data format and serial clock format. With this pin at +5 V, the output data for-mat is 12-bit parallel only. With this pin at 0 V, either byte or serial data is available and SCLK is not continuous. With this pin at −5 V, either byte or serial data is again available but SCLK is now continuous.
23	27	$\overline{\text{CONVST}}$	Convert Start. A low to high transition on this input puts the track-and-hold into its hold mode and starts conversion. This input is asynchronous to the CLK input.
24	28	$\overline{\text{CS}}$	Chip Select. Active low logic input. The device is selected when this input is active. With $\overline{\text{CONVST}}$ tied low, a new conversion is initiated when $\overline{\text{CS}}$ goes low.

Table 6. Output Data for Byte Interfacing

HBEN	DB7/Low	DB6/Low	DB5/Low	DB4/Low	DB3/DB11	DB2/DB10	DB1/DB9	DB0/DB8
High	Low	Low	Low	Low	DB11(MSB)	DB10	DB9	DB8
Low	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0 (LSB)

LOAD CIRCUITS

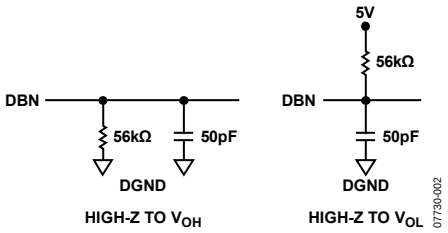


Figure 4. Load Circuits for Access Time

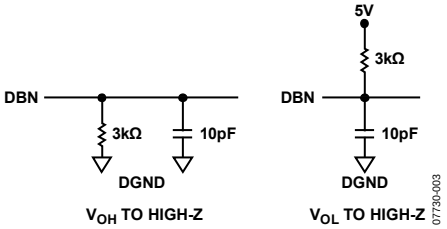


Figure 5. Load Circuits for Output Float Delay

CONVERTER DETAILS

The AD7870/AD7875/AD7876 is a complete 12-bit ADC, requiring no external components apart from power supply decoupling capacitors. It is comprised of a 12-bit successive approximation ADC based on a fast settling voltage output DAC, a high speed comparator and SAR, a track-and-hold amplifier, a 3 V buried Zener reference, a clock oscillator, and control logic.

INTERNAL REFERENCE

The AD7870/AD7875/AD7876 have on-chip temperature compensated buried Zener reference that is factory trimmed to 3 V ± 10 mV. Internally it provides both the DAC reference and the dc bias required for bipolar operation (AD7870 and AD7876). The reference output is available (REF OUT) and capable of providing up to 500 μA to an external load.

The maximum recommended capacitance on REF OUT for normal operation is 50 pF. If the reference is required for use external to the ADC, it should be decoupled with a 200 Ω resistor in series with a parallel combination of a 10 μF tantalum capacitor and a 0.1 μF ceramic capacitor. These decoupling components are required to remove voltage spikes caused by the ADC's internal operation.

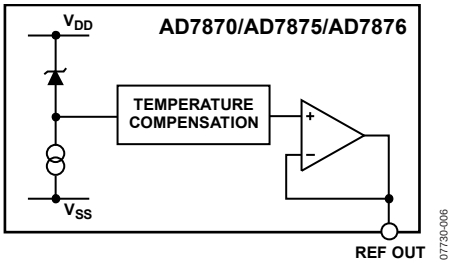


Figure 6. Reference Circuit

The reference output voltage is 3 V. For applications using the AD7875 or AD7876, a 5 V or 10 V reference may be required. Figure 7 shows how to scale the 3 V REF OUT voltage to provide either a 5 V or 10 V external reference.

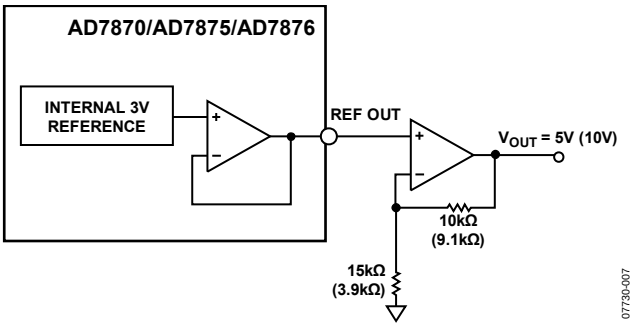


Figure 7. Generating a 5 V or 10 V Reference

TRACK-AND-HOLD AMPLIFIER

The track-and-hold amplifier on the analog input of the AD7870/AD7875/AD7876 allows the ADC to accurately convert input frequencies to 12-bit accuracy. The input bandwidth of the track-and-hold amplifier is much greater than the Nyquist rate of the ADC even when the ADC is operated at its maximum throughput rate. The 0.1 dB cutoff frequency occurs typically at 500 kHz. The track-and-hold amplifier acquires an input signal to 12-bit accuracy in less than 2 μs. The overall throughput rate is equal to the conversion time plus the track-and-hold amplifier acquisition time. For a 2.5 MHz input clock the throughput rate is 10 μs max.

The operation of the track-and-hold is essentially transparent to the user. The track-and-hold amplifier goes from its tracking mode to its hold mode at the start of conversion.

If the $\overline{\text{CONVST}}$ input is used to start conversion then the track to hold transition occurs on the rising edge of $\overline{\text{CONVST}}$. If $\overline{\text{CS}}$ starts conversion, this transition occurs on the falling edge of $\overline{\text{CS}}$.

ANALOG INPUT

The three parts differ from each other in the analog input voltage range that they can handle. The AD7870 accepts ±3 V input signals, the AD7876 accepts a ±10 V input range, while the input range for the AD7875 is 0 V to +5 V.

Figure 8 shows the AD7870 analog input. The analog input range is ±3 V into an input resistance of typically 15 kΩ. The designed code transitions occur midway between successive integer LSB values (that is, 1/2 LSB, 3/2 LSBs, 5/2 LSBs . . . FS–3/2 LSBs). The output code is twos complement binary with 1 LSB = FS/4096 = 6 V/4096 = 1.46 mV. The ideal input/output transfer function is shown in Figure 11.

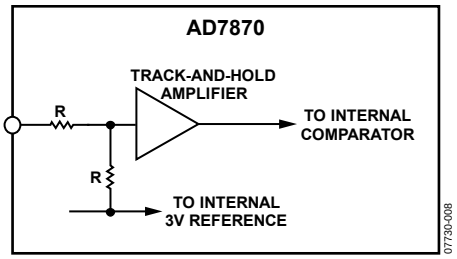


Figure 8. AD7970 Analog Input

The AD7876 analog input structure is shown in Figure 9. The analog input range is ±10 V into an input resistance of typically 33 kΩ. As before, the designed code transitions occur midway between successive integer LSB values. The output code is twos complement with 1 LSB = FS/4096 = 20 V/4096 = 4.88 mV. The ideal input/output transfer function is shown in Figure 11.

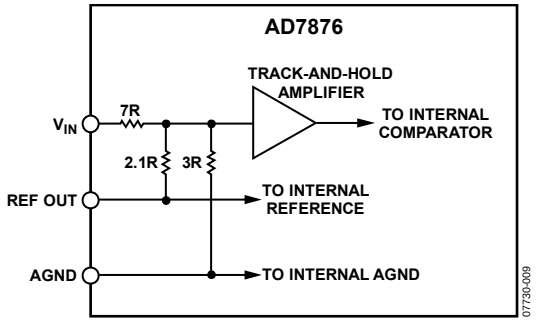


Figure 9. AD7876 Analog Input

Figure 10 shows the analog input for the AD7875. The input range is 0 V to +5 V into an input resistance of typically 25 kΩ. Once again, the designed code transitions occur midway between successive integer LSB values. The output code is straight binary with 1 LSB = FS/4096 = 5 V/4096 = 1.22 mV. The ideal input/output transfer function is shown in Figure 12.

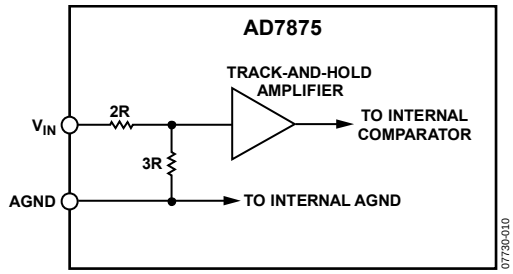


Figure 10. AD7875 Analog Input

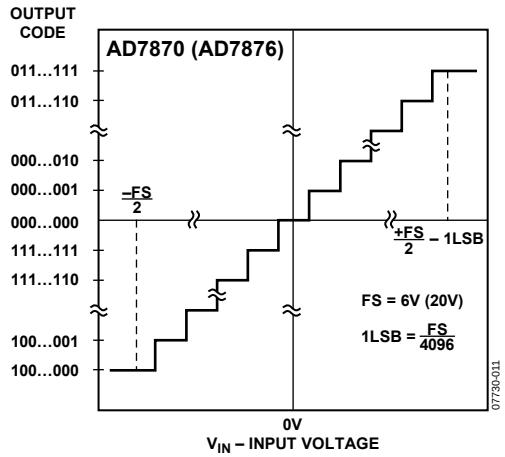


Figure 11. AD7870/AD7876 Transfer Function

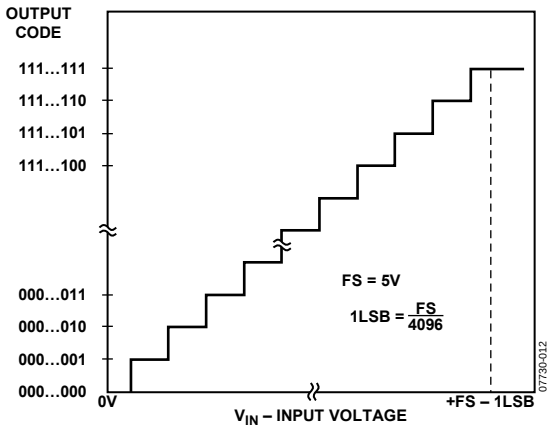


Figure 12. AD7875 Transfer Function

OFFSET AND FULL-SCALE ADJUSTMENT—AD7870

In most digital signal processing (DSP) applications, offset and full-scale errors have little or no effect on system performance. Offset error can always be eliminated in the analog domain by ac coupling. Full-scale error effect is linear and does not cause problems as long as the input signal is within the full dynamic range of the ADC. Some applications will require that the input signal span the full analog input dynamic range. In such applications, offset and full-scale error have to be adjusted to zero.

Where adjustment is required, offset error must be adjusted before full-scale error. This is achieved by trimming the offset of the op amp driving the analog input of the AD7870 while the input voltage is 1/2 LSB below ground. The trim procedure is as follows: apply a voltage of −0.73 mV(−1/2 LSB) at V_1 in Figure 13 and adjust the op amp offset voltage until the ADC output code flickers between 1111 1111 1111 and 0000 0000 0000. Gain error can be adjusted at either the first code transition (ADC negative full-scale) or the last code transition (ADC positive full scale). The trim procedures for both cases are as follows (see Figure 13).

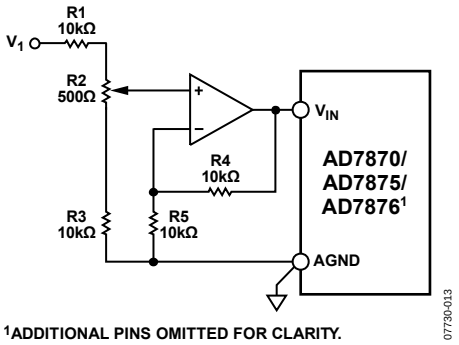


Figure 13. Offset and Full-Scale Adjust Circuit

Positive Full-Scale Adjust

Apply a voltage of 2.9978 V (FS/2 − 3/2 LSBs) at V_1. Adjust R2 until the ADC output code flickers between 0111 1111 1110 and 0111 1111 1111.

Negative Full-Scale Adjust

Apply a voltage of −2.9993 V (−FS/2 + 1/2 LSB) at V_1 and adjust R2 until the ADC output code flickers between 1000 0000 0000 and 1000 0000 0001.

OFFSET AND FULL-SCALE ADJUSTMENT—AD7876

The offset and full-scale adjustment for the AD7876 is similar to that just outlined for the AD7870. The trim procedure, for those applications that do require adjustment, is as follows: apply a voltage of −2.44 mV (−1/2 LSB) at V_1 and adjust the op amp offset voltage until the ADC output code flickers between 1111 1111 1111 and 0000 0000 0000. Full-scale error can be adjusted at either the first code transition (ADC negative full scale) or the last code transition (ADC positive full scale). The trim procedure for both case is as described in the following sections (see Figure 13).

Positive Full-Scale Adjust

Apply a voltage of 9.9927 V (FS/2 − 3/2 LSBs) at V_1. Adjust R2 until the ADC output code flickers between 0111 1111 1110 and 0111 1111 1111.

Negative Full-Scale Adjust

Apply a voltage of −9.9976 V (FS/2 + 1/2 LSB) at V_1 and adjust R2 until the ADC output code flickers between 1000 0000 0000 and 1000 0000 0001.

OFFSET AND FULL-SCALE ADJUSTMENT—AD7875

Similar to the AD7870, most of the DSP applications in which the AD7875 is used do not require offset and full-scale adjustment. For applications that do require adjustment, offset error must be adjusted before full-scale (gain) error. This is achieved by applying an input voltage of 0.61 mV (1/2 LSB) to V_1 in Figure 13 and adjusting the op amp offset voltage until the ADC output code flickers between 0000 0000 0000 and 0000 0000 0001. For full-scale adjustment, apply an input voltage of 4.9982 V (FS − 3/2 LSBs) to V_1 and adjust R2 until the ADC output code flickers between 1111 1111 1110 and 1111 1111 1111.

TIMING AND CONTROL

The AD7870/AD7875/AD7876 is capable of two basic operating modes. In the first mode (Mode 1), the CONVST line is used to start conversion and drive the track-and-hold into its hold mode. At the end of conversion, the track-and-hold returns to its tracking mode. It is intended principally for digital signal processing and other applications where precise sampling in time is required. In these applications, it is important that the signal sampling occur at exactly equal intervals to minimize errors due to sampling uncertainty or jitter. For these cases, the CONVST line is driven by a timer or some precise clock source.

The second mode is achieved by hardwiring the CONVST line low. This mode (Mode 2) is intended for use in systems where the microprocessor has total control of the ADC, both initiating the conversion and reading the data. CS starts conversion and the microprocessor is normally driven into a WAIT state for the duration of conversion by BUSY/INT.

DATA OUTPUT FORMATS

In addition to the two operating modes, the AD7870/AD7875/AD7876 also offers a choice of three data output formats, one serial and two parallel. The parallel data formats are a single, 12-bit parallel word for 16-bit data buses and a two-byte format for 8-bit data buses. The data format is controlled by the 12/8/CLK input. A logic high on this pin selects the 12-bit parallel output format only. A logic low or −5 V applied to this pin allows the user access to either serial or byte formatted data. Three of the pins previously assigned to the four MSBs in parallel form are now used for serial communications while the fourth pin becomes a control input for the byte-formatted data. The three possible data output formats can be selected in either of the modes of operation.

Parallel Output Format

The two parallel formats available on the part are a 12-bit wide data word and a two-byte data word. In the first format, all 12 bits of data are available at the same time on DB11 (MSB) through DB0 (LSB). In the second, two reads are required to access the data. When this data format is selected, the DB11/HBEN pin assumes the HBEN function. HBEN selects which byte of data is to be read from the ADC. When HBEN is low, the lower eight bits of data are placed on the data bus during a read operation; with HBEN high, the upper four bits of the 12-bit word are placed on the data bus. These four bits are right justified and thereby occupy the lower nibble of data while the upper nibble contains four zeros.

Serial Output Format

Serial data is available on the AD7870/AD7875/AD7876 when the 12/8/CLK input is at 0 V or −5 V and in this case the DB10/SSTRB, DB9/SCLK and DB8/SDATA pins assume their serial functions. Serial data is available during conversion with a word length of 16 bits; four leading zeros, followed by the 12-bit conversion result starting with the MSB. The data is synchronized to the serial clock output (SCLK) and framed by the serial strobe (SSTRB). Data is clocked out on a low to high transition of the serial clock and is valid on the falling edge of this clock while the SSTRB output is low. SSTRB goes low within three clock cycles after CONVST, and the first serial data bit (the first leading zero) is valid on the first falling edge of SCLK. All three serial lines are open-drain outputs and require external pull-up resistors.

The serial clock out is derived from the ADC clock source, which may be internal or external. Normally, SCLK is required during the serial transmission only. In these cases, it can be shut down at the end of conversion to allow multiple ADCs to share a common serial bus. However, some serial systems (such as the TMS32020) require a serial clock that runs continuously. Both options are available on the AD7870/AD7875/AD7876 using the 12/8/CLK input. With this input at −5 V, the serial clock (SCLK) runs continuously; when 12/8/CLK is at 0 V, SCLK is turned off at the end of transmission.

MODE 1 INTERFACE

Conversion is initiated by a low going pulse on the CONVST input. The rising edge of this CONVST pulse starts conversion and drives the track-and-hold amplifier into its hold mode (AD7870/AD7875/AD7876). The falling edge of the CONVST pulse starts conversion and drives the track-and-hold amplifier into its hold mode (AD7870A). Conversion is not initiated if the CS is low. The BUSY/INT status output assumes its INT function in this mode. INT is normally high and goes low at the end of conversion. This INT line can be used to interrupt the microprocessor. A read operation to the ADC accesses the data and the INT line is reset high on the falling edge of CS and RD. The CONVST input must be high when CS and RD are brought low for the ADC to operate correctly in this mode. The CS or RD input should not be hardwired low in this mode. Data cannot be read from the part during conversion because the on-chip latches are disabled when conversion is in progress. In applications where precise sampling is not critical, the CONVST pulse can be generated from a microprocessor WR line OR-gated with a decoded address. In some applications, depending on power supply turn-on time, the AD7870/AD7875/AD7876 may perform a conversion on power-up. In this case, the INT line powers-up low and a dummy read to the AD7870/AD7875/AD7876 is required to reset the INT line before starting conversion.

Figure 18 shows the Mode 1 timing diagram for a 12-bit parallel data output format (12/8/CLK = +5 V). A read to the ADC at the end of conversion accesses all 12 bits of data at the same time. Serial data is not available for this data output format.

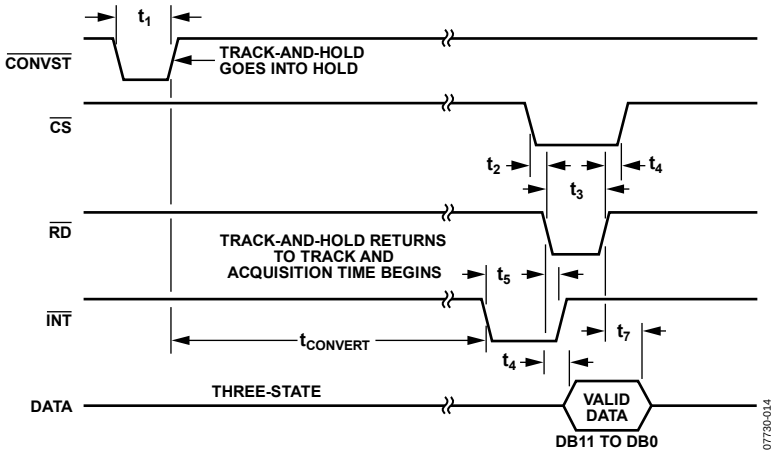


Figure 14. Mode 1 Timing Diagram, 12-Bit Parallel Read

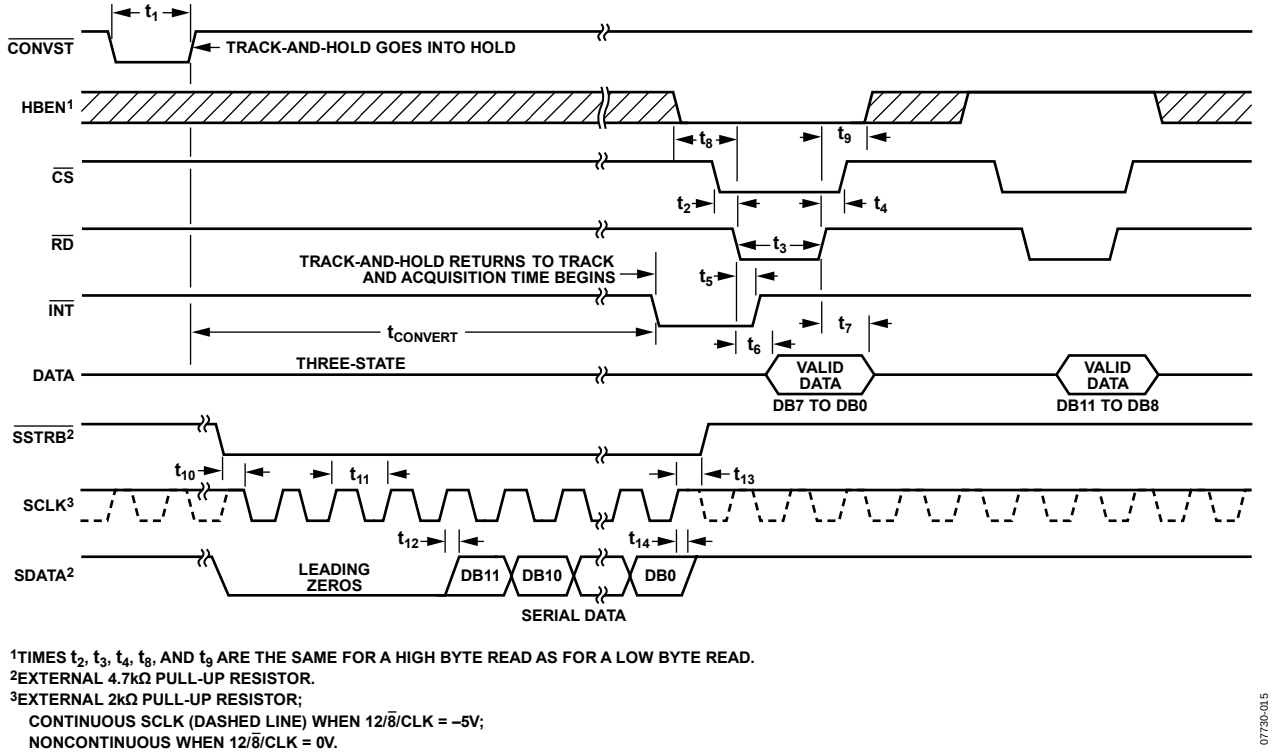


Figure 15. Mode 1 Timing Diagram, Byte or Serial Read

The Mode 1 timing diagram for byte and serial data is shown in Figure 15. $\overline{INT}$ goes low at the end of conversion and is reset high by the first falling edge of $\overline{CS}$ and $\overline{RD}$. This first read at the end of conversion can either access the low byte or high byte of data depending on the status of HBEN (Figure 15 shows low byte only for example). The diagram shows both a noncontinuously and a continuously running clock (dashed line).

MODE 2 INTERFACE

The second interface mode is achieved by hard wiring $\overline{CONVST}$ low and conversion is initiated by taking $\overline{CS}$ low while HBEN is low. The track-and-hold amplifier goes into the hold mode on the falling edge of $\overline{CS}$. In this mode, the $\overline{BUSY}$/$\overline{INT}$ pin assumes its $\overline{BUSY}$ function. $\overline{BUSY}$ goes low at the start of conversion, stays low during the conversion and returns high when the conversion is complete. It is normally used in parallel interfaces to drive the microprocessor into a WAIT state for the duration of conversion. Mode 2 is not relevant for the AD7870A device.

Figure 16 shows the Mode 2 timing diagram for the 12-bit parallel data output format (12/$\overline{8}$/CLK = +5 V). In this case, the ADC behaves like slow memory. The major advantage of this interface is that it allows the microprocessor to start conversion, WAIT and then read data with a single READ instruction. The user does not have to worry about servicing interrupts or ensuring that software delays are long enough to avoid reading during conversion.

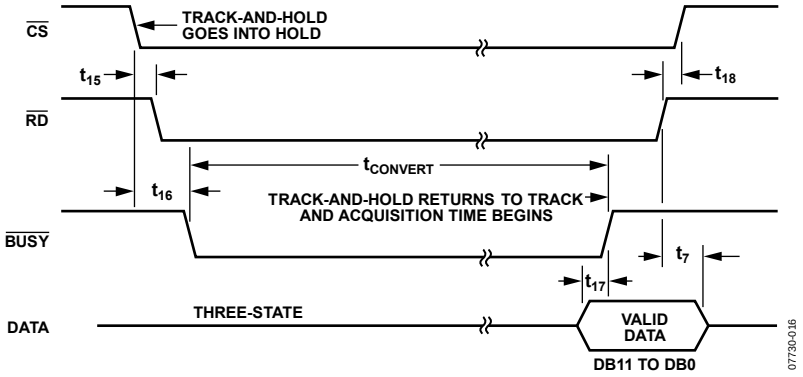


Figure 16. Mode 2 Timing Diagram, 12-Bit Parallel Read

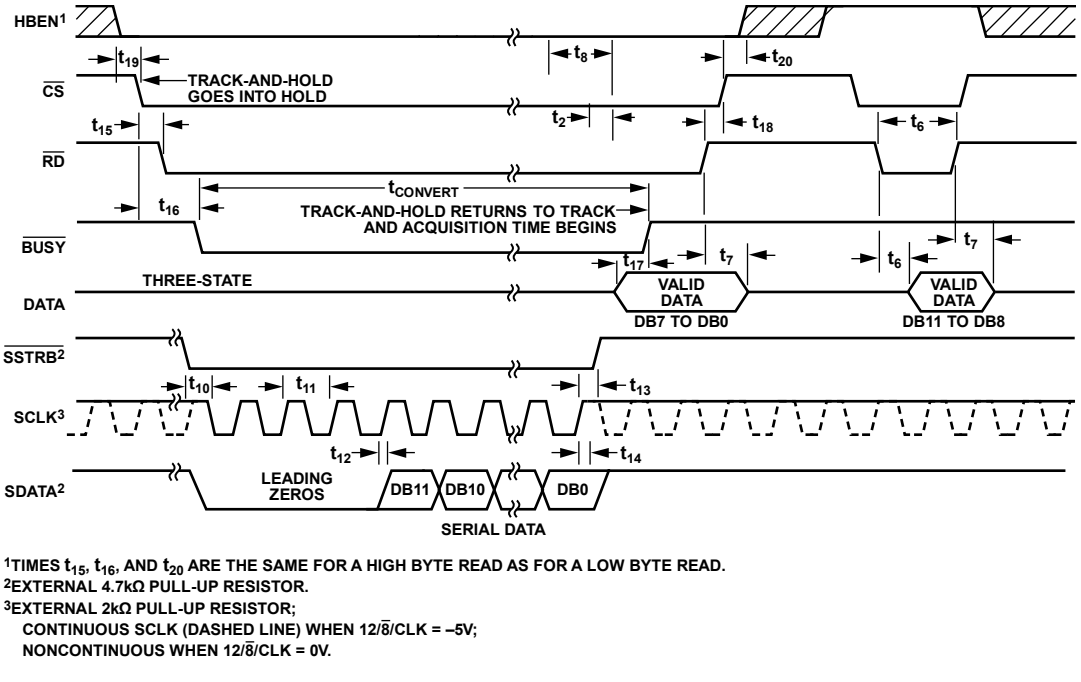


Figure 17. Mode 2 Timing Diagram, Byte or Serial Read

The Mode 2 timing diagram for byte and serial data is shown in Figure 17. For a two-byte data read, the lower byte (DB0 – DB7) has to be accessed first since HBEN must be low to start conversion. The ADC behaves like slow memory for this first read, but the second read to access the upper byte of data is a normal read. Operation of the serial functions is identical between Mode 1 and Mode 2. The timing diagram of Figure 17 shows both a noncontinuously and a continuously running SCLK (dashed line).

DYNAMIC SPECIFICATIONS

The AD7870 and AD7875 are specified and 100% tested for dynamic performance specifications as well as traditional dc specifications such as integral and differential nonlinearity. Although the AD7876 is not production tested for ac parameters, its dynamic performance is similar to the AD7870 and AD7875. The ac specifications are required for signal processing applications such as speech recognition, spectrum analysis and high speed modems. These applications require information on the ADC's effect on the spectral content of the input signal. Thus, the parameters for which the AD7870 and AD7875 are specified include SNR, harmonic distortion, intermodulation distortion and peak harmonics. These terms are discussed in more detail in the following sections.

Signal-to-Noise Ratio (SNR)

SNR is the measured signal-to-noise ratio at the output of the ADC. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all the nonfundamental signals up to half the sampling frequency (FS/2) excluding dc. SNR is dependent upon the number of quantization levels used in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal-to-noise ratio for a sine wave input is given by

$$SNR = (6.02N + 1.76)\ dB \quad (1)$$

where N is the number of bits. Thus for an ideal 12-bit converter, SNR = 74 dB.

Note that a sine wave signal is of very low distortion to the V_{IN} input which is sampled at a 100 kHz sampling rate. A fast

Fourier transform (FFT) plot is generated from which the SNR data can be obtained. Figure 18 shows a typical 2048 point FFT plot of the AD7870KN/AD7875KN with an input signal of 25 kHz and a sampling frequency of 100 kHz. The SNR obtained from this graph is 72.6 dB. It should be noted that the harmonics are taken into account when calculating the SNR.

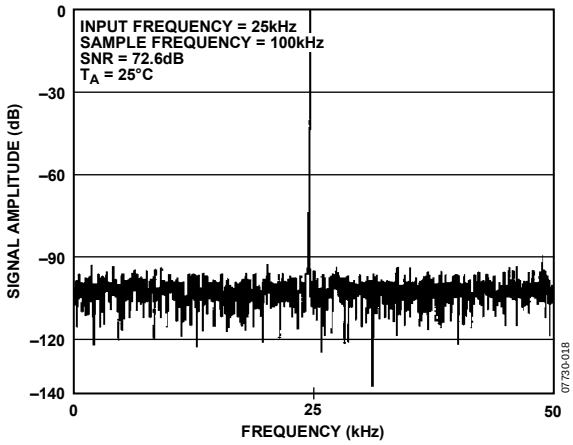


Figure 18. FFT Plot

Effective Number of Bits

The formula given in Equation 1 relates SNR to the number of bits. Rewriting the formula, as in Equation 2, it is possible to get a measure of performance expressed in effective number of bits (N).

$$N = \frac{SNR - 1.76}{6.02} \quad (2)$$

The effective number of bits for a device can be calculated directly from its measured SNR.

Figure 19 shows a typical plot of effective number of bits vs. frequency for an AD7870KN/AD7875KN with a sampling frequency of 100 kHz. The effective number of bits typically falls between 11.7 and 11.85 corresponding to SNR figures of 72.2 and 73.1 dB.

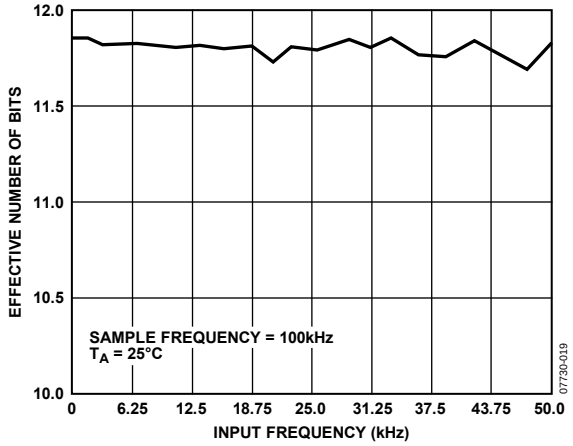


Figure 19. Effective Number of Bits vs. Frequency

Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of harmonics to the rms value of the fundamental. For the AD7870/AD7875, THD is defined as

$$THD = 20\log\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through the sixth harmonic. The THD is also derived from the FFT plot of the ADC output spectrum.

Intermodulation Distortion

With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities creates distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, and so on. Intermodulation terms are those for which neither m nor n are equal to zero. For example, the second order terms include (fa + fb) and (fa − fb), while the third order terms include (2fa + fb), (2fa − fb), (fa + 2fb) and (fa − 2fb).

Using the CCIF standard, where two input frequencies near the top end of the input bandwidth are used, the second and third order terms are of different significance. The second order terms are usually distanced in frequency from the original sine waves while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the fundamental expressed in dBs. In this case, the input consists of two, equal amplitude, low distortion sine waves. Figure 20 shows a typical IMD plot for the AD7870/AD7875.

Peak Harmonic or Spurious Noise

Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to FS/2 and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for parts where the harmonics are buried in the noise floor the peak is a noise peak.

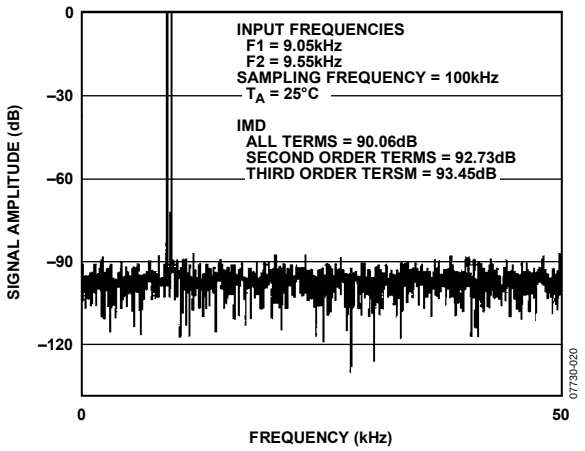


Figure 20. IMD Plot

AC Linearity Plot

When a sine wave of specified frequency is applied to the V_{IN} input of the AD7870/AD7875 and several million samples are taken, a histogram showing the frequency of occurrence of each of the 4096 ADC codes can be generated. From this histogram data it is possible to generate an ac integral linearity plot as shown in Figure 21. This shows very good integral linearity performance from the AD7870/AD7875 at an input frequency of 25 kHz. The absence of large spikes in the plot shows good differential linearity. Simplified versions of the formulae used are outlined below.

$$INL(i) = \left[\frac{V(i) - V(o)}{V(fs) - V(o)} \times 4096 \right] - i$$

where:
INL(i) is the integral linearity at code i.
V(fs) and *V(o)* are the estimated full-scale and offset transitions.
V(i) is the estimated transition for the ith code.

V(i), the estimated code transition point, is derived as follows:

$$V(i) = -A \times Cos \frac{\left[\pi \times cum(i)\right]}{N}$$

where:
A is the peak signal amplitude.
N is the number of histogram samples.
$cum(i) = \sum_{n=0}^{i} V(n)$ occurrences.

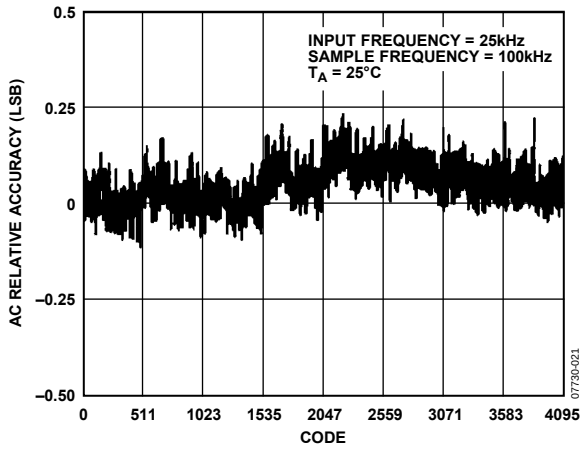


Figure 21. AC INL Plot

MICROPROCESSOR INTERFACE

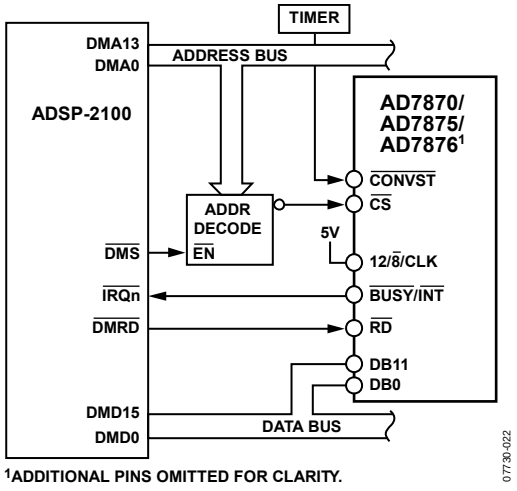
The AD7870/AD7875/AD7876 have a wide variety of interfacing options. They offer two operating modes and three data-output formats. Fast data access times allow direct interfacing to most microprocessors including the DSP processors.

PARALLEL READ INTERFACING

Figure 22, Figure 23, and Figure 24 show interfaces to the ADSP-2100, TMS32010 and the TMS32020 DSP processors. The ADC is operating in Mode 1, parallel read for all three interfaces. An external timer controls conversion start asynchronously to the microprocessor. At the end of each conversion the ADC $\overline{BUSY}/\overline{INT}$ interrupts the microprocessor. The conversion result is read from the ADC with the following instruction:

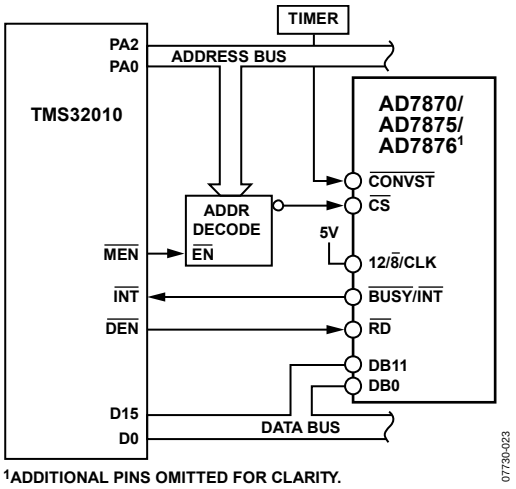
ADSP-2100: MR0 = DM(ADC)
TMS32010: IN D,ADC
TMS32020: IN D,ADC
MR0 = ADSP-2100 MR0 Register
D = Data Memory Address
ADC = AD7870/AD7875/AD7876 Address

Some applications may require that conversions be initiated by the microprocessor rather than an external timer. One option is to decode the $\overline{CONVST}$ signal from the address bus so that a write operation to the ADC starts a conversion. Data is read at the end of conversion as described earlier. Note: a read operation must not be attempted during conversion.



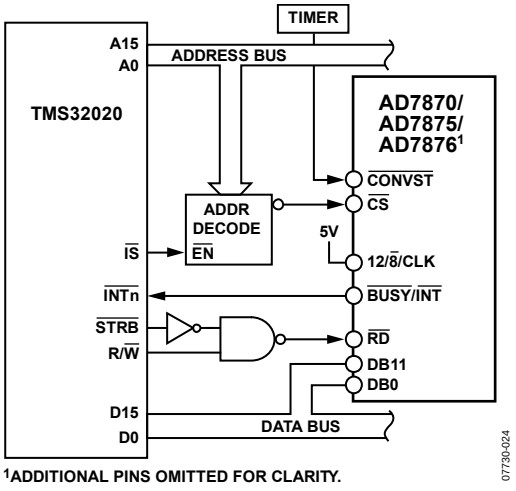
[1]ADDITIONAL PINS OMITTED FOR CLARITY.

Figure 22. ADSP-2100 Parallel Interface



[1]ADDITIONAL PINS OMITTED FOR CLARITY.

Figure 23. TMS32010 Parallel Interface



[1]ADDITIONAL PINS OMITTED FOR CLARITY.

Figure 24. TMS32020 Parallel Interface

TWO-BYTE READ INTERFACING

68008 Interface

Figure 25 shows an 8-bit bus interface for the MC68008 microprocessor. For this interface, the 12/$\overline{8}$/CLK input is tied to 0 V and the DB11/HBEN pin is driven from the microprocessor least significant address bit. Conversion start control is provided by the microprocessor. In this interface example, a Move instruction from the ADC address both starts a conversion and reads the conversion result.

MOVEW ADC,DO

ADC = AD7870/AD7875/AD7876 address

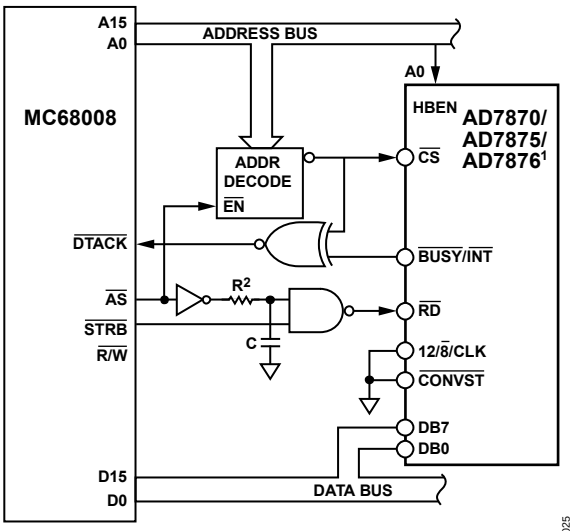
D0 = 68008 D0 register

This is a two-byte read instruction. During the first read operation $\overline{BUSY}$, in conjunction with $\overline{CS}$, forces the microprocessor to WAIT for the ADC conversion. At the end of conversion the ADC low byte (DB7 – DB0) is loaded into D15 – D8 of the D0 register and the ADC high byte (DB15 – DB7) is loaded into Bits D7 – D0 of the D0 register.

The following rotate instruction to the D0 register swaps the high and low bytes to the correct format.

R0L = 8, D0.

Note that while executing the two-byte read instruction above, WAIT states are inserted during the first read operation only and not for the second.



[1]ADDITIONAL PINS OMITTED FOR CLARITY.
[2]RESISTOR AND CAPACITOR REQUIRED TO GUARANTEE t_{15}.

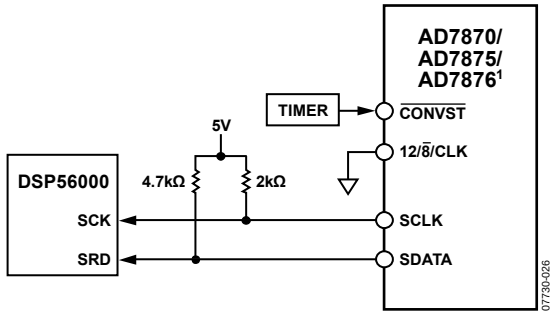
Figure 25. MC68008 Byte Interface

SERIAL INTERFACING

Figure 26, Figure 27, Figure 28, and Figure 29 show the AD7870/AD7875/AD7876 configured for serial interfacing. In all four interfaces, the ADC is configured for Mode 1 operation. The interfaces show a timer driving the $\overline{CONVST}$ input, but this could be generated from a decoded address if required. The SCLK, SDAT and $\overline{SSTRB}$ are open-drain outputs. If these are required to drive capacitive loads in excess 35 pF, buffering is recommended.

DSP56000 Serial Interface

Figure 26 shows a serial interface between the AD7870/AD7875/AD7876, and the DSP56000. The interface arrangement is two-wire with the ADC configured for noncontinuous clock operation (12/$\overline{8}$/CLK = 0 V). The DSP56000 is configured for normal mode asynchronous operation with gated clock. It is also set up for a 16-bit word with SCK and SC1 as inputs and the FSL control bit set to a 0. In this configuration, the DSP56000 assumes valid data on the first falling edge of SCK. Since the ADC provides valid data on this first edge, there is no need for a strobe or framing pulse for the data. SCLK and SDATA are gated off when the ADC is not performing a conversion. During conversion, data is valid on the SDATA output of the ADC and is clocked into the receive data shift register of the DSP56000. When this register has received 16 bits of data, it generates an internal interrupt on the DSP56000 to read the data from the register.



[1]ADDITIONAL PINS OMITTED FOR CLARITY.

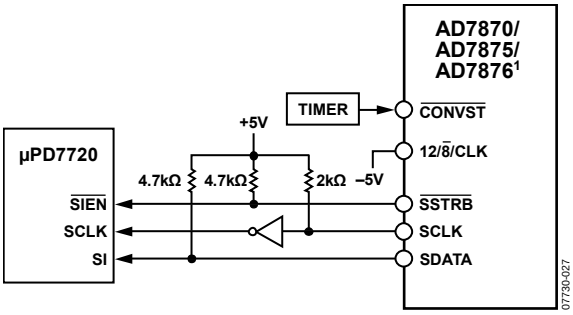
Figure 26. DSP56000 Serial Interface

The DSP56000 and AD7870/AD7875/AD7876 can also be configured for continuous clock operation (12/$\overline{8}$/CLK = –5 V). In this case, a strobe pulse is required by the DSP56000 to indicate when data is valid. The $\overline{SSTRB}$ output of the ADC is inverted and applied to the SC1 input of the DSP56000 to provide this strobe pulse. All other conditions and connections are the same as for gated clock operation.

NEC7720/77230 Serial Interface

A serial interface between the AD7870/AD7875/AD7876 and the NEC7720 is shown in Figure 27. In the interface shown, the ADC is configured for continuous clock operation. This can be changed to a noncontinuous clock by simply tying the 12/$\overline{8}$/CLK input of the ADC to 0 V with all other connections remaining the same. The NEC7720 expects valid data on the rising edge of its SCK input and therefore an inverter is required on the SCLK output of the ADC. The NEC7720 is configured for a 16-bit data word. Once the 16 bits of data have been received by the SI register of the NEC7720, an internal interrupt is generated to read the contents of the SI register.

The NEC77230 interface is similar to that just outlined for the NEC7720. However, the clock input of the NEC77230 is SICLK. Additionally, no inverter is required between the ADC SCLK output and this SICLK input since the NEC77230 assumes data is valid on the falling edge of SICLK.

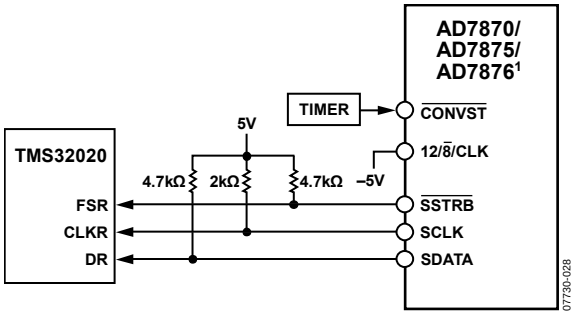


[1]ADDITIONAL PINS OMITTED FOR CLARITY.

Figure 27. NEC7720 Serial Interface

TMS32020 Serial Interface

Figure 28 shows a serial interface between the AD7870/AD7875/AD7876 and the TMS32020. The AD7870/AD7875/AD7876 is configured for continuous clock operation. Note that the ADC will not interface correctly to the TMS32020 if the ADC is configured for a noncontinuous clock. Data is clocked into the data receive register (DRR) of the TMS32020 during conversion. As with the previous interfaces, when a 16-bit word is received by the TMS32020 it generates an internal interrupt to read the data from the DRR.

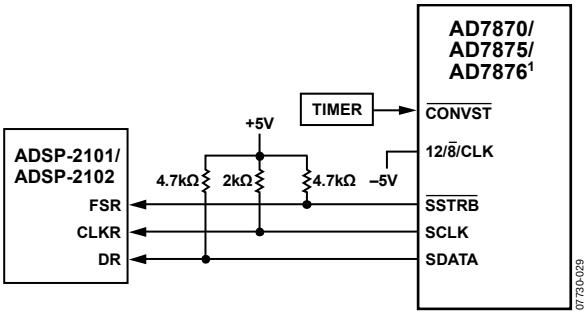


[1]ADDITIONAL PINS OMITTED FOR CLARITY.

Figure 28. TMS32020 Serial Interface

ADSP-2101/ADSP-2102 Serial Interface

Figure 29 shows a serial interface between the AD7870/AD7875/AD7876 and the ADSP-2101/ADSP-2102. The ADC is configured for continuous clock operation. Data is clocked into the serial port register of the ADSP-2101/ADSP-2102 during conversion. As with the previous interfaces, when a 16-bit data word is received by the ADSP-2101/ADSP-2102 an internal microprocessor interrupt is generated and the data is read from the serial port register.

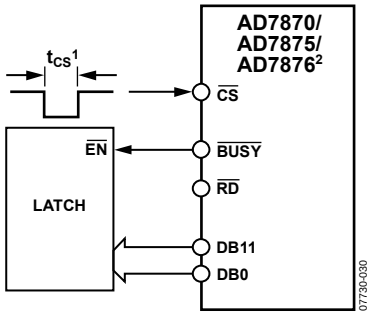


[1]ADDITIONAL PINS OMITTED FOR CLARITY.

Figure 29. ADSP-2101/ADSP-2102 Serial Interface

STANDALONE OPERATION

The AD7870/AD7875/AD7876 can be used in its Mode 2, parallel interface mode for standalone operation. In this case, conversion is initiated with a pulse to the ADC $\overline{CS}$ input. This pulse must be longer than the conversion time of the ADC. The $\overline{BUSY}$ output is used to drive the $\overline{RD}$ input. Data is latched from the ADC DB0–DB11 outputs to an external latch on the rising edge of $\overline{BUSY}$.



[1]$t_{CS} > t_{16} + t_{CONVERT}$.
[2]ADDITIONAL PINS OMITTED FOR CLARITY.

Figure 30. Stand-Alone Operation

APPLICATIONS INFORMATION

Good printed circuit board (PCB) layout is as important as the overall circuit design itself in achieving high speed analog-to-digital performance. The designer has to be conscious of noise both in the ADC itself and in the preceding analog circuitry. Switching mode power supplies are not recommended because the switching spikes feed through to the comparator causing noisy code transitions. Other causes of concern are ground loops and digital feedthrough from microprocessors. These are factors which influence any ADC, and a proper PCB layout which minimizes these effects is essential for best performance.

LAYOUT HINTS

Ensure that the layout for the printed circuit board has the digital and analog signal lines separated as much as possible. Take care not to run any digital track alongside an analog signal track. Guard (screen) the analog input with AGND.

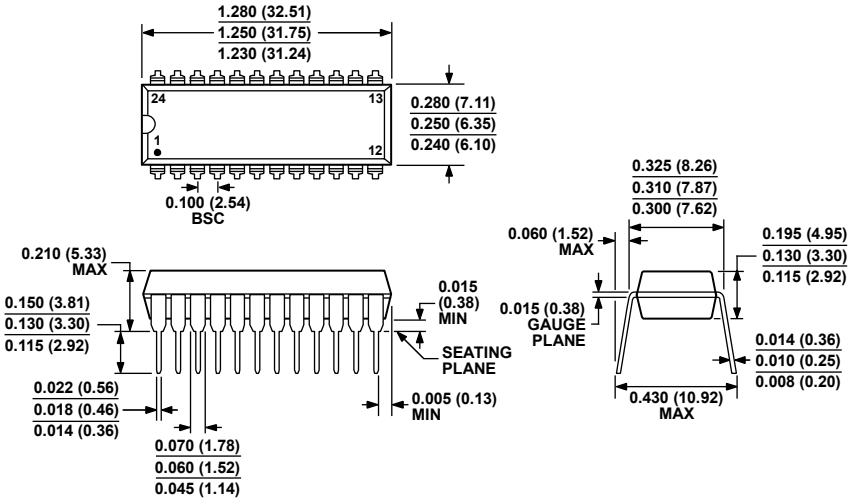
Establish a single point analog ground (star ground) separate from the logic system ground at the AGND pin or as close as possible to the ADC. Connect all other grounds and the AD7870/AD7875/AD7876 DGND to this single analog ground point. Do not connect any other digital grounds to this analog ground point.

Low impedance analog and digital power supply common returns are essential to low noise operation of the ADC, so make the foil width for these tracks as wide as possible. The use of ground planes minimizes impedance paths and also guards the analog circuitry from digital noise. The circuit layout has both analog and digital ground planes which are kept separated and only joined together at the AD7870/AD7875/AD7876 AGND pin.

NOISE

Keep the input signal leads to V_{IN} and signal return leads from AGND as short as possible to minimize input noise coupling. In applications where this is not possible, use a shielded cable between the source and the ADC. Reduce the ground circuit impedance as much as possible since any potential difference in grounds between the signal source and the ADC appears as an error voltage in series with the input signal.

OUTLINE DIMENSIONS



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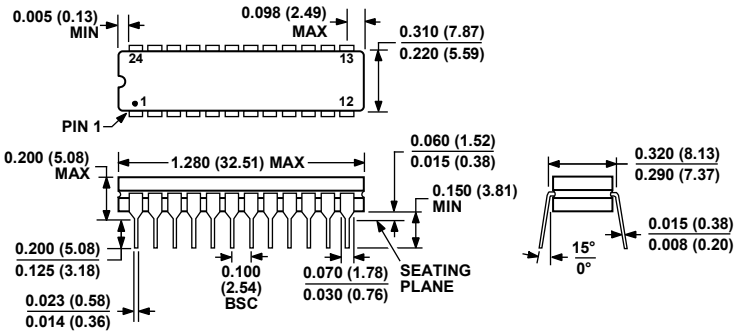
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

071006-A

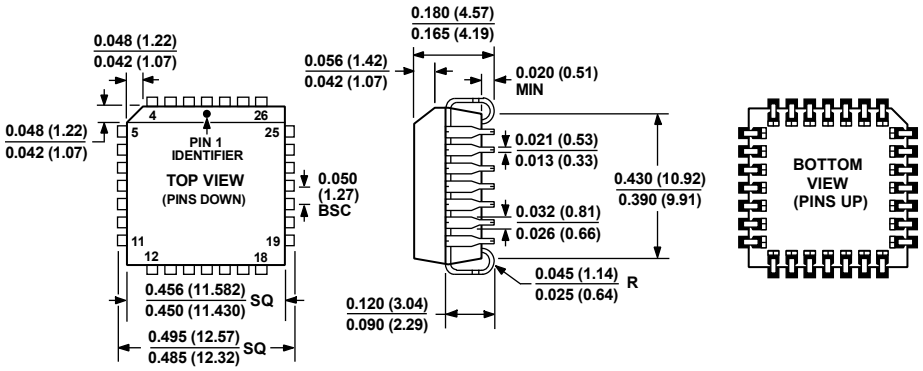
Figure 31. 24-Lead Plastic Dual In-Line Package [PDIP]
Narrow Body
(N-24-1)
Dimensions shown in inches and (millimeters)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

100808-A

Figure 32. 24-Lead Ceramic Dual In-Line Package [CERDIP]
Narrow Body
(Q-24-1)
Dimensions shown in inches and (millimeters)



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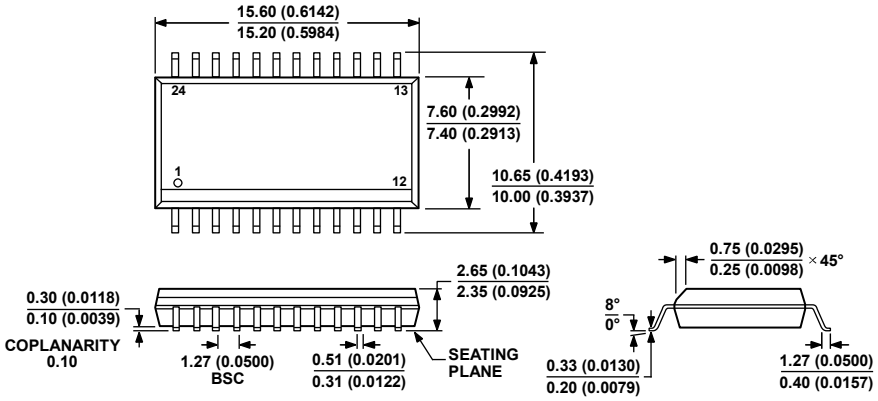
042508-A

Figure 33. 28-Lead Plastic Leaded Chip Carrier [PLCC]
(P-28)
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-013-AD
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

06070 6-A

Figure 34. 24-Lead Standard Small Outline Package [SOIC_W]
Wide Body
(RW-24)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Table 7.

Model	Temperature Range	V_{IN} Voltage Range (V)	SNR (dBs)	Integral Nonlinearity (LSB)	Package Description	Package Option
AD7870JN	0°C to +70°C	±3	70 min	±1/2 typ	24-Lead PDIP	N-24-1
AD7870JNZ[1]	0°C to +70°C	±3	70 min	±1/2 typ	24-Lead PDIP	N-24-1
AD7870KN	0°C to +70°C	±3	70 min	±1 max	24-Lead PDIP	N-24-1
AD7870KNZ[1]	0°C to +70°C	±3	70 min	±1 max	24-Lead PDIP	N-24-1
AD7870LN	0°C to +70°C	±3	72 min	±1/2 max	24-Lead PDIP	N-24-1
AD7870LNZ[1]	0°C to +70°C	±3	72 min	±1/2 max	24-Lead PDIP	N-24-1
AD7870JP	0°C to +70°C	±3	70 min	±1/2 typ	28-Lead PLCC	P-28
AD7870JP-REEL	0°C to +70°C	±3	70 min	±1/2 typ	28-Lead PLCC	P-28
AD7870JPZ[1]	0°C to +70°C	±3	70 min	±1/2 typ	28-Lead PLCC	P-28
AD7870JPZ-REEL[1]	0°C to +70°C	±3	70 min	±1/2 typ	28-Lead PLCC	P-28
AD7870KP	0°C to +70°C	±3	70 min	±1 max	28-Lead PLCC	P-28
AD7870KP-REEL	0°C to +70°C	±3	70 min	±1 max	28-Lead PLCC	P-28
AD7870KPZ[1]	0°C to +70°C	±3	70 min	±1 max	28-Lead PLCC	P-28
AD7870KPZ-REEL[1]	0°C to +70°C	±3	70 min	±1 max	28-Lead PLCC	P-28
AD7870LP	0°C to +70°C	±3	72 min	±1/2 max	28-Lead PLCC	P-28
AD7870LP-REEL	0°C to +70°C	±3	72 min	±1/2 max	28-Lead PLCC	P-28
AD7870LPZ[1]	0°C to +70°C	±3	72 min	±1/2 max	28-Lead PLCC	P-28
AD7870AQ	−25°C to +85°C	±3	70 min	±1/2 typ	24-Lead CERDIP	Q-24-1
AD7870BQ	−25°C to +85°C	±3	70 min	±1 max	24-Lead CERDIP	Q-24-1
AD7870CQ	−25°C to +85°C	±3	72 min	±1/2 max	24-Lead CERDIP	Q-24-1
AD7870TQ	−55°C to +125°C	±3	70 min	±1 max	24-Lead CERDIP	Q-24-1
AD7875KN	0°C to +70°C	0 to +5	70 min	±1 max	24-Lead PDIP	N-24-1
AD7875KNZ[1]	0°C to +70°C	0 to +5	70 min	±1 max	24-Lead PDIP	N-24-1
AD7875LN	0°C to +70°C	0 to +5	72 min	±1/2 max	24-Lead PDIP	N-24-1
AD7875LNZ[1]	0°C to +70°C	0 to +5	72 min	±1/2 max	24-Lead PDIP	N-24-1
AD7875KP	0°C to +70°C	0 to +5	70 min	±1 max	28-Lead PLCC	P-28
AD7875KPZ[1]	0°C to +70°C	0 to +5	70 min	±1 max	28-Lead PLCC	P-28
AD7875KPZ-REEL[1]	0°C to +70°C	0 to +5	70 min	±1 max	28-Lead PLCC	P-28
AD7875LP-REEL	0°C to +70°C	0 to +5	72 min	±1/2 max	28-Lead PLCC	P-28
AD7875LPZ[1]	0°C to +70°C	0 to +5	72 min	±1/2 max	28-Lead PLCC	P-28
AD7875LPZ-REEL[1]	0°C to +70°C	0 to +5	72 min	±1/2 max	28-Lead PLCC	P-28
AD7875BQ	−40°C to +85°C	0 to +5	70 min	±1 max	24-Lead CERDIP	Q-24-1
AD7875CQ	−40°C to +85°C	0 to +5	72 min	±1/2 max	24-Lead CERDIP	Q-24-1
AD7875TQ	−55°C to +125°C	0 to +5	70 min	±1 max	24-Lead CERDIP	Q-24-1
AD7876BN	−40°C to +85°C	±10		±1 max	24-Lead PDIP	N-24-1
AD7876BNZ[1]	−40°C to +85°C	±10		±1 max	24-Lead PDIP	N-24-1
AD7876CN	−40°C to +85°C	±10		±1/2 max	24-Lead PDIP	N-24-1
AD7876CNZ[1]	−40°C to +85°C	±10		±1/2 max	24-Lead PDIP	N-24-1
AD7876BR	−40°C to +85°C	±10		±1 max	24-Lead SOIC_W	RW-24
AD7876BR-REEL	−40°C to +85°C	±10		±1 max	24-Lead SOIC_W	RW-24
AD7876BR-REEL7	−40°C to +85°C	±10		±1 max	24-Lead SOIC_W	RW-24
AD7876BRZ[1]	−40°C to +85°C	±10		±1 max	24-Lead SOIC_W	RW-24
AD7876BRZ-REEL[1]	−40°C to +85°C	±10		±1 max	24-Lead SOIC_W	RW-24
AD7876BRZ-REEL7[1]	−40°C to +85°C	±10		±1 max	24-Lead SOIC_W	RW-24
AD7876CR	−40°C to +85°C	±10		±1/2 max	24-Lead SOIC_W	RW-24
AD7876CR-REEL	−40°C to +85°C	±10		±1/2 max	24-Lead SOIC_W	RW-24
AD7876CRZ[1]	−40°C to +85°C	±10		±1/2 max	24-Lead SOIC_W	RW-24
AD7876BQ	−40°C to +85°C	±10		±1 max	24-Lead CERDIP	Q-24-1
AD7876TQ	−55°C to +125°C	±10		±1 max	24-Lead CERDIP	Q-24-1

[1] Z = RoHS Compliant Part.

NOTES

NOTES

NOTES

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