Phase Detector/Frequency Synthesizer

Data Sheet

ADF4002

FEATURES

400 MHz bandwidth
2.7 V to 3.3 V power supply
Separate charge pump supply (V_P) allows extended tuning voltage in 3 V systems
Programmable charge pump currents
3-wire serial interface
Analog and digital lock detect
Hardware and software power-down mode
104 MHz phase detector

APPLICATIONS

Clock conditioning
Clock generation
IF LO generation

GENERAL DESCRIPTION

The ADF4002 frequency synthesizer is used to implement local oscillators in the upconversion and downconversion sections of wireless receivers and transmitters. It consists of a low noise digital phase frequency detector (PFD), a precision charge pump, a programmable reference divider, and programmable N divider. The 14-bit reference counter (R counter) allows selectable REFIN frequencies at the PFD input. A complete phase-locked loop (PLL) can be implemented if the synthesizer is used with an external loop filter and voltage controlled oscillator (VCO). In addition, by programming R and N to 1, the device can be used as a standalone PFD and charge pump.

FUNCTIONAL BLOCK DIAGRAM

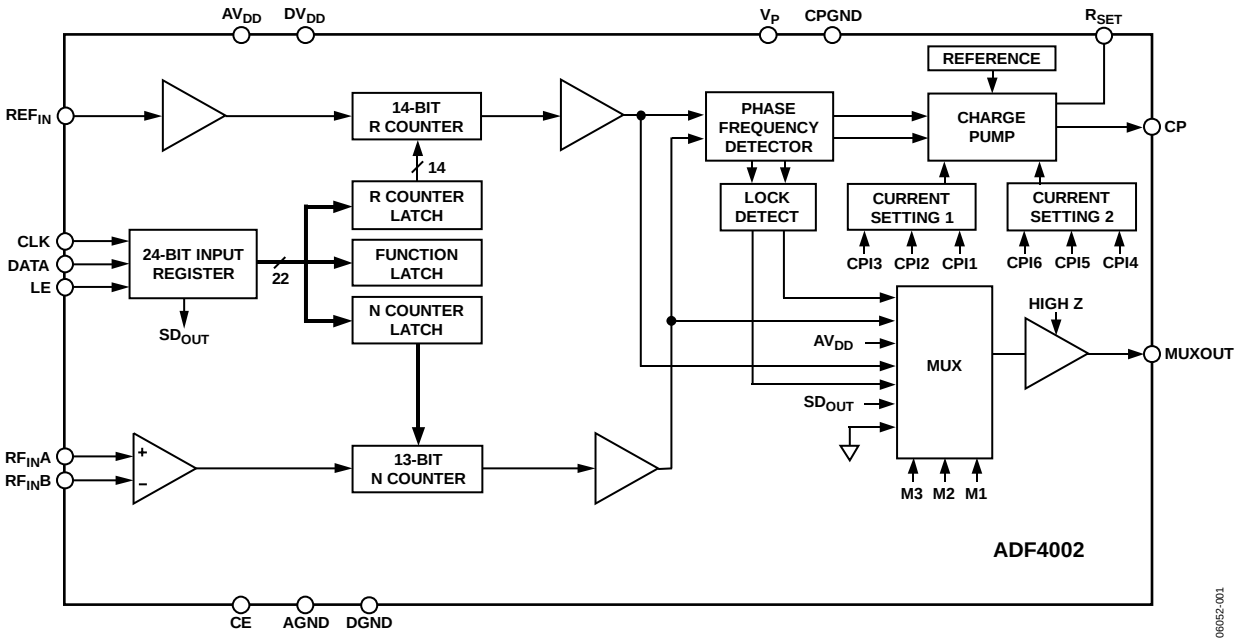

Figure 1.

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REVISION HISTORY

9/15—Rev. C to Rev. D

Changed ADSP21xx to ADSP-2181 ... Throughout
Changes to Table 3 ... 5
Changes to Figure 4 ... 6
Changes to Very Low Jitter Encode Clock for High Speed Converters Section and Figure 20 ... 17
Update Outline Dimensions ... 19
Changes to Ordering Guide ... 19

12/12—Rev. B to Rev. C

Change to Table 1 ... 4
Added $RF_{IN}A$ to $RF_{IN}B$ Parameter, Table 3 ... 5
Updated Outline Dimensions ... 19
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9/11—Rev. A to Rev. B

Changes to Normalized Phase Noise Floor (PN_{SYNTH}) Parameter and Endnote 6, Table 1 ... 4
Added Normalized 1/f Noise (PN_{1_f}) Parameter and Endnote 7, Table 1 ... 4
Changes to Figure 4 and Table 5 ... 6
Updated Outline Dimensions ... 19

4/07—Rev. 0 to Rev. A

Changes to Features List ... 1
Changes to Table 1 ... 3
Deleted Figure ... 7
Changes to Figure 16 ... 11

4/06—Revision 0: Initial Version

SPECIFICATIONS

$AV_{DD} = DV_{DD} = 3$ V ± 10%, $AV_{DD} \leq V_P \leq 5.5$ V, AGND = DGND = CPGND = 0 V, $R_{SET} = 5.1$ kΩ, dBm referred to 50 Ω, $T_A = T_{MAX}$ to T_{MIN}, unless otherwise noted.

Table 1.

	B Version[1]				
Parameter	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
RF CHARACTERISTICS					See Figure 11 for input circuit
RF Input Sensitivity	−10		0	dBm	
RF Input Frequency (RF_{IN})	5		400	MHz	For RF_{IN} < 5 MHz, ensure slew rate (SR) > 4 V/µs
REFIN CHARACTERISTICS					
REFIN Input Frequency	20		300	MHz	For REFIN < 20 MHz, ensure SR > 50 V/µs
REFIN Input Sensitivity[2]	0.8		V_{DD}	V p-p	Biased at $AV_{DD}/2$[3]
REFIN Input Capacitance			10	pF	
REFIN Input Current			±100	µA	
PHASE DETECTOR					
Phase Detector Frequency[4]			104	MHz	ABP = 0, 0 (2.9 ns antibacklash pulse width)
CHARGE PUMP					Programmable, see Figure 18
I_{CP} Sink/Source					
High Value		5		mA	With $R_{SET} = 5.1$ kΩ
Low Value		625		µA	
Absolute Accuracy		2.5		%	With $R_{SET} = 5.1$ kΩ
R_{SET} Range	3.0		11	kΩ	See Figure 18
I_{CP} Three-State Leakage		1		nA	$T_A = 25°C$
I_{CP} vs. V_{CP}		1.5		%	$0.5 V \leq V_{CP} \leq V_P - 0.5 V$
Sink and Source Current Matching		2		%	$0.5 V \leq V_{CP} \leq V_P - 0.5 V$
I_{CP} vs. Temperature		2		%	$V_{CP} = V_P/2$
LOGIC INPUTS					
V_{IH}, Input High Voltage	1.4			V	
V_{IL}, Input Low Voltage			0.6	V	
I_{INH}, I_{INL}, Input Current			±1	µA	
C_{IN}, Input Capacitance			10	pF	
LOGIC OUTPUTS					
V_{OH}, Output High Voltage	1.4			V	Open-drain output chosen, 1 kΩ pull-up resistor to 1.8 V
V_{OH}, Output High Voltage	$V_{DD} - 0.4$			V	CMOS output chosen
I_{OH}			100	µA	
V_{OL}, Output Low Voltage			0.4	V	$I_{OL} = 500$ µA
POWER SUPPLIES					
AV_{DD}	2.7		3.3	V	
DV_{DD}	AV_{DD}				
V_P	AV_{DD}		5.5	V	$AV_{DD} \leq V_P \leq 5.5$ V
I_{DD}[5] ($AI_{DD} + DI_{DD}$)		5.0	6.0	mA	
I_P			0.4	mA	$T_A = 25°C$
Power-Down Mode		1		µA	$AI_{DD} + DI_{DD}$

Parameter	B Version[1] Min	Typ	Max	Unit	Test Conditions/Comments
NOISE CHARACTERISTICS					
Normalized Phase Noise Floor (PN_{SYNTH})[6]		−222		dBc/Hz	PLL loop bandwidth = 500 kHz, measured at 100 kHz offset
Normalized 1/f Noise (PN_{1_f})[7]		−119		dBc/Hz	10 kHz offset; normalized to 1 GHz

[1] Operating temperature range (B version) is −40°C to +85°C.
[2] $AV_{DD} = DV_{DD} = 3$ V.
[3] AC coupling ensures $AV_{DD}/2$ bias.
[4] Guaranteed by design. Sample tested to ensure compliance.
[5] $T_A = 25°C$; $AV_{DD} = DV_{DD} = 3$ V; $RF_{IN} = 350$ MHz. The current for any other setup (25°C, 3.0 V) in mA is given by 2.35 + 0.0046 (REFIN) + 0.0062 (RF), RF frequency and REFIN frequency in MHz.
[6] The synthesizer phase noise floor is estimated by measuring the in-band phase noise at the output of the VCO and subtracting 20 logN (where N is the N divider value) and 10 $\log F_{PFD}$. $PN_{SYNTH} = PN_{TOT} - 10 \log F_{PFD} - 20 \log N$.
[7] The PLL phase noise is composed of 1/f (flicker) noise plus the normalized PLL noise floor. The formula for calculating the 1/f noise contribution at an RF frequency, f_{RF}, and at a frequency offset, f, is given by $PN = PN_{1_f} + 10 \log(10 \text{ kHz}/f) + 20 \log(f_{RF}/1 \text{ GHz})$. All phase noise measurements were performed with the EV-ADF4002SD1Z and the Agilent E5500 phase noise system. Both the normalized phase noise floor and flicker noise are modeled in ADIsimPLL.

TIMING CHARACTERISTICS

$AV_{DD} = DV_{DD} = 3$ V ± 10%, $AV_{DD} \leq V_P \leq 5.5$ V, AGND = DGND = CPGND = 0 V, $R_{SET} = 5.1$ kΩ, dBm referred to 50 Ω, $T_A = T_{MAX}$ to T_{MIN}, unless otherwise noted.[1]

Table 2.

Parameter	Limit (B Version)[2]	Unit	Test Conditions/Comments
t_1	10	ns min	DATA to CLK setup time
t_2	10	ns min	DATA to CLK hold time
t_3	25	ns min	CLK high duration
t_4	25	ns min	CLK low duration
t_5	10	ns min	CLK to LE setup time
t_6	20	ns min	LE pulse width

[1] Guaranteed by design, but not production tested.
[2] Operating temperature range (B version) is −40°C to +85°C.

Timing Diagram

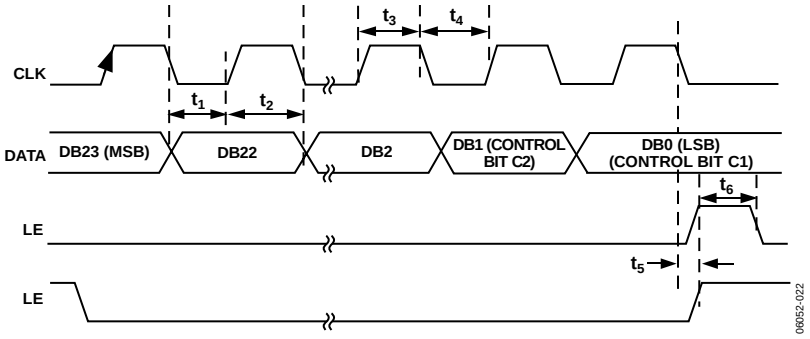


Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
AV_{DD} to GND[1]	−0.3 V to +3.6 V
AV_{DD} to DV_{DD}	−0.3 V to +0.3 V
V_P to GND	−0.3 V to +5.8 V
V_P to AV_{DD}	−0.3 V to +5.8 V
Digital I/O Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Analog I/O Voltage to GND	−0.3 V to V_P + 0.3 V
REF_{IN}, $RF_{IN}A$, $RF_{IN}B$ to GND	−0.3 V to V_{DD} + 0.3 V
$RF_{IN}A$ to $RF_{IN}B$	±600 mV
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +125°C
Maximum Junction Temperature	150°C
Reflow Soldering	
Peak Temperature (60 sec)	260°C
Time at Peak Temperature	40 sec
Transistor Count	
CMOS	6425
Bipolar	303

[1] GND = AGND = DGND = 0 V.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

This device is a high performance RF integrated circuit with an ESD rating of <2 kV, and it is ESD sensitive. Take proper precautions for handling and assembly.

THERMAL CHARACTERISTICS

Table 4. Thermal Impedance

Package Type	θ_{JA}	Unit
TSSOP	150.4	°C/W
LFCSP	122	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

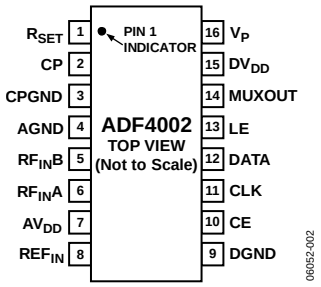


Figure 3. TSSOP Pin Configuration (Top View)

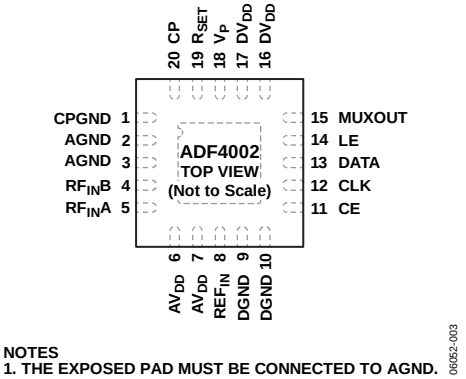


Figure 4. LFCSP Pin Configuration (Top View)

Table 5. Pin Function Descriptions

Pin No.			
TSSOP	**LFCSP**	**Mnemonic**	**Description**
1	19	R_{SET}	Connecting a resistor between this pin and CPGND sets the maximum charge pump output current. The nominal voltage potential at the R_{SET} pin is 0.66 V. The relationship between I_{CP} and R_{SET} is $$I_{CP\,MAX} = \frac{25.5}{R_{SET}}$$ where R_{SET} = 5.1 kΩ and $I_{CP\,MAX}$ = 5 mA.
2	20	CP	Charge Pump Output. When enabled, this provides $\pm I_{CP}$ to the external loop filter that, in turn, drives the external VCO.
3	1	CPGND	Charge Pump Ground. This is the ground return path for the charge pump.
4	2, 3	AGND	Analog Ground. This is the ground return path of the RF input.
5	4	$RF_{IN}B$	Complementary Input to the RF Input. This point must be decoupled to the ground plane with a small bypass capacitor, typically 100 pF. See Figure 11.
6	5	$RF_{IN}A$	Input to the RF Input. This small signal input is ac-coupled to the external VCO.
7	6, 7	AV_{DD}	Analog Power Supply. This can range from 2.7 V to 3.3 V. Decoupling capacitors to the analog ground plane should be placed as close as possible to the AV_{DD} pin. AV_{DD} must be the same value as DV_{DD}.
8	8	REF_{IN}	Reference Input. This is a CMOS input with a nominal threshold of $V_{DD}/2$ and a dc equivalent input resistance of 100 kΩ. See Figure 10. This input can be driven from a TTL or CMOS crystal oscillator or it can be ac-coupled.
9	9, 10	DGND	Digital Ground.
10	11	CE	Chip Enable. A logic low on this pin powers down the device and puts the charge pump output into three-state mode. Taking this pin high powers up the device, depending on the status of the Power-Down Bit F2.
11	12	CLK	Serial Clock Input. This serial clock is used to clock in the serial data to the registers. The data is latched into the 24-bit shift register on the CLK rising edge. This input is a high impedance CMOS input.
12	13	DATA	Serial Data Input. The serial data is loaded MSB first with the two LSBs being the control bits. This input is a high impedance CMOS input.
13	14	LE	Load Enable, CMOS Input. When LE goes high, the data stored in the shift registers is loaded into one of the four latches; the latch is selected using the control bits.
14	15	MUXOUT	Multiplexer Output. This allows either the lock detect, the scaled RF, or the scaled reference frequency to be accessed externally.
15	16, 17	DV_{DD}	Digital Power Supply. This can range from 2.7 V to 3.3 V. Decoupling capacitors to the digital ground plane should be placed as close as possible to this pin. DV_{DD} must be the same value as AV_{DD}.
16	18	V_P	Charge Pump Power Supply. This should be greater than or equal to V_{DD}. In systems where V_{DD} is 3 V, it can be set to 5.5 V and used to drive a VCO with a tuning range of up to 5 V.
		EP	Exposed Pad. The exposed pad must be connected to AGND.

TYPICAL PERFORMANCE CHARACTERISTICS

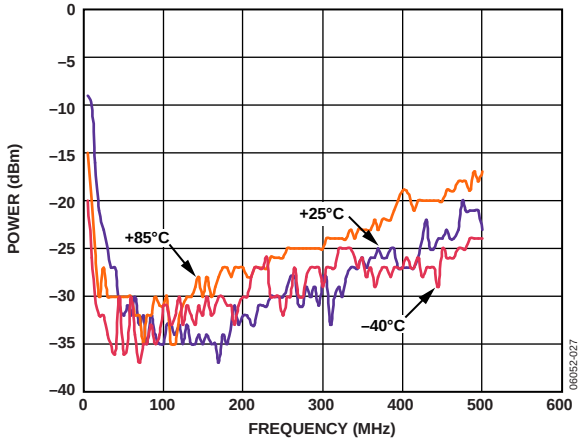


Figure 5. RF Input Sensitivity

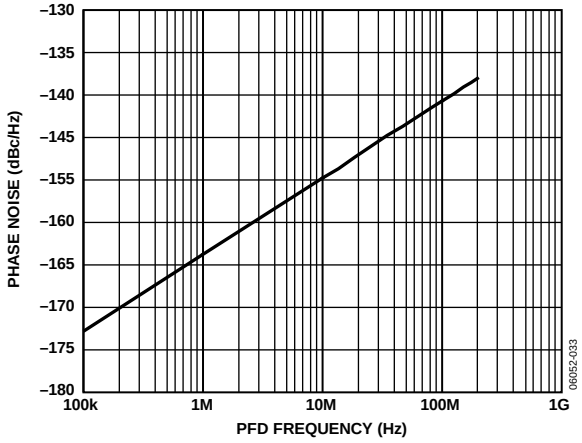


Figure 8. Phase Noise (Referred to CP Output) vs. PFD Frequency

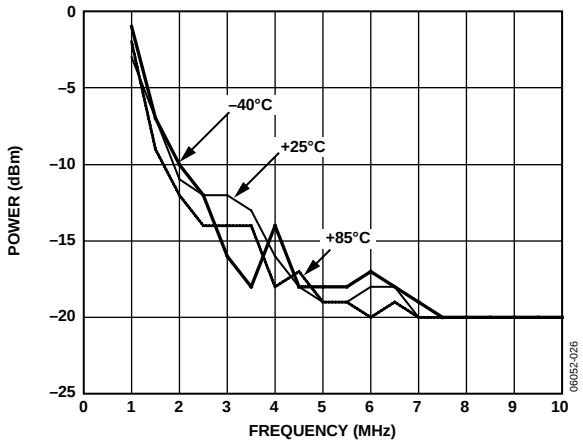


Figure 6. RF Input Sensitivity, Low Frequency

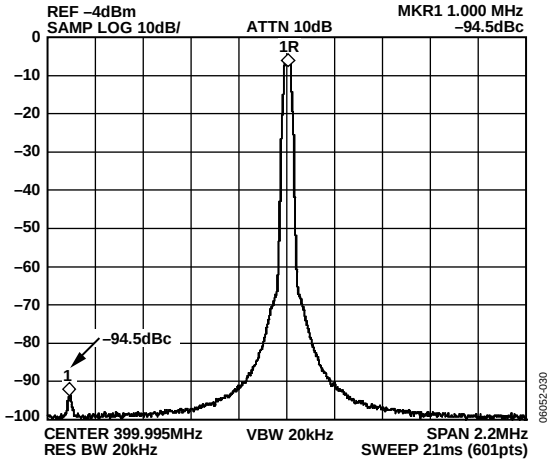


Figure 9. Reference Spurs (400 MHz, 1 MHz, 7 kHz)

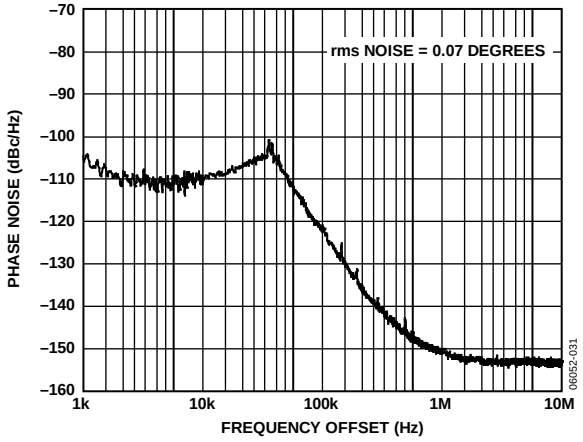


Figure 7. Integrated Phase Noise (400 MHz, 1 MHz, 50 kHz)

THEORY OF OPERATION

REFERENCE INPUT SECTION

The reference input stage is shown in Figure 10. SW1 and SW2 are normally closed switches. SW3 is normally open. When power-down is initiated, SW3 is closed and SW1 and SW2 are opened. This ensures that there is no loading of the REF_{IN} pin on power-down.

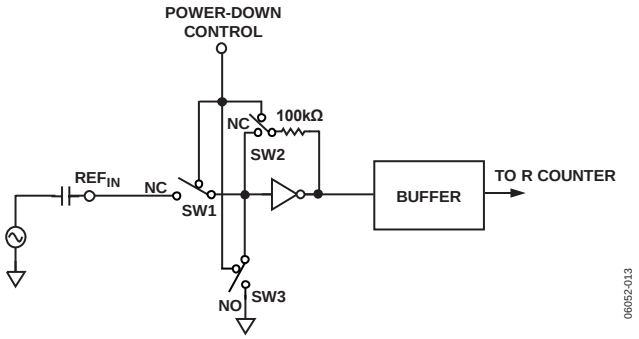


Figure 10. Reference Input Stage

RF INPUT STAGE

The RF input stage is shown in Figure 11. It is followed by a 2-stage limiting amplifier to generate the CML clock levels needed for the N counter.

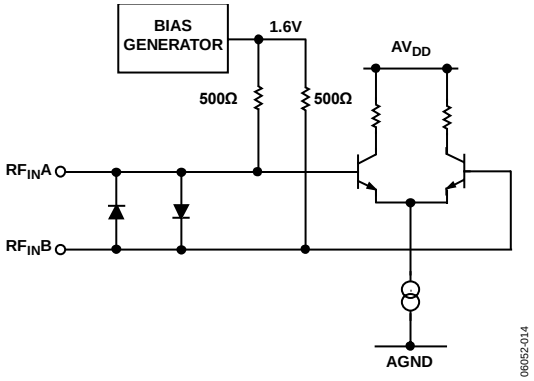


Figure 11. RF Input Stage

N COUNTER

The N CMOS counter allows a wide ranging division ratio in the PLL feedback counter. Division ratios from 1 to 8191 are allowed.

N and R Relationship

The N counter makes it possible to generate output frequencies that are spaced only by the reference frequency divided by R.

The equation for the VCO frequency is

$$f_{VCO} = N \times \frac{f_{REFIN}}{R}$$

where:

f_{VCO} is the output frequency of external voltage controlled oscillator (VCO).
N is the preset divide ratio of binary 13-bit counter (1 to 8191).
f_{REFIN} is the external reference frequency oscillator.

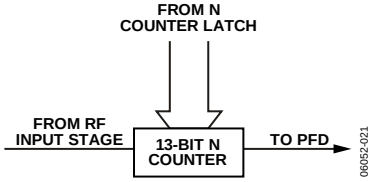


Figure 12. N Counter

R COUNTER

The 14-bit R counter allows the input reference frequency to be divided down to produce the reference clock to the phase frequency detector (PFD). Division ratios from 1 to 16,383 are allowed.

PHASE FREQUENCY DETECTOR (PFD) AND CHARGE PUMP

The PFD takes inputs from the R counter and N counter and produces an output proportional to the phase and frequency difference between them. Figure 13 is a simplified schematic. The PFD includes a programmable delay element that controls the width of the antibacklash pulse. This pulse ensures that there is no dead zone in the PFD transfer function, and minimizes phase noise and reference spurs. Two bits in the reference counter latch (ABP2 and ABP1) control the width of the pulse. See Figure 16 for details. The smallest antibacklash pulse width is not recommended.

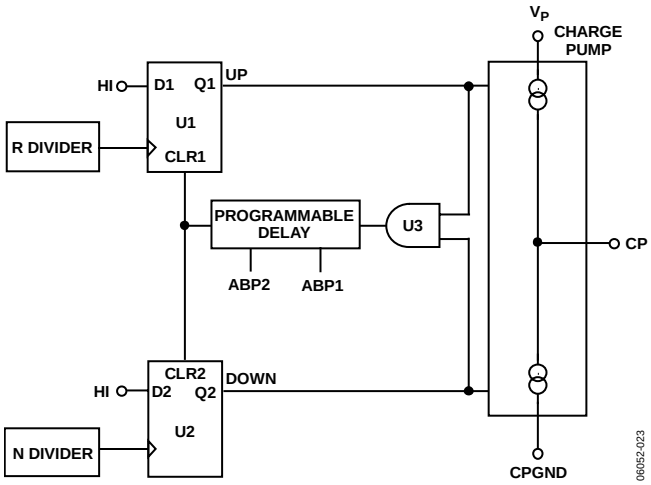


Figure 13. PFD Simplified Schematic and Timing (In Lock)

MUXOUT AND LOCK DETECT

The output multiplexer on the ADF4002 allows the user to access various internal points on the chip. The state of MUXOUT is controlled by M3, M2, and M1 in the function latch. Figure 18 shows the full truth table. Figure 14 shows the MUXOUT section in block diagram form.

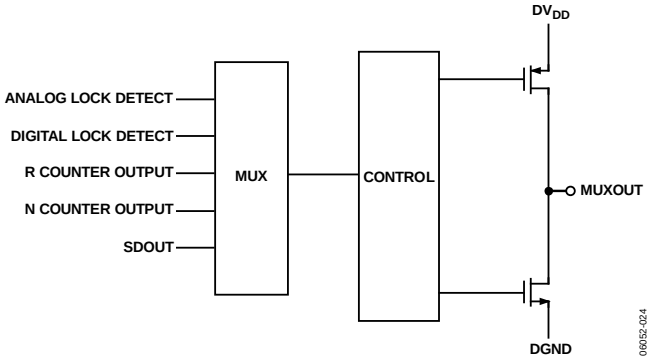


Figure 14. MUXOUT Circuit

Lock Detect

MUXOUT can be programmed for two types of lock detect: digital lock detect and analog lock detect.

Digital lock detect is active high. When LDP in the R counter latch is set to 0, digital lock detect is set high when the phase error on three consecutive phase detector (PD) cycles is less than 15 ns. With LDP set to 1, five consecutive cycles of less than 15 ns are required to set the lock detect. It stays set at high until a phase error of greater than 25 ns is detected on any subsequent PD cycle. For PFD frequencies greater than 10 MHz, analog lock detect is more accurate because of the smaller pulse widths.

The N-channel, open-drain, analog lock detect should be operated with an external pull-up resistor of 10 kΩ nominal. When lock has been detected, this output is high with narrow, low going pulses.

INPUT SHIFT REGISTER

The ADF4002 digital section includes a 24-bit input shift register, a 14-bit R counter, and a 13-bit N counter. Data is clocked into the 24-bit shift register on each rising edge of CLK. The data is clocked in MSB first. Data is transferred from the shift register to one of four latches on the rising edge of LE. The destination latch is determined by the state of the two control bits (C2, C1) in the shift register. These are the two LSBs, DB1 and DB0, as shown in the timing diagram (see Figure 2). Table 6 provides the truth table for these bits. Figure 15 shows a summary of how the latches are programmed.

Table 6. C2, C1 Truth Table

Control Bits		
C2	**C1**	**Data Latch**
0	0	R Counter
0	1	N Counter
1	0	Function Latch
1	1	Initialization Latch

LATCH MAPS AND DESCRIPTIONS

LATCH SUMMARY

REFERENCE COUNTER LATCH

RESERVED			LOCK DETECT PRECISION	TEST MODE BITS		ANTI-BACKLASH WIDTH		14-BIT REFERENCE COUNTER														CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
X	0	0	LDP	T2	T1	ABP2	ABP1	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (0)	C1 (0)

N COUNTER LATCH

RESERVED		CP GAIN	13-BIT N COUNTER													RESERVED						CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
X	X	G1	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	X	X	X	X	X	X	C2 (0)	C1 (1)

FUNCTION LATCH

RESERVED		POWER-DOWN 2	CURRENT SETTING 2			CURRENT SETTING 1			TIMER COUNTER CONTROL				FASTLOCK MODE	FASTLOCK ENABLE	CP THREE-STATE	PD POLARITY	MUXOUT CONTROL			POWER-DOWN 1	COUNTER RESET	CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
X	X	PD2	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	TC4	TC3	TC2	TC1	F5	F4	F3	F2	M3	M2	M1	PD1	F1	C2 (1)	C1 (0)

INITIALIZATION LATCH

RESERVED		POWER-DOWN 2	CURRENT SETTING 2			CURRENT SETTING 1			TIMER COUNTER CONTROL				FASTLOCK MODE	FASTLOCK ENABLE	CP THREE-STATE	PD POLARITY	MUXOUT CONTROL			POWER-DOWN 1	COUNTER RESET	CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
X	X	PD2	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	TC4	TC3	TC2	TC1	F5	F4	F3	F2	M3	M2	M1	PD1	F1	C2 (1)	C1 (1)

06052-015

Figure 15. Latch Summary

REFERENCE COUNTER LATCH MAP

RESERVED			LOCK DETECT PRECISION	TEST MODE BITS		ANTI-BACKLASH WIDTH		14-BIT REFERENCE COUNTER														CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
X	0	0	LDP	T2	T1	ABP2	ABP1	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (0)	C1 (0)

X = DON'T CARE

R14	R13	R12	.....	R3	R2	R1	DIVIDE RATIO
0	0	0	.....	0	0	1	1
0	0	0	.....	0	1	0	2
0	0	0	.....	0	1	1	3
0	0	0	.....	1	0	0	4
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
1	1	1	.....	1	0	0	16380
1	1	1	.....	1	0	1	16381
1	1	1	.....	1	1	0	16382
1	1	1	.....	1	1	1	16383

ABP2	ABP1	ANTIBACKLASH PULSE WIDTH
0	0	2.9ns
0	1	NOT ALLOWED
1	0	6.0ns
1	1	2.9ns

TEST MODE BITS SHOULD BE SET TO 00 FOR NORMAL OPERATION.

LDP	OPERATION
0	THREE CONSECUTIVE CYCLES OF PHASE DELAY LESS THAN 15ns MUST OCCUR BEFORE LOCK DETECT IS SET.
1	FIVE CONSECUTIVE CYCLES OF PHASE DELAY LESS THAN 15ns MUST OCCUR BEFORE LOCK DETECT IS SET.

BOTH OF THESE BITS MUST BE SET TO 0 FOR NORMAL OPERATION.

06052-025

Figure 16. Reference Counter Latch Map

N COUNTER LATCH MAP

RESERVED		CP GAIN	13-BIT N COUNTER												RESERVED						CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
X	X	G1	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	X	X	X	X	X	X	C2 (0)	C1 (1)

X = DON'T CARE

N13	N12	N11		N3	N2	N1	N COUNTER DIVIDE RATIO
0	0	0	.....	0	0	0	NOT ALLOWED
0	0	0	.....	0	0	1	1
0	0	0	.....	0	1	0	2
0	0	0	.....	0	1	1	3
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
1	1	1	.....	1	0	0	8188
1	1	1	.....	1	0	1	8189
1	1	1	.....	1	1	0	8190
1	1	1	.....	1	1	1	8191

F4 (FUNCTION LATCH) FASTLOCK ENABLE	CP GAIN	OPERATION
0	0	CHARGE PUMP CURRENT SETTING 1 IS PERMANENTLY USED.
0	1	CHARGE PUMP CURRENT SETTING 2 IS PERMANENTLY USED.
1	0	CHARGE PUMP CURRENT SETTING 1 IS USED.
1	1	CHARGE PUMP CURRENT IS SWITCHED TO SETTING 2. THE TIME SPENT IN SETTING 2 IS DEPENDENT ON WHICH FASTLOCK MODE IS USED. SEE FUNCTION LATCH DESCRIPTION.

THESE BITS ARE NOT USED BY THE DEVICE AND ARE DON'T CARE BITS.

THESE BITS ARE NOT USED BY THE DEVICE AND ARE DON'T CARE BITS.

06052-016

Figure 17. N Counter Latch Map

FUNCTION LATCH MAP

RESERVED		POWER-DOWN 2	CURRENT SETTING 2			CURRENT SETTING 1			TIMER COUNTER CONTROL				FASTLOCK MODE	FASTLOCK ENABLE	CP THREE-STATE	PD POLARITY	MUXOUT CONTROL			POWER-DOWN 1	COUNTER RESET	CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
X	X	PD2	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	TC4	TC3	TC2	TC1	F5	F4	F3	F2	M3	M2	M1	PD1	F1	C2 (1)	C1 (0)

F2	PHASE DETECTOR POLARITY
0	NEGATIVE
1	POSITIVE

F1	COUNTER OPERATION
0	NORMAL
1	R COUNTER AND N COUNTER HELD IN RESET

F3	CHARGE PUMP OUTPUT
0	NORMAL
1	THREE-STATE

F4	F5	FASTLOCK MODE
0	X	FASTLOCK DISABLED
1	0	FASTLOCK MODE 1
1	1	FASTLOCK MODE 2

TC4	TC3	TC2	TC1	TIMEOUT (PFD CYCLES)
0	0	0	0	3
0	0	0	1	7
0	0	1	0	11
0	0	1	1	15
0	1	0	0	19
0	1	0	1	23
0	1	1	0	27
0	1	1	1	31
1	0	0	0	35
1	0	0	1	39
1	0	1	0	43
1	0	1	1	47
1	1	0	0	51
1	1	0	1	55
1	1	1	0	59
1	1	1	1	63

SEE PAGE 15

M3	M2	M1	OUTPUT
0	0	0	THREE-STATE OUTPUT
0	0	1	DIGITAL LOCK DETECT (ACTIVE HIGH)
0	1	0	N DIVIDER OUTPUT
0	1	1	DV_{DD}
1	0	0	R DIVIDER OUTPUT
1	0	1	N-CHANNEL OPEN-DRAIN LOCK DETECT
1	1	0	SERIAL DATA OUTPUT
1	1	1	DGND

CPI6	CPI5	CP14	I_{CP} (mA)		
CPI3	CPI2	CPI1	3kΩ	5.1kΩ	11kΩ
0	0	0	1.088	0.625	0.294
0	0	1	2.176	1.250	0.588
0	1	0	3.264	1.875	0.882
0	1	1	4.352	2.500	1.176
1	0	0	5.440	3.125	1.470
1	0	1	6.528	3.750	1.764
1	1	0	7.616	4.375	2.058
1	1	1	8.704	5.000	2.352

CE PIN	PD2	PD1	MODE
0	X	X	ASYNCHRONOUS POWER-DOWN
1	X	0	NORMAL OPERATION
1	0	1	ASYNCHRONOUS POWER-DOWN
1	1	1	SYNCHRONOUS POWER-DOWN

THESE BITS ARE NOT USED BY THE DEVICE AND ARE DON'T CARE BITS.

06052-017

Figure 18. Function Latch Map

INITIALIZATION LATCH MAP

RESERVED		POWER-DOWN 2	CURRENT SETTING 2			CURRENT SETTING 1			TIMER COUNTER CONTROL				FASTLOCK MODE	FASTLOCK ENABLE	CP THREE-STATE	PD POLARITY	MUXOUT CONTROL			POWER-DOWN 1	COUNTER RESET	CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
X	X	PD2	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	TC4	TC3	TC2	TC1	F5	F4	F3	F2	M3	M2	M1	PD1	F1	C2 (1)	C1 (1)

F2	PHASE DETECTOR POLARITY
0	NEGATIVE
1	POSITIVE

F1	COUNTER OPERATION
0	NORMAL
1	R COUNTER AND N COUNTER HELD IN RESET

F3	CHARGE PUMP OUTPUT
0	NORMAL
1	THREE-STATE

F4	F5	FASTLOCK MODE
0	X	FASTLOCK DISABLED
1	0	FASTLOCK MODE 1
1	1	FASTLOCK MODE 2

TC4	TC3	TC2	TC1	TIMEOUT (PFD CYCLES)
0	0	0	0	3
0	0	0	1	7
0	0	1	0	11
0	0	1	1	15
0	1	0	0	19
0	1	0	1	23
0	1	1	0	27
0	1	1	1	31
1	0	0	0	35
1	0	0	1	39
1	0	1	0	43
1	0	1	1	47
1	1	0	0	51
1	1	0	1	55
1	1	1	0	59
1	1	1	1	63

SEE PAGE 16

M3	M2	M1	OUTPUT
0	0	0	THREE-STATE OUTPUT
0	0	1	DIGITAL LOCK DETECT (ACTIVE HIGH)
0	1	0	N DIVIDER OUTPUT
0	1	1	DV_{DD}
1	0	0	R DIVIDER OUTPUT
1	0	1	N-CHANNEL OPEN-DRAIN LOCK DETECT
1	1	0	SERIAL DATA OUTPUT
1	1	1	DGND

CPI6	CPI5	CP14	I_{CP} (mA)		
CPI3	CPI2	CPI1	3kΩ	5.1kΩ	11kΩ
0	0	0	1.088	0.625	0.294
0	0	1	2.176	1.250	0.588
0	1	0	3.264	1.875	0.882
0	1	1	4.352	2.500	1.176
1	0	0	5.440	3.125	1.470
1	0	1	6.528	3.750	1.764
1	1	0	7.616	4.375	2.058
1	1	1	8.704	5.000	2.352

CE PIN	PD2	PD1	MODE
0	X	X	ASYNCHRONOUS POWER-DOWN
1	X	0	NORMAL OPERATION
1	0	1	ASYNCHRONOUS POWER-DOWN
1	1	1	SYNCHRONOUS POWER-DOWN

THESE BITS ARE NOT USED BY THE DEVICE AND ARE DON'T CARE BITS.

06052-036

Figure 19. Initialization Latch Map

FUNCTION LATCH

With C2, C1 set to 1, 0, the on-chip function latch is programmed. Figure 18 shows the input data format for programming the function latch.

Counter Reset

DB2 (F1) is the counter reset bit. When this bit is set to 1, the R counter and the N counter are reset. For normal operation, set this bit to 0. Upon powering up, the F1 bit needs to be disabled (set to 0). Then, the N counter resumes counting in close alignment with the R counter (the maximum error is one prescaler cycle).

Power-Down

DB3 (PD1) and DB21 (PD2) provide programmable power-down modes. These bits are enabled by the CE pin.

When the CE pin is low, the device is immediately disabled regardless of the states of the PD2, PD1 bits.

In the programmed asynchronous power-down, the device powers down immediately after latching a 1 into Bit PD1, with the condition that Bit PD2 has been loaded with a 0.

In the programmed synchronous power-down, the device power-down is gated by the charge pump to prevent unwanted frequency jumps. Once the power-down is enabled by writing a 1 into Bit PD1 (on condition that a 1 has also been loaded to Bit PD2), then the device enters power-down on the occurrence of the next charge pump event.

When a power-down is activated (either in synchronous or asynchronous mode, including a CE pin activated power-down), the following events occur:

- All active dc current paths are removed.
- The R, N, and timeout counters are forced to their load state conditions.
- The charge pump is forced into three-state mode.
- The digital lock detect circuitry is reset.
- The RFIN input is debiased.
- The reference input buffer circuitry is disabled.
- The input register remains active and capable of loading and latching data.

MUXOUT Control

The on-chip multiplexer is controlled by M3, M2, and M1 on the ADF4002. Figure 18 shows the truth table.

Fastlock Enable Bit

DB9 of the function latch is the fastlock enable bit. Only when this is 1 is fastlock enabled.

Fastlock Mode Bit

DB10 of the function latch is the fastlock mode bit. When fastlock is enabled, this bit determines the fastlock mode to be used. If the fastlock mode bit is 0, then Fastlock Mode 1 is selected, and if the fastlock mode bit is 1, then Fastlock Mode 2 is selected.

Fastlock Mode 1

In this mode, the charge pump current is switched to the contents of Current Setting 2. The device enters fastlock by having a 1 written to the CP gain bit in the N counter latch. The device exits fastlock by having a 0 written to the CP gain bit in the AB counter latch.

Fastlock Mode 2

In this mode, the charge pump current is switched to the contents of Current Setting 2. The device enters fastlock by having a 1 written to the CP gain bit in the N counter latch. The device exits fastlock under the control of the timer counter. After the timeout period determined by the value in TC4 to TC1, the CP gain bit in the N counter latch is automatically reset to 0 and the device reverts to normal mode instead of fastlock. See Figure 18 for the timeout periods.

Timer Counter Control

The user has the option of programming two charge pump currents. The intent is to use the Current Setting 1 when the RF output is stable and the system is in a static state. Current Setting 2 is meant to be used when the system is dynamic and in a state of change, that is, when a new output frequency is programmed.

The normal sequence of events is as follows:

The user initially decides the referred charge pump currents. For example, the choice can be 2.5 mA as Current Setting 1 and 5 mA as Current Setting 2.

At the same time, the decision must be made as to how long the secondary current is to stay active before reverting to the primary current. This is controlled by Timer Counter Control Bit DB14 to Timer Counter Control Bit DB11 (TC4 to TC1) in the function latch. See Figure 18 for the truth table.

To program a new output frequency, simply program the N counter latch with a new value for N. At the same time, the CP gain bit can be set to 1. This sets the charge pump with the value in CPI6 to CPI4 for a period of time determined by TC4 to TC1. When this time is up, the charge pump current reverts to the value set by CPI3 to CPI1. At the same time, the CP gain bit in the N counter latch is reset to 0 and is ready for the next time that the user wishes to change the frequency.

Note that there is an enable feature on the timer counter. It is enabled when Fastlock Mode 2 is chosen by setting the Fastlock Mode Bit DB10 in the function latch to 1.

Charge Pump Currents

CPI3, CPI2, and CPI1 program Current Setting 1 for the charge pump. CPI6, CPI5, and CPI4 program Current Setting 2 for the charge pump. See Figure 18 for the truth table.

PD Polarity

This bit sets the phase detector polarity bit (see Figure 18).

CP Three-State

This bit controls the CP output pin. Setting the bit high puts the CP output into three-state. With the bit set low, the CP output is enabled.

INITIALIZATION LATCH

The initialization latch is programmed when C2, C1 = 1, 1. This is essentially the same as the function latch (programmed when C2, C1 = 1, 0).

However, when the initialization latch is programmed there is an additional internal reset pulse applied to the R and N counters. This pulse ensures that the N counter is at load point when the N counter data is latched and the device begins counting in close phase alignment.

If the latch is programmed for synchronous power-down (CE pin is high; PD1 bit is high; and PD2 bit is low), the internal pulse also triggers this power-down. The prescaler reference and the oscillator input buffer are unaffected by the internal reset pulse, thereby maintaining close phase alignment when counting resumes.

When the first N counter data is latched after initialization, the internal reset pulse is reactivated. However, successive AB counter loads after this do not trigger the internal reset pulse.

Device Programming After Initial Power-Up

After initially powering up the device, there are three ways to program the device.

Initialization Latch Method

1. Apply V_{DD}.
2. Program the initialization latch (11 in two LSBs of input word). Make sure that the F1 bit is programmed to 0.
3. Conduct a function latch load (10 in two LSBs of the control word). Make sure that the F1 bit is programmed to 0.
4. Perform an R load (00 in two LSBs).
5. Perform an N load (01 in two LSBs).

When the initialization latch is loaded, the following occurs:

- The function latch contents are loaded.
- An internal pulse resets the R, N, and timeout counters to load state conditions and three-states the charge pump. Note that the prescaler band gap reference and the oscillator input buffer are unaffected by the internal reset pulse, allowing close phase alignment when counting resumes.
- Latching the first N counter data after the initialization word activates the same internal reset pulse. Successive N loads do not trigger the internal reset pulse unless there is another initialization.

CE Pin Method

1. Apply V_{DD}.
2. Bring CE low to put the device into power-down. This is an asynchronous power-down because it happens immediately.
3. Program the function latch (10).
4. Program the R counter latch (00).
5. Program the N counter latch (01).
6. Bring CE high to take the device out of power-down. The R and N counters resume counting in close alignment. Note that after CE goes high, a duration of 1 µs can be required for the prescaler band gap voltage and oscillator input buffer bias to reach steady state.

CE can be used to power the device up and down to check for channel activity. The input register does not need to be reprogrammed each time the device is disabled and enabled, as long as it has been programmed at least once after V_{DD} was initially applied.

Counter Reset Method

1. Apply V_{DD}.
2. Do a function latch load (10 in two LSBs). As part of this step, load 1 to the F1 bit. This enables the counter reset.
3. Perform an R counter load (00 in two LSBs).
4. Perform an N counter load (01 in two LSBs).
5. Do a function latch load (10 in two LSBs). As part of this step, load 0 to the F1 bit. This disables the counter reset.

This sequence provides the same close alignment as the initialization method. It offers direct control over the internal reset. Note that counter reset holds the counters at load point and three-states the charge pump, but does not trigger synchronous power-down.

APPLICATIONS INFORMATION

VERY LOW JITTER ENCODE CLOCK FOR HIGH SPEED CONVERTERS

Figure 20 shows the ADF4002 with a VCXO to provide the encode clock for a high speed analog-to-digital converter (ADC).

The converter used in this application is an AD9215-80, a 12-bit converter that accepts up to an 80 MHz encode clock. To realize a stable low jitter clock, use a 77.76 MHz, narrow-band VCXO. This example assumes a 19.44 MHz reference clock.

To minimize the phase noise contribution of the ADF4002, the smallest multiplication factor of 4 is used. Thus, the R divider is programmed to 1, and the N divider is programmed to 4.

The charge pump output of the ADF4002 (Pin 2) drives the loop filter. The loop filter bandwidth is optimized for the best possible rms jitter, a key factor in the signal-to-noise ratio (SNR) of the ADC. Too narrow a bandwidth allows the VCXO noise to dominate at small offsets from the carrier frequency. Too wide a bandwidth allows the ADF4002 noise to dominate at offsets where the VCXO noise is lower than the ADF4002 noise. Thus, the intersection of the VCXO noise and the ADF4002 in-band noise is chosen as the optimum loop filter bandwidth.

The design of the loop filter uses the ADIsimPLL (Version 3.0) and is available as a free download from www.analog.com/ADIsimPLL. The rms jitter is measured at <1.2 ps. This level is lower than the maximum allowable 6 ps rms required to ensure the theoretical SNR performance of 59 dB for this converter.

The setup shown in Figure 20 using the ADF4002, AD9215, and an ADC FIFO evaluation board allows the user to quickly and effectively determine the suitability of the converter and encode clock. The SPI® interface is used to control the ADF4002, and the USB interface helps control the operation of the AD9215-80. The controller board sends back FFT information to the PC that, if using an ADC analyzer, provides all conversion results from the ADC.

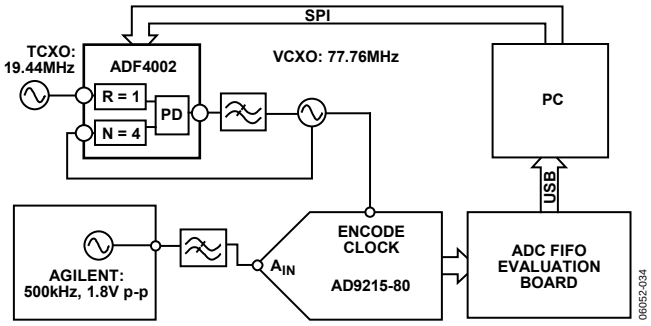


Figure 20. ADF4002 as Encode Clock

PFD

As the ADF4002 permits both R and N counters to be programmed to 1, the part can effectively be used as a standalone PFD and charge pump. This is particularly useful in either a clock cleaning application or a high performance LO. Additionally, the very low normalized phase noise floor (−222 dBc/Hz) enables very low in-band phase noise levels. It is possible to operate the PFD up to a maximum frequency of 104 MHz.

In Figure 21, the reference frequency equals the PFD; therefore, R = 1. The charge pump output integrates into a stable control voltage for the VCXO, and the output from the VCXO is divided down to the desired PFD frequency using an external divider.

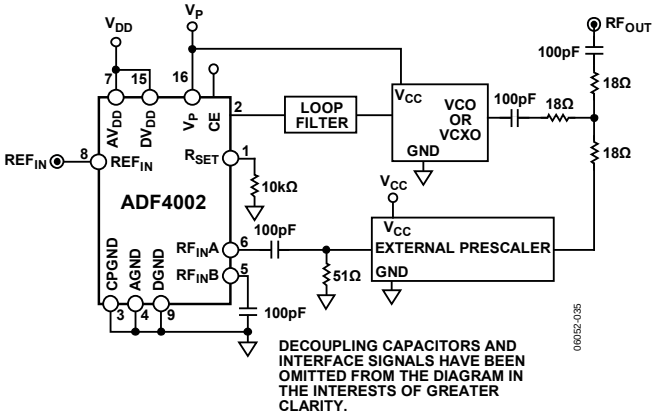


Figure 21. ADF4002 as a PFD

INTERFACING

The ADF4002 has a simple SPI-compatible serial interface for writing to the device. CLK, DATA, and LE control the data transfer. When the latch enable (Pin LE) goes high, the 24 bits that have been clocked into the input register on each rising edge of CLK are transferred to the appropriate latch. For more information, see Figure 2 for the timing diagram and Table 6 for the latch truth table.

The maximum allowable serial clock rate is 20 MHz. This means that the maximum update rate possible for the device is 833 kHz, or one update every 1.2 µs. This is certainly more than adequate for systems that have typical lock times in hundreds of microseconds.

ADuC812 Interface

Figure 22 shows the interface between the ADF4002 and the ADuC812 MicroConverter®. Because the ADuC812 is based on an 8051 core, this interface can be used with any 8051-based microcontroller. The MicroConverter is set up for SPI master mode with CPHA = 0. To initiate the operation, the I/O port driving LE is brought low. Each latch of the ADF4002 needs a 24-bit word. This is accomplished by writing three 8-bit bytes from the MicroConverter to the device. When the third byte has been written, bring the LE input high to complete the transfer.

On first applying power to the ADF4002, it needs four writes (one each to the initialization latch, function latch, R counter latch, and N counter latch) for the output to become active.

I/O port lines on the ADuC812 are also used to control power-down (CE input) and to detect lock (MUXOUT configured as lock detect and polled by the port input).

When operating in the SPI master mode, the maximum SCLOCK rate of the ADuC812 is 4 MHz. This means that the maximum rate at which the output frequency can be changed is 166 kHz.

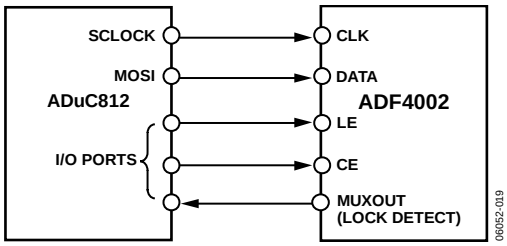


Figure 22. ADuC812 to ADF4002 Interface

ADSP-2181 Interface

Figure 23 shows the interface between the ADF4002 and the ADSP-2181 digital signal processor. The ADF4002 needs a 24-bit serial word for each latch write. The easiest way to accomplish this using the ADSP-2181 family is to use the autobuffered transmit mode of operation with alternate framing. This provides a means for transmitting an entire block of serial data before an interrupt is generated. Set up the word length for eight bits and use three memory locations for each 24-bit word. To program each 24-bit latch, store the three 8-bit bytes, enable the autobuffered mode, and then write to the transmit register of the DSP. This last operation initiates the autobuffer transfer.

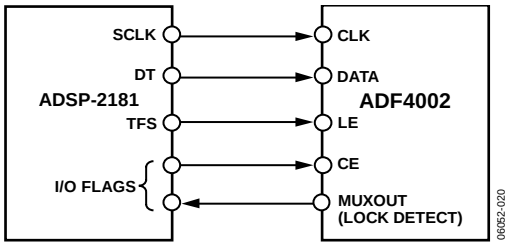


Figure 23. ADSP-2181 to ADF4002 Interface

PCB DESIGN GUIDELINES FOR CHIP SCALE PACKAGE

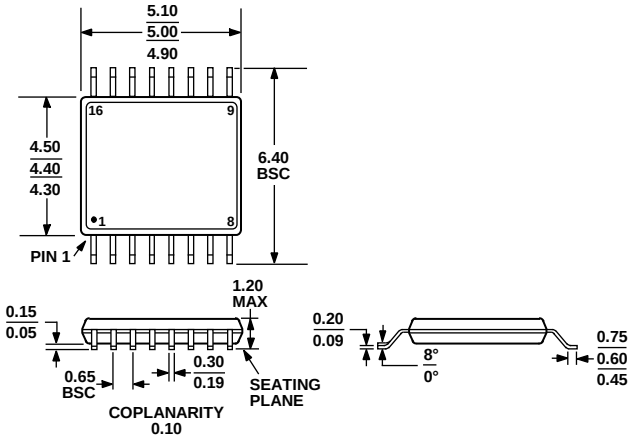
The lands on the lead frame chip scale package (CP-20-1) are rectangular. The printed circuit board pad for these should be 0.1 mm longer than the package land length and 0.05 mm wider than the package land width. The land should be centered on the pad. This ensures that the solder joint size is maximized. The bottom of the lead frame chip scale package has a central thermal pad.

The thermal pad on the printed circuit board should be at least as large as this exposed pad. On the printed circuit board, there should be a clearance of at least 0.25 mm between the thermal pad and the inner edges of the pad pattern. This ensures that shorting is avoided.

Thermal vias can be used on the printed circuit board thermal pad to improve thermal performance of the package. If vias are used, they should be incorporated into the thermal pad at a 1.2 mm pitch grid. The via diameter should be between 0.3 mm and 0.33 mm and the via barrel should be plated with 1 oz copper to plug the via.

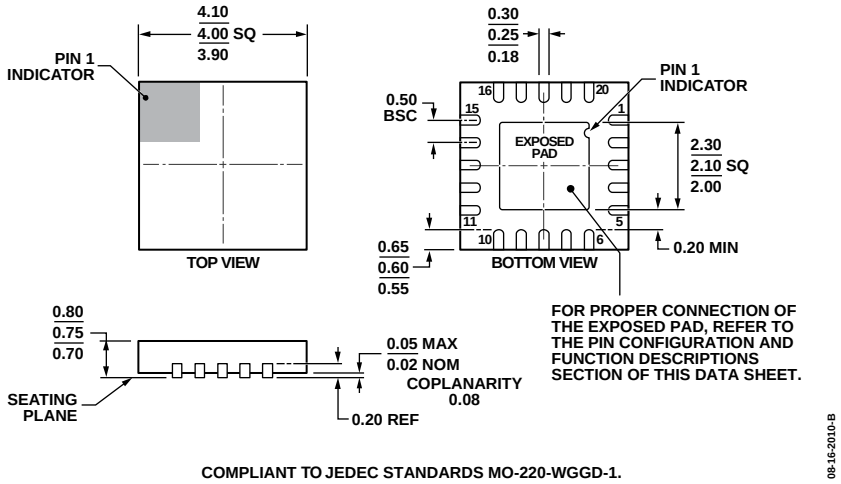
The user should connect the printed circuit board thermal pad to AGND.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 24. 16-Lead Thin Shrink Small Outline Package [TSSOP] (RU-16) Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WGGD-1.

Figure 25. 20-Lead Lead Frame Chip Scale Package [LFCSP] 4 mm × 4 mm Body, and 0.75 mm Package Height (CP-20-6) Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADF4002BRUZ	−40°C to +85°C	16-Lead TSSOP	RU-16
ADF4002BRUZ-RL	−40°C to +85°C	16-Lead TSSOP	RU-16
ADF4002BRUZ-RL7	−40°C to +85°C	16-Lead TSSOP	RU-16
ADF4002BCPZ	−40°C to +85°C	20-Lead LFCSP	CP-20-6
ADF4002BCPZ-RL	−40°C to +85°C	20-Lead LFCSP	CP-20-6
ADF4002BCPZ-RL7	−40°C to +85°C	20-Lead LFCSP	CP-20-6
EV-ADF4002SD1Z		Evaluation Board	
EV-ADF411XSD1Z		Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

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Мы молодая и активно развивающаяся компания в области поставок электронных компонентов. Мы поставляем электронные компоненты отечественного и импортного производства напрямую от производителей и с крупнейших складов мира.

Благодаря сотрудничеству с мировыми поставщиками мы осуществляем комплексные и плановые поставки широчайшего спектра электронных компонентов.

Собственная эффективная логистика и склад в обеспечивает надежную поставку продукции в точно указанные сроки по всей России.

Мы осуществляем техническую поддержку нашим клиентам и предпродажную проверку качества продукции. На все поставляемые продукты мы предоставляем гарантию .

Осуществляем поставки продукции под контролем ВП МО РФ на предприятия военно-промышленного комплекса России , а также работаем в рамках 275 ФЗ с открытием отдельных счетов в уполномоченном банке. Система менеджмента качества компании соответствует требованиям ГОСТ ISO 9001.

Минимальные сроки поставки, гибкие цены, неограниченный ассортимент и индивидуальный подход к клиентам являются основой для выстраивания долгосрочного и эффективного сотрудничества с предприятиями радиоэлектронной промышленности, предприятиями ВПК и научно-исследовательскими институтами России.

С нами вы становитесь еще успешнее!

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