FemtoClock® Crystal-to-HCSL Clock Generator

841608
Datasheet

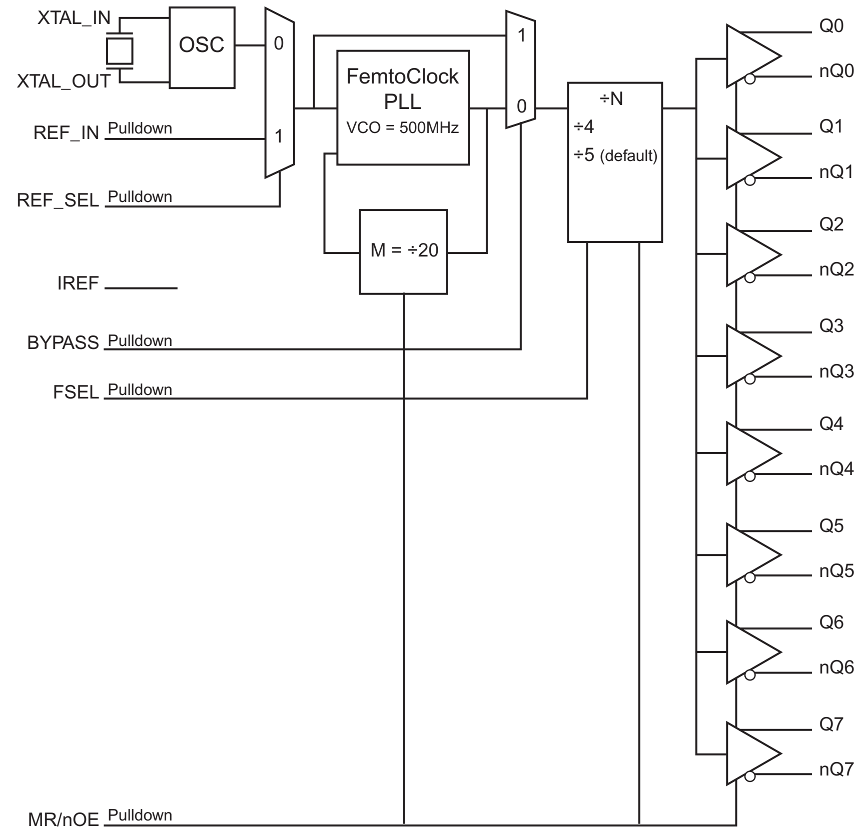
General Description

The 841608 is an optimized PCIe and sRIO clock generator. The device uses a 25MHz parallel crystal to generate 100MHz and 125MHz clock signals, replacing solutions requiring multiple oscillator and fanout buffer solutions. The device has excellent phase jitter (< 1ps rms) suitable to clock components requiring precise and low-jitter PCIe or sRIO or both clock signals. Designed for telecom, networking and industrial applications, the 841608 can also drive the high-speed sRIO and PCIe SerDes clock inputs of communication processors, DSPs, switches and bridges.

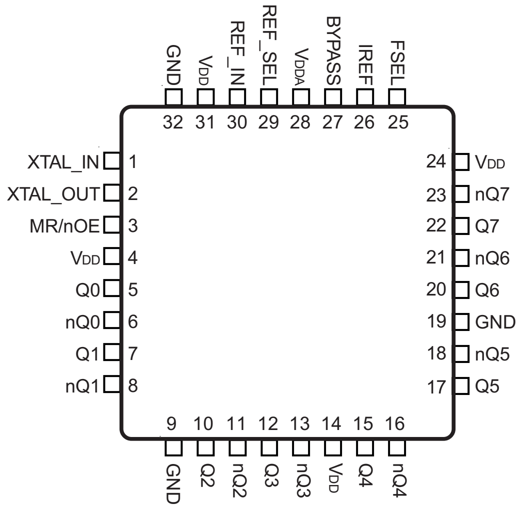
Features

- Eight HCSL outputs: configurable for PCIe (100MHz) and sRIO (125MHz) clock signals
- Selectable crystal oscillator interface, 25MHz, 18pF parallel resonant crystal or LVCMOS/LVTTL single-ended reference clock input
- Supports the following output frequencies: 100MHz or 125MHz
- VCO: 500MHz
- PLL bypass and output enable
- PCI Express (2.5 Gb/S) and Gen 2 (5 Gb/s) jitter compliant
- RMS phase jitter @ 125MHz, using a 25MHz crystal (1.875MHz – 20MHz): 0.37ps (typical)
- Full 3.3V operating supply
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Block Diagram



Pin Assignment



841608
32-Lead VFQFN
5mm x 5mm x 0.925mm package body
K Package
Top View

Pin Description and Pin Characteristic Tables

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	XTAL_IN, XTAL_OUT	Input		Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input.
3	MR/nOE	Input	Pulldown	Active HIGH master reset. Active LOW output enable. When logic HIGH, the internal dividers are reset and the outputs are in high impedance (Hi-Z). When logic LOW, the internal dividers and the outputs are enabled. Asynchronous function. LVCMOS/LVTTL interface levels. See Table 3D.
4, 14, 24, 31	V_{DD}	Power		Core supply pins.
5, 6	Q0, nQ0	Output		Differential output pair. HCSL interface levels.
7, 8	Q1, nQ1	Output		Differential output pair. HCSL interface levels.
9, 19, 32	GND	Power		Power supply ground.
10, 11	Q2, nQ2	Output		Differential output pair. HCSL interface levels.
12,13	Q3, nQ3	Output		Differential output pair. HCSL interface levels.
15, 16	Q4, nQ4	Output		Differential output pair. HCSL interface levels.
17, 18	Q5, nQ5	Output		Differential output pair. HCSL interface levels.
20, 21	Q6, nQ6	Output		Differential output pair. HCSL interface levels.
22, 23	Q7, nQ7	Output		Differential output pair. HCSL interface levels.
25	FSEL	Input	Pulldown	Output frequency select pin. LVCMOS/LVTTL interface levels. See Table 3B.
26	IREF	Output		HCSL current reference resistor output. An external fixed precision resistor (475Ω) from this pin to ground provides a reference current used for differential current-mode Qx, nQx clock outputs.
27	BYPASS	Input	Pulldown	Selects PLL operation/PLL bypass operation. Asynchronous function. LVCMOS/LVTTL interface levels. See Table 3C.
28	V_{DDA}	Power		Analog supply pin.
29	REF_SEL	Input	Pulldown	Reference select. Selects the input reference source. LVCMOS/LVTTL interface levels. See Table 3A.
30	REF_IN	Input	Pulldown	LVCMOS/LVTTL PLL reference clock input.

NOTE: *Pulldown* refers to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Function Tables

Table 3A. REF_SEL Function Table

Input	
REF_SEL	**Input Reference**
0	XTAL (default)
1	REF_IN

Table 3B. FSEL Function Table (f_{REF} = 25MHz)

Inputs		Outputs
FSEL	**N Divider**	**Q[0:7], nQ[0:7]**
0	5	VCO/5 (100MHz) PCIe (default)
1	4	VCO/4 (125MHz) sRIO

Table 3C. BYPASS Function Table

Input	
BYPASS	**PLL Configuration**
0	PLL enabled (default)
1	PLL bypassed ($f_{OUT} = f_{REF}/N$)

Table 3D. MR/nOE Function Table

Inputs	
MR/nOE	**Function**
0	Outputs enabled (default)
1	Device reset, outputs disabled (high-impedance)

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	**Rating**
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DD} + 0.5V
Package Thermal Impedance, θ_{JA}	37°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $T_A = -40°C$ to 85°C

Symbol	**Parameter**	**Test Conditions**	**Minimum**	**Typical**	**Maximum**	**Units**
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.15	3.3	V_{DD}	V
I_{DD}	Power Supply Current				87	mA
I_{DDA}	Analog Supply Current				15	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $T_A = -40°C$ to 85°C

Symbol	**Parameter**		**Test Conditions**	**Minimum**	**Typical**	**Maximum**	**Units**
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	REF_IN, REF_SEL, BYPASS, FSEL, MR/nOE	$V_{DD} = V_{IN} = 3.465V$			150	µA
I_{IL}	Input Low Current	REF_IN, REF_SEL, BYPASS, FSEL, MR/nOE	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-5			µA

Table 5. Crystal Characteristics

Parameter	**Test Conditions**	**Minimum**	**Typical**	**Maximum**	**Units**
Mode of Oscillation		Fundamental			
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

NOTE: Characterized using an 18pF parallel resonant crystal.

AC Electrical Characteristics

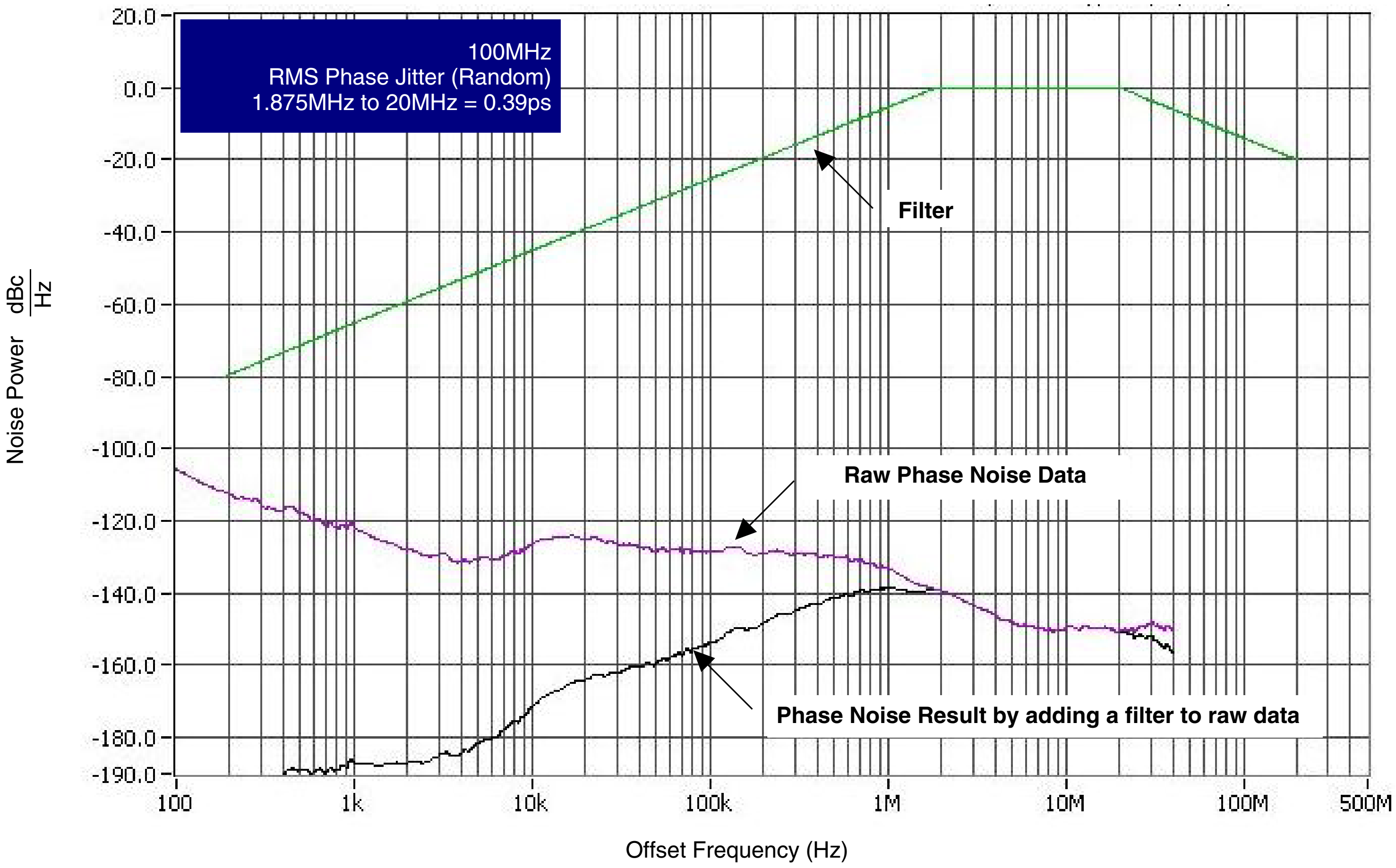
Table 6B. AC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency	VCO/5		100		MHz
		VCO/4		125		MHz
tjit(Ø)	RMS Phase Jitter (Random); NOTE 1	100MHz (1.875MHz – 20MHz)		0.39		ps
		125MHz (1.875MHz – 20MHz)		0.37		ps
t_j	Phase Jitter Peak-to-Peak; NOTE 2	100MHz, (1.2MHz – 50MHz 10^6 Samples, 25MHz Crystal Input		24.36		ps
		125MHz, (1.2MHz – 62.5MHz 10^6 Samples, 25MHz Crystal Input		23.76		ps
$t_{REFCLK\_HF\_RMS}$	Phase Jitter RMS; NOTE 3	100MHz, 10^6 Samples, 25MHz Crystal Input		2.44		ps
		125MHz, 10^6 Samples, 25MHz Crystal Input		2.37		ps
tjit(cc)	Cycle-to-Cycle Jitter; NOTE 4				50	ps
tsk(o)	Output Skew; NOTE 4, 5				105	ps
Rise Edge Rate	Rising Edge Rate; NOTE 6, 7		0.6		4	V/ns
Fall Edge Rate	Falling Edge Rate; NOTE 6, 7		0.6		4	V/ns
V_{RB}	Ringback Voltage; NOTE 6, 8		-100		100	mV
V_{MAX}	Absolute Maximum Output Voltage; NOTE 9, 10				1150	mV
V_{MIN}	Absolute Minimum Output Voltage; NOTE 9, 11		-300			mV
V_{CROSS}	Absolute Crossing Voltage; NOTE 9, 12, 13		250		550	mV
ΔV_{CROSS}	Total Variation of V_{CROSS}; NOTE 9, 12, 14				140	mV
odc	Output Duty Cycle; NOTE 6, 15		48		52	%
t_{STABLE}	Power-up Stable Clock Output; NOTE 6, 8		500			ps
t_L	PLL Lock Time				90	ms

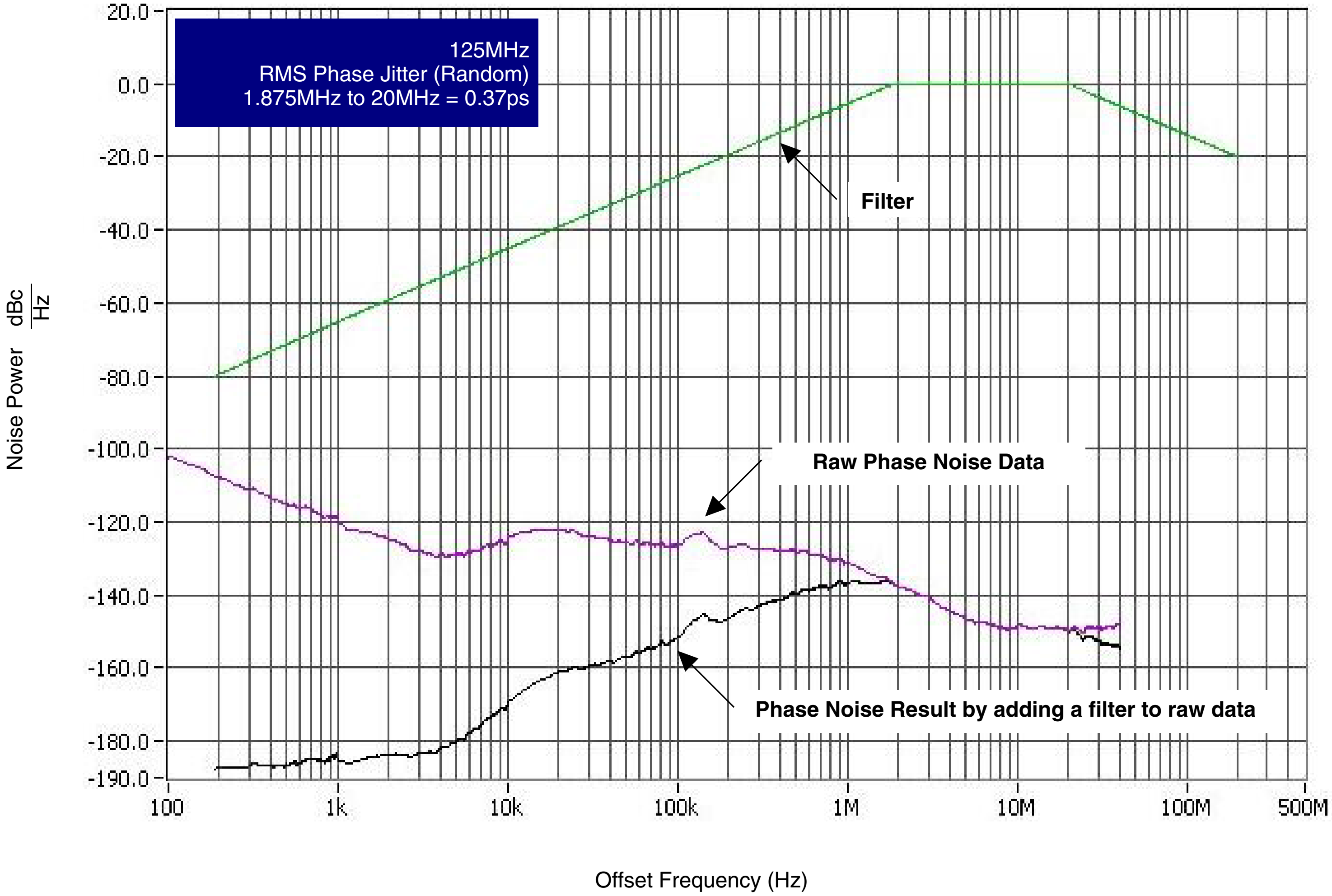
NOTE: All specifications are taken at 100MHz and 125MHz.
NOTE 1: Refer to the Phase Noise Plot.
NOTE 2: RMS jitter after applying system transfer function. See IDT Application Note, *PCI Express Reference Clock Requirements.* Maximum limit for PCI Express is 86ps peak-to-peak.
NOTE 3: RMS jitter after applying system transfer function. The pole frequencies for H1 and H2 for PCIe Gen 2 are 8-16MHz and 5-16MHz. See IDT Application Note, *PCI Express Reference Clock Requirements.* Maximum limit for PCI Express Generation 2 is 3.1ps RMS.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 5: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 6: Measurement taken from a differential waveform.
NOTE 7: Measured from -150mV to +150mV on the differential waveform (derived from Qx minus nQx). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing. See Parameter Measurement Information Section.
NOTE 8: T_{STABLE} is the time the differential clock must maintain a minimum ±150mV differential voltage after rising/falling edges before it is allowed to drop back into the V_{RB} ±100 differential range. See Parameter Measurement Information Section.
NOTE 9: Measurement taken from a single-ended waveform.
NOTE 10: Defined as the maximum instantaneous voltage including overshoot. See Parameter Measurement Information Section.
NOTE 11: Defined as the minimum instantaneous voltage including undershoot. See Parameter Measurement Information Section.

NOTE 12: Measured at crossing point where the instantaneous voltage value of the rising edge of Qx equals the falling edge of nQx. See Parameter Measurement Information Section.
NOTE 13: Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement. See Parameter Measurement Information Section.
NOTE 14: Defined as the total variation of all crossing voltage of rising Qx and falling nQx. This is the maximum allowed variance in the V_{CROSS} for any particular system. See Parameter Measurement Information Section.
NOTE 15: Input duty cycle must be 50%.

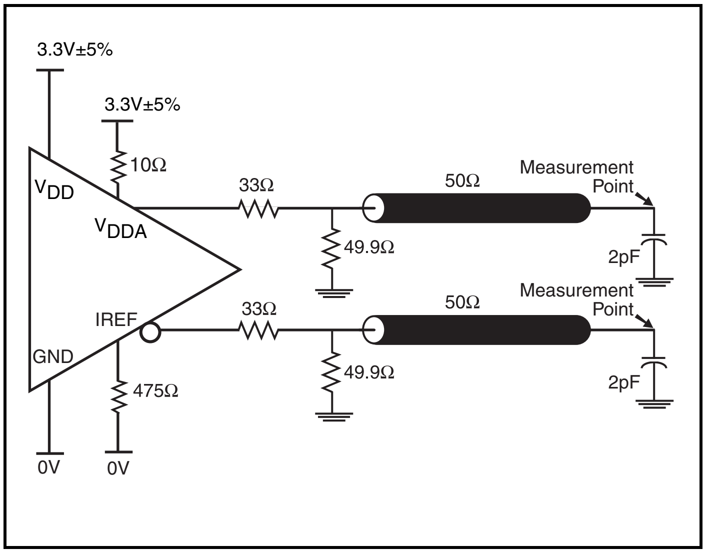
Typical Phase Noise at 100MHz



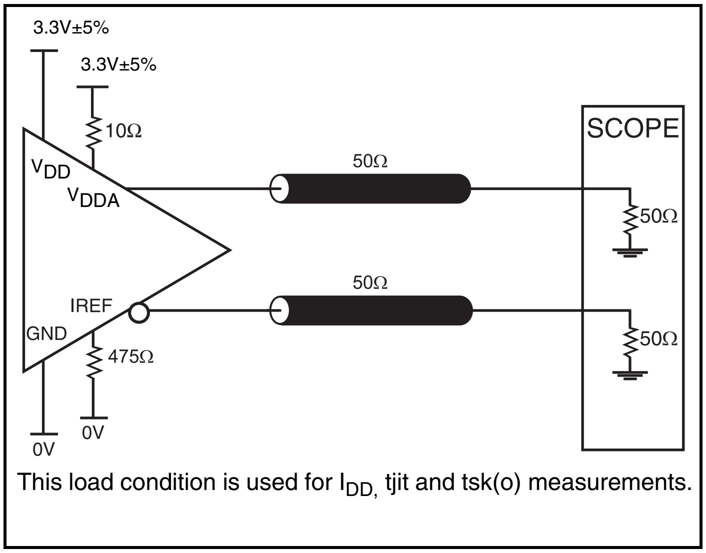
Typical Phase Noise at 125MHz



Parameter Measurement Information

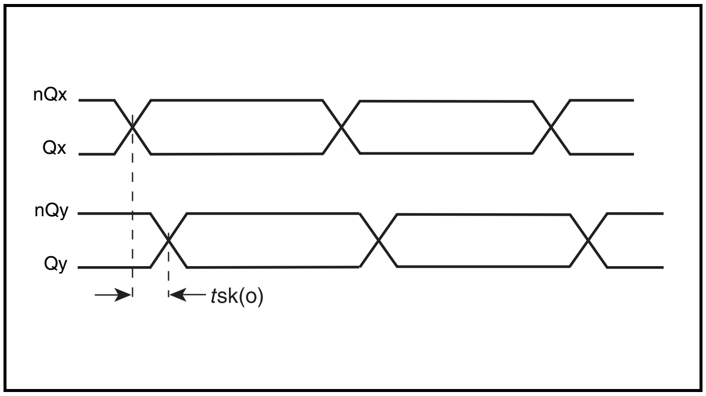


3.3V HCSL Output Load AC Test Circuit

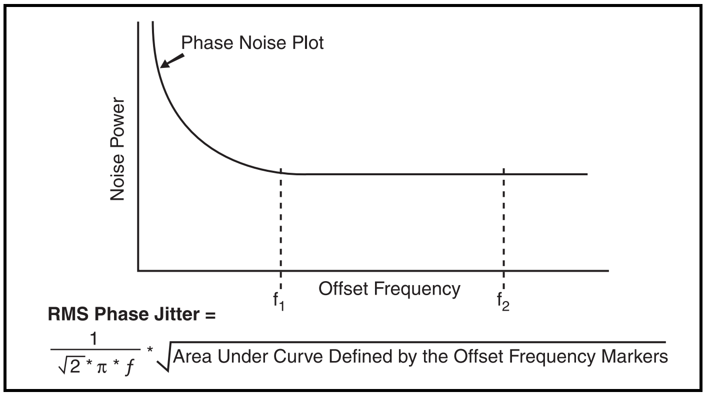


This load condition is used for I_{DD}, tjit and tsk(o) measurements.

3.3V HCSL Output Load AC Test Circuit



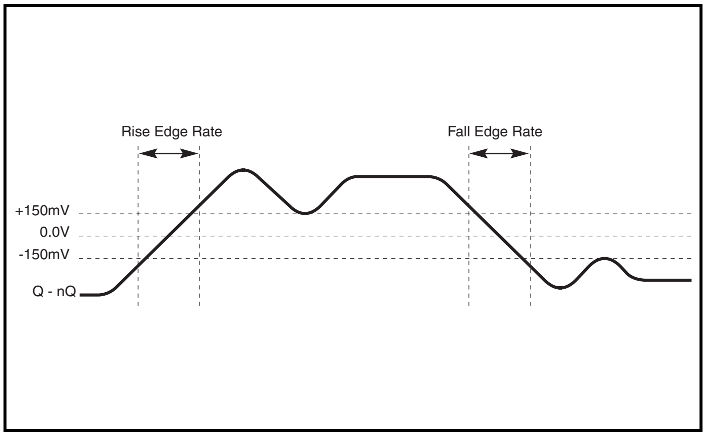
Output Skew



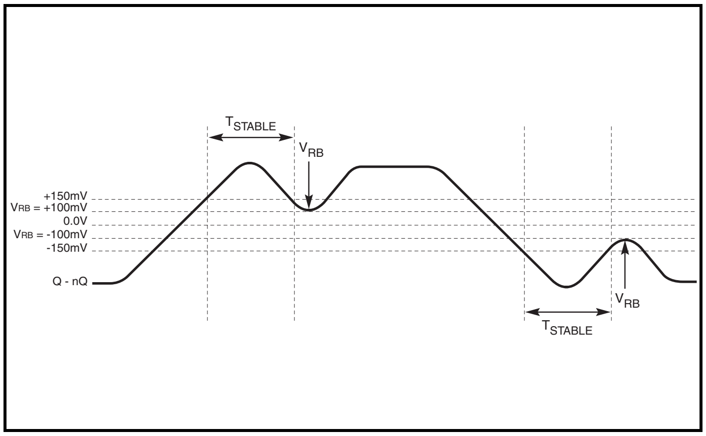
RMS Phase Jitter =

$$\frac{1}{\sqrt{2} * \pi * f} * \sqrt{\text{Area Under Curve Defined by the Offset Frequency Markers}}$$

RMS Phase Jitter

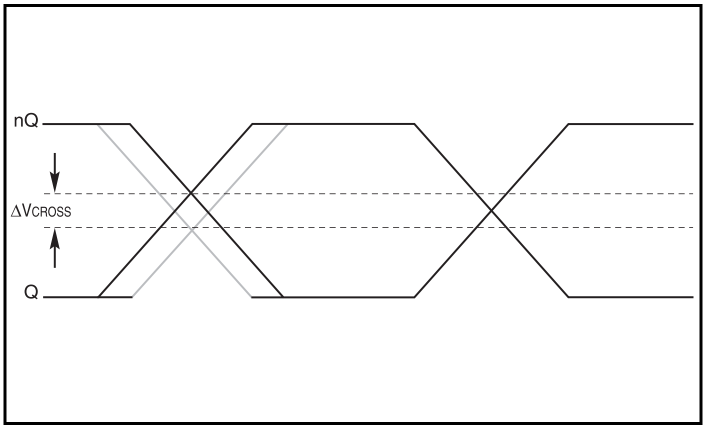


Differential Measurement Points for Rise/Fall Time

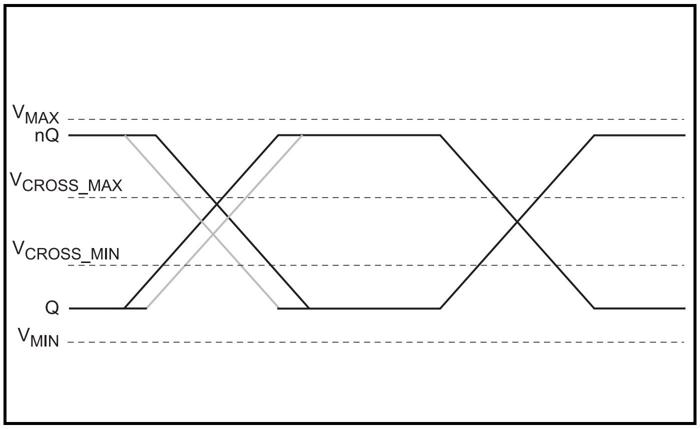


Differential Measurement Points for Ringback

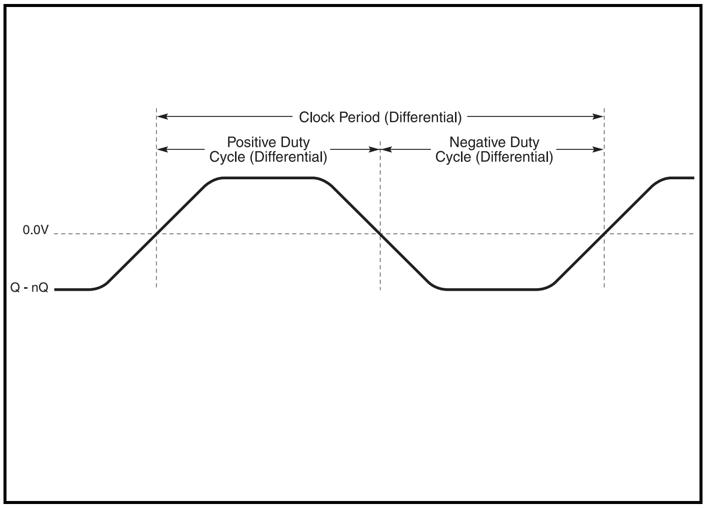
Parameter Measurement Information, continued



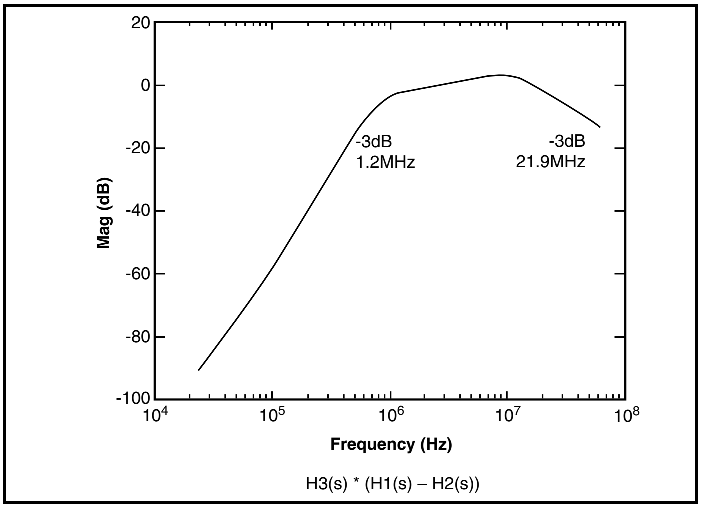
Single-ended Measurement Points for Delta Cross Point



Single-ended Measurement Points for Absolute Cross Point/Swing



Differential Measurement Points for Duty Cycle/Period



Composite PCIe Transfer Function

Applications Information

Recommendations for Unused Input and Output Pins

Inputs:

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

LVCMOS Control Pins

All control pins have internal pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

REF_IN Input

For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the REF_IN to ground.

Outputs:

HCSL Outputs

All unused HCSL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 841608 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD} and V_{DDA} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{DDA} pin.

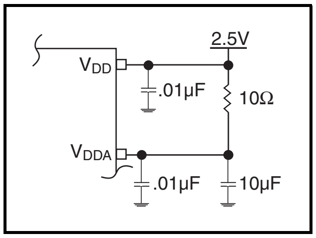


Figure 1. Power Supply Filtering

Crystal Input Interface

The 841608 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in Figure 2 below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.

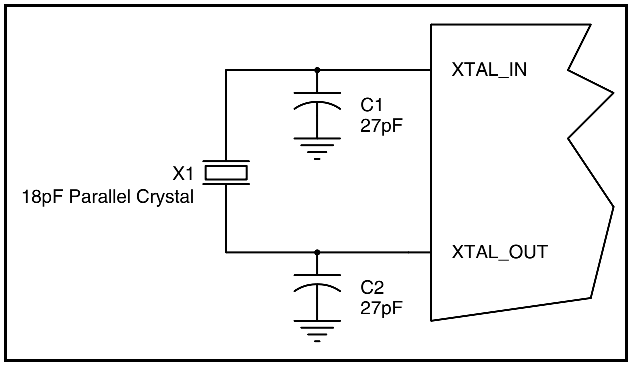


Figure 2. Crystal Input Interface

LVCMOS to XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupler capacitor. A general interface diagram is shown in *Figure 3.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.

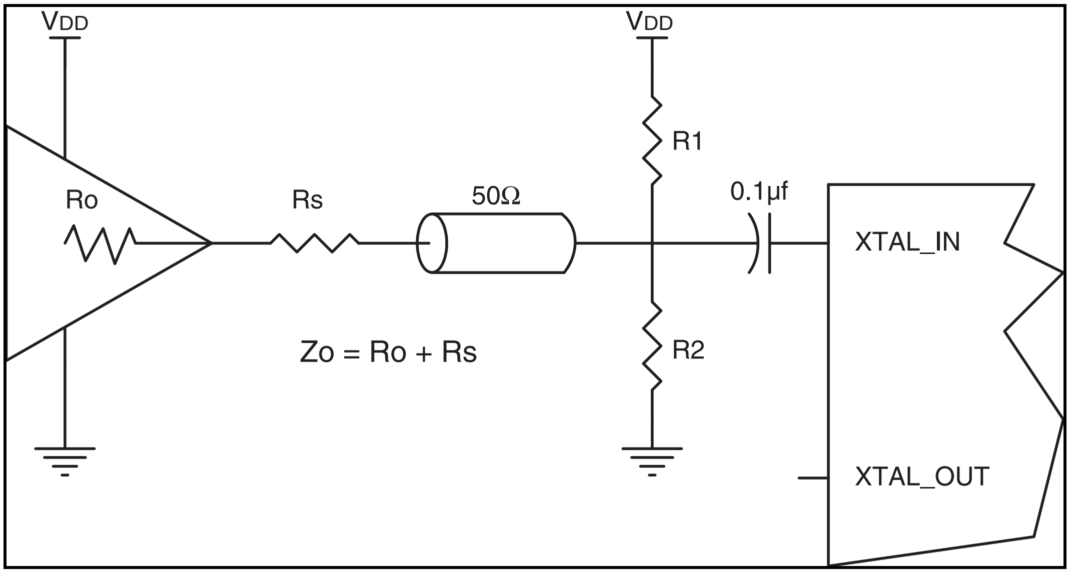


Figure 3. General Diagram for LVCMOS Driver to XTAL Input Interface

Recommended Termination

Figure 4A is the recommended termination for applications which require the receiver and driver to be on a separate PCB. All traces should be 50Ω impedance.

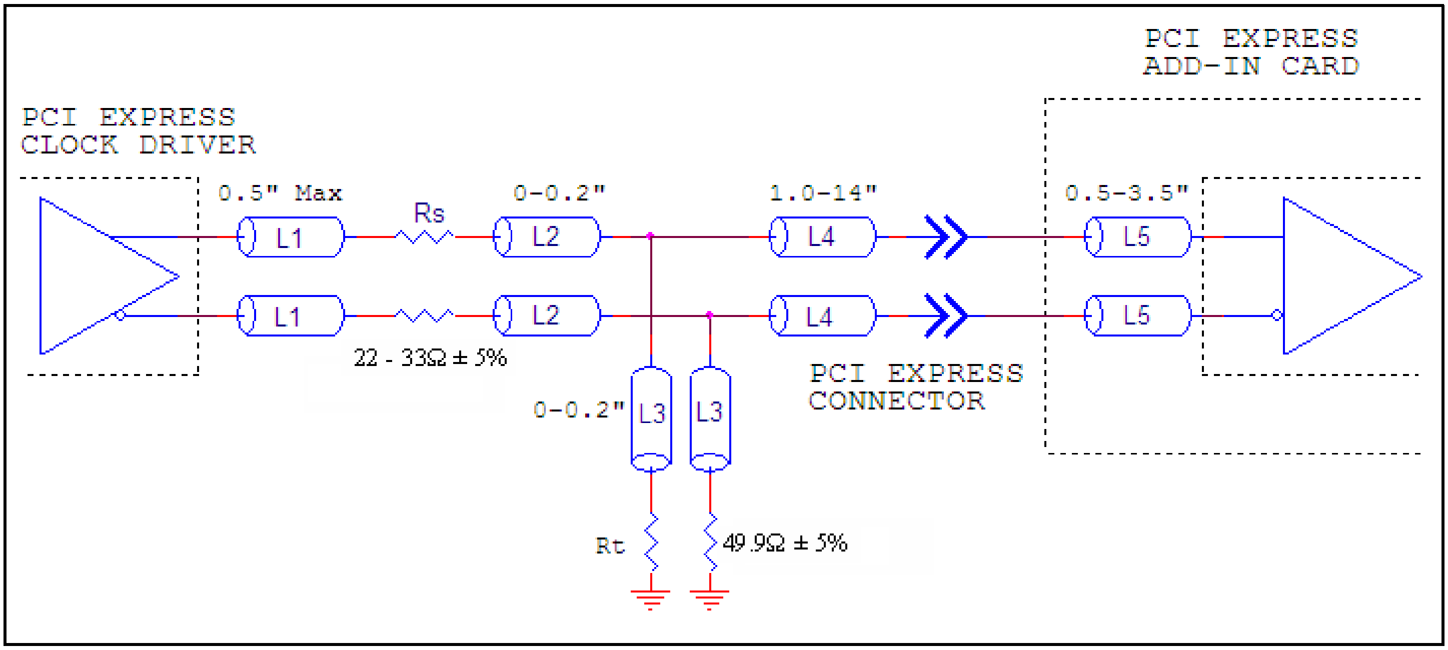


Figure 4A. Recommended Termination

Figure 4B is the recommended termination for applications which require a point to point connection and contain the driver and receiver on the same PCB. All traces should all be 50Ω impedance.

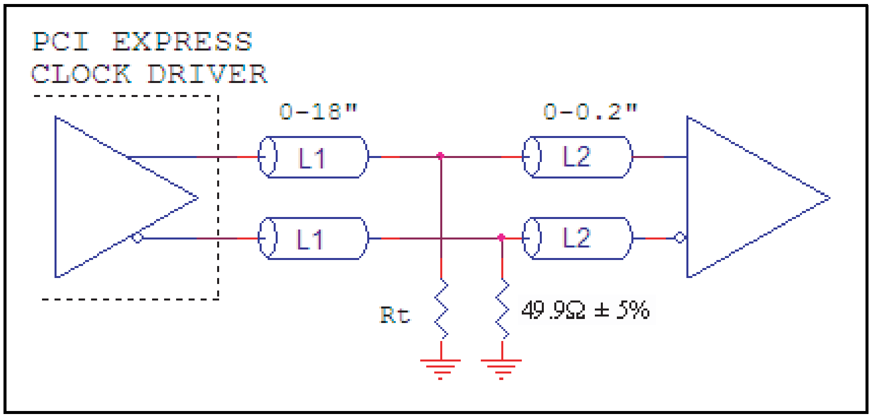


Figure 4A. Recommended Termination

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 5.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as "heat pipes". The number of vias (i.e. "heat pipes") are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor's Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

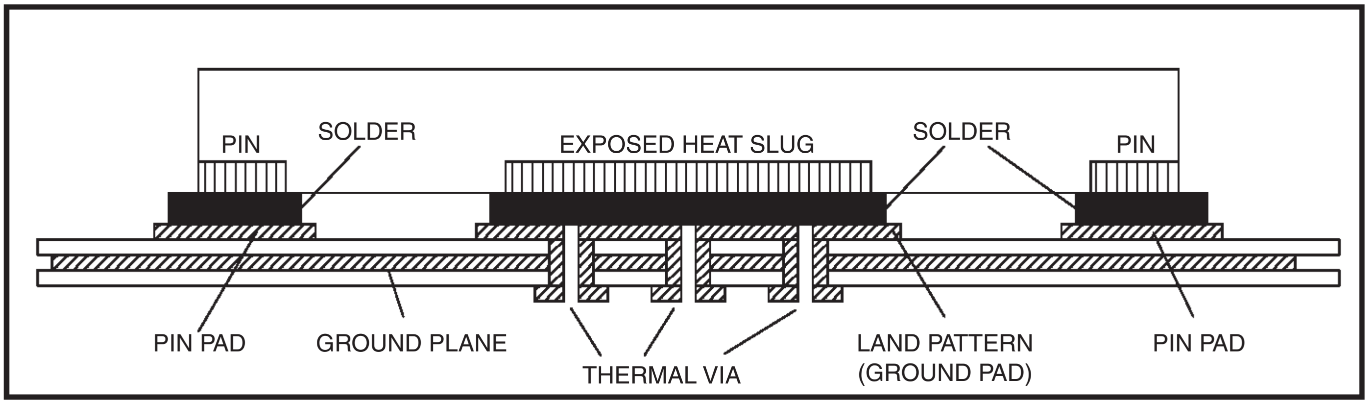


Figure 5. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Schematic Example

Figure 6 shows an example of 841608 application schematic. In this example, the device is operated at V_{DD} = 3.3V. The 18pF parallel resonant 25MHz crystal is used. The C1 = 27pF and C2 = 27pF are recommended for frequency accuracy. For different board layout, the C1 and C2 may be slightly adjusted for optimizing frequency accuracy. Two examples of HCSL terminations are shown in this schematic. The decoupling capacitors should be located as close as possible to the power pin.

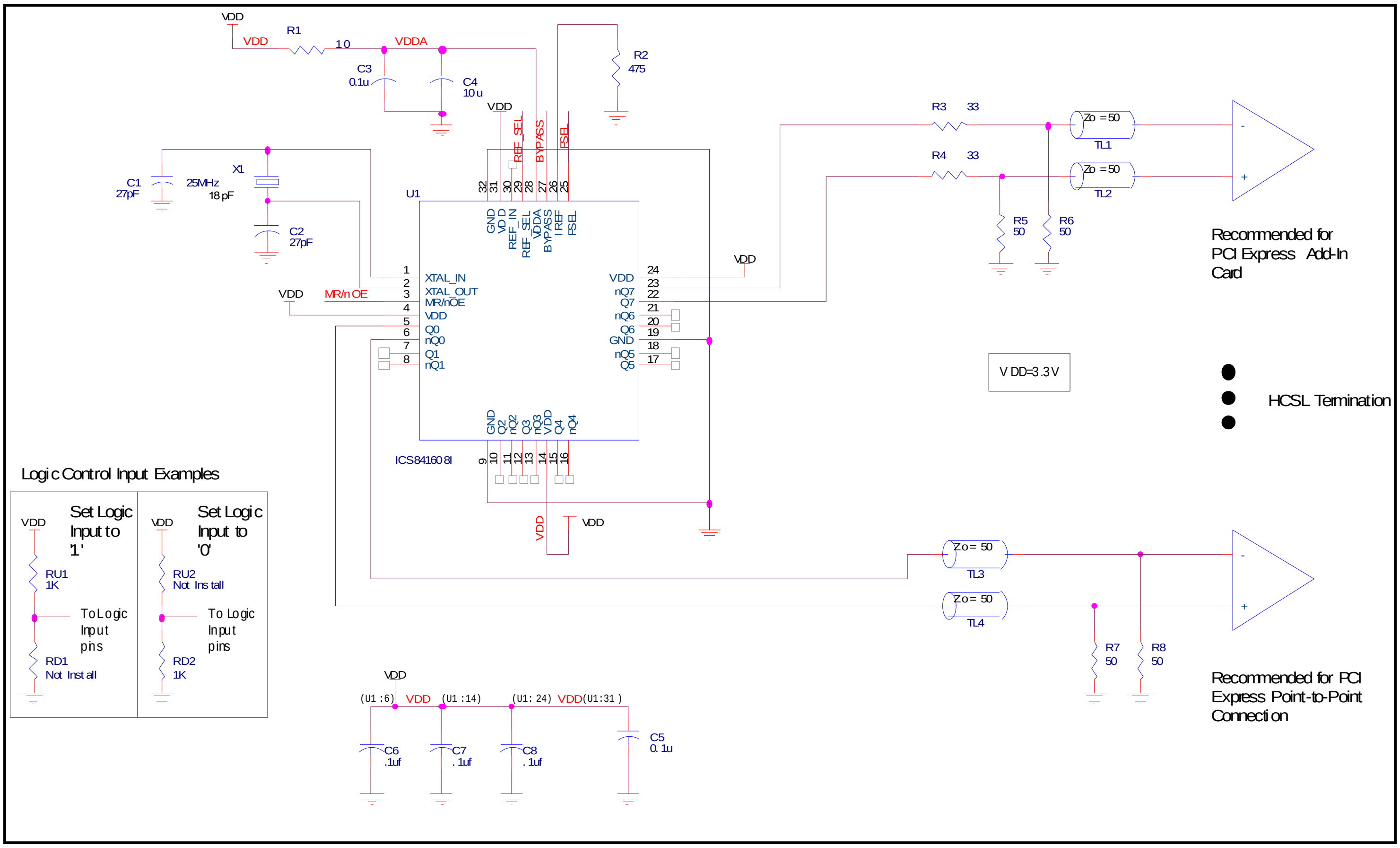


Figure 6. 841608 Application Schematic

Power Considerations

This section provides information on power dissipation and junction temperature for the 841608
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 841608 is the sum of the core power plus the analog power plus the power dissipation in the load(s). The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipation in the load.

- Power $(\text{core})_{MAX} = V_{DD\_MAX} * (I_{DD\_MAX} + I_{DDA\_MAX})$ = 3.465V * (87mA + 15mA) = **353.43mW**
- Power $(\text{outputs})_{MAX}$ = **44.5mW/Loaded Output pair**
  If all outputs are loaded, the total power is 8 * 44.5mW = **356mW**

Total Power$_{\_MAX}$ = (3.465V, with all outputs switching) = 353.43mW + 356mW = **709.43mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature for devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 37°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.709W * 37°C/W = 111.2°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7. Thermal Resistance θ_{JA} for 32-Pin VFQFN, Forced Convection

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	37.0°C/W	32.4°C/W	29.0°C/W

3. Calculations and Equations.

The purpose of this section is to calculate power dissipation on the IC per HCSL output pair.

HCSL output driver circuit and termination are shown in *Figure 7.*

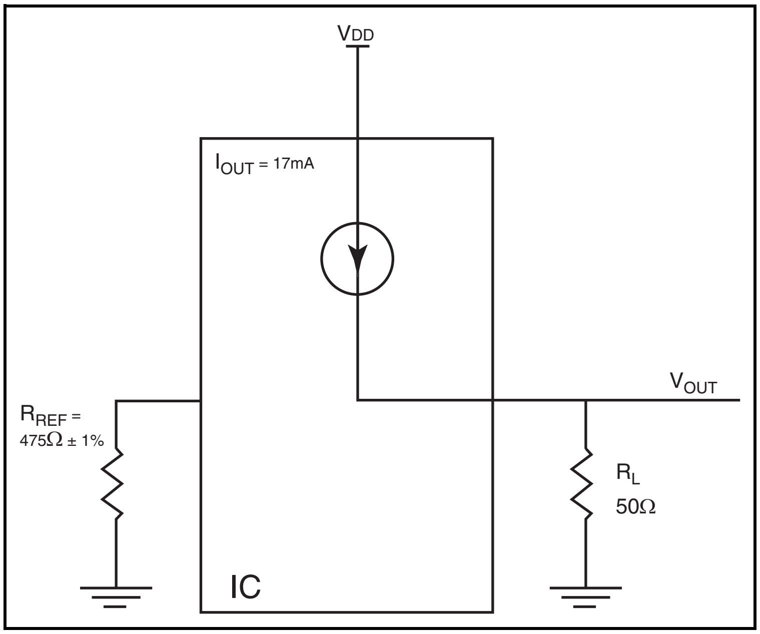


Figure 7. HCSL Driver Circuit and Termination

HCSL is a current steering output which sources a maximum of 17mA of current per output. To calculate worst case on-chip power dissipation, use the following equations which assume a 50Ω load to ground.

The highest power dissipation occurs when V_{DD} is HIGH.

Power $= (V_{DD\_HIGH} - V_{OUT}) * I_{OUT}$, since $V_{OUT} - I_{OUT} * R_L$

$= (V_{DD\_HIGH} - I_{OUT} * R_L) * I_{OUT}$

$= (3.465V - 17mA * 50\Omega) * 17mA$

Total Power Dissipation per output pair = **44.5mW**

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for a 32 Lead VFQFN

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	37.0°C/W	32.4°C/W	29.0°C/W

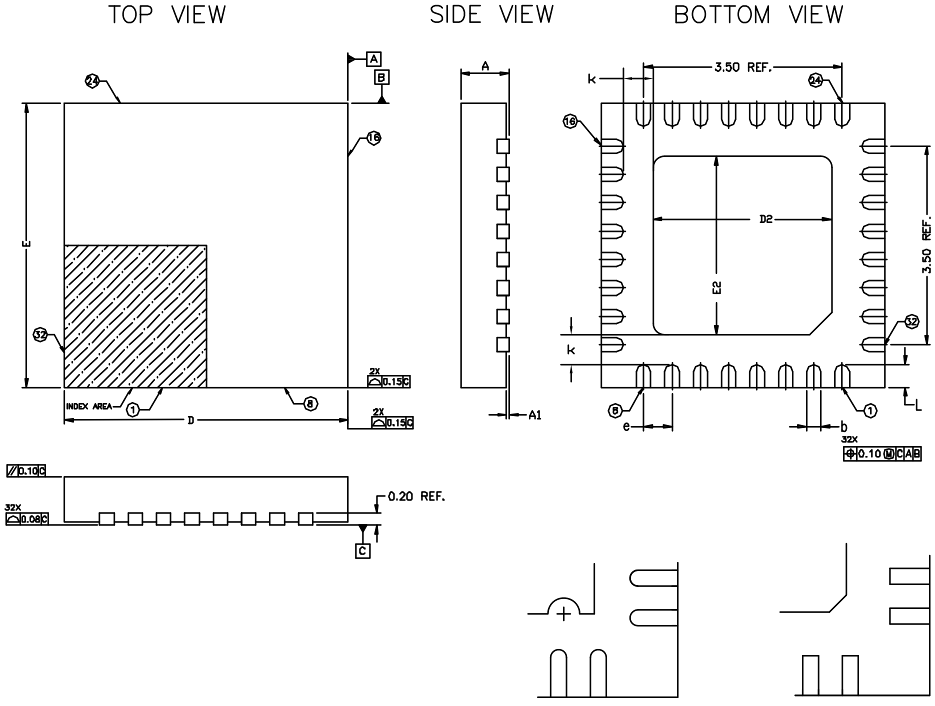
Transistor Count

The transistor count for 841608 is: 2785

32-Lead VFQFN Package Outline and Package Dimensions

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	2/1/16	JH
01	ADD "k" VALUE MIN 0.20	2/8/16	JH



PIN #1 ID OPTION

SYMBOL	DIMENSION		
	MIN	NOM	MAX
b	0.18	0.25	0.30
D	5.00 BSC		
E	5.00 BSC		
D2	3.00	3.15	3.30
E2	3.00	3.15	3.30
L	0.30	0.40	0.50
e	0.50 BSC		
N	32		
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3	0.2 REF		
k	0.20	0.53 REF	

NOTES:

1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.

TOLERANCES
UNLESS SPECIFIED
DECIMAL ANGULAR
X± .1 ±1°
XX± .05
XXX± .030

APPROVALS	DATE
DRAWN RAC	2/1/16
CHECKED	

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TITLE NL/NLG 32 PACKAGE OUTLINE
5.0 x 5.0 mm BODY EPAD 3.15 x 3.15
0.50 mm PITCH QFN

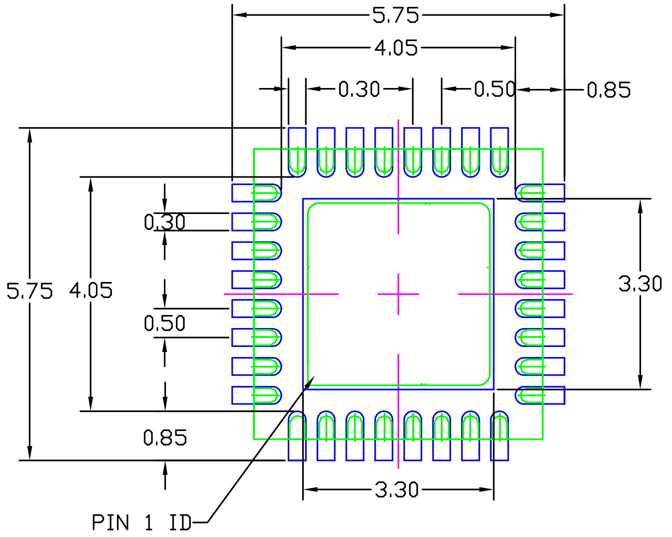
SIZE	DRAWING No.	REV
C	PSC-4171-01	01

DO NOT SCALE DRAWING
SHEET 1 OF 2

32-Lead VFQFN Package Outline and Package Dimensions

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	2/1/16	JH
01	ADD "k" VALUE MIN 0.20	2/8/16	JH



RECOMMENDED LAND PATTERN

NOTES:

1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOWS FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

TOLERANCES
UNLESS SPECIFIED
DECIMAL ANGULAR
X± .1 ±1°
XX± .05
XXX± .030

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APPROVALS	DATE
DRAWN RAC	2/1/16
CHECKED	

TITLE NL/NLG 32 PACKAGE OUTLINE
5.0 x 5.0 mm BODY EPAD 3.15 x 3.15
0.50 mm PITCH QFN

SIZE	DRAWING No.	REV
C	PSC-4171-01	01

DO NOT SCALE DRAWING
SHEET 2 OF 2

Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
841608AKILF	ICS41608AIL	“Lead-Free”, 32 Lead TSSOP	Tray	-40°C to 85°C
841608AKILFT	ICS41608AIL	“Lead-Free”, 32 Lead TSSOP	Tape & Reel	-40°C to 85°C

Revision History Sheet

Rev	Table	Page	Description of Change	Date
B	T10	P19 20	Updated Package Information. Ordering Information Table - deleted tray count and table note. Deleted HiperClocks references through out the datasheet. Deletec “ICS” prefix and “I” suffix in part number. Updated datasheet header/footer.	5/4/2016

Corporate Headquarters
6024 Silver Creek Valley Road
San Jose, CA 95138 USA
www.IDT.com

Sales
1-800-345-7015 or 408-284-8200
Fax: 408-284-2775
www.IDT.com/go/sales

Tech Support
www.idt.com/go/support

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Телефон: +7 812 627 14 35

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Адрес: 198099, Санкт-Петербург,
Промышленная ул, дом № 19, литера Н,
помещение 100-Н Офис 331