

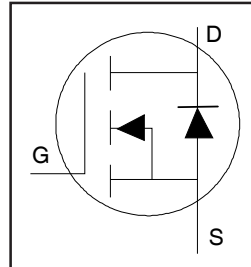
Applications

- Brushed Motor drive applications
- BLDC Motor drive applications
- Battery powered circuits
- Half-bridge and full-bridge topologies
- Synchronous rectifier applications
- Resonant mode power supplies
- OR-ing and redundant power switches
- DC/DC and AC/DC converters
- DC/AC Inverters

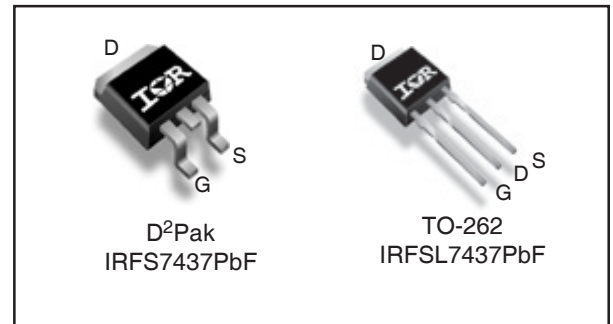
Benefits

- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free
- Halogen-Free

HEXFET® Power MOSFET



V_{DSS}	40V
R_{DS(on)} typ.	1.4mΩ
max.	1.8mΩ
I_D (Silicon Limited)	250A^①
I_D (Package Limited)	195A



G	D	S
Gate	Drain	Source

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFSL7437PbF	TO-262	Tube	50	IRFSL7437PbF
IRFS7437PbF	D2Pak	Tube	50	IRFS7437PbF
IRFS7437PbF	D2Pak	Tape and Reel Left	800	IRFS7437TRLpbF

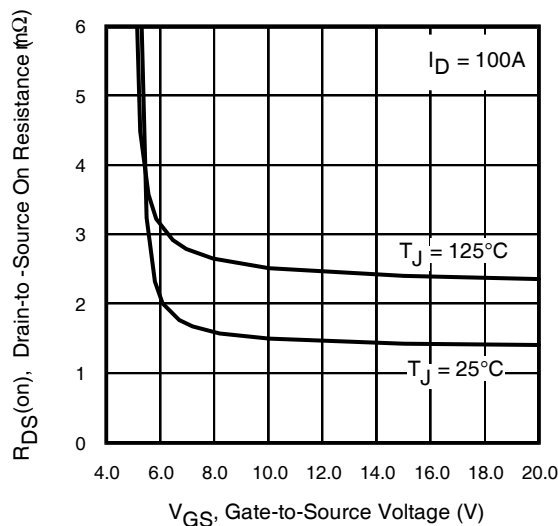


Fig 1. Typical On-Resistance vs. Gate Voltage

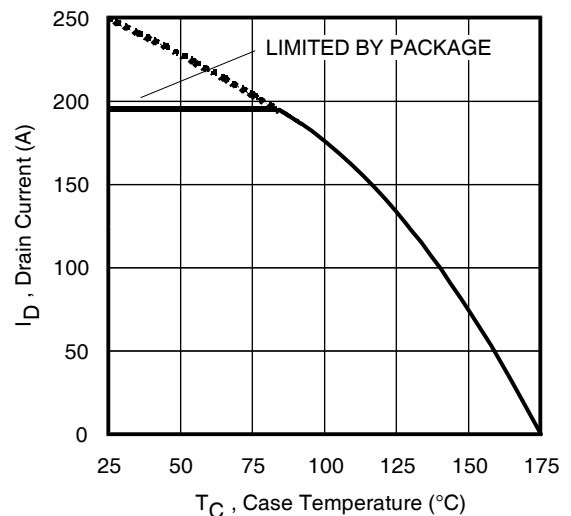


Fig 2. Maximum Drain Current vs. Case Temperature

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	250 ^①	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	180	
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Wire Bond Limited)	195	
I_{DM}	Pulsed Drain Current ^②	1000	
$P_D @ T_C = 25^\circ\text{C}$	Maximum Power Dissipation	230	W
	Linear Derating Factor	1.5	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery ^④	3.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10lbf·in (1.1N·m)	

Avalanche Characteristics

E_{AS} (Thermally limited)	Single Pulse Avalanche Energy ^③	350	mJ
E_{AS} (Thermally limited)	Single Pulse Avalanche Energy ^③	802	
I_{AR}	Avalanche Current ^②	See Fig. 14, 15, 22a, 22b	
E_{AR}	Repetitive Avalanche Energy ^②		
			mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ^③	—	0.65	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) , D ² Pak ^③	—	40	

Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	—	—	V	$V_{GS} = 0\text{V}$, $I_D = 250\mu\text{A}$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.029	—	V/°C	Reference to 25°C , $I_D = 1\text{mA}$ ^②
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	1.4	1.8	mΩ	$V_{GS} = 10\text{V}$, $I_D = 100\text{A}$
		—	2.0	—		$V_{GS} = 6.0\text{V}$, $I_D = 50\text{A}$
$V_{GS(th)}$	Gate Threshold Voltage	2.2	3.0	3.9	V	$V_{DS} = V_{GS}$, $I_D = 150\mu\text{A}$
I_{DSS}	Drain-to-Source Leakage Current	—	—	1.0	μA	$V_{DS} = 40\text{V}$, $V_{GS} = 0\text{V}$
		—	—	150		$V_{DS} = 40\text{V}$, $V_{GS} = 0\text{V}$, $T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20\text{V}$
R_G	Internal Gate Resistance	—	2.2	—	Ω	

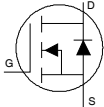
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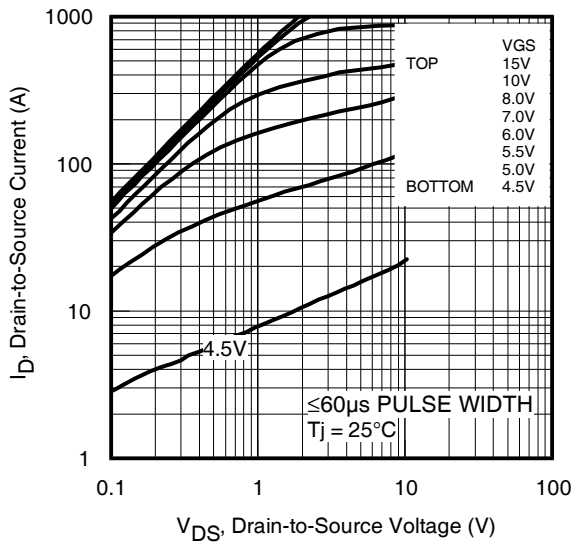
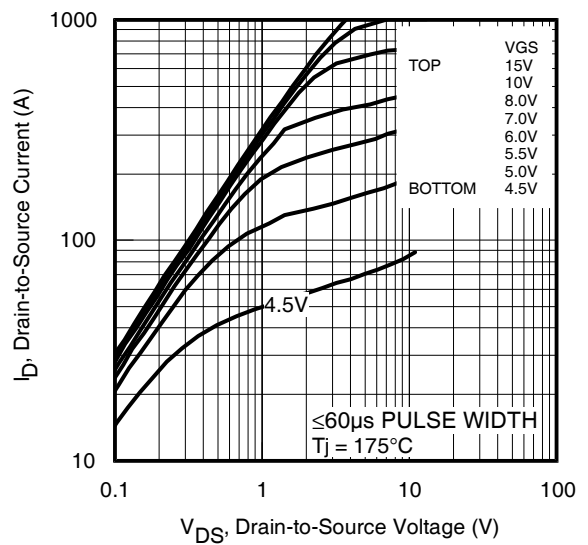
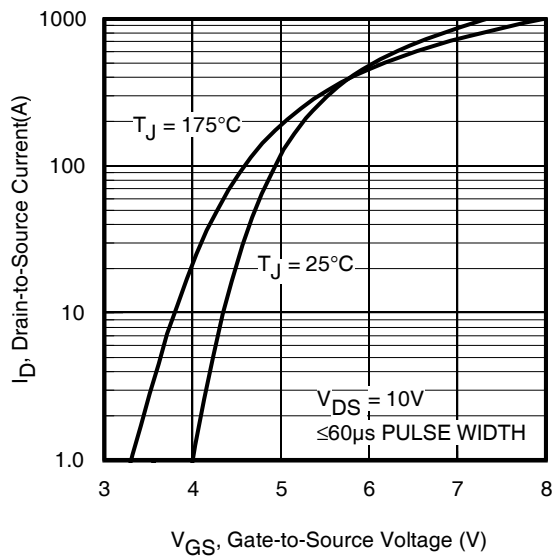
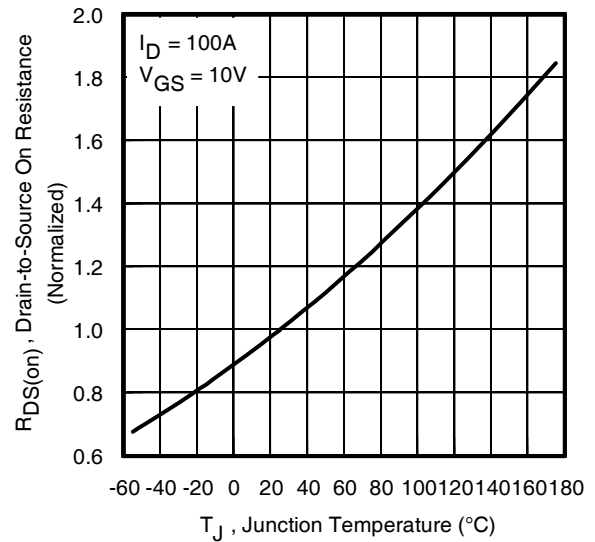
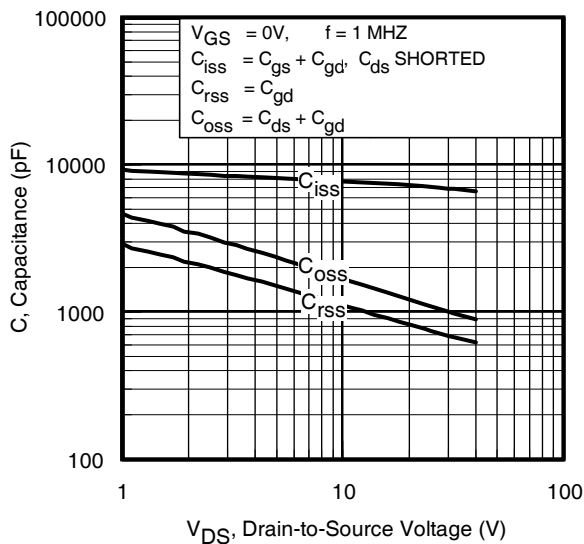
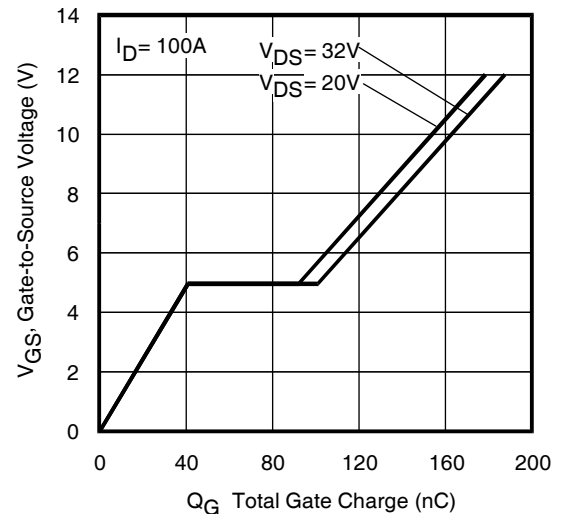
- ① Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 195A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements. (Refer to AN-1140)
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ Limited by T_{Jmax} , starting $T_J = 25^\circ\text{C}$, $L = 0.069\text{mH}$
 $R_G = 50\Omega$, $I_{AS} = 100\text{A}$, $V_{GS} = 10\text{V}$.
- ④ $I_{SD} \leq 100\text{A}$, $di/dt \leq 1166\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175^\circ\text{C}$.
- ⑤ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑥ C_{OSS} eff. (TR) is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑦ C_{OSS} eff. (ER) is a fixed capacitance that gives the same energy as C_{OSS} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑧ R_θ is measured at T_J approximately 90°C .
- ⑨ Limited by T_{Jmax} starting $T_J = 25^\circ\text{C}$, $L = 1\text{mH}$, $R_G = 50\Omega$, $I_{AS} = 40\text{A}$, $V_{GS} = 10\text{V}$.

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions	
g_{fs}	Forward Transconductance	160	---	---	S	$V_{DS} = 10\text{V}, I_D = 100\text{A}$	
Q_g	Total Gate Charge	---	150	225	nC	$I_D = 100\text{A}$ $V_{DS} = 20\text{V}$ $V_{GS} = 10\text{V} \textcircled{5}$	
Q_{gs}	Gate-to-Source Charge	---	41	---			
Q_{gd}	Gate-to-Drain ("Miller") Charge	---	51	---			
Q_{sync}	Total Gate Charge Sync. ($Q_g - Q_{gd}$)	---	99	---			
$t_{d(on)}$	Turn-On Delay Time	---	19	---			ns
t_r	Rise Time	---	70	---			
$t_{d(off)}$	Turn-Off Delay Time	---	78	---			
t_f	Fall Time	---	53	---			
C_{iss}	Input Capacitance	---	7330	---	pF	$V_{GS} = 0\text{V}$ $V_{DS} = 25\text{V}$ $f = 1.0\text{ MHz}$, See Fig. 5	
C_{oss}	Output Capacitance	---	1095	---			
C_{rss}	Reverse Transfer Capacitance	---	745	---			
$C_{oss\text{ eff. (ER)}}$	Effective Output Capacitance (Energy Related) $\textcircled{2}$	---	1310	---			$V_{GS} = 0\text{V}, V_{DS} = 0\text{V to } 32\text{V}$, See Fig. 11
$C_{oss\text{ eff. (TR)}}$	Effective Output Capacitance (Time Related) $\textcircled{6}$	---	1735	---			$V_{GS} = 0\text{V}, V_{DS} = 0\text{V to } 32\text{V}$

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	---	---	250 $\textcircled{1}$	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) $\textcircled{2}$	---	---	1000	A	
V_{SD}	Diode Forward Voltage	---	1.0	1.3	V	$T_J = 25^\circ\text{C}, I_S = 100\text{A}, V_{GS} = 0\text{V} \textcircled{5}$
t_{rr}	Reverse Recovery Time	---	30	---	ns	$T_J = 25^\circ\text{C}$ $V_R = 34\text{V}$, $T_J = 125^\circ\text{C}$ $I_F = 100\text{A}$ $di/dt = 100\text{A}/\mu\text{s} \textcircled{5}$
Q_{rr}	Reverse Recovery Charge	---	24	---		
		---	25	---		
I_{RRM}	Reverse Recovery Current	---	1.3	---	A	$T_J = 25^\circ\text{C}$
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				


Fig 3. Typical Output Characteristics

Fig 4. Typical Output Characteristics

Fig 5. Typical Transfer Characteristics

Fig 6. Normalized On-Resistance vs. Temperature

Fig 7. Typical Capacitance vs. Drain-to-Source Voltage

Fig 8. Typical Gate Charge vs. Gate-to-Source Voltage

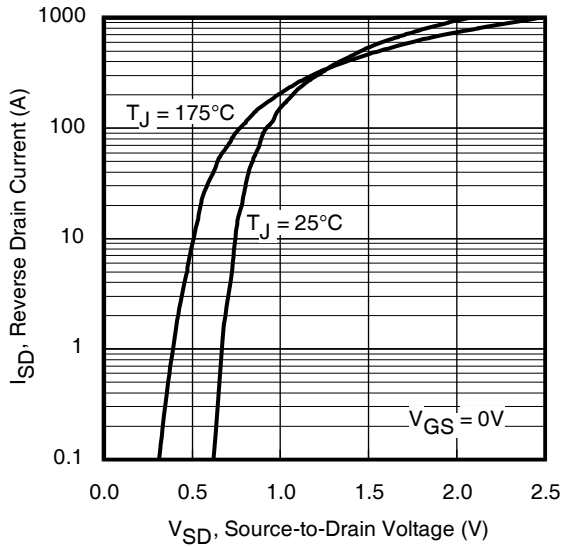


Fig 9. Typical Source-Drain Diode Forward Voltage

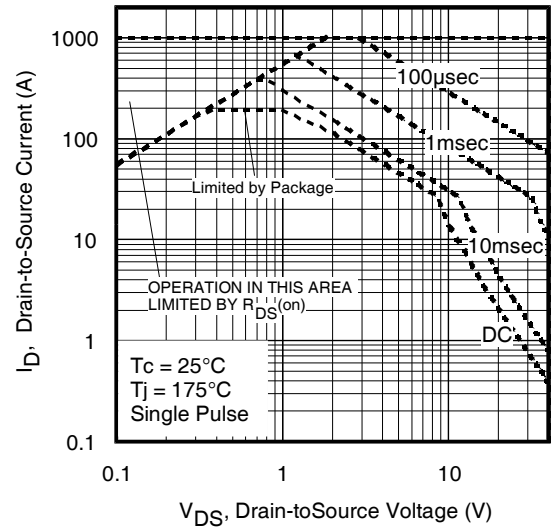


Fig 10. Maximum Safe Operating Area

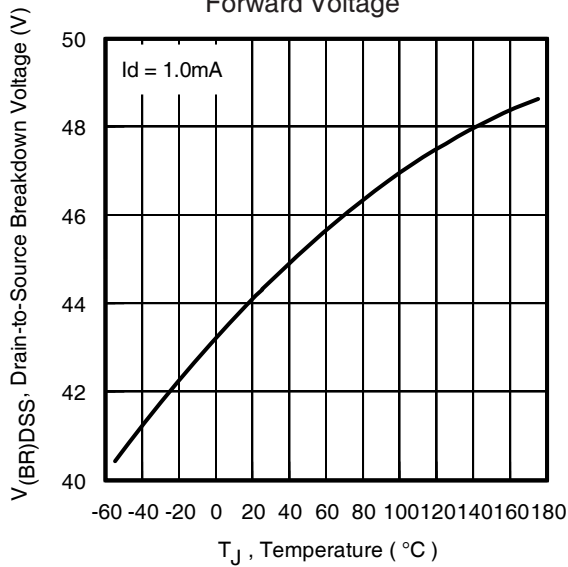


Fig 11. Drain-to-Source Breakdown Voltage

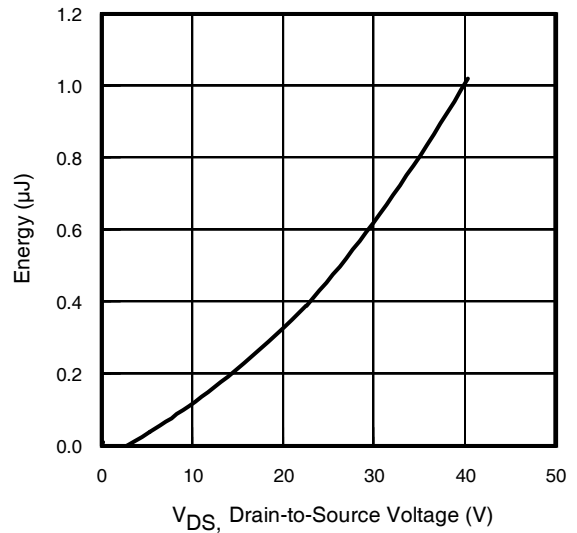


Fig 12. Typical C_{OSS} Stored Energy

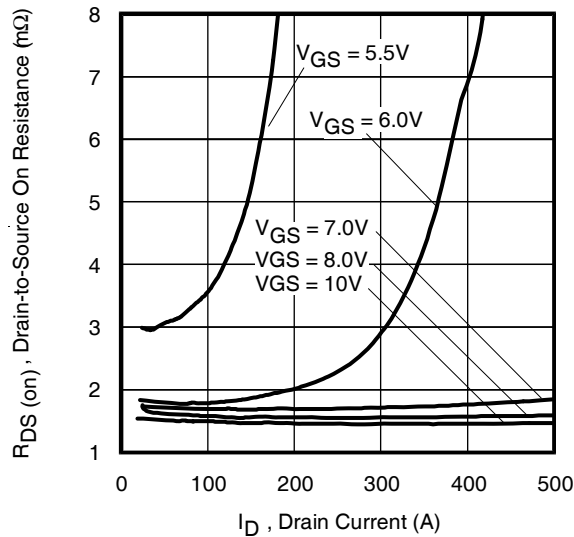
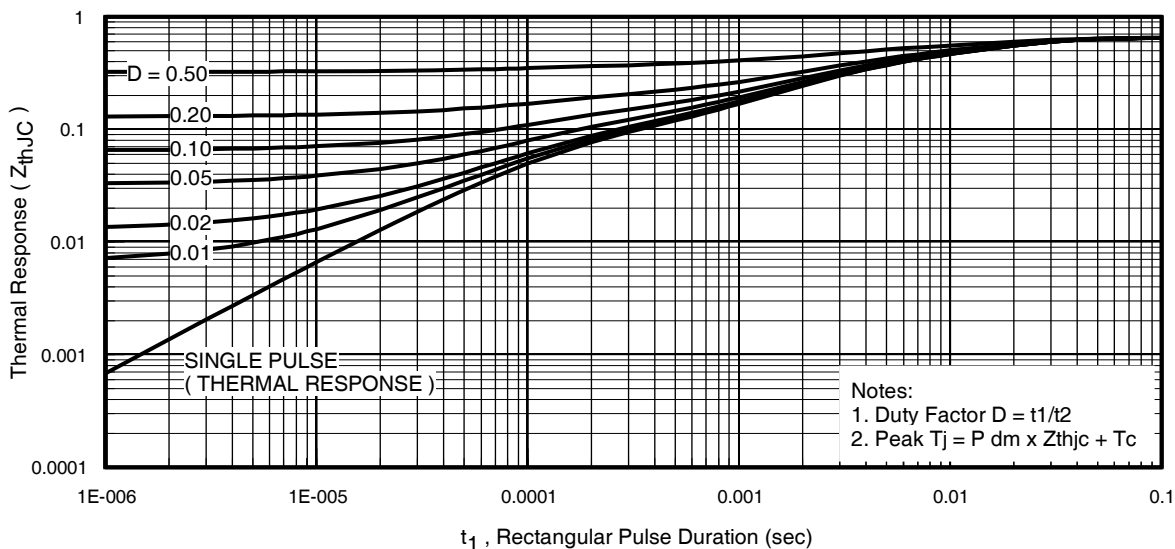
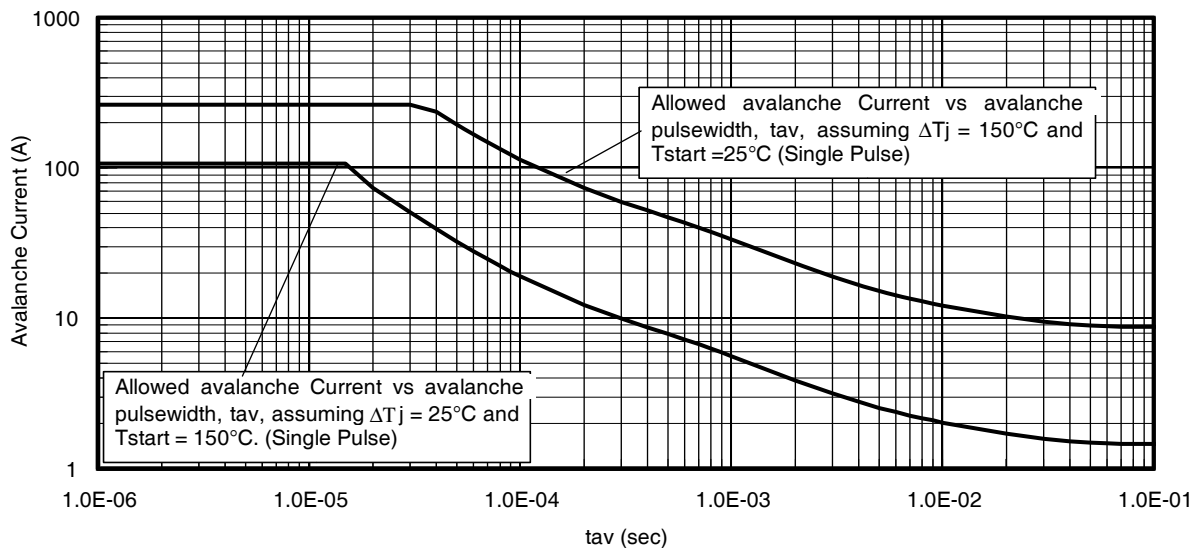
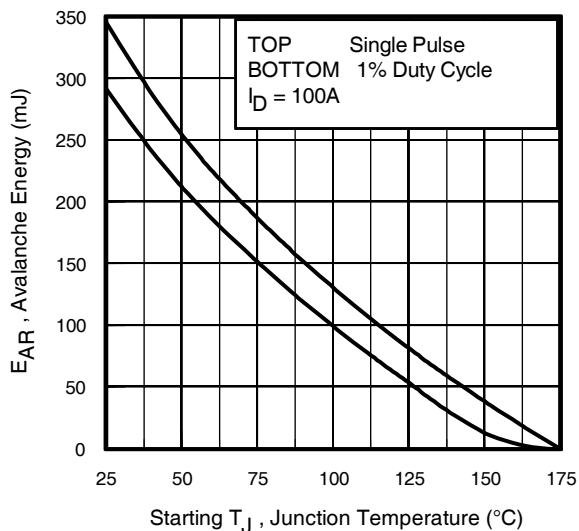


Fig 13. Typical On-Resistance vs. Drain Current

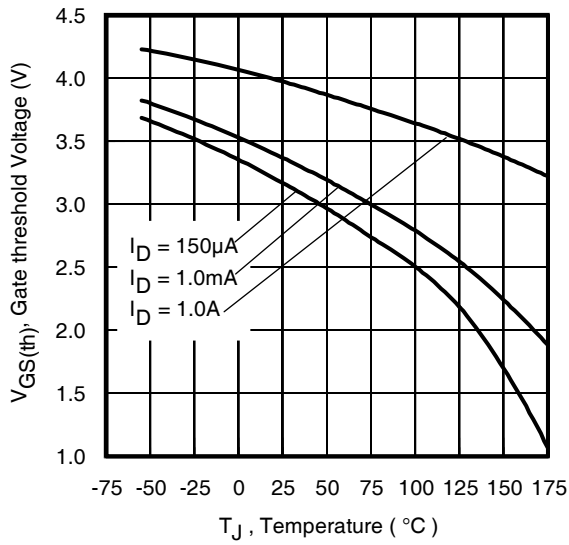
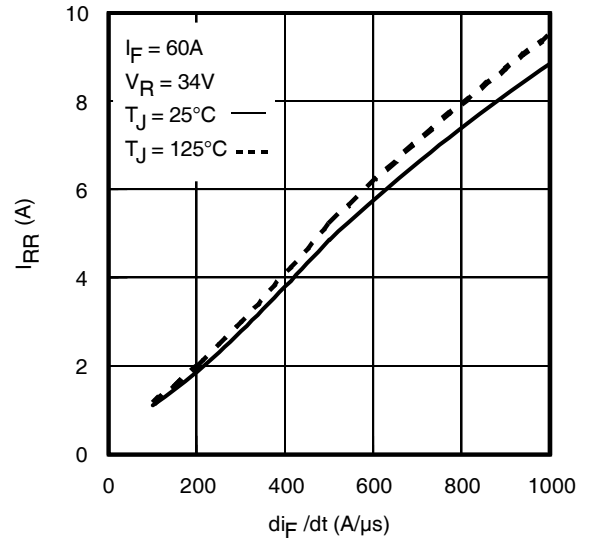
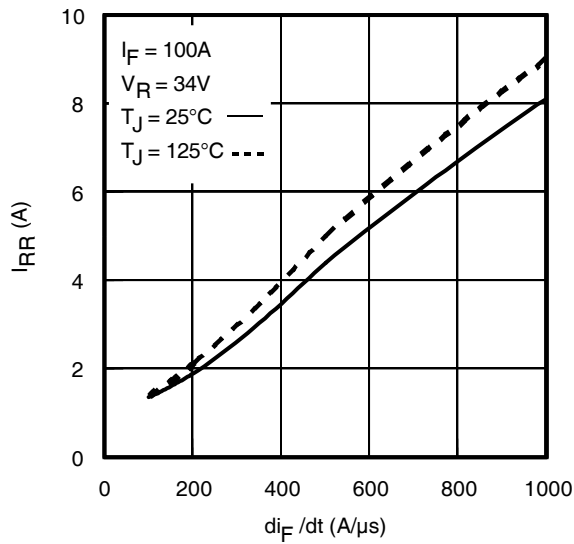
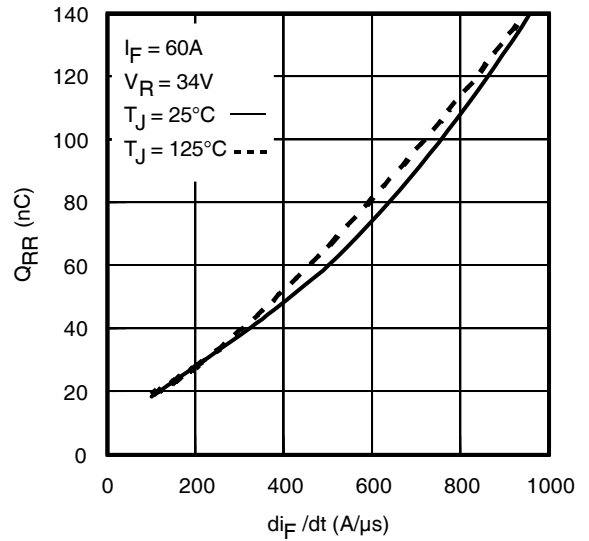
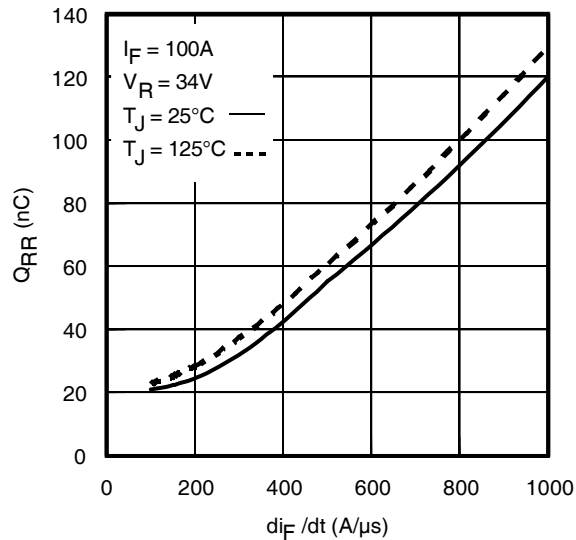

Fig 14. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Fig 15. Typical Avalanche Current vs. Pulsewidth

Fig 16. Maximum Avalanche Energy vs. Temperature
**Notes on Repetitive Avalanche Curves , Figures 14, 15:
(For further info, see AN-1005 at www.irf.com)**

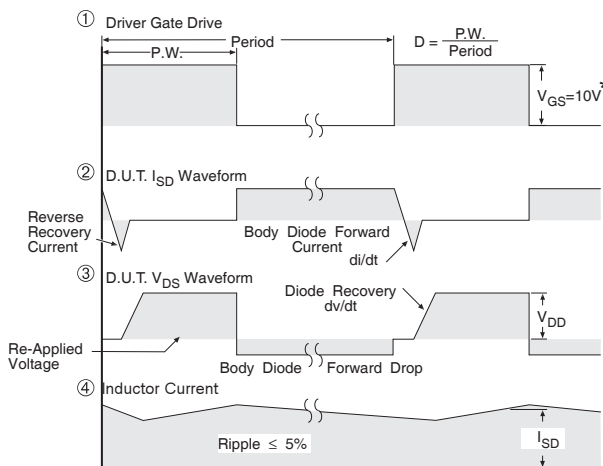
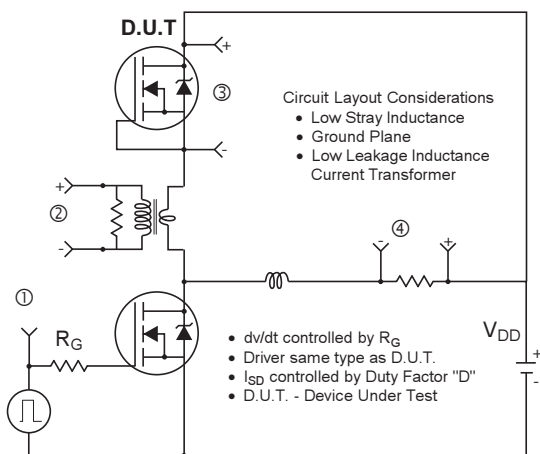
1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 22a, 22b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$


Fig 17. Threshold Voltage vs. Temperature

Fig. 18 - Typical Recovery Current vs. di_F/dt

Fig. 19 - Typical Recovery Current vs. di_F/dt

Fig. 20 - Typical Stored Charge vs. di_F/dt

Fig. 21 - Typical Stored Charge vs. di_F/dt



* $V_{GS} = 5V$ for Logic Level Devices

Fig 22. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

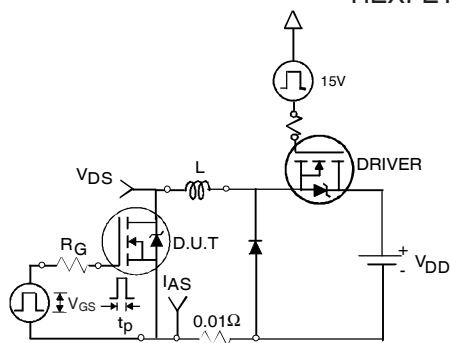


Fig 23a. Unclamped Inductive Test Circuit

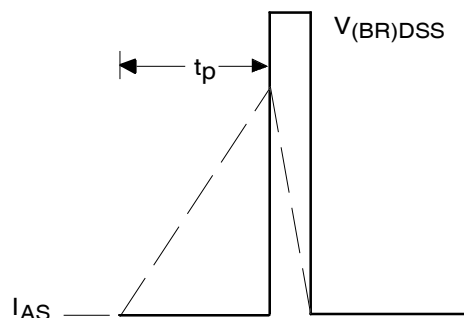


Fig 23b. Unclamped Inductive Waveforms

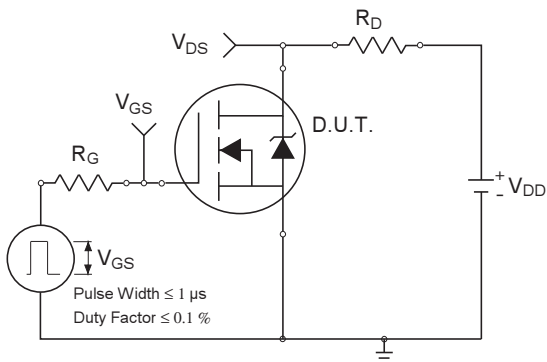


Fig 24a. Switching Time Test Circuit

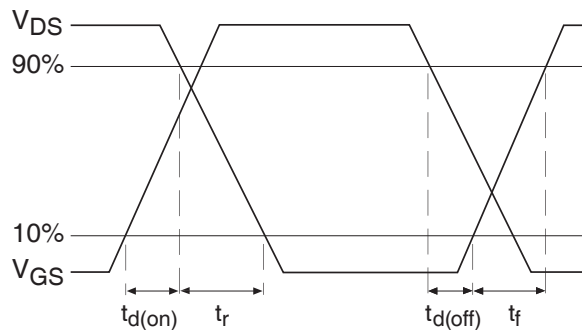


Fig 24b. Switching Time Waveforms

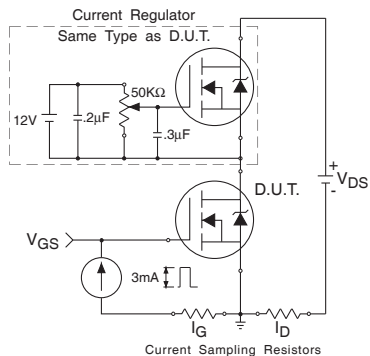


Fig 25a. Gate Charge Test Circuit

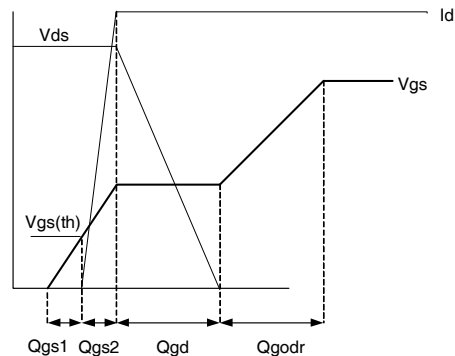
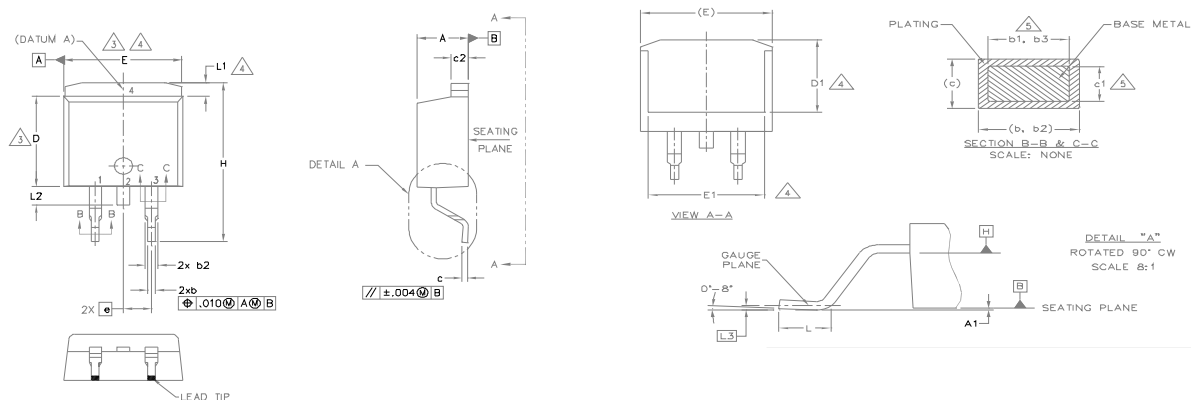


Fig 25b. Gate Charge Waveform

D²Pak (TO-263AB) Package Outline

Dimensions are shown in millimeters (inches)



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	0.00	0.254	.000	.010	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	-	.270	-	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	-	.245	-	4
e	2.54 BSC		.100 BSC		
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1	-	1.68	-	.066	4
L2	-	1.78	-	.070	
L3	0.25 BSC		.010 BSC		

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1, b3 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.

LEAD ASSIGNMENTS

DIODES

- 1.- ANODE (TWO DIE) / OPEN (ONE DIE)
- 2, 4.- CATHODE
- 3.- ANODE

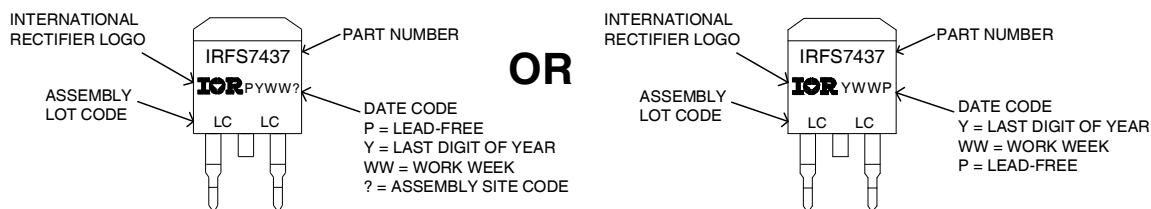
HEXFET

- 1.- GATE
- 2, 4.- DRAIN
- 3.- SOURCE

IGBTs, CoPACK

- 1.- GATE
- 2, 4.- COLLECTOR
- 3.- EMITTER

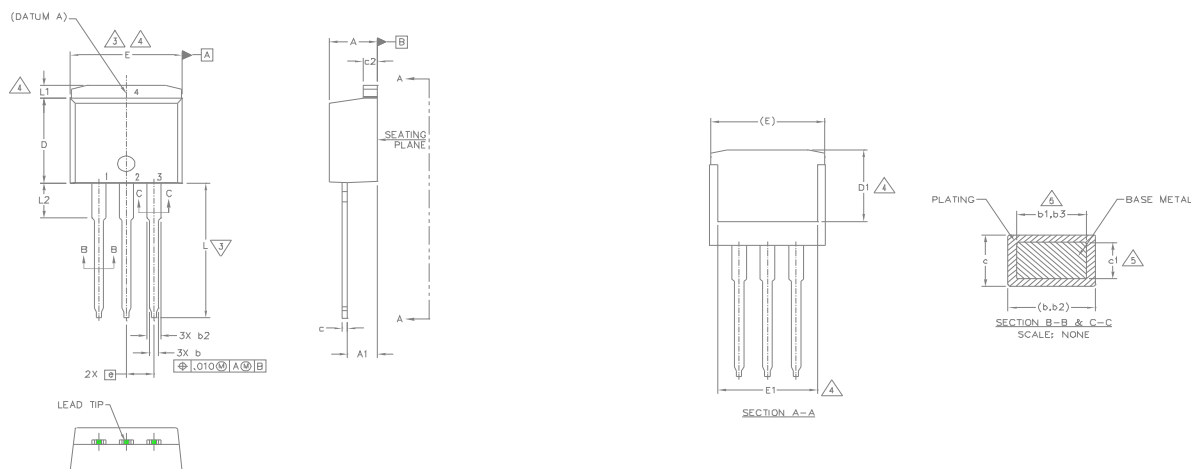
D²Pak (TO-263AB) Part Marking Information



Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

TO-262 Package Outline

Dimensions are shown in millimeters (inches)



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	2.03	3.02	.080	.119	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	-	.270	-	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	-	.245	-	4
e	2.54 BSC		.100 BSC		
L	13.46	14.10	.530	.555	
L1	-	1.65	-	.065	4
L2	3.56	3.71	.140	.146	

NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
- DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES]
- DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
- DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
- CONTROLLING DIMENSION: INCH.
- OUTLINE CONFORM TO JEDEC TO-262 EXCEPT A1(max.), b(min.) AND D1(min.) WHERE DIMENSIONS DERIVED THE ACTUAL PACKAGE OUTLINE.

LEAD ASSIGNMENTS

IGBTs, CoPACK

- GATE
- COLLECTOR
- EMITTER
- COLLECTOR

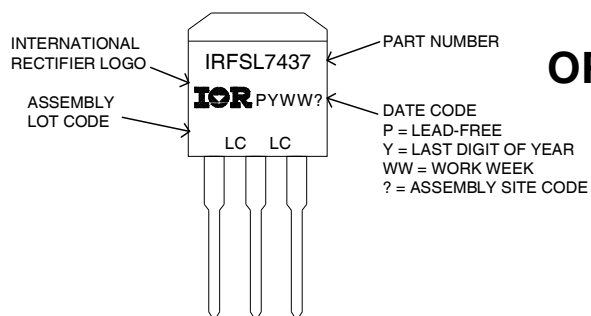
HEXFET

- GATE
- DRAIN
- SOURCE
- DRAIN

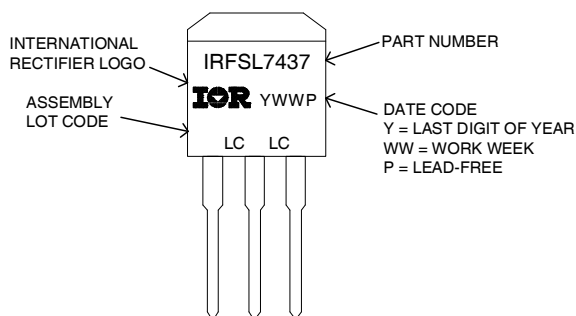
DIODES

- ANODE (TWO DIE) / OPEN (ONE DIE)
- CATHODE
- ANODE

TO-262 Part Marking Information

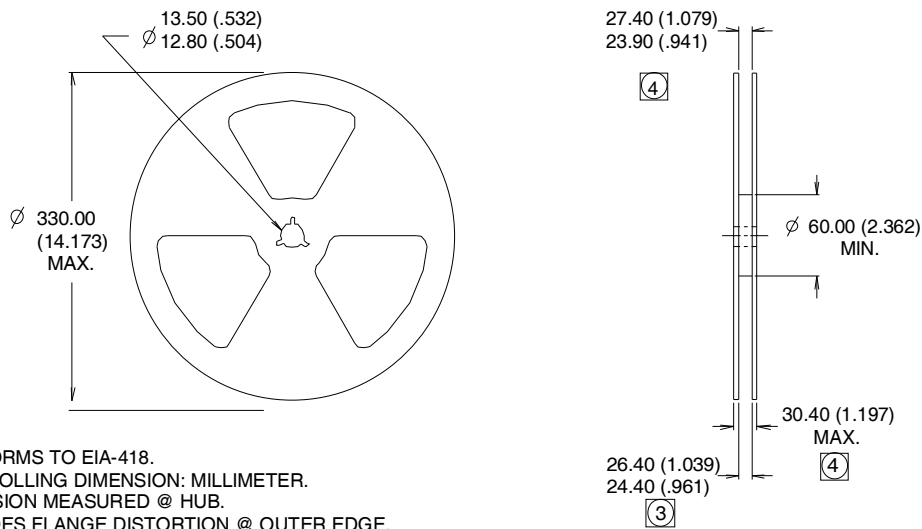
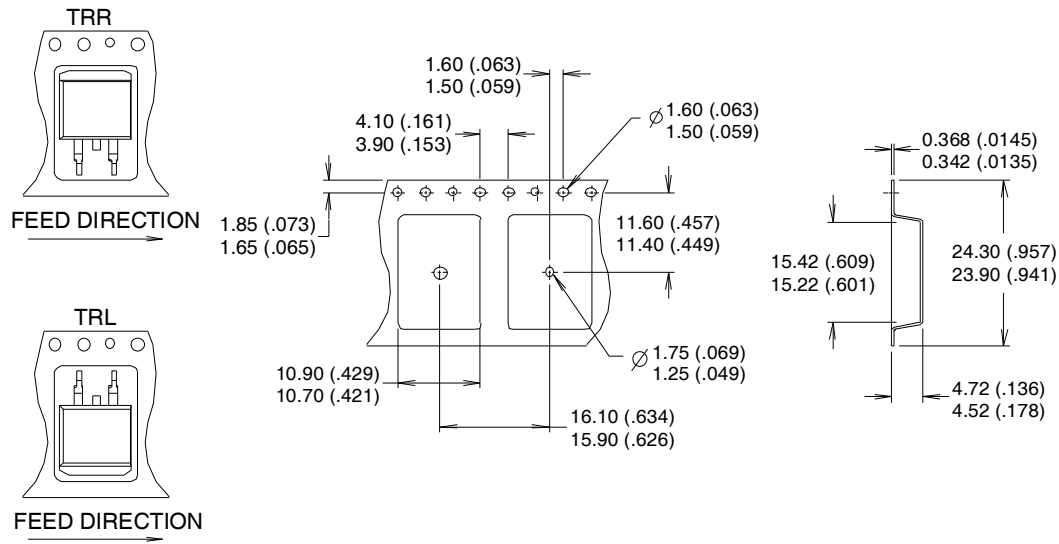


OR



Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

D²Pak Tape & Reel Information



- NOTES :
1. COMFORMS TO EIA-418.
 2. CONTROLLING DIMENSION: MILLIMETER.
 - ③ DIMENSION MEASURED @ HUB.
 - ④ INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

Qualification information†

Qualification level	Industrial ^{††} (per JEDEC JESD47F ^{†††} guidelines)	
Moisture Sensitivity Level	D2Pak	MSL1 (per JEDEC J-STD-020D ^{†††})
	TO-262	
RoHS compliant	Yes	

† Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/product-info/reliability/>

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information: <http://www.irf.com/whoto-call/salesrep/>

††† Applicable version of JEDEC standard at the time of product release.

Revision History

Date	Comment
4/30/2014	<ul style="list-style-type: none"> • Updated data sheet based on corporate template. • Updated typo on the fig.19 and fig.21, unit of y-axis from "A" to "nC" on page7. • Updated package outline and part marking on page 9 & 10.
1/6/2015	<ul style="list-style-type: none"> • Updated $E_{AS(L=1mH)} = 802mJ$ on page 2 • Updated note 9 "Limited by T_{Jmax}, starting $T_J = 25^{\circ}C$, $L = 1mH$, $R_G = 50\Omega$, $I_{AS} = 40A$, $V_{GS} = 10V$". on page 2



Стандарт Электрон Связь

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