

FEATURES

- Latch-up proof
- 8 kV HBM ESD rating
- Low on resistance ($<10 \Omega$)
- $\pm 9 \text{ V}$ to $\pm 22 \text{ V}$ dual-supply operation
- 9 V to 40 V single-supply operation
- 48 V supply maximum ratings
- Fully specified at $\pm 15 \text{ V}$, $\pm 20 \text{ V}$, $+12 \text{ V}$, and $+36 \text{ V}$
- V_{SS} to V_{DD} analog signal range

APPLICATIONS

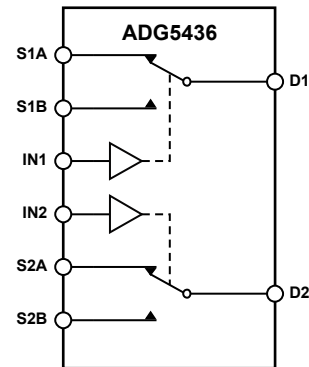
- Relay replacement
- Automatic test equipment
- Data acquisition
- Instrumentation
- Avionics
- Audio and video switching
- Communication systems

GENERAL DESCRIPTION

The [ADG5436](#) is a monolithic CMOS device containing two independently selectable single-pole/double-throw (SPDT) switches. An EN input on the LFCSP package enables or disables the device. When disabled, all channels switch off. Each switch conducts equally well in both directions when on and has an input signal range that extends to the supplies. In the off condition, signal levels up to the supplies are blocked. Both switches exhibit break-before-make switching action for use in multiplexer applications.

The on-resistance profile is very flat over the full analog input range, ensuring excellent linearity and low distortion when switching audio signals.

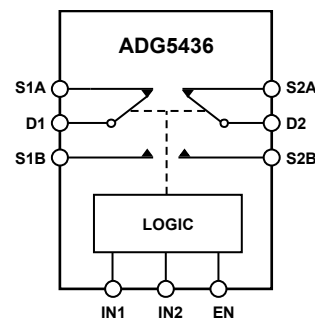
FUNCTIONAL BLOCK DIAGRAMS



SWITCHES SHOWN FOR A LOGIC 1 INPUT.

Figure 1. TSSOP Package

09204-001



SWITCHES SHOWN FOR A LOGIC 1 INPUT.

Figure 2. LFCSP Package

09204-002

PRODUCT HIGHLIGHTS

1. Trench isolation guards against latch-up. A dielectric trench separates the P and N channel transistors thereby preventing latch-up even under severe overvoltage conditions.
2. Low R_{ON} .
3. Dual-supply operation. For applications where the analog signal is bipolar, the [ADG5436](#) can be operated from dual supplies up to $\pm 22 \text{ V}$.
4. Single-supply operation. For applications where the analog signal is unipolar, the [ADG5436](#) can be operated from a single-rail power supply up to 40 V.
5. 3 V logic compatible digital inputs: $V_{INH} = 2.0 \text{ V}$, $V_{INL} = 0.8 \text{ V}$.
6. No V_L logic power supply required.

Rev. C

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REVISION HISTORY

11/2017—Rev. B to Rev. C

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Updated Outline Dimensions	19
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8/2015—Rev. A to Rev. B

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6/2011—Rev. 0 to Rev. A

Added I _{SS} -40°C to +125°C Parameter	5
Updated Outline Dimensions	19
Changes to Ordering Guide	19

7/2010—Revision 0: Initial Version

SPECIFICATIONS

±15 V DUAL SUPPLY

$V_{DD} = +15\text{ V} \pm 10\%$, $V_{SS} = -15\text{ V} \pm 10\%$, GND = 0 V, unless otherwise noted.

Table 1.

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance, R_{ON}	9.8			Ω typ	$V_S = \pm 10\text{ V}$, $I_S = -10\text{ mA}$; see Figure 25
	11	14	16	Ω max	$V_{DD} = +13.5\text{ V}$, $V_{SS} = -13.5\text{ V}$
On-Resistance Match Between Channels, ΔR_{ON}	0.35			Ω typ	$V_S = \pm 10\text{ V}$, $I_S = -10\text{ mA}$
On-Resistance Flatness, $R_{FLAT(ON)}$	0.7	0.9	1.1	Ω max	
	1.2			Ω typ	$V_S = \pm 10\text{ V}$, $I_S = -10\text{ mA}$
	1.6	2	2.2	Ω max	
LEAKAGE CURRENTS					
Source Off Leakage, I_S (Off)	± 0.05			nA typ	$V_{DD} = +16.5\text{ V}$, $V_{SS} = -16.5\text{ V}$
	± 0.25	± 0.75	± 6	nA max	$V_S = \pm 10\text{ V}$, $V_D = \mp 10\text{ V}$; see Figure 28
Drain Off Leakage, I_D (Off)	± 0.1			nA typ	$V_S = \pm 10\text{ V}$, $V_D = \mp 10\text{ V}$; see Figure 28
	± 0.4	± 2	± 12	nA max	
Channel On Leakage, I_D (On), I_S (On)	± 0.1			nA typ	$V_S = V_D = \pm 10\text{ V}$; see Figure 24
	± 0.4	± 2	± 12	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002			μA typ	$V_{IN} = V_{GND}$ or V_{DD}
			± 0.1	μA max	
Digital Input Capacitance, C_{IN}	5			pF typ	
DYNAMIC CHARACTERISTICS¹					
Transition Time, $t_{TRANSITION}$	170			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	235	285	316	ns max	$V_S = 10\text{ V}$; see Figure 31
t_{ON}	173			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	230	280	351	ns max	$V_S = 10\text{ V}$; see Figure 33
t_{OFF}	124			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	160	193	218	ns max	$V_S = 10\text{ V}$; see Figure 33
Break-Before-Make Time Delay, t_D	55			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
			18	ns min	$V_{S1} = V_{S2} = 10\text{ V}$; see Figure 32
Charge Injection, Q_{INJ}	200			pC typ	$V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 34
Off Isolation	-78			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 27
Channel-to-Channel Crosstalk	-58			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 26
Total Harmonic Distortion + Noise	0.009			% typ	$R_L = 1\text{ k}\Omega$, 15 V p-p , $f = 20\text{ Hz}$ to 20 kHz ; see Figure 29
-3 dB Bandwidth	102			MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 30
Insertion Loss	-0.7			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 30
C_S (Off)	18			pF typ	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$
C_D (Off)	62			pF typ	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$
C_D (On), C_S (On)	83			pF typ	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
POWER REQUIREMENTS					
I_{DD}	45			$\mu\text{A typ}$	$V_{DD} = +16.5\text{ V}$, $V_{SS} = -16.5\text{ V}$ Digital inputs = 0 V or V_{DD}
	55		70	$\mu\text{A max}$	
I_{SS}	0.001			$\mu\text{A typ}$	Digital inputs = 0 V or V_{DD}
			1	$\mu\text{A max}$	
V_{DD}/V_{SS}			$\pm 9/\pm 22$	V min/V max	GND = 0 V

¹ Guaranteed by design; not subject to production test.

±20 V DUAL SUPPLY

$V_{DD} = +20\text{ V} \pm 10\%$, $V_{SS} = -20\text{ V} \pm 10\%$, GND = 0 V, unless otherwise noted.

Table 2.

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analogue Signal Range			V_{DD} to V_{SS}	V	
On Resistance, R_{ON}	9			Ω typ	$V_S = \pm 15\text{ V}$, $I_S = -10\text{ mA}$; see Figure 25
	10	13	15	Ω max	$V_{DD} = +18\text{ V}$, $V_{SS} = -18\text{ V}$
On-Resistance Match Between Channels, ΔR_{ON}	0.35			Ω typ	$V_S = \pm 15\text{ V}$, $I_S = -10\text{ mA}$
	0.7	0.9	1.1	Ω max	
On-Resistance Flatness, $R_{FLAT(ON)}$	1.5			Ω typ	$V_S = \pm 15\text{ V}$, $I_S = -10\text{ mA}$
	1.8	2.2	2.5	Ω max	
LEAKAGE CURRENTS					
Source Off Leakage, I_S (Off)	± 0.05			nA typ	$V_{DD} = +22\text{ V}$, $V_{SS} = -22\text{ V}$ $V_S = \pm 15\text{ V}$, $V_D = \mp 15\text{ V}$; see Figure 28
	± 0.25	± 0.75	± 6	nA max	
Drain Off Leakage, I_D (Off)	± 0.1			nA typ	$V_S = \pm 15\text{ V}$, $V_D = \mp 15\text{ V}$; see Figure 28
	± 0.4	± 2	± 12	nA max	
Channel On Leakage, I_D (On), I_S (On)	± 0.1			nA typ	$V_S = V_D = \pm 15\text{ V}$; see Figure 24
	± 0.4	± 2	± 12	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002			$\mu\text{A typ}$	$V_{IN} = V_{GND}$ or V_{DD}
			± 0.1	$\mu\text{A max}$	
Digital Input Capacitance, C_{IN}	5			pF typ	
DYNAMIC CHARACTERISTICS¹					
Transition Time, $t_{TRANSITION}$	158			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 10\text{ V}$; see Figure 31
	217	260	293	ns max	
t_{ON}	164			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 10\text{ V}$; see Figure 33
	213	256	287	ns max	
t_{OFF}	110			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 10\text{ V}$; see Figure 33
	152	173	194	ns max	
Break-Before-Make Time Delay, t_D	50			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_{S1} = V_{S2} = 10\text{ V}$; see Figure 32
			15	ns min	$V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 34
Charge Injection, Q_{INJ}	250			pC typ	
Off Isolation	-78			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 27
Channel-to-Channel Crosstalk	-58			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 26
Total Harmonic Distortion + Noise	0.007			% typ	$R_L = 1\text{ k}\Omega$, 20 V p-p, $f = 20\text{ Hz}$ to 20 kHz; see Figure 29
-3 dB Bandwidth	100			MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 30

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
Insertion Loss	-0.6			dB typ	$R_L = 50\ \Omega$, $C_L = 5\ \text{pF}$, $f = 1\ \text{MHz}$; see Figure 30
C_S (Off)	18			pF typ	$V_S = 0\ \text{V}$, $f = 1\ \text{MHz}$
C_D (Off)	63			pF typ	$V_S = 0\ \text{V}$, $f = 1\ \text{MHz}$
C_D (On), C_S (On)	82			pF typ	$V_S = 0\ \text{V}$, $f = 1\ \text{MHz}$
POWER REQUIREMENTS					
I_{DD}	50			μA typ	$V_{DD} = +22\ \text{V}$, $V_{SS} = -22\ \text{V}$ Digital inputs = 0 V or V_{DD}
	70		110	μA max	
I_{SS}	0.001			μA typ	Digital inputs = 0 V or V_{DD}
			1	μA max	
V_{DD}/V_{SS}			$\pm 9/\pm 22$	V min/V max	GND = 0 V

¹ Guaranteed by design; not subject to production test.

12 V SINGLE SUPPLY

$V_{DD} = 12\ \text{V} \pm 10\%$, $V_{SS} = 0\ \text{V}$, GND = 0 V, unless otherwise noted.

Table 3.

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance, R_{ON}	19			Ω typ	$V_S = 0\ \text{V}$ to 10 V, $I_S = -10\ \text{mA}$; see Figure 25
	22	27	31	Ω max	$V_{DD} = 10.8\ \text{V}$, $V_{SS} = 0\ \text{V}$
On-Resistance Match Between Channels, ΔR_{ON}	0.4			Ω typ	$V_S = 0\ \text{V}$ to 10 V, $I_S = -10\ \text{mA}$
	0.8	1	1.2	Ω max	
On-Resistance Flatness, $R_{FLAT(ON)}$	4.4			Ω typ	$V_S = 0\ \text{V}$ to 10 V, $I_S = -10\ \text{mA}$
	5.5	6.5	7.5	Ω max	
LEAKAGE CURRENTS					
Source Off Leakage, I_S (Off)	± 0.05			nA typ	$V_{DD} = 13.2\ \text{V}$, $V_{SS} = 0\ \text{V}$ $V_S = 1\ \text{V}/10\ \text{V}$, $V_D = 10\ \text{V}/1\ \text{V}$; see Figure 28
	± 0.25	± 0.75	± 6	nA max	
Drain Off Leakage, I_D (Off)	± 0.1			nA typ	$V_S = 1\ \text{V}/10\ \text{V}$, $V_D = 10\ \text{V}/1\ \text{V}$; see Figure 28
	± 0.4	± 2	± 12	nA max	
Channel On Leakage, I_D (On), I_S (On)	± 0.1			nA typ	$V_S = V_D = 1\ \text{V}/10\ \text{V}$; see Figure 24
	± 0.4	± 2	± 12	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002			μA typ	$V_{IN} = V_{GND}$ or V_{DD}
			± 0.1	μA max	
Digital Input Capacitance, C_{IN}	5			pF typ	
DYNAMIC CHARACTERISTICS¹					
Transition Time, $t_{TRANSITION}$	250			ns typ	$R_L = 300\ \Omega$, $C_L = 35\ \text{pF}$
	346	437	501	ns max	$V_S = 8\ \text{V}$; see Figure 31
t_{ON}	250			ns typ	$R_L = 300\ \Omega$, $C_L = 35\ \text{pF}$
	358	445	512	ns max	$V_S = 8\ \text{V}$; see Figure 33
t_{OFF}	135			ns typ	$R_L = 300\ \Omega$, $C_L = 35\ \text{pF}$
	178	212	237	ns max	$V_S = 8\ \text{V}$; see Figure 33
Break-Before-Make Time Delay, t_D	125			ns typ	$R_L = 300\ \Omega$, $C_L = 35\ \text{pF}$
			50	ns min	$V_{S1} = V_{S2} = 8\ \text{V}$; see Figure 32
Charge Injection, Q_{INJ}	80			pC typ	$V_S = 6\ \text{V}$, $R_S = 0\ \Omega$, $C_L = 1\ \text{nF}$; see Figure 34

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
Off Isolation	-78			dB typ	$R_L = 50\ \Omega$, $C_L = 5\ \text{pF}$, $f = 1\ \text{MHz}$; see Figure 27
Channel-to-Channel Crosstalk	-58			dB typ	$R_L = 50\ \Omega$, $C_L = 5\ \text{pF}$, $f = 1\ \text{MHz}$; see Figure 26
Total Harmonic Distortion + Noise	0.075			% typ	$R_L = 1\ \text{k}\Omega$, 6 V p-p, $f = 20\ \text{Hz}$ to 20 kHz; see Figure 29
-3 dB Bandwidth	106			MHz typ	$R_L = 50\ \Omega$, $C_L = 5\ \text{pF}$; see Figure 30
Insertion Loss	-1.3			dB typ	$R_L = 50\ \Omega$, $C_L = 5\ \text{pF}$, $f = 1\ \text{MHz}$; see Figure 30
C_S (Off)	22			pF typ	$V_S = 6\ \text{V}$, $f = 1\ \text{MHz}$
C_D (Off)	67			pF typ	$V_S = 6\ \text{V}$, $f = 1\ \text{MHz}$
C_D (On), C_S (On)	85			pF typ	$V_S = 6\ \text{V}$, $f = 1\ \text{MHz}$
POWER REQUIREMENTS					$V_{DD} = 13.2\ \text{V}$
I_{DD}	40			μA typ	Digital inputs = 0 V or V_{DD}
	50		65	μA max	
V_{DD}			9/40	V min/V max	$\text{GND} = 0\ \text{V}$, $V_{SS} = 0\ \text{V}$

¹ Guaranteed by design; not subject to production test.

36 V SINGLE SUPPLY

$V_{DD} = 36\ \text{V} \pm 10\%$, $V_{SS} = 0\ \text{V}$, $\text{GND} = 0\ \text{V}$, unless otherwise noted.

Table 4.

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance, R_{ON}	10.6			Ω typ	$V_S = 0\ \text{V}$ to 30 V, $I_S = -10\ \text{mA}$; see Figure 25
On-Resistance Match Between Channels, ΔR_{ON}	12	15	17	Ω max	$V_{DD} = 32.4\ \text{V}$, $V_{SS} = 0\ \text{V}$
On-Resistance Flatness, $R_{FLAT(ON)}$	0.35			Ω typ	$V_S = 0\ \text{V}$ to 30 V, $I_S = -10\ \text{mA}$
	0.7	0.9	1.1	Ω max	
	2.7			Ω typ	$V_S = 0\ \text{V}$ to 30 V, $I_S = -10\ \text{mA}$
	3.2	3.8	4.5	Ω max	
LEAKAGE CURRENTS					
Source Off Leakage, I_S (Off)	± 0.05			nA typ	$V_{DD} = 39.6\ \text{V}$, $V_{SS} = 0\ \text{V}$ $V_S = 1\ \text{V}/30\ \text{V}$, $V_D = 30\ \text{V}/1\ \text{V}$; see Figure 28
Drain Off Leakage, I_D (Off)	± 0.25	± 0.75	± 6	nA max	
	± 0.1			nA typ	$V_S = 1\ \text{V}/30\ \text{V}$, $V_D = 30\ \text{V}/1\ \text{V}$; see Figure 28
Channel On Leakage, I_D (On), I_S (On)	± 0.4	± 2	± 12	nA max	
	± 0.1			nA typ	$V_S = V_D = 1\ \text{V}/30\ \text{V}$; see Figure 24
	± 0.4	± 2	± 12	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002			μA typ	$V_{IN} = V_{GND}$ or V_{DD}
			± 0.1	μA max	
Digital Input Capacitance, C_{IN}	5			pF typ	

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
DYNAMIC CHARACTERISTICS¹					
Transition Time, $t_{\text{TRANSITION}}$	174			ns typ	$R_L = 300 \Omega$, $C_L = 35 \text{ pF}$
	246	270	303	ns max	$V_S = 18 \text{ V}$; see Figure 31
t_{ON}	180			ns typ	$R_L = 300 \Omega$, $C_L = 35 \text{ pF}$
	247	270	301	ns max	$V_S = 18 \text{ V}$; see Figure 33
t_{OFF}	127			ns typ	$R_L = 300 \Omega$, $C_L = 35 \text{ pF}$
	179	193	215	ns max	$V_S = 18 \text{ V}$; see Figure 33
Break-Before-Make Time Delay, t_D	55			ns typ	$R_L = 300 \Omega$, $C_L = 35 \text{ pF}$
			18	ns min	$V_{S1} = V_{S2} = 18 \text{ V}$; see Figure 32
Charge Injection, Q_{INJ}	250			pC typ	$V_S = 18 \text{ V}$, $R_S = 0 \Omega$, $C_L = 1 \text{ nF}$; see Figure 34
Off Isolation	-78			dB typ	$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, $f = 1 \text{ MHz}$; see Figure 27
Channel-to-Channel Crosstalk	-58			dB typ	$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, $f = 1 \text{ MHz}$; see Figure 26
Total Harmonic Distortion + Noise	0.03			% typ	$R_L = 1 \text{ k}\Omega$, 18 V p-p , $f = 20 \text{ Hz}$ to 20 kHz ; see Figure 29
-3 dB Bandwidth	98			MHz typ	$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$; see Figure 30
Insertion Loss	-0.8			dB typ	$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, $f = 1 \text{ MHz}$; see Figure 30
C_S (Off)	19			pF typ	$V_S = 18 \text{ V}$, $f = 1 \text{ MHz}$
C_D (Off)	40			pF typ	$V_S = 18 \text{ V}$, $f = 1 \text{ MHz}$
C_D (On), C_S (On)	78			pF typ	$V_S = 18 \text{ V}$, $f = 1 \text{ MHz}$
POWER REQUIREMENTS					
I_{DD}	80			$\mu\text{A typ}$	$V_{\text{DD}} = 39.6 \text{ V}$
	100		130	$\mu\text{A max}$	Digital inputs = 0 V or V_{DD}
V_{DD}			9/40	V min/V max	$\text{GND} = 0 \text{ V}$, $V_{\text{SS}} = 0 \text{ V}$

¹ Guaranteed by design; not subject to production test.

CONTINUOUS CURRENT PER CHANNEL, Sx OR Dx

Table 5.

Parameter	25°C	85°C	125°C	Unit
CONTINUOUS CURRENT, Sx OR Dx				
$V_{\text{DD}} = +15 \text{ V}$, $V_{\text{SS}} = -15 \text{ V}$				
TSSOP ($\theta_{\text{JA}} = 112.6^\circ\text{C/W}$)	122	77	44	mA maximum
LFCSP ($\theta_{\text{JA}} = 30.4^\circ\text{C/W}$)	217	116	53	mA maximum
$V_{\text{DD}} = +20 \text{ V}$, $V_{\text{SS}} = -20 \text{ V}$				
TSSOP ($\theta_{\text{JA}} = 112.6^\circ\text{C/W}$)	130	80	45	mA maximum
LFCSP ($\theta_{\text{JA}} = 30.4^\circ\text{C/W}$)	229	121	54	mA maximum
$V_{\text{DD}} = 12 \text{ V}$, $V_{\text{SS}} = 0 \text{ V}$				
TSSOP ($\theta_{\text{JA}} = 112.6^\circ\text{C/W}$)	84	56	36	mA maximum
LFCSP ($\theta_{\text{JA}} = 30.4^\circ\text{C/W}$)	150	90	48	mA maximum
$V_{\text{DD}} = 36 \text{ V}$, $V_{\text{SS}} = 0 \text{ V}$				
TSSOP ($\theta_{\text{JA}} = 112.6^\circ\text{C/W}$)	110	70	42	mA maximum
LFCSP ($\theta_{\text{JA}} = 30.4^\circ\text{C/W}$)	196	109	52	mA maximum

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 6.

Parameter	Rating
V_{DD} to V_{SS}	48 V
V_{DD} to GND	-0.3 V to +48 V
V_{SS} to GND	+0.3 V to -48 V
Analog Inputs ¹	$V_{SS} - 0.3\text{ V}$ to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first
Digital Inputs ¹	$V_{SS} - 0.3\text{ V}$ to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first
Peak Current, Sx or Dx Pins	375 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, Sx or Dx ²	Data + 15%
Temperature Range	
Operating	-40°C to +125°C
Storage	-65°C to +150°C
Junction Temperature	150°C
Thermal Impedance, θ_{JA}	
16-Lead TSSOP (4-Layer Board)	112°C/W
16-Lead LFCSP	30.4°C/W
Reflow Soldering Peak Temperature, Pb Free	260(+0/-5)°C

¹ Overvoltages at the INx, Sx, and Dx pins are clamped by internal diodes. Current should be limited to the maximum ratings given.

² See Table 5.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

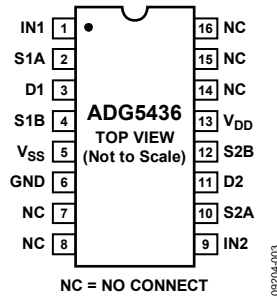
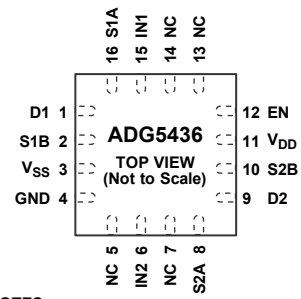


Figure 3. TSSOP Pin Configuration



NOTES
 1. EXPOSED PAD TIED TO SUBSTRATE, V_{SS}.
 2. NC = NO CONNECT.

Figure 4. LFCSP Pin Configuration

Table 7. Pin Function Descriptions

Pin No.		Mnemonic	Function
TSSOP	LFCSP		
1	15	IN1	Logic Control Input 1.
2	16	S1A	Source Terminal 1A. This pin can be an input or output.
3	1	D1	Drain Terminal 1. This pin can be an input or output.
4	2	S1B	Source Terminal 1B. This pin can be an input or output.
5	3	V _{SS}	Most Negative Power Supply Potential.
6	4	GND	Ground (0 V) Reference.
7, 8, 14 to 16	5, 7, 13, 14	NC	No Connect.
9	6	IN2	Logic Control Input 2.
10	8	S2A	Source Terminal 2A. This pin can be an input or output.
11	9	D2	Drain Terminal 2. This pin can be an input or output.
12	10	S2B	Source Terminal 2B. This pin can be an input or output.
13	11	V _{DD}	Most Positive Power Supply Potential.
Not applicable	12	EN	Active High Digital Input. When this pin is low, the device is disabled and all switches are off. When this pin is high, IN _x logic inputs determine the on switches.
Not applicable		EPAD	The exposed pad is connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the substrate, V _{SS} .

TRUTH TABLE FOR SWITCHES

Table 8. ADG5436 TSSOP Truth Table

IN _x	S _x A	S _x B
0	Off	On
1	On	Off

Table 9. ADG5436 LFCSP Truth Table

EN	IN _x	S _x A	S _x B
0	X ¹	Off	Off
1	0	Off	On
1	1	On	Off

¹ X is don't care.

TYPICAL PERFORMANCE CHARACTERISTICS

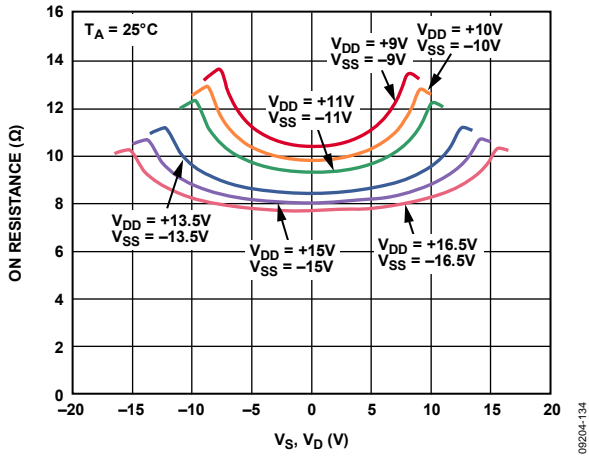


Figure 5. On Resistance vs. V_S , V_D (Dual Supply)

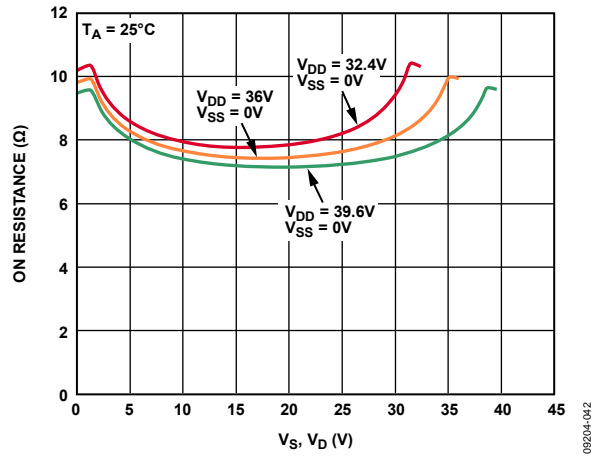


Figure 8. On Resistance vs. V_S , V_D (Single Supply)

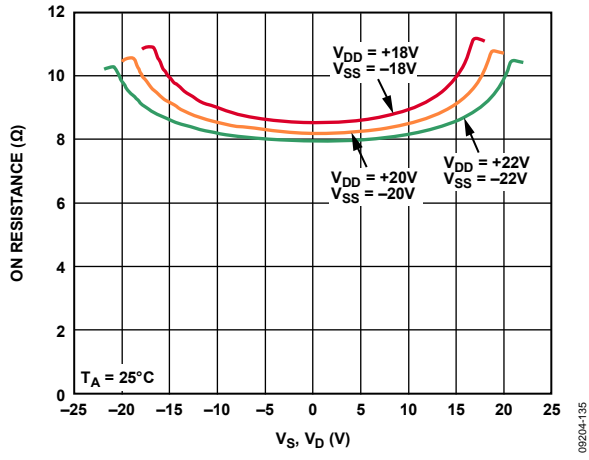


Figure 6. On Resistance vs. V_S , V_D (Dual Supply) Included

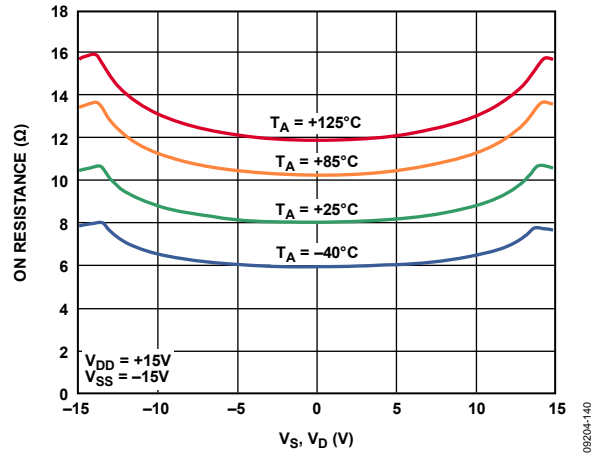


Figure 9. On Resistance vs. V_D or V_S for Different Temperatures, ± 15 V Dual Supply

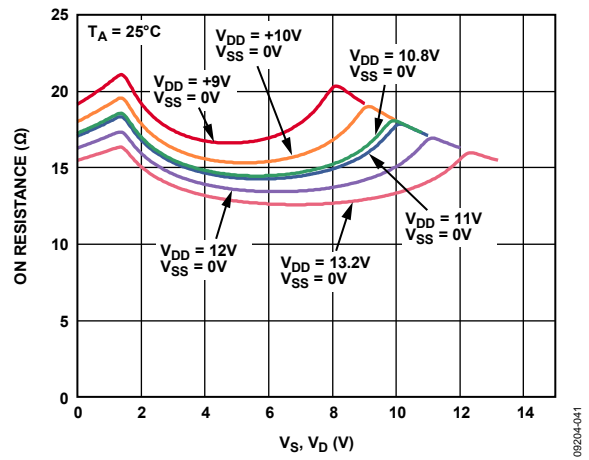


Figure 7. On Resistance vs. V_S , V_D (Single Supply)

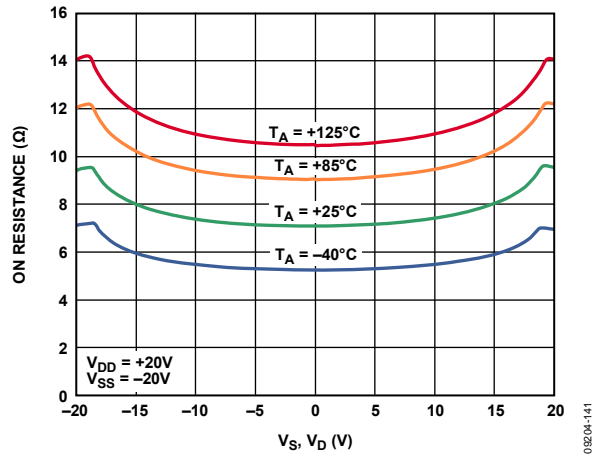


Figure 10. On Resistance vs. V_D or V_S for Different Temperatures, ± 20 V Dual Supply

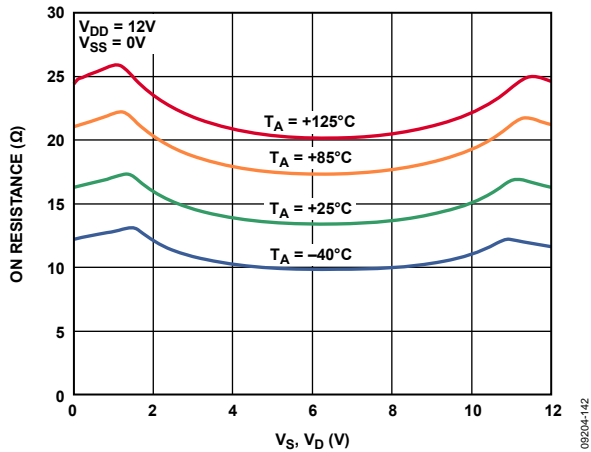


Figure 11. On Resistance vs. V_D or V_S for Different Temperatures, 12 V Single Supply

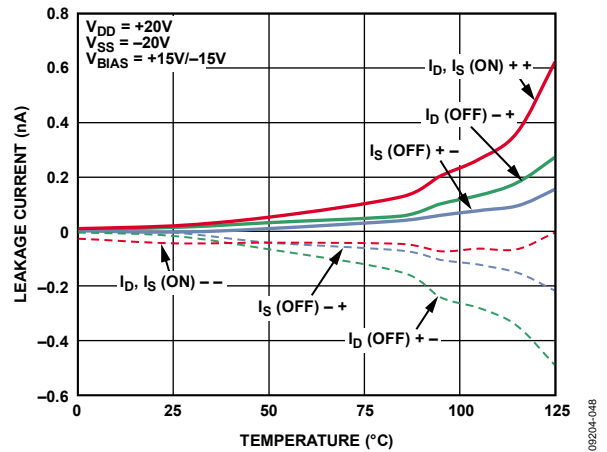


Figure 14. Leakage Currents vs. Temperature, ± 20 V Single Supply

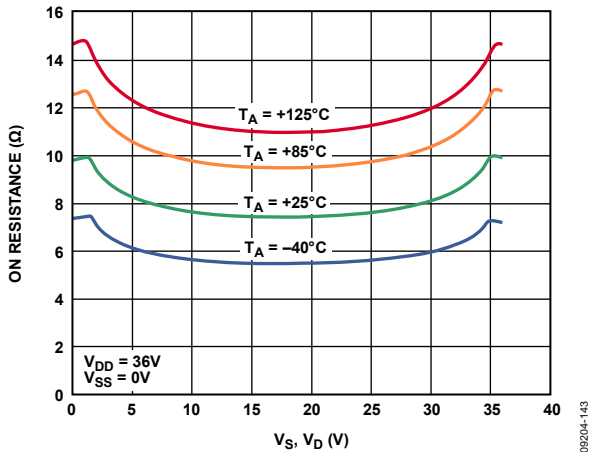


Figure 12. On Resistance vs. V_S (V_D) for Different Temperatures, 36 V Single Supply

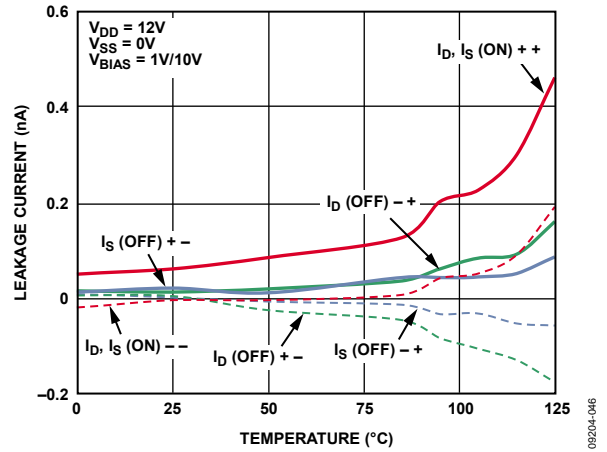


Figure 15. Leakage Currents vs. Temperature, 12 V Single Supply

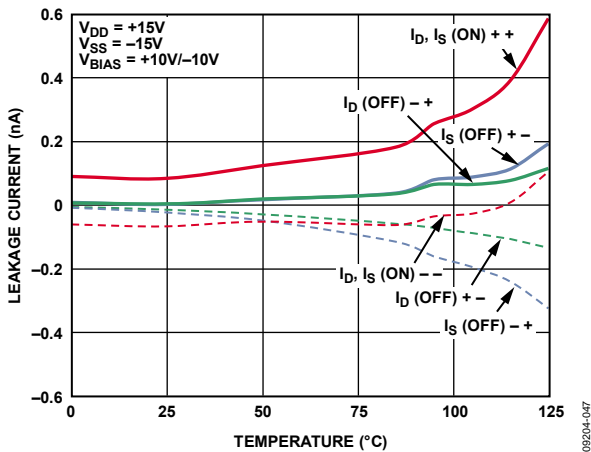


Figure 13. Leakage Currents vs. Temperature, ± 15 V Dual Supply

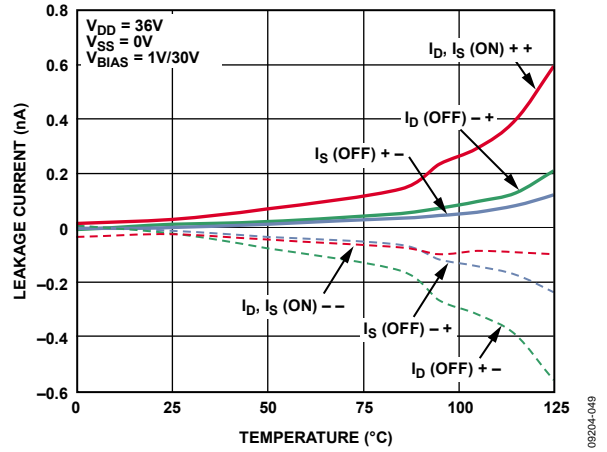


Figure 16. Leakage Currents vs. Temperature, 36 V Single Supply

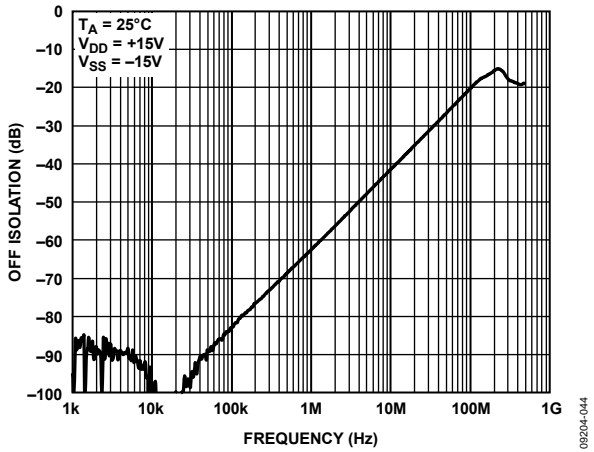


Figure 17. Off Isolation vs. Frequency

09204-044

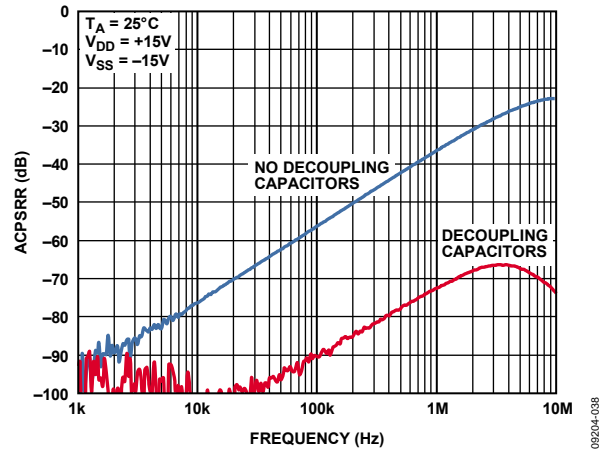


Figure 20. ACPSRR vs. Frequency

09204-038

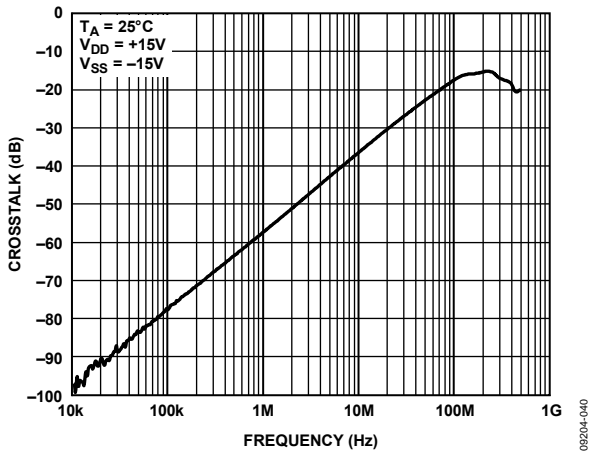


Figure 18. Crosstalk vs. Frequency

09204-040

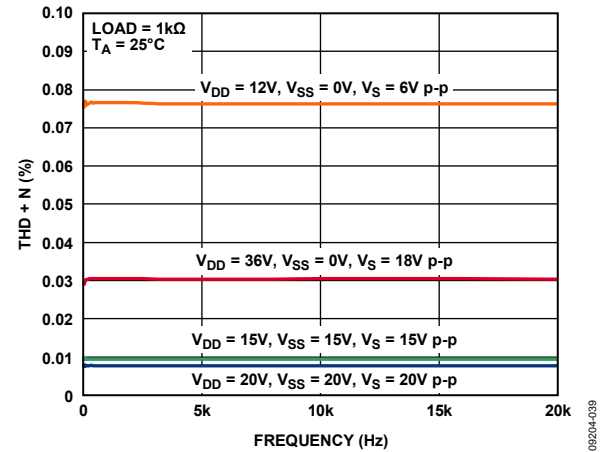


Figure 21. THD + N vs. Frequency

09204-039

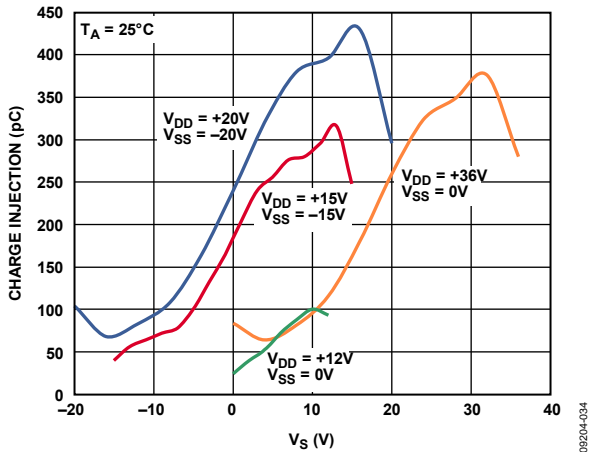


Figure 19. Charge Injection vs. Source Voltage

09204-034

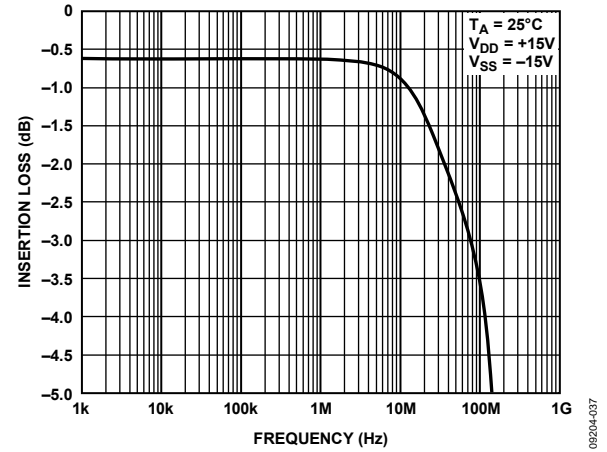


Figure 22. Bandwidth

09204-037

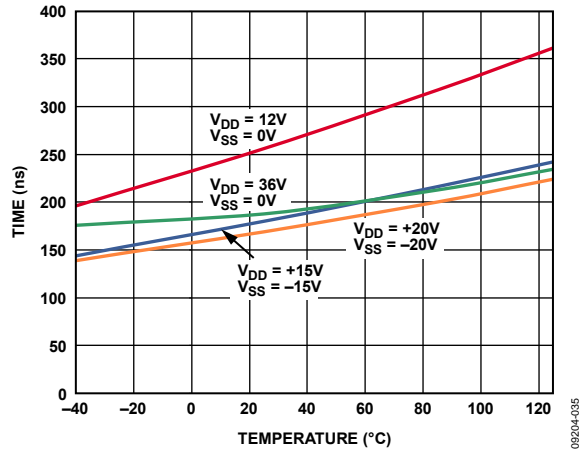


Figure 23. $t_{\text{TRANSITION}}$ Time vs. Temperature

TEST CIRCUITS

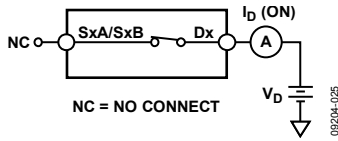


Figure 24. On Leakage



Figure 28. Off Leakage

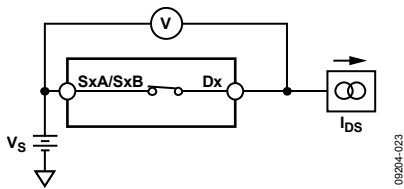


Figure 25. On Resistance

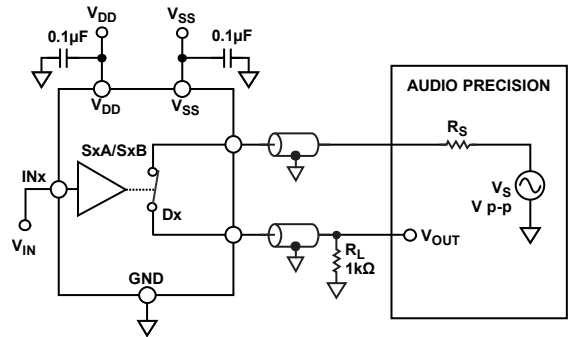
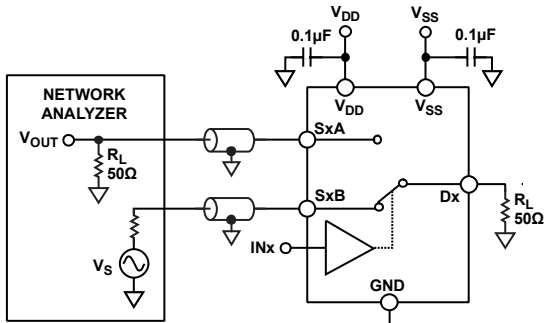
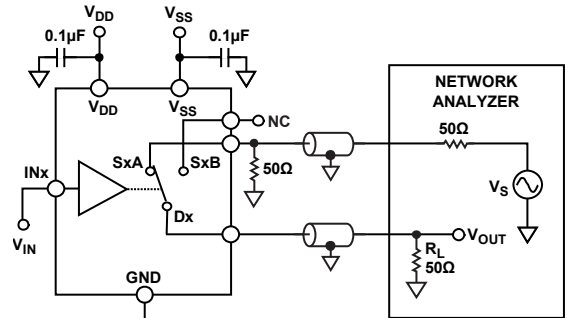


Figure 29. THD + Noise



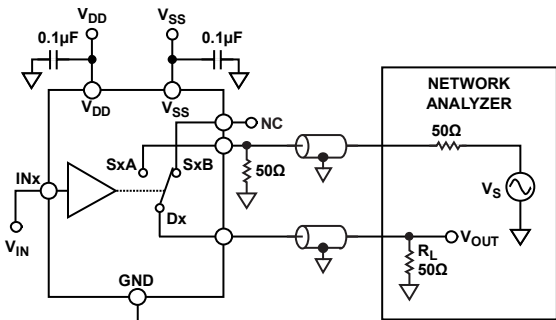
$$\text{CHANNEL-TO-CHANNEL CROSSTALK} = 20 \log \frac{V_{OUT}}{V_S}$$

Figure 26. Channel-to-Channel Crosstalk



$$\text{INSERTION LOSS} = 20 \log \frac{V_{OUT \text{ WITH SWITCH}}}{V_{OUT \text{ WITHOUT SWITCH}}}$$

Figure 30. Bandwidth



$$\text{OFF ISOLATION} = 20 \log \frac{V_{OUT}}{V_S}$$

Figure 27. Off Isolation

09204-032

09204-030

09204-033

09204-031

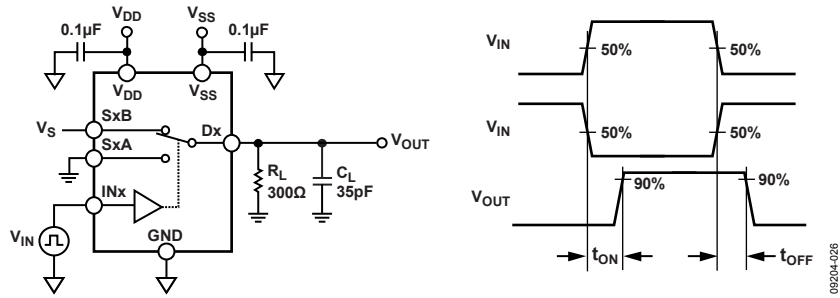


Figure 31. Switching Times

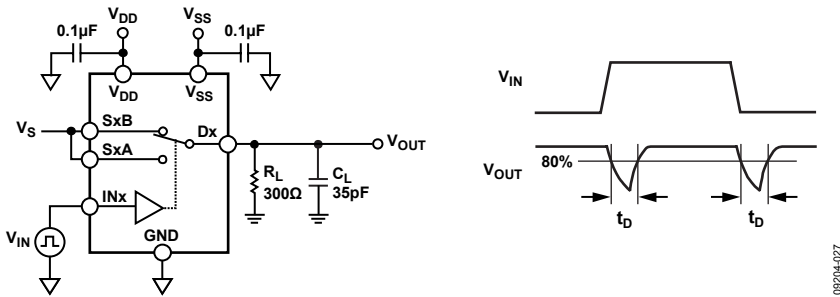


Figure 32. Break-Before-Make Time Delay t_D

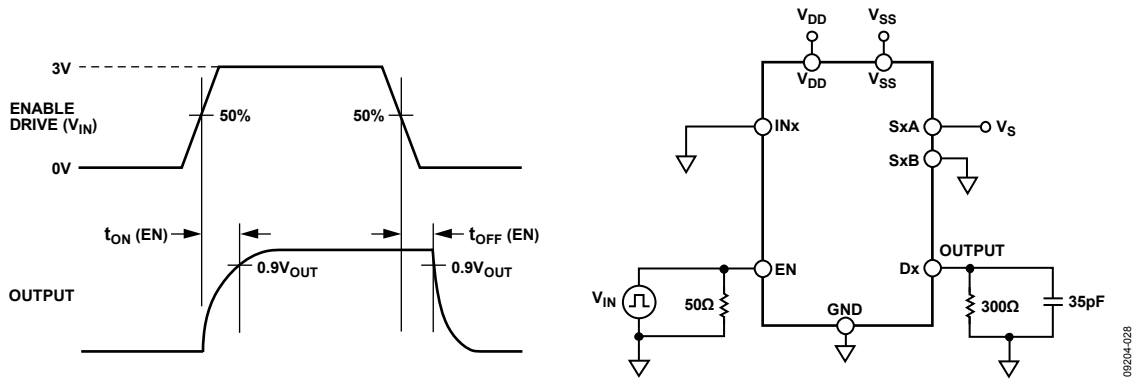


Figure 33. Enable Delay, $t_{ON} (EN)$, $t_{OFF} (EN)$

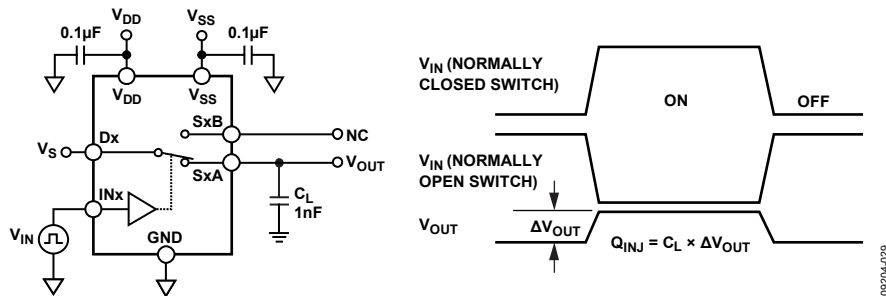


Figure 34. Charge Injection

TERMINOLOGY

I_{DD}

I_{DD} represents the positive supply current.

I_{SS}

I_{SS} represents the negative supply current.

V_D, V_S

V_D and V_S represent the analog voltage on Terminal D and Terminal S, respectively.

R_{ON}

R_{ON} represents the ohmic resistance between Terminal D and Terminal S.

ΔR_{ON}

ΔR_{ON} represents the difference between the R_{ON} of any two channels.

$R_{FLAT(ON)}$

Flatness that is defined as the difference between the maximum and minimum value of on resistance measured over the specified analog signal range is represented by $R_{FLAT(ON)}$.

I_S (Off)

I_S (Off) is the source leakage current with the switch off.

I_D (Off)

I_D (Off) is the drain leakage current with the switch off.

I_D (On), I_S (On)

I_D (On) and I_S (On) represent the channel leakage currents with the switch on.

V_{INL}

V_{INL} is the maximum input voltage for Logic 0.

V_{INH}

V_{INH} is the minimum input voltage for Logic 1.

I_{INL}, I_{INH}

I_{INL} and I_{INH} represent the low and high input currents of the digital inputs.

C_D (Off)

C_D (Off) represents the off switch drain capacitance, which is measured with reference to ground.

C_S (Off)

C_S (Off) represents the off switch source capacitance, which is measured with reference to ground.

C_D (On), C_S (On)

C_D (On) and C_S (On) represent on switch capacitances, which are measured with reference to ground.

C_{IN}

C_{IN} is the digital input capacitance.

t_{ON}

t_{ON} represents the delay between applying the digital control input and the output switching on.

t_{OFF}

t_{OFF} represents the delay between applying the digital control input and the output switching off.

t_D

t_D represents the off time measured between the 80% point of both switches when switching from one address state to another.

Off Isolation

Off isolation is a measure of unwanted signal coupling through an off switch.

Charge Injection

Charge injection is a measure of the glitch impulse transferred from the digital input to the analog output during switching.

Crosstalk

Crosstalk is a measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Bandwidth

Bandwidth is the frequency at which the output is attenuated by 3 dB.

On Response

On response is the frequency response of the on switch.

Insertion Loss

Insertion loss is the loss due to the on resistance of the switch.

Total Harmonic Distortion + Noise (THD + N)

The ratio of the harmonic amplitude plus noise of the signal to the fundamental is represented by THD + N.

AC Power Supply Rejection Ratio (ACPSRR)

ACPSRR is the ratio of the amplitude of signal on the output to the amplitude of the modulation. This is a measure of the ability of the part to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p.

TRENCH ISOLATION

In the [ADG5436](#), an insulating oxide layer (trench) is placed between the NMOS and the PMOS transistors of each CMOS switch. Parasitic junctions, which occur between the transistors in junction isolated switches, are eliminated, and the result is a completely latch-up proof switch.

In junction isolation, the N and P wells of the PMOS and NMOS transistors form a diode that is reverse-biased under normal operation. However, during overvoltage conditions, this diode can become forward-biased. A silicon controlled rectifier (SCR) type circuit is formed by the two transistors causing a significant amplification of the current that, in turn, leads to latch-up. With trench isolation, this diode is removed, and the result is a latch-up proof switch.

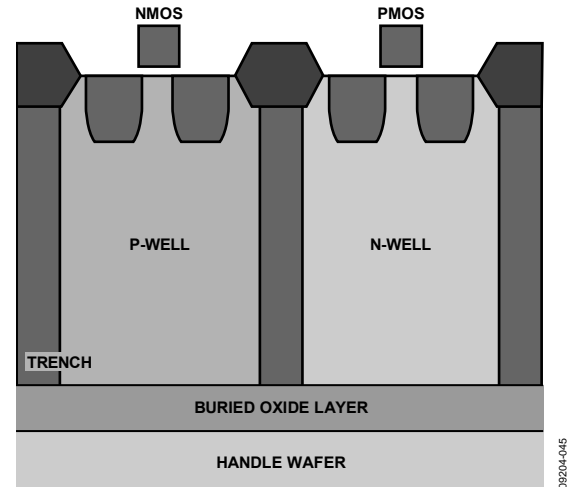


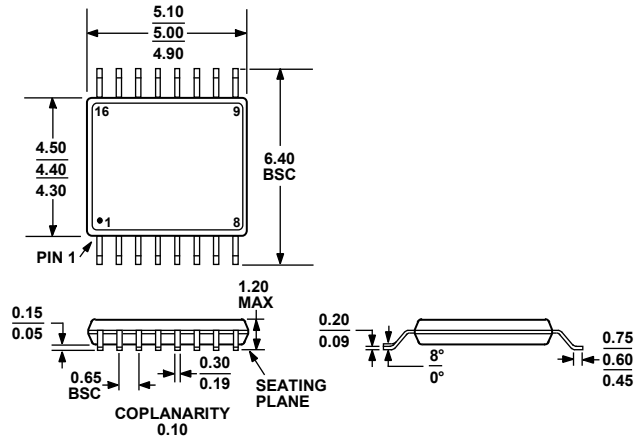
Figure 35. Trench Isolation

APPLICATIONS INFORMATION

The Analog Devices, Inc., family of switches and multiplexers provide a robust solution for instrumentation, industrial, automotive, aerospace and other harsh environments that are prone to latch-up, which is an undesirable high current state that can lead to device failure and persist until the power supply is turned off. The [ADG5436](#) high voltage switches allow single-

supply operation from +9 V to +40 V and dual-supply operation from ± 9 V to ± 22 V. The [ADG5436](#) (as well as other select devices within this family) achieves an 8 kV human body model ESD rating, which provides a robust solution eliminating the need for separate protect circuitry designs in some applications.

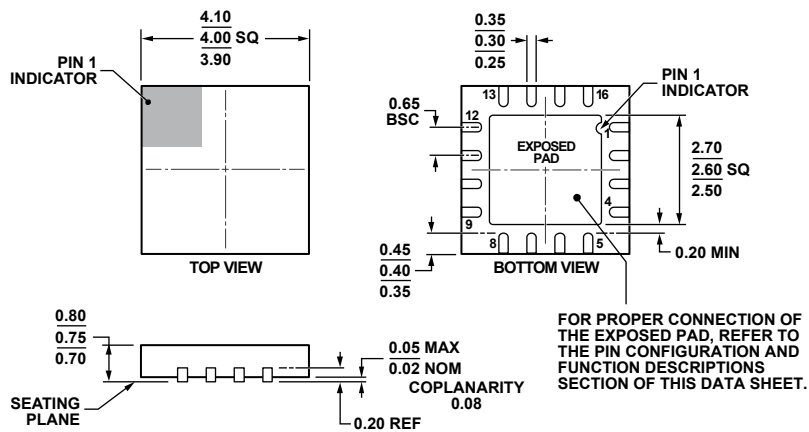
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 36. 16-Lead Thin Shrink Small Outline Package [TSSOP] (RU-16)

Dimensions shown in millimeters



FOR PROPER CONNECTION OF THE EXPOSED PAD, REFER TO THE PIN CONFIGURATION AND FUNCTION DESCRIPTIONS SECTION OF THIS DATA SHEET.

COMPLIANT TO JEDEC STANDARDS MO-220-WGGC.

Figure 37. 16-Lead Lead Frame Chip Scale Package [LFCSP] 4 mm x 4 mm Body and 0.75 mm Package Height (CP-16-17)

Dimensions shown in millimeters

08-16-2010-C

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
ADG5436BRUZ	-40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG5436BRUZ-REEL7	-40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG5436BCPZ-REEL7	-40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-17

¹ Z = RoHS Compliant Part.



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