

# BGS18MA12

## MIPI 2.0 SP8T switch for LTE diversity, Tx and LAA applications

### Key Features

- 0.1 to 6 GHz coverage for LTE and LAA application
- LTE TX Power handling capabilities
- Ultra low insertion loss: 0.78dB at Band 42
- Small form factor 1.1mm x 1.9mm
- Fully compatible with MIPI 2.0 RFFE standard
- No decoupling capacitors required if no DC applied on RF lines

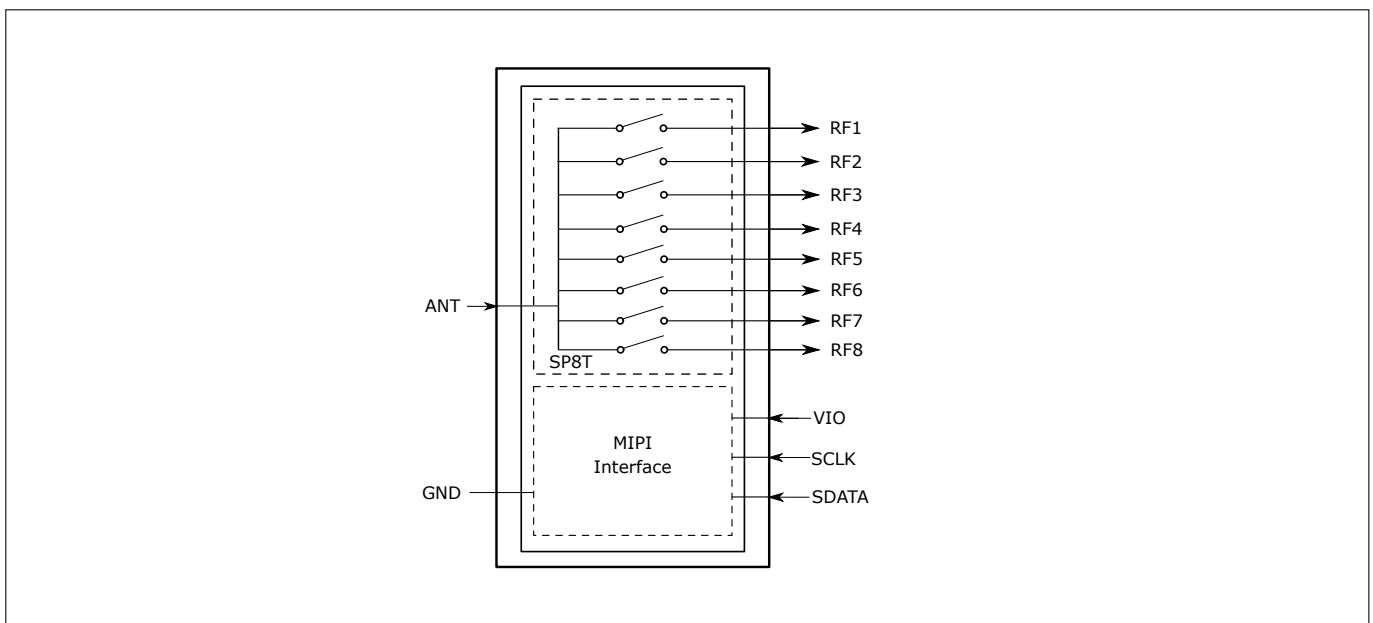
### Applications

The SP8T switch is a band selection switch for LTE applications. With LTE TX power handling capability it is suitable for both LTE diversity path and LTE uplink Tx applications. The switch covers up to 6 GHz, so it supports Band 42, Band 43 and LAA.

### Product Validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

### Block diagram



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## MIPI 2.0 SP8T switch for LTE diversity, Tx and LAA applications

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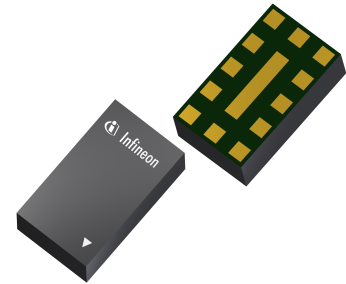
# BGS18MA12

## MIPI 2.0 SP8T switch for LTE diversity, Tx and LAA applications

### Features

## 1 Features

- 0.1 to 6 GHz coverage for LTE and LAA application
- Suitable for LTE / WCDMA / TDCDMA Applications
- LTE TX Power handling capabilities
- Ultra low insertion loss: 0.78dB at Band 42
- Small form factor 1.1mm x 1.9mm
- Fully compatible with MIPI 2.0 RFFE standard
- No decoupling capacitors required if no DC applied on RF lines
- Low harmonic generation
- High port-to-port-isolation
- On chip control logic including ESD protection
- No power supply blocking required
- High EMI robustness
- RoHS and WEEE compliant package



## Description

This SP8T RF switch is a perfect solution for multimode handsets based on LTE, WCDMA and TDCDMA. It is based on Infineon's proprietary technology and has excellent RF performance. The ultra-low insertion loss helps customers to achieve high system sensitivity, the coverage of LTE Tx power and 6 GHz enables very broad application. It features DC-free RF ports, external DC blocking capacitors at the RF ports are only required if DC voltage is applied externally. Its on chip MIPI RFFE 2.0 controller is fully compatible with industry standard.

| Product Name | Marking | Package     |
|--------------|---------|-------------|
| BGS18MA12    | B1      | ATSLP-12-10 |

# BGS18MA12

## MIPI 2.0 SP8T switch for LTE diversity, Tx and LAA applications

### Maximum Ratings

## 2 Maximum Ratings

**Table 1: Maximum Ratings, Table I** at  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified

| Parameter  | Symbol         | Values |      |      | Unit             | Note / Test Condition                        |
|--|----------------|--------|------|------|------------------|--|
|  |                | Min.   | Typ. | Max. |                  |  |
| Frequency Range                                      | $f$            | 0.1    | –    | 6.0  | GHz              | 1)   |
| Supply voltage <sup>2)</sup>                         | $V_{IO}$       | 0      | –    | 2.1  | V                | –  |
| Storage temperature range                            | $T_{STG}$      | -55    | –    | 150  | $^\circ\text{C}$ | –  |
| RF input power at all TRx ports                      | $P_{RF\_max}$  | –      | –    | 35   | dBm              | Short momentary / $50\Omega$                 |
| ESD capability, CDM <sup>4)</sup>                    | $V_{ESD\_CDM}$ | -500   | –    | +500 | V                |  |
| ESD capability, HBM <sup>5)</sup>                    | $V_{ESD\_HBM}$ | -1     | –    | +1   | kV               |  |
| ESD capability, system level (RF port) <sup>6)</sup> | $V_{ESD\_ANT}$ | -8     | –    | +8   | kV               | ANT vs system GND, with 27 nH shunt inductor |
| Junction temperature                                 | $T_j$          | –      | –    | 125  | $^\circ\text{C}$ | –  |

<sup>1)</sup> Switch has a low-pass response. For higher frequencies, losses have to be considered for their impact on thermal heating. The DC voltage at RF ports  $V_{RFDC}$  has to be 0V.

<sup>2)</sup> Note: Consider any ripple voltages on top of  $V_{IO}$ . Including RF ripple,  $V_{IO}$  must not exceed the maximum ratings:  $V_{IO} = V_{DC} + V_{Ripple}$ .

<sup>4)</sup> Field-Induced Charged-Device Model ANSI/ESDA/JEDEC JS-002. Simulates charging/discharging events that occur in production equipment and processes. Potential for CDM ESD events occurs whenever there is metal-to-metal contact in manufacturing.

<sup>5)</sup> Human Body Model ANSI/ESDA/JEDEC JS-001 ( $R = 1,5\text{ k}\Omega$ ,  $C = 100\text{ pF}$ ).

<sup>6)</sup> IEC 61000-4-2 ( $R = 330\ \Omega$ ,  $C = 150\text{ pF}$ ), contact discharge.

**Warning: Stresses above the max. values listed here may cause permanent damage to the device. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit. Exposure to conditions at or below absolute maximum rating but above the specified maximum operation conditions may affect device reliability and life time. Functionality of the device might not be given under these conditions.**

**Table 2: Maximum Ratings, Table II** at  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified

| Parameter                                     | Symbol     | Values |      |      | Unit | Note / Test Condition              |
|---|------------|--------|------|------|------|------------------------------------|
|   |            | Min.   | Typ. | Max. |      |                                    |
| Thermal resistance junction - soldering point | $R_{thJS}$ | –      | –    | 62   | K/W  | –                                  |
| Maximum DC-voltage on RF-Ports and RF-Ground  | $V_{RFDC}$ | 0      | –    | 0    | V    | No DC voltages allowed on RF-Ports |

**Operation ranges**

**3 Operation ranges**

**Table 3: Operation ranges at  $T_A = -40\text{ °C}$  to  $85\text{ °C}$**

| Parameter                             | Symbol     | Values             |      |                    | Unit          | Note / Test Condition |
|---------------------------------------|------------|--------------------|------|--------------------|---------------|-----------------------|
|                                       |            | Min.               | Typ. | Max.               |               |                       |
| Supply Voltage                        | $V_{IO}$   | 1.65               | 1.8  | 1.95               | V             | –                     |
| RFFE input high voltage <sup>1</sup>  | $V_{IH}$   | $0.7 \cdot V_{IO}$ | –    | $V_{IO}$           | V             | –                     |
| RFFE input low voltage <sup>1</sup>   | $V_{IL}$   | 0                  | –    | $0.3 \cdot V_{IO}$ | V             | –                     |
| RFFE output high voltage <sup>1</sup> | $V_{OH}$   | $0.8 \cdot V_{IO}$ | –    | $V_{IO}$           | V             | –                     |
| RFFE output low voltage <sup>1</sup>  | $V_{OL}$   | 0                  | –    | $0.2 \cdot V_{IO}$ | V             | –                     |
| RFFE control input capacitance        | $C_{Ctrl}$ | –                  | –    | 2                  | pF            | –                     |
| Supply Current                        | $I_{IO}$   | –                  | 60   | 125                | $\mu\text{A}$ | Operating state       |
| Supply Current                        | $I_{IO}$   | –                  | 2    | –                  | $\mu\text{A}$ | Idle State            |

<sup>1</sup>SCLK and SDATA

**Table 4: RF input power**

| Parameter                   | Symbol   | Values |      |      | Unit | Note / Test Condition |
|-----------------------------|----------|--------|------|------|------|-----------------------|
|                             |          | Min.   | Typ. | Max. |      |                       |
| RF input power on TRX ports | $P_{RF}$ | –      | –    | 32   | dBm  | CW / VSWR 1:1 / 25 °C |
| RF input power on TRX ports | $P_{RF}$ | –      | –    | 30   | dBm  | CW / VSWR 6:1 / 25 °C |

**RF Characteristics**

**4 RF Characteristics**

**Table 5: RF Characteristics** at  $T_A = -40\text{ }^{\circ}\text{C} \dots 85\text{ }^{\circ}\text{C}$ ,  $P_{IN} = 0\text{ dBm}$ , Supply Voltage  $V_{IO} = 1.65\text{ V} \dots 1.95\text{ V}$ , unless otherwise specified. Open ports are terminated with  $50\ \Omega$ .

| Parameter  | Symbol                 | Values |      |      | Unit | Note / Test Condition         |
|--|------------------------|--------|------|------|------|-------------------------------|
|  |                        | Min.   | Typ. | Max. |      |                               |
| <b>Insertion Loss<sup>1)</sup></b>                                   |                        |        |      |      |      |                               |
| All TRx Ports  | IL                     | -      | 0.35 | 0.41 | dB   | 698–960 MHz                   |
|  |                        | -      | 0.42 | 0.46 | dB   | 1428–1920 MHz                 |
|  |                        | -      | 0.46 | 0.50 | dB   | 1990–2170 MHz                 |
|  |                        | -      | 0.55 | 0.60 | dB   | 2170–2690 MHz                 |
|  |                        | -      | 0.65 | 0.80 | dB   | 3400–3600 MHz                 |
|  |                        | -      | 0.70 | 0.90 | dB   | 3600–3800 MHz                 |
|  |                        | -      | 1.20 | 1.80 | dB   | 5000–6000 MHz                 |
| <b>Return Loss<sup>1)</sup></b>                                      |                        |        |      |      |      |                               |
| All TRx Ports  | RL                     | 27     | 30   | -    | dB   | 698–960 MHz                   |
|  |                        | 19     | 26   | -    | dB   | 1428–1920 MHz                 |
|  |                        | 17     | 21   | -    | dB   | 1990–2170 MHz                 |
|  |                        | 14     | 19   | -    | dB   | 2170–2690 MHz                 |
|  |                        | 13     | 16   | -    | dB   | 3400–3600 MHz                 |
|  |                        | 12     | 16   | -    | dB   | 3600–3800 MHz                 |
|  |                        | 7      | 10   | -    | dB   | 5000–6000 MHz                 |
| <b>Isolation<sup>1) 2)</sup></b>                                     |                        |        |      |      |      |                               |
| All TRx Ports  | ISO                    | 32     | 47   | -    | dB   | 698–960 MHz                   |
|  |                        | 26     | 40   | -    | dB   | 1428–1920 MHz                 |
|  |                        | 26     | 37   | -    | dB   | 1990–2170 MHz                 |
|  |                        | 23     | 36   | -    | dB   | 2170–2690 MHz                 |
|  |                        | 18     | 31   | -    | dB   | 3400–3600 MHz                 |
|  |                        | 18     | 30   | -    | dB   | 3600–3800 MHz                 |
|  |                        | 12     | 26   | -    | dB   | 5000–6000 MHz                 |
| <b>Harmonic Generation (UMTS Band 1, Band 5)<sup>1)</sup></b>        |                        |        |      |      |      |                               |
| 2 <sup>nd</sup> harmonic generation                                  | $P_{H2}$               | -70    | -80  | -    | dBm  | 27 dBm, 50 $\Omega$ , CW mode |
| 3 <sup>rd</sup> harmonic generation                                  | $P_{H3}$               | -61    | -60  | -    | dBm  | 27 dBm, 50 $\Omega$ , CW mode |
| <b>Intermodulation Distortion (UMTS Band 1, Band 5)<sup>1)</sup></b> |                        |        |      |      |      |                               |
| 2 <sup>nd</sup> order intermodulation                                | IMD2 low <sup>3)</sup> | -      | -    | -110 | dBm  | IMT, US Cell (see Tab. 7)     |
| 3 <sup>rd</sup> order intermodulation                                | IMD3                   | -      | -    | -105 | dBm  | IMT, US Cell (see Tab. 8)     |
| 2 <sup>nd</sup> order intermodulation                                | IMD2 high              | -      | -    | -110 | dBm  | IMT, US Cell (see Tab. 7)     |

<sup>1)</sup>On application board without any matching components.

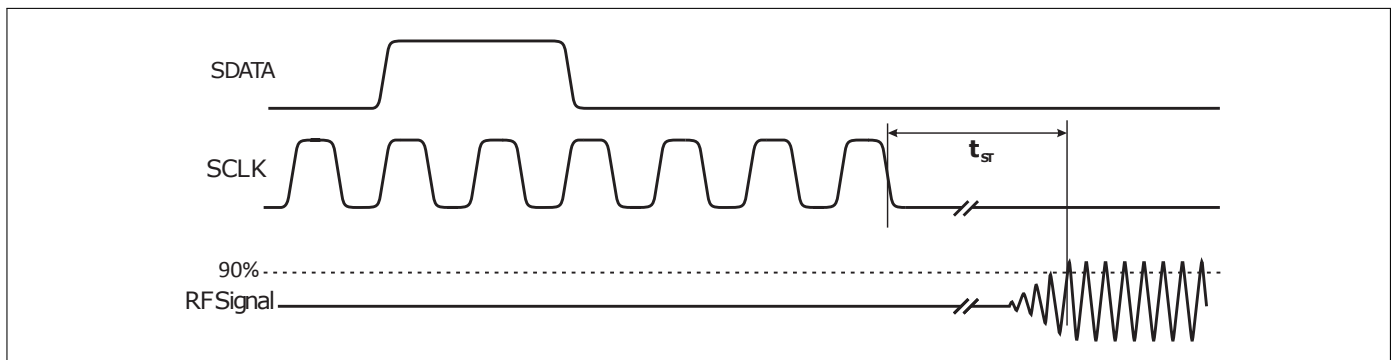
<sup>2)</sup>Isolation to inactive ports when one path is active.

<sup>3)</sup>With 27 nH shunt inductor at the ANT.

### RF Characteristics

**Table 6: Switching Time** at  $T_A = 25\text{ }^\circ\text{C}$ ,  $P_{IN} = 0\text{ dBm}$ , Supply Voltage  $V_{IO} = 1.65\text{V} \dots 1.95\text{V}$ , unless otherwise specified

| Parameter              | Symbol    | Values |      |      | Unit          | Note / Test Condition                                   |
|------------------------|-----------|--------|------|------|---------------|---|
|                        |           | Min.   | Typ. | Max. |               |   |
| <b>Switching Time</b>  |           |        |      |      |               |   |
| RF Rise Time           | $t_{RT}$  | -      | -    | 2    | $\mu\text{s}$ | 10 % to 90 % RF signal                                  |
| Switching Time         | $t_{ST}$  | -      | 3    | 4.5  | $\mu\text{s}$ | 50% last SCLK falling edge to 90% RF signal, see Fig. 1 |
| Power Up Settling Time | $t_{Pup}$ | -      | 10   | 25   | $\mu\text{s}$ | After power down mode                                   |



**Figure 1:** MIPI to RF time

**Table 7: IMD2 Testcases**

| Band    | CW tone 1 (MHz) | CW tone 1 (dBm) | CW tone 2 (MHz)  | CW tone 2 (dBm) |
|---------|-----------------|-----------------|------------------|-----------------|
| IMT     | 1950            | 20              | 190 (IMD2 low)   | -15             |
|         |                 |                 | 4090 (IMD2 high) |                 |
| US Cell | 835             | 20              | 45 (IMD2 low)    | -15             |
|         |                 |                 | 1715 (IMD2 high) |                 |

**Table 8: IMD3 Testcases**

| Band    | CW tone 1 (MHz) | CW tone 1 (dBm) | CW tone 2 (MHz) | CW tone 2 (dBm) |
|---------|-----------------|-----------------|-----------------|-----------------|
| IMT     | 1950            | 20              | 1760            | -15             |
| US Cell | 835             | 20              | 790             | -15             |

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## MIPI 2.0 SP8T switch for LTE diversity, Tx and LAA applications

### MIPI RFFE Specification

## 5 MIPI RFFE Specification

All sequences are implemented according to the 'MIPI Alliance Specification for RF Front-End Control Interface' document version 2.0 - 25. September 2014.

**Table 9: MIPI Features**

| Feature  | Supported | Comment   |
|--|-----------|---|
| MIPI RFFE 1.10 and 2.0 standards                         | Yes       |   |
| Register 0 write command sequence                        | Yes       |   |
| Register read and write command sequence                 | Yes       |   |
| Extended register read and write command sequence        | Yes       |   |
| Support for standard frequency range operations for SCLK | Yes       | Up to 26 MHz for read and write                     |
| Support for extended frequency range operations for SCLK | Yes       | Up to 52 MHz for write <sup>1)</sup>                |
| Half speed read  | Yes       |   |
| Full speed read  | Yes       |   |
| Full speed write   | Yes       |   |
| Programmable Group SID                                   | Yes       |   |
| Trigger functionality                                    | Yes       |   |
| Broadcast / GSID write to PM TRIG register               | Yes       |   |
| Reset  | Yes       | Via VIO, PM TRIG or software register <sup>1)</sup> |
| Status / error sum register                              | Yes       |   |
| Extended product ID register                             | Yes       |   |
| Revision ID register                                     | Yes       |   |
| Group SID register                                       | Yes       |   |
| USID_Sel pin   | No        | External pin for changing USID is not implemented   |

<sup>1)</sup> only supported by MIPI 2.0 Standard

**Table 10: Startup Behavior**

| Feature          | State     | Comment  |
|------------------|-----------|--|
| Power status     | Low power | Lower power mode after start-up                                    |
| Trigger function | Enabled   | Enabled after start-up. Programmable via behavior control register |



**MIPI RFFE Specification**

**Table 11: Register Mapping, Table I**

| Register Address                                      | Register Name | Data Bits                              | Function                      | Description   | Default   | Broadcast_ID Support | Trigger Support | R/W |    |
|---|---------------|--|-------------------------------|---|---|----------------------|-----------------|-----|----|
| 0x00  | SW_CTRL0      | 6:0                                    | SW_CTRL0                      | RF Switch Control   | 0   | No                   | Yes             | R/W |    |
| 0x1C  | PM_TRIG       | 7                                      | PWR_MODE(1), Operation Mode   | 0: Normal operation (ACTIVE)  | 1   | Yes                  | No              | R/W |    |
|   |               |  |                               | 1: Low Power Mode (LOW POWER)   |   |                      |                 |     |    |
|   |               | 6                                      | PWR_MODE(0), State Bit Vector | 0: No action (ACTIVE)   | 0   |                      |                 |     |    |
|   |               |  |                               | 1: Powered Reset (STARTUP to ACTIVE to LOW POWER)   |   |                      |                 |     |    |
|   |               | 5                                      | TRIGGER_MASK_2                | 0: Data masked (held in shadow REG)   | 0   |                      |                 |     | No |
|   |               |  |                               | 1: Data not masked (ready for transfer to active REG)   |   |                      |                 |     |    |
|   |               | 4                                      | TRIGGER_MASK_1                | 0: Data masked (held in shadow REG)   | 0   |                      |                 |     |    |
|   |               |  |                               | 1: Data not masked (ready for transfer to active REG)   |   |                      |                 |     |    |
|   |               | 3                                      | TRIGGER_MASK_0                | 0: Data masked (held in shadow REG)   | 0   |                      |                 |     |    |
| 1: Data not masked (ready for transfer to active REG) |               |  |                               |   |   |                      |                 |     |    |
| 2   | TRIGGER_2     | 0: No action (data held in shadow REG) | 0                             | Yes   |   |                      |                 |     |    |
|   |               | 1: Data transferred to active REG      |                               |   |   |                      |                 |     |    |
| 1   | TRIGGER_1     | 0: No action (data held in shadow REG) | 0                             |   |   |                      |                 |     |    |
|   |               | 1: Data transferred to active REG      |                               |   |   |                      |                 |     |    |
| 0   | TRIGGER_0     | 0: No action (data held in shadow REG) | 0                             |   |   |                      |                 |     |    |
|   |               | 1: Data transferred to active REG      |                               |   |   |                      |                 |     |    |
| 0x1D  | PRODUCT_ID    | 7:0                                    | PRODUCT_ID                    |   | This is a read-only register. However, during the programming of the USID a write command sequence is performed on this register, even though the write does not change its value.  | 0xCD                 | No              | No  | R  |
| 0x1E  | MAN_ID        | 7:0                                    | MANUFACTURER_ID [7:0]         |   | This is a read-only register. However, during the programming of the USID, a write command sequence is performed on this register, even though the write does not change its value. | 0x1A                 | No              | No  | R  |
| 0x1F  | MAN_USID      | 7:6                                    | RESERVED                      |   | Reserved for future use   | 00                   | No              | No  | R  |
|   |               | 5:4                                    | MANUFACTURER_ID [9:8]         | These bits are read-only. However, during the programming of the USID, a write command sequence is performed on this register even though the write does not change its value.                      | 01  |                      |                 |     |    |
|   |               | 3:0                                    | USID[3:0]                     | Programmable USID. Performing a write to this register using the described programming sequences will program the USID in devices supporting this feature. These bits store the USID of the device. | 0x8   | No                   | No              | R/W |    |

### MIPI RFFE Specification

**Table 12: Register Mapping, Table II**

| Register Address | Register Name             | Data Bits                                     | Function              | Description   | Default | Broadcast_ID Support | Trigger Support | R/W |
|------------------|---------------------------|---|-----------------------|---|---------|----------------------|-----------------|-----|
| 0x20             | EXT_PROD_ID <sup>1)</sup> | 7:0   | EXT_PRODUCT_ID        |   | 0x00    | No                   | No              | R   |
| 0x21             | REV_ID                    | 7:4   | MAIN_REVISION         |   | 0x4     | No                   | No              | R/W |
|                  |                           | 3:0   | SUB_REVISION          |   | 0x0     |                      |                 |     |
| 0x22             | GSID <sup>1)</sup>        | 7:4   | GSID0[3:0]            | Primary Group Slave ID.   | 0x0     | No                   | No              | R/W |
|                  |                           | 3:0   | RESERVED              | Reserved for secondary Group Slave ID.  | 0x0     |                      |                 |     |
| 0x23             | UDR_RST                   | 7   | UDR_RST               | Reset all configurable non-RFFE Reserved registers to default values.<br>0: Normal operation<br>1: Software reset | 0       | No                   | No              | R/W |
|                  |                           | 6:0   | RESERVED              | Reserved for future use   | 0000000 |                      |                 |     |
| 0x24             | ERR_SUM <sup>1)</sup>     | 7   | RESERVED              | Reserved for future use   | 0       | No                   | No              | R   |
|                  |                           | 6   | COMMAND_FRAME_PAR_ERR | Command Sequence received with parity error – discard command.  | 0       |                      |                 |     |
|                  |                           | 5   | COMMAND_LENGTH_ERR    | Command length error.   | 0       |                      |                 |     |
|                  |                           | 4   | ADDRESS_FRAME_PAR_ERR | Address frame with parity error.  | 0       |                      |                 |     |
|                  |                           | 3   | DATA_FRAME_PAR_ERR    | Data frame with parity error.   | 0       |                      |                 |     |
|                  |                           | 2   | READ_UNUSED_REG       | Read command to an invalid address.   | 0       |                      |                 |     |
|                  |                           | 1   | WRITE_UNUSED_REG      | Write command to an invalid address.  | 0       |                      |                 |     |
| 0                | BID_GID_ERR               | Read command with a BROADCAST_ID or GROUP_ID. | 0                     |   |         |                      |                 |     |

<sup>1)</sup>Only supported by MIPI 2.0 Standard

**Table 13: Modes of Operation (Truth Table, Register\_0)**

| State <sup>1)</sup> | Value (Bin.) | Mode                |
|---------------------|--------------|---------------------|
| 0                   | 00000000     | ALL OFF (Isolation) |
| 1                   | 00000001     | RF1 ON              |
| 2                   | 00000010     | RF2 ON              |
| 3                   | 00000100     | RF3 ON              |
| 4                   | 00001000     | RF4 ON              |
| 5                   | 00010000     | RF5 ON              |
| 6                   | 00100000     | RF6 ON              |
| 7                   | 01000000     | RF7 ON              |
| 8                   | 01000001     | RF8 ON              |

<sup>1)</sup> Chip state is 0 (isolation) in unused states

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## MIPI 2.0 SP8T switch for LTE diversity, Tx and LAA applications

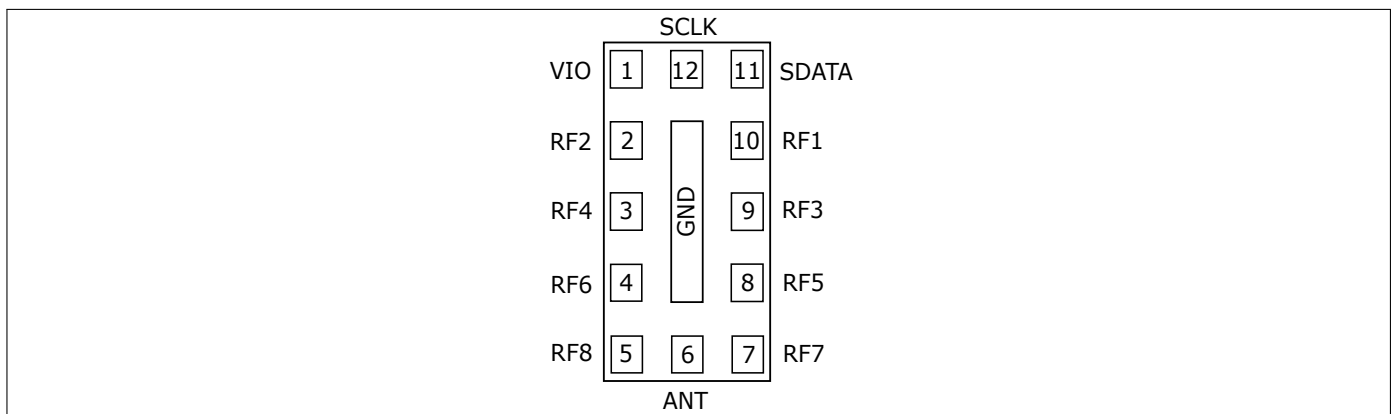
### Package related information

## 6 Package related information

The switch has a package size of 1100  $\mu\text{m}$  in x-dimension and 1900  $\mu\text{m}$  in y-dimension with a maximum deviation of  $\pm 50 \mu\text{m}$  in each dimension. Fig. 2 shows the footprint from top view. The definition of each pin can be found in Tab. 15.

**Table 14: Mechanical Data**

| Parameter           | Symbol | Value         | Unit          |
|---------------------|--------|---------------|---------------|
| Package X-Dimension | X      | 1100 $\pm$ 50 | $\mu\text{m}$ |
| Package Y-Dimension | Y      | 1900 $\pm$ 50 | $\mu\text{m}$ |
| Package Height      | H      | 0.65 max      | $\mu\text{m}$ |



**Figure 2:** Footprint, top view

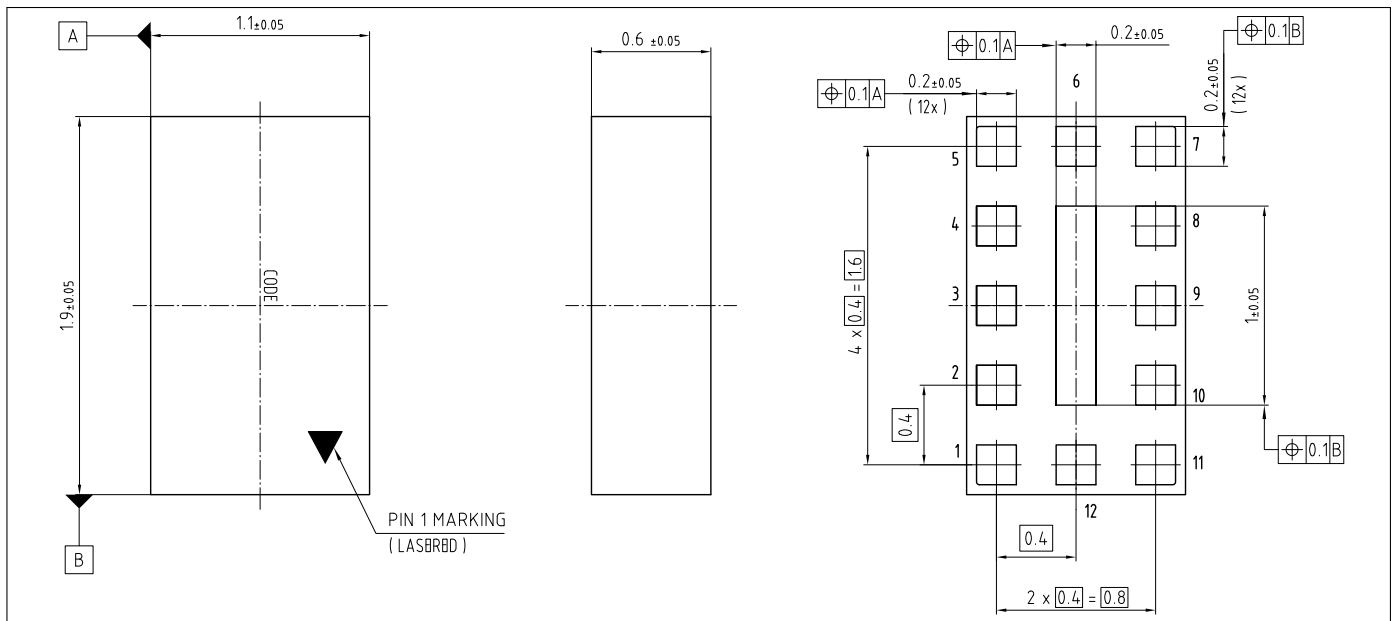
**Table 15: Pin Definition**

| No. | Name  | Pin Type | Function               |
|-----|-------|----------|------------------------|
| 1   | VIO   | Power    | MIPI RFFE Power Supply |
| 2   | RF2   | RF       | RF-Port TRX No. 2      |
| 3   | RF4   | RF       | RF-Port TRX No. 4      |
| 4   | RF6   | RF       | RF-Port TRX No. 6      |
| 5   | RF8   | RF       | RF-Port TRX No. 8      |
| 6   | ANT   | RF       | RF Antenna Port        |
| 7   | RF7   | RF       | RF-Port TRX No. 7      |
| 8   | RF5   | RF       | RF-Port TRX No. 5      |
| 9   | RF3   | RF       | RF-Port TRX No. 3      |
| 10  | RF1   | RF       | RF-Port TRX No. 1      |
| 11  | SDATA | I/O      | MIPI RFFE Data I/O     |
| 12  | SCLK  | I/O      | MIPI RFFE Clock        |
| GND | GND   | GND      | Ground                 |

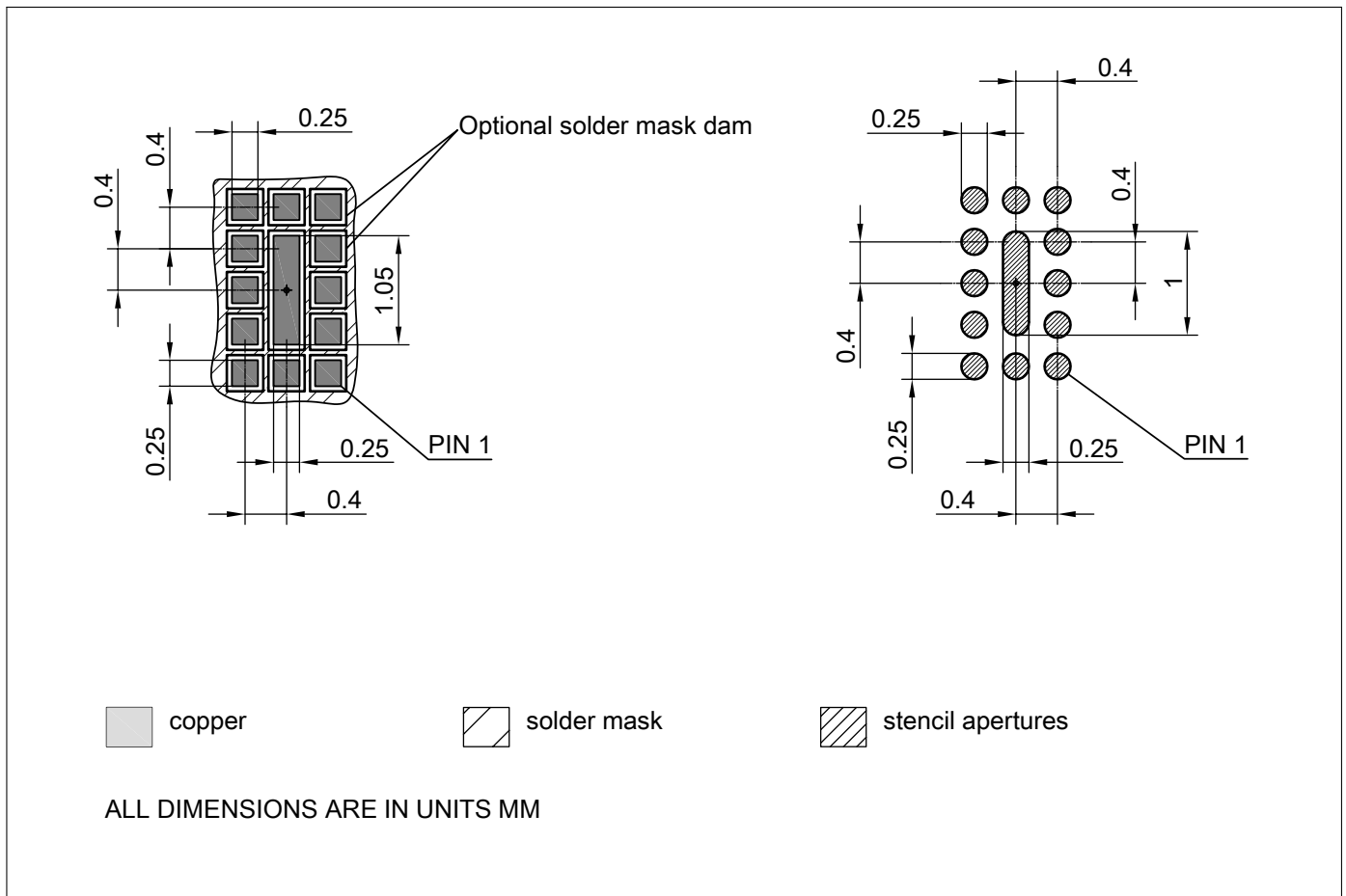
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## MIPI 2.0 SP8T switch for LTE diversity, Tx and LAA applications

### Package related information



**Figure 3:** Package Outline Drawing (top, side and bottom views)

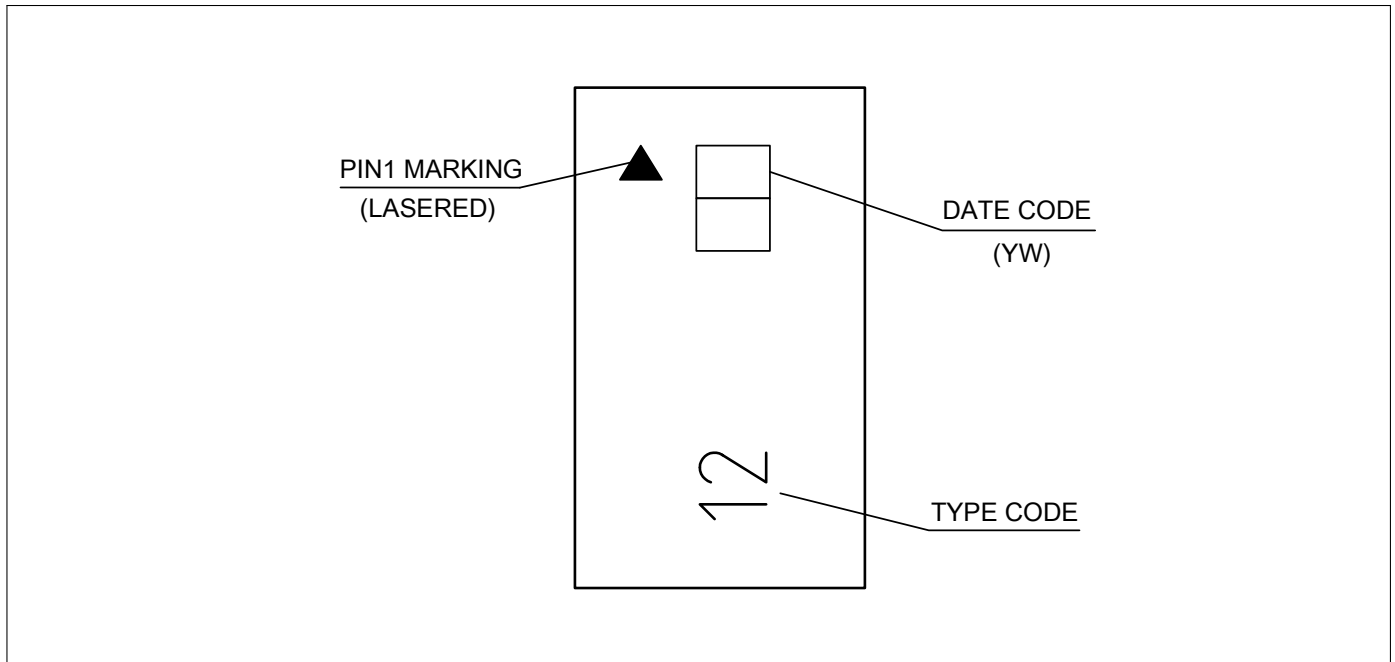


**Figure 4:** Land Pattern Drawing

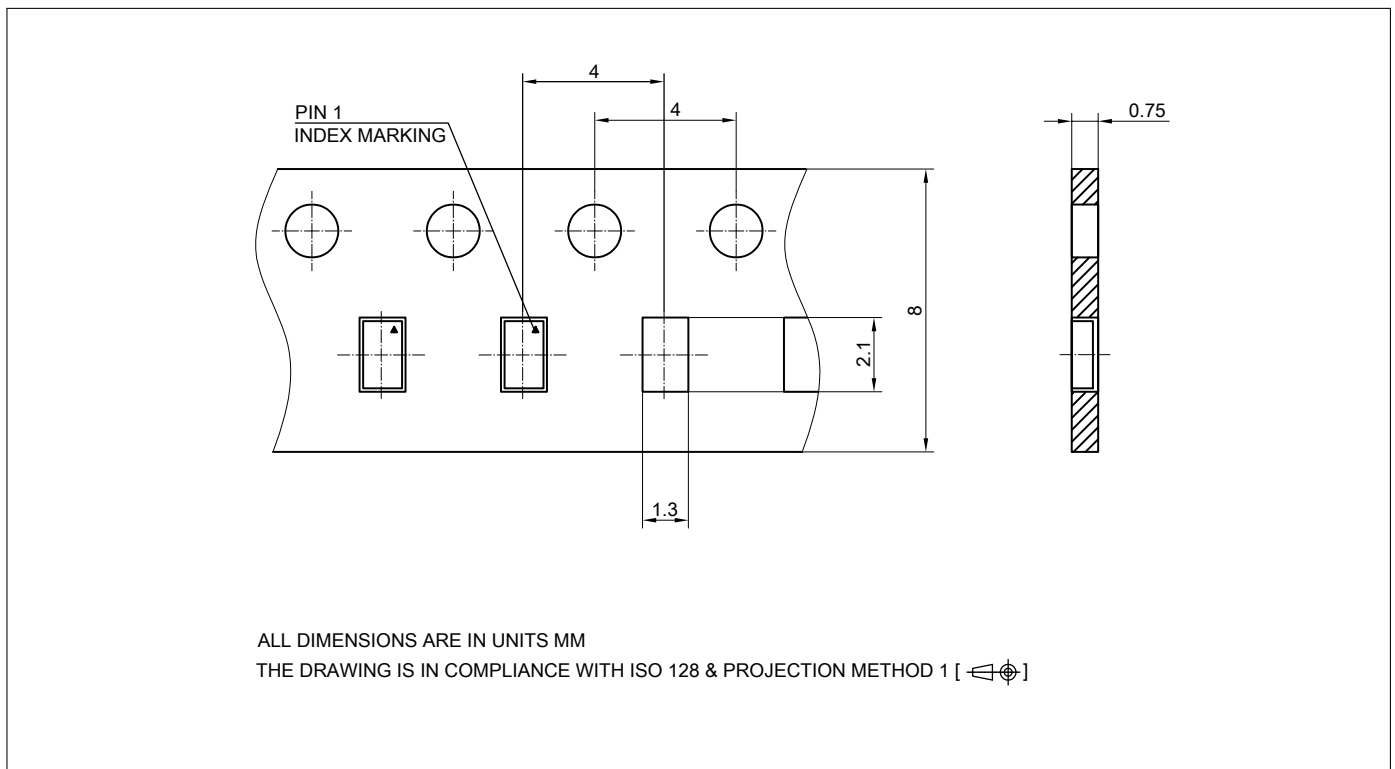
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## MIPI 2.0 SP8T switch for LTE diversity, Tx and LAA applications

### Package related information



**Figure 5:** Laser marking



**Figure 6:** Carrier Tape

**Table 16: Year date code marking - digit "Y"**

| Year | "Y" | Year | "Y" | Year | "Y" |
|------|-----|------|-----|------|-----|
| 2000 | 0   | 2010 | 0   | 2020 | 0   |
| 2001 | 1   | 2011 | 1   | 2021 | 1   |
| 2002 | 2   | 2012 | 2   | 2022 | 2   |
| 2003 | 3   | 2013 | 3   | 2023 | 3   |
| 2004 | 4   | 2014 | 4   | 2024 | 4   |
| 2005 | 5   | 2015 | 5   | 2025 | 5   |
| 2006 | 6   | 2016 | 6   | 2026 | 6   |
| 2007 | 7   | 2017 | 7   | 2027 | 7   |
| 2008 | 8   | 2018 | 8   | 2028 | 8   |
| 2009 | 9   | 2019 | 9   | 2029 | 9   |

**Table 17: Week date code marking - digit "W"**

| Week | "W" | Week | "W" | Week | "W" | Week | "W" | Week | "W" |
|------|-----|------|-----|------|-----|------|-----|------|-----|
| 1    | A   | 12   | N   | 23   | 4   | 34   | h   | 45   | v   |
| 2    | B   | 13   | P   | 24   | 5   | 35   | j   | 46   | x   |
| 3    | C   | 14   | Q   | 25   | 6   | 36   | k   | 47   | y   |
| 4    | D   | 15   | R   | 26   | 7   | 37   | l   | 48   | z   |
| 5    | E   | 16   | S   | 27   | a   | 38   | n   | 49   | 8   |
| 6    | F   | 17   | T   | 28   | b   | 39   | p   | 50   | 9   |
| 7    | G   | 18   | U   | 29   | c   | 40   | q   | 51   | 2   |
| 8    | H   | 19   | V   | 30   | d   | 41   | r   | 52   | 3   |
| 9    | J   | 20   | W   | 31   | e   | 42   | s   |      |     |
| 10   | K   | 21   | Y   | 32   | f   | 43   | t   |      |     |
| 11   | L   | 22   | Z   | 33   | g   | 44   | u   |      |     |

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**Revision History**

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| Page or Item | Subjects (major changes since previous revision) |
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| Revision 1.1, 2018-09-10 |  |
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