

# 1-Mbit (64 K x 16) Static RAM

## Features

- Temperature ranges
  - Industrial: -40 °C to 85 °C
  - Automotive-A: -40 °C to 85 °C
- Pin-and function-compatible with CY7C1021CV33
- High speed
  - $t_{AA} = 10$  ns
- Low active power
  - $I_{CC} = 60$  mA @ 10 ns
- Low CMOS standby power
  - $I_{SB2} = 3$  mA
- 2.0 V data retention
- Automatic power-down when deselected
- CMOS for optimum speed/power
- Independent control of upper and lower bits
- Available in Pb-free 44-pin 400-Mil wide molded SOJ, 44-pin TSOP II and 48-ball VFBGA packages

## Functional Description<sup>[1]</sup>

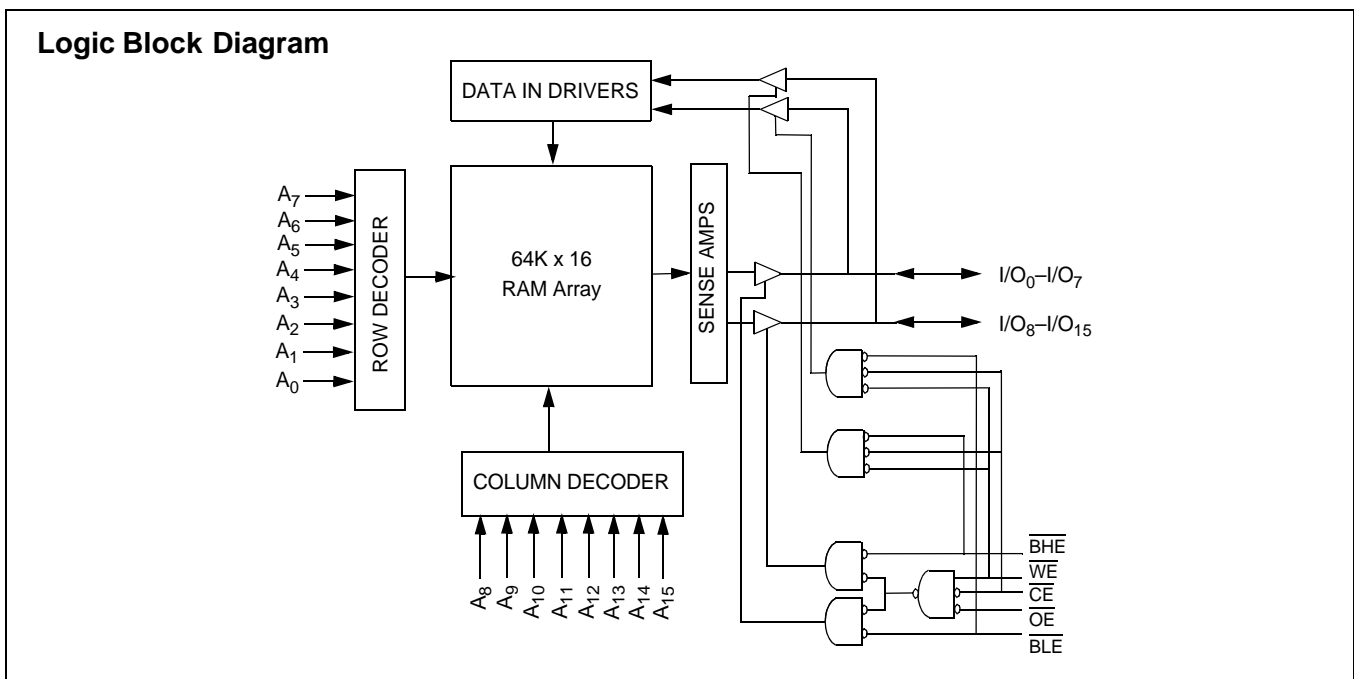
The CY7C1021DV33 is a high-performance CMOS static RAM organized as 65,536 words by 16 bits. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

Writing to the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from I/O pins ( $I/O_0$  through  $I/O_7$ ), is written into the location specified on the address pins ( $A_0$  through  $A_{15}$ ). If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from I/O pins ( $I/O_8$  through  $I/O_{15}$ ) is written into the location specified on the address pins ( $A_0$  through  $A_{15}$ ).

Reading from the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from the memory location specified by the address pins will appear on  $I/O_0$  to  $I/O_7$ . If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from memory will appear on  $I/O_8$  to  $I/O_{15}$ . See the truth table at the end of this data sheet for a complete description of Read and Write modes.

The input/output pins ( $I/O_0$  through  $I/O_{15}$ ) are placed in a high-impedance state when the device is deselected ( $\overline{CE}$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), the  $\overline{BHE}$  and  $\overline{BLE}$  are disabled ( $\overline{BHE}$ ,  $\overline{BLE}$  HIGH), or during a Write operation ( $\overline{CE}$  LOW, and  $\overline{WE}$  LOW).

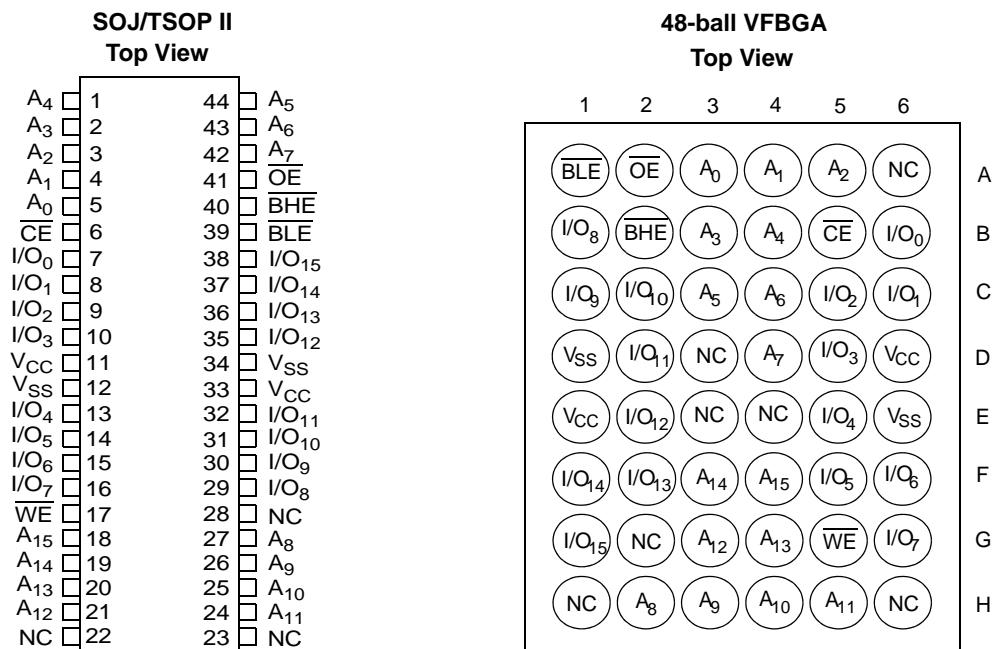
The CY7C1021DV33 is available in Pb-free 44-pin 400-Mil wide Molded SOJ, 44-pin TSOP II and 48-ball VFBGA packages.



**Selection Guide**

	-10 (Industrial/Automotive-A)	Unit
Maximum access time	10	ns
Maximum operating current	60	mA
Maximum CMOS standby current	3	mA

**Pin Configuration<sup>[1]</sup>**



**Notes**

1. NC pins are not connected on the die.

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage temperature .....	-65 °C to +150 °C
Ambient temperature with power applied .....	-55 °C to +125 °C
Supply voltage on V <sub>CC</sub> to Relative GND <sup>[2]</sup> ...	-0.3 V to +4.6 V
DC Voltage applied to outputs in high-Z State <sup>[2]</sup> .....	-0.3 V to V <sub>CC</sub> +0.3 V
DC input voltage <sup>[2]</sup> .....	-0.3 V to V <sub>CC</sub> +0.3 V

Current into outputs (LOW) .....	20 mA
Static discharge voltage.....	> 2001 V (per MIL-STD-883, method 3015)
Latch-up current .....	>200 mA

## Operating Range

Range	Ambient Temperature	V <sub>CC</sub>	Speed
Industrial	-40 °C to +85°C	3.3 V ± 0.3 V	10 ns
Automotive-A	-40 °C to +85°C		10 ns

## DC Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	-10 (Ind/I/Auto-A)		Unit
			Min.	Max.	
V <sub>OH</sub>	Output HIGH voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA	2.4		V
V <sub>OL</sub>	Output LOW voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA		0.4	V
V <sub>IH</sub>	Input HIGH voltage		2.0	V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Input LOW voltage <sup>[2]</sup>		-0.3	0.8	V
I <sub>IX</sub>	Input leakage current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1	+1	μA
I <sub>OZ</sub>	Output leakage current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub> , Output Disabled	-1	+1	μA
I <sub>CC</sub>	V <sub>CC</sub> operating supply current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>RC</sub>	100 MHz	60	mA
			83 MHz	55	mA
			66 MHz	45	mA
			40 MHz	30	mA
I <sub>SB1</sub>	Automatic CE Power-Down Current —TTL Inputs	Max. V <sub>CC</sub> , $\overline{CE} \geq V_{IH}$ V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>		10	mA
I <sub>SB2</sub>	Automatic CE Power-Down Current —CMOS Inputs	Max. V <sub>CC</sub> , $\overline{CE} \geq V_{CC} - 0.3 V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3 V or V <sub>IN</sub> ≤ 0.3 V, f = 0		3	mA

## Capacitance<sup>[3]</sup>

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 3.3 V	8	pF
C <sub>OUT</sub>	Output capacitance		8	pF

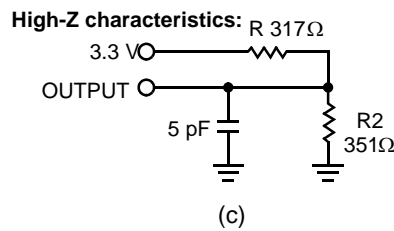
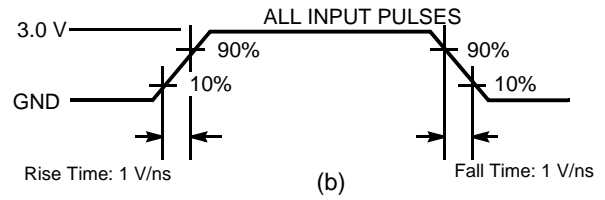
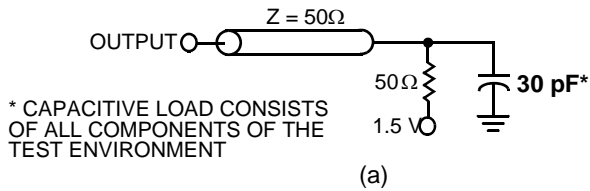
## Thermal Resistance<sup>[3]</sup>

Parameter	Description	Test Conditions	SOJ	TSOP II	VFBGA	Unit
Θ <sub>JA</sub>	Thermal resistance (Junction to Ambient)	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	59.52	53.91	36	°C/W
Θ <sub>JC</sub>	Thermal resistance (Junction to Case)		36.75	21.24	9	°C/W

### Notes

- V<sub>IL</sub> (min.) = -2.0 V and V<sub>IH</sub> (max) = V<sub>CC</sub> + 1 V for pulse durations of less than 5 ns.
- Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms<sup>[4]</sup>



Note

4. AC characteristics (except High-Z) are tested using the load conditions shown in Figure (a). High-Z characteristics are tested for all speeds using the test load shown in Figure (c).

**Switching Characteristics** Over the Operating Range<sup>[5]</sup>

Parameter	Description	-10 (Ind'I/Auto-A)		Unit
		Min.	Max.	
<b>Read Cycle</b>				
$t_{power}^{[6]}$	$V_{CC}$ (typical) to the first access	100		$\mu$ s
$t_{RC}$	Read cycle time	10		ns
$t_{AA}$	Address to data valid		10	ns
$t_{OHA}$	Data hold from address change	3		ns
$t_{ACE}$	$\overline{CE}$ LOW to data valid		10	ns
$t_{DOE}$	$\overline{OE}$ LOW to data valid		5	ns
$t_{LZOE}$	$\overline{OE}$ LOW to low-Z <sup>[8]</sup>	0		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to high-Z <sup>[7, 8]</sup>		5	ns
$t_{LZCE}$	$\overline{CE}$ LOW to low-Z <sup>[8]</sup>	3		ns
$t_{HZCE}$	$\overline{CE}$ HIGH to high-Z <sup>[7, 8]</sup>		5	ns
$t_{PU}^{[9]}$	$\overline{CE}$ LOW to power-up	0		ns
$t_{PD}^{[9]}$	$\overline{CE}$ HIGH to power-down		10	ns
$t_{DBE}$	Byte Enable to data valid		5	ns
$t_{LZBE}$	Byte Enable to low-Z	0		ns
$t_{HZBE}$	Byte Disable to high-Z		6	ns
<b>Write Cycle<sup>[10]</sup></b>				
$t_{WC}$	Write cycle time	10		ns
$t_{SCE}$	$\overline{CE}$ LOW to write end	8		ns
$t_{AW}$	Address set-up to write end	8		ns
$t_{HA}$	Address hold from write end	0		ns
$t_{SA}$	Address set-up to write start	0		ns
$t_{PWE}$	$\overline{WE}$ pulse width	7		ns
$t_{SD}$	Data set-up to write end	5		ns
$t_{HD}$	Data hold from write end	0		ns
$t_{LZWE}$	$\overline{WE}$ HIGH to low-Z <sup>[8]</sup>	3		ns
$t_{HZWE}$	$\overline{WE}$ LOW to high-Z <sup>[7, 8]</sup>		5	ns
$t_{BW}$	Byte enable to end of write	7		ns

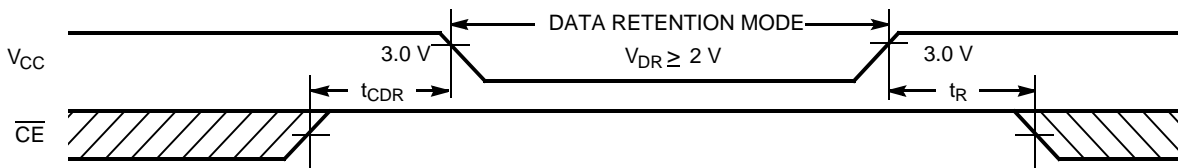
**Notes**

5. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V.
6.  $t_{POWER}$  gives the minimum amount of time that the power supply should be at typical  $V_{CC}$  values until the first memory access can be performed.
7.  $t_{HZOE}$ ,  $t_{HZBE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with a load capacitance of 5 pF as in (c) of AC Test Loads. Transition is measured when the outputs enter a high impedance state.
8. At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
9. This parameter is guaranteed by design and is not tested.
10. The internal Write time of the memory is defined by the overlap of  $\overline{CE}$  LOW,  $\overline{WE}$  LOW and  $\overline{BHE}/\overline{BLE}$  LOW.  $\overline{CE}$ ,  $\overline{WE}$  and  $\overline{BHE}/\overline{BLE}$  must be LOW to initiate a Write and the transition of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.

**Data Retention Characteristics** Over the Operating Range

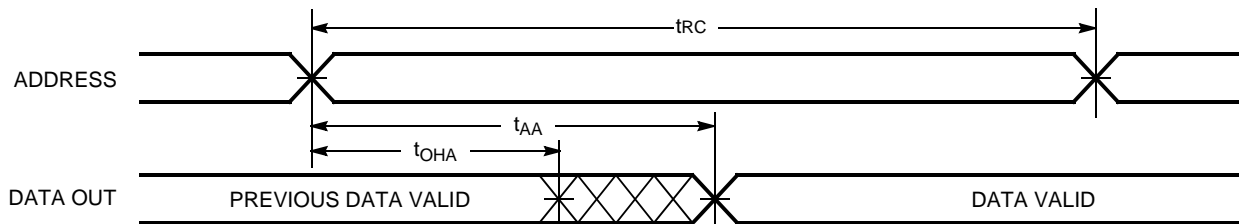
Parameter	Description	Conditions	Min.	Max.	Unit
$V_{DR}$	$V_{CC}$ for data retention		2		V
$I_{CCDR}$	Data retention current	$V_{CC} = V_{DR} = 2.0\text{ V}$ , $\overline{CE} \geq V_{CC} - 0.3\text{ V}$ , $V_{IN} \geq V_{CC} - 0.3\text{ V}$ or $V_{IN} \leq 0.3\text{ V}$		3	mA
$t_{CDR}^{[3]}$	Chip deselect to data retention time		0		ns
$t_R^{[11]}$	Operation recovery time		$t_{RC}$		ns

**Data Retention Waveform**

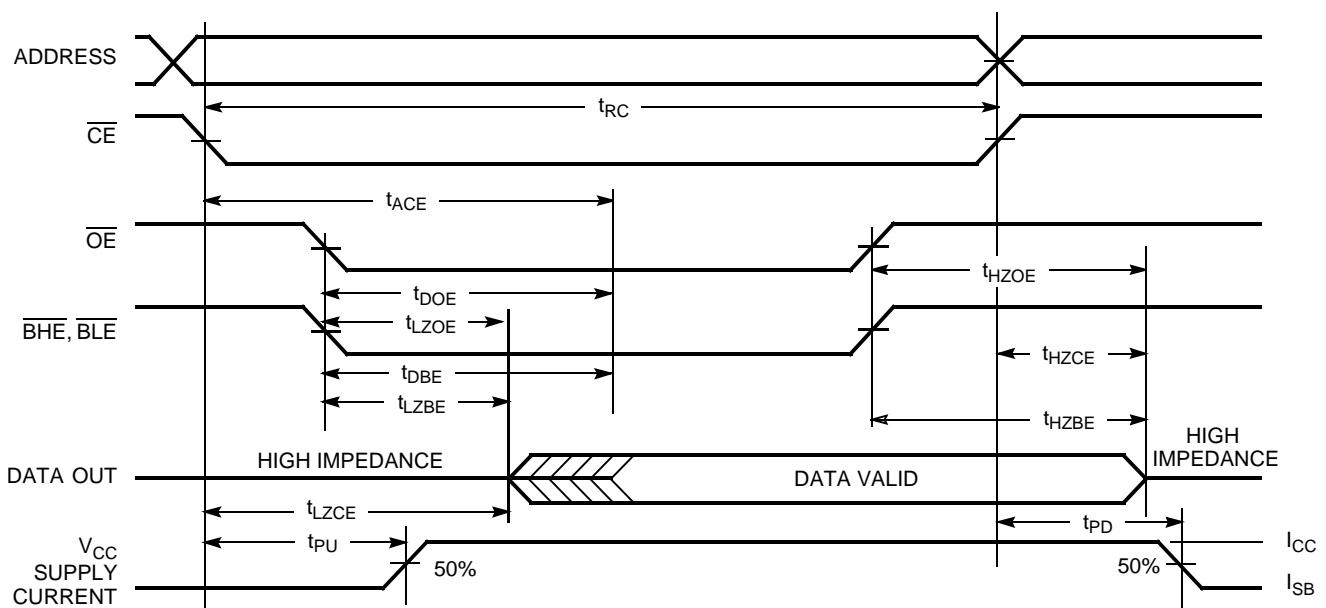


**Switching Waveforms**

**Read Cycle No. 1 (Address Transition Controlled)<sup>[12, 13]</sup>**



**Read Cycle No. 2 ( $\overline{OE}$  Controlled)<sup>[13, 14]</sup>**

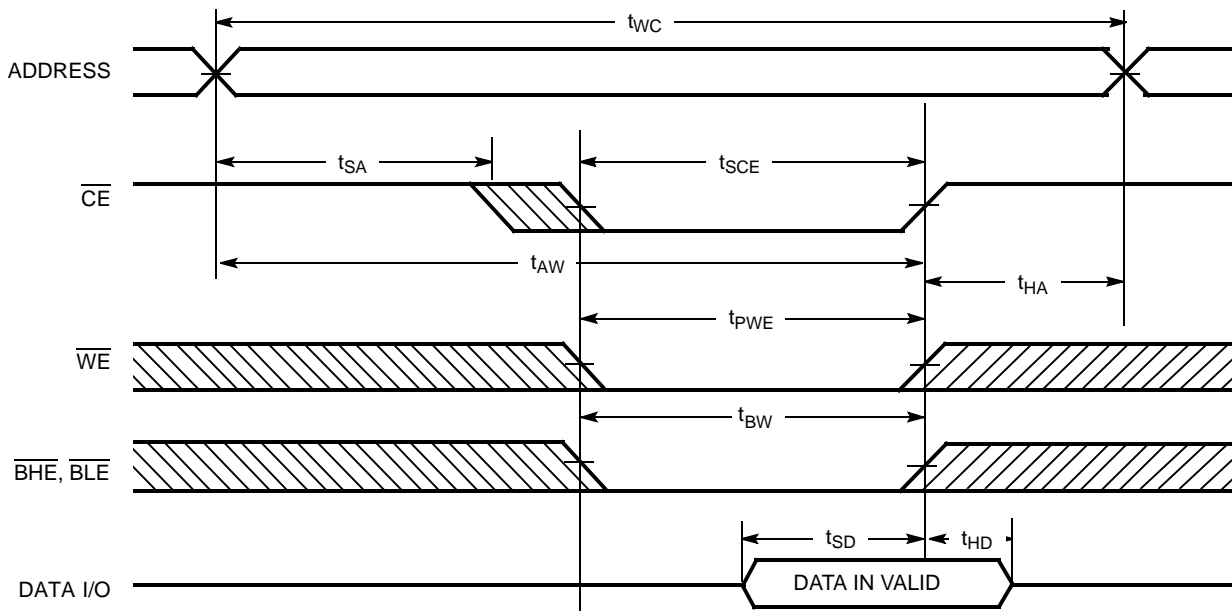


**Notes**

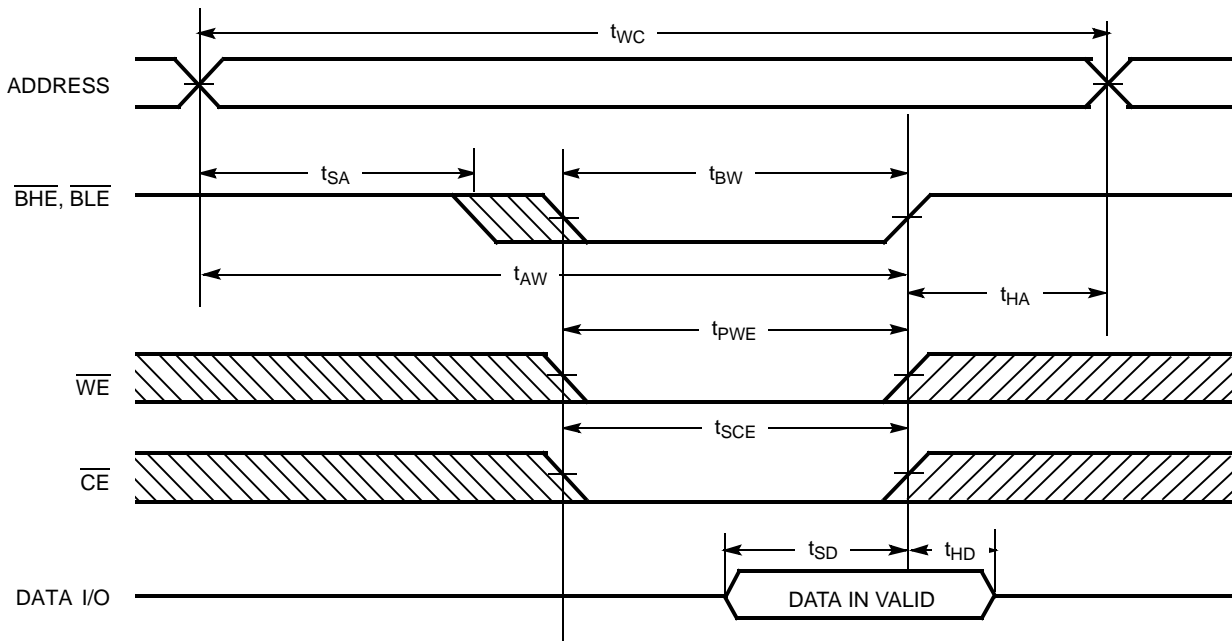
- 11. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min.)} \geq 50\ \mu\text{s}$  or stable at  $V_{CC(min.)} \geq 50\ \mu\text{s}$ .
- 12. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$ ,  $\overline{BHE}$  and/or  $\overline{BLE} = V_L$ .
- 13.  $\overline{WE}$  is HIGH for Read cycle.
- 14. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

**Switching Waveforms** (continued)

**Write Cycle No. 1 ( $\overline{\text{CE}}$  Controlled)<sup>[15, 16]</sup>**



**Write Cycle No. 2 ( $\overline{\text{BLE}}$  or  $\overline{\text{BHE}}$  Controlled)**

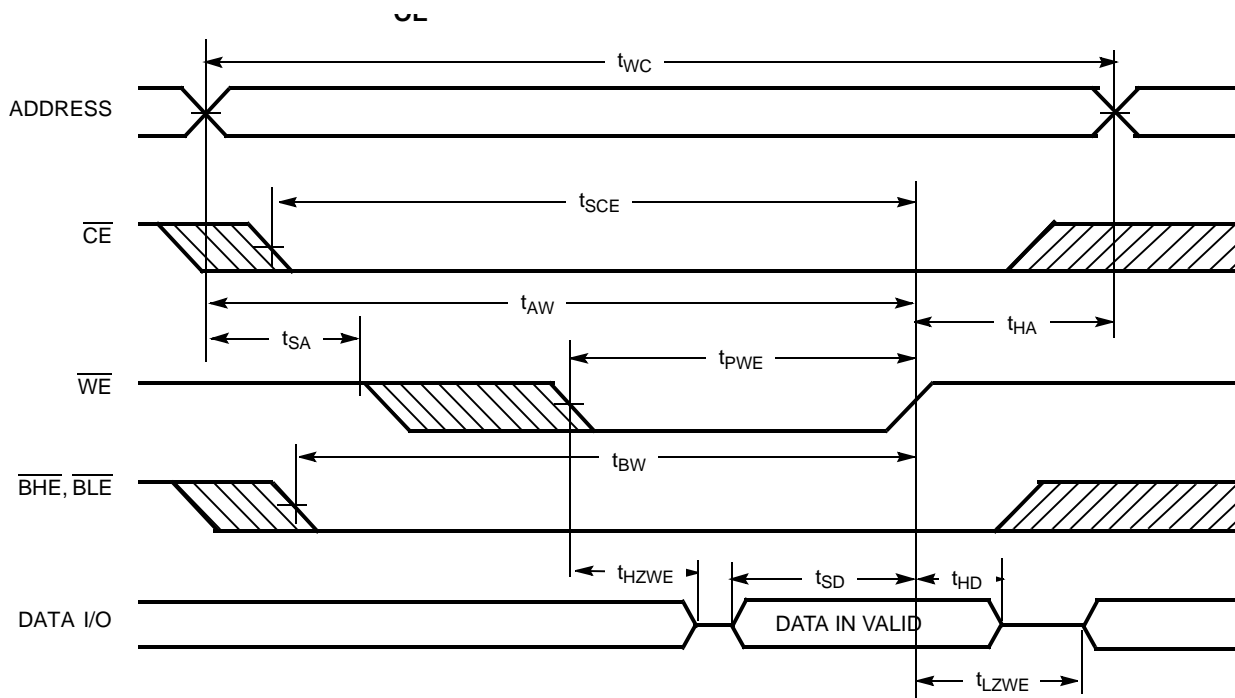


**Notes**

- 15. Data I/O is high impedance if  $\overline{\text{OE}}$  or  $\overline{\text{BHE}}$  and/or  $\overline{\text{BLE}} = V_{IH}$ .
- 16. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  going HIGH, the output remains in a high-impedance state.

**Switching Waveforms** (continued)

**Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)**



**Truth Table**

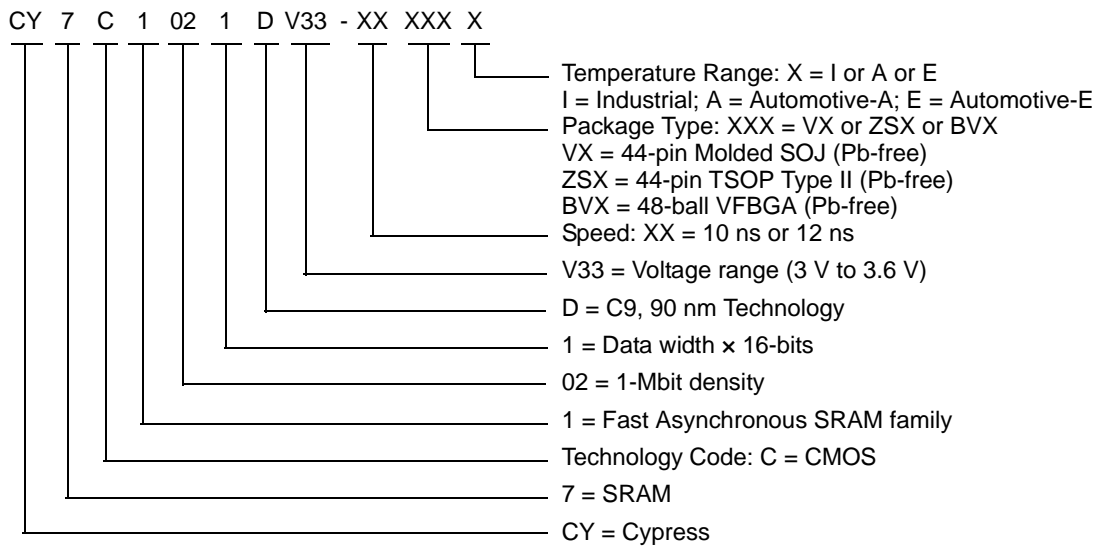
$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	I/O <sub>0</sub> -I/O <sub>7</sub>	I/O <sub>8</sub> -I/O <sub>15</sub>	Mode	Power
H	X	X	X	X	High-Z	High-Z	Power-down	Standby ( $I_{SB}$ )
L	L	H	L	L	Data Out	Data Out	Read – All bits	Active ( $I_{CC}$ )
			L	H	Data Out	High-Z	Read – Lower bits only	Active ( $I_{CC}$ )
			H	L	High-Z	Data Out	Read – Upper bits only	Active ( $I_{CC}$ )
L	X	L	L	L	Data In	Data In	Write – All bits	Active ( $I_{CC}$ )
			L	H	Data In	High-Z	Write – Lower bits only	Active ( $I_{CC}$ )
			H	L	High-Z	Data In	Write – Upper bits only	Active ( $I_{CC}$ )
L	H	H	X	X	High-Z	High-Z	Selected, outputs disabled	Active ( $I_{CC}$ )
L	X	X	H	H	High-Z	High-Z	Selected, outputs disabled	Active ( $I_{CC}$ )



**Ordering Information**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C1021DV33-10VXI	51-85082	44-pin (400-Mil) Molded SOJ (Pb-free)	Industrial
	CY7C1021DV33-10ZSXI	51-85087	44-pin TSOP Type II (Pb-free)	
	CY7C1021DV33-10BVXI	51-85150	48-ball VFBGA (Pb-free)	
10	CY7C1021DV33-10ZSXA	51-85087	44-pin TSOP Type II (Pb-free)	Automotive-A

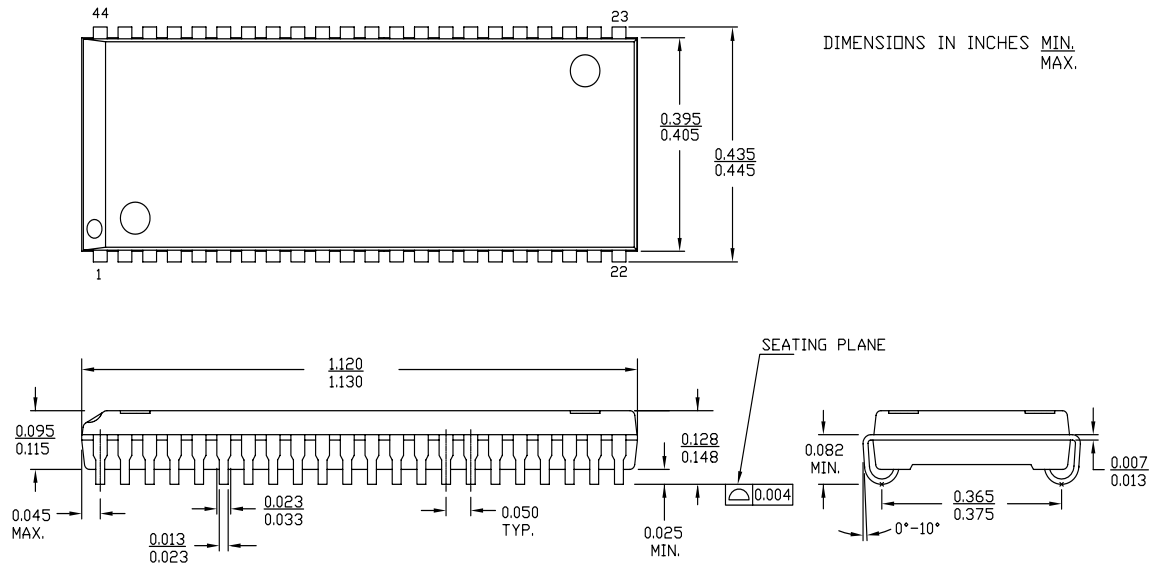
**Ordering Code Definitions**



Please contact your local Cypress sales representative for availability of these parts.

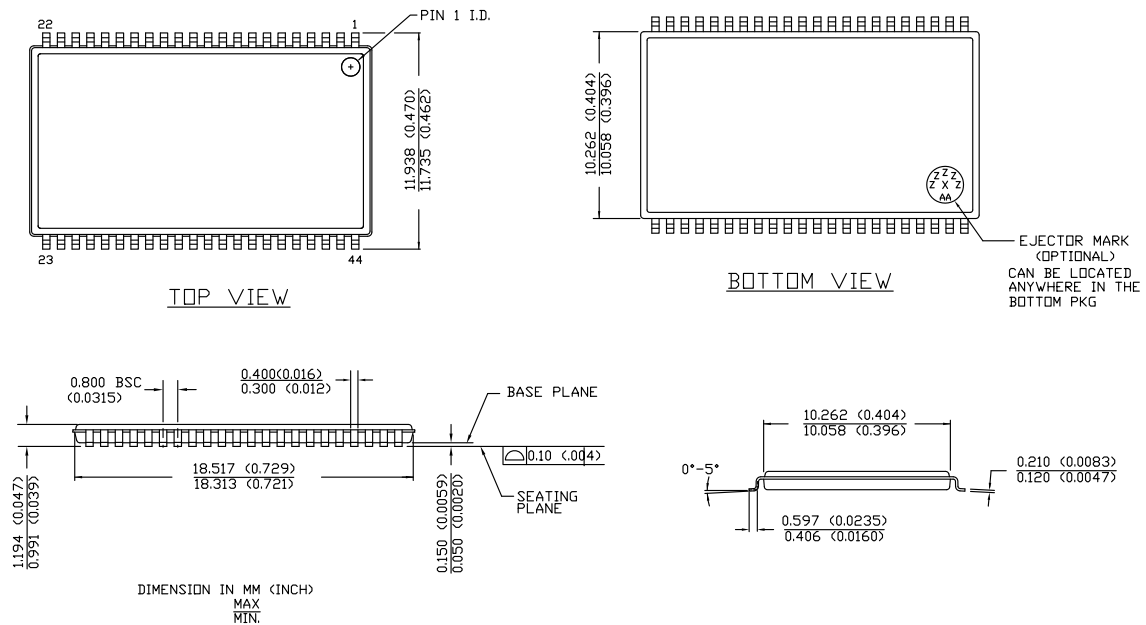
### Package Diagrams

Figure 1. 44-pin (400-Mil) Molded SOJ (51-85082)



51-85082 \*D

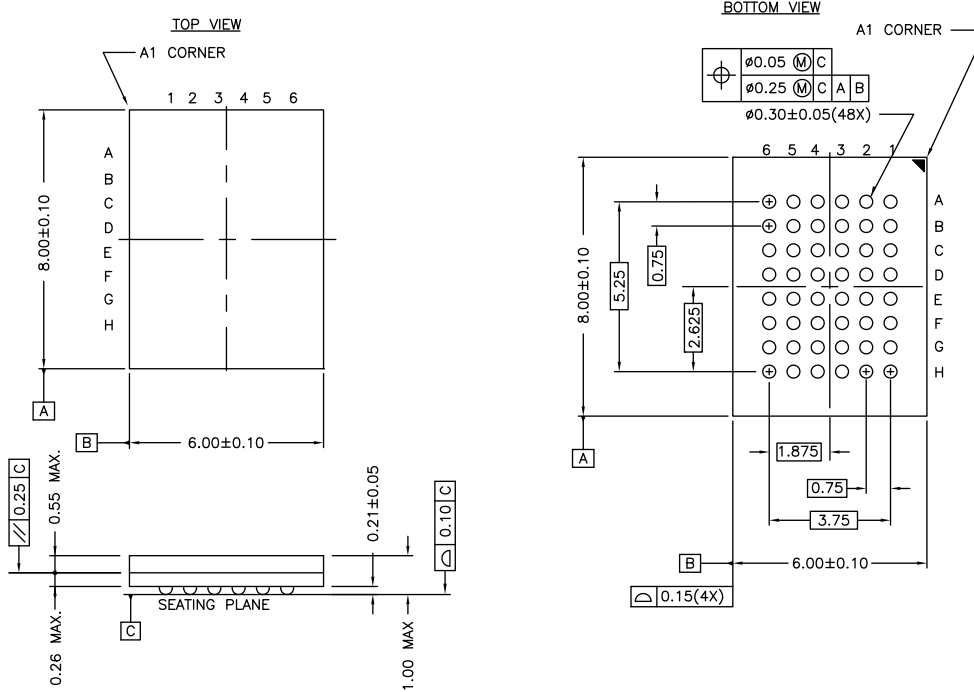
Figure 2. 44-pin Thin Small Outline Package Type II (51-85087)



51-85087 \*D

Package Diagrams (continued)

Figure 3. 48-ball VFBGA (6 x 8 x 1 mm) (51-85150)



51-85150 \*G

Document History Page

Document Title: CY7C1021DV33, 1-Mbit (64K x 16) Static RAM				
Document Number: 38-05460				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	201560	See ECN	SWI	Advance Information data sheet for C9 IPP
*A	233693	See ECN	RKF	DC parameters are modified as per Eros (Spec # 01-02165). Pb-free Offering In Ordering Information
*B	263769	See ECN	RKF	Changed I/O <sub>1</sub> – I/O <sub>16</sub> to I/O <sub>0</sub> – I/O <sub>15</sub> Added Data Retention Characteristics table Added T <sub>power</sub> Spec in Switching Characteristics table Shaded Ordering Information
*C	307601	See ECN	RKF	Reduced Speed bins to –8 and –10 ns
*D	520652	See ECN	VKN	Converted from Preliminary to Final Removed Commercial Operating range Removed 8 ns speed bin Added I <sub>CC</sub> values for the frequencies 83MHz, 66MHz and 40MHz Added Automotive Information Updated Thermal Resistance table Updated Ordering Information Table Changed Overshoot spec from V <sub>CC</sub> +2 V to V <sub>CC</sub> +1 V in footnote #4
*E	2898399	03/24/2010	AJU	Updated Package Diagrams
*F	3109897	12/14/2010	AJU	Added <a href="#">Ordering Code Definitions</a> . Updated <a href="#">Package Diagrams</a> .
*G	3421856	10/25/2011	TAVA	Template Update Updated <a href="#">Features, Selection Guide, Operating Range, DC Electrical Characteristics Over the Operating Range, Switching Characteristics Over the Operating Range<sup>[5]</sup>, Data Retention Characteristics Over the Operating Range, Switching Waveforms, and Ordering Information</a> Updated <a href="#">Package Diagrams</a>

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