

# Model 334C

## Advanced PLL HCMOS VCXO



Part Dimensions:  
3.2 × 2.5 × 1.1mm • 24mg

### Features

- Ceramic Surface Mount Package
- Low Phase Jitter Performance, 600fs Typical
- Advanced PLL Design w/ Low Fundamental Crystal
- Frequency Range 10 – 250MHz \*
- +2.5V or +3.3V Operation
- Output Enable Standard
- Tape and Reel Packaging, EIA-418

### Applications

- Broadcast Video Systems
- Storage Area Networking
- Broadband Access
- Phase-Locked Loop
- Networking Equipment
- Ethernet/GbE/SyncE
- Fiber Channel
- Test and Measurement

#### Standard Frequencies

- 50.00MHz
- 77.76MHz
- 100.00MHz
- 122.88MHz
- 125.00MHz
- 155.52MHz
- 156.25MHz
- 200.00MHz

\* See Page 7 for additional developed frequencies.  
Check with factory for availability of frequencies not listed.

### Description

CTS Model 334C is a low cost, high performance PLL voltage controlled oscillator supporting HCMOS output. Employing the latest IC technology, M334C has excellent stability and low phase jitter performance.

### Ordering Information

Model	Output Type	Frequency Code [MHz]	Absolute Pull Range	Frequency Stability	Temperature Range	Supply Voltage	Packaging
334	C	XXX or XXXX	B	3	I	3	T
	Code    Output C       HCMOS		Code    APR B       ±50ppm		Code    Temp. Range C       -20°C to +70°C I       -40°C to +85°C		Code    Packing T       1k pcs./reel
		Code    Frequency Product Frequency Code <sup>1</sup>		Code    Stability 5       ±25ppm <sup>2</sup> 4       ±30ppm 3       ±50ppm		Code    Voltage 2       +2.5Vdc 3       +3.3Vdc	

Notes:

- 1] Refer to document 016-1454-0, Frequency Code Tables.  
3-digits for frequencies <100MHz, 4-digits for frequencies 100MHz or greater.
- 2] Check factory availability when paired with "I" temperature code.

**Not all performance combinations and frequencies may be available.  
Contact your local CTS Representative or CTS Customer Service for availability.**

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## Electrical Specifications

### Operating Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Maximum Supply Voltage	$V_{CC}$	-	-0.5	-	4.0	V
Maximum Control Voltage	$V_C$	$V_{CC} = +2.5V$	-0.5	-	3.0	V
		$V_{CC} = +3.3V$	-0.5	-	3.8	V
Supply Voltage	$V_{CC}$	$\pm 5\%$	2.375	2.5	2.625	V
			3.135	3.3	3.465	
Supply Current	$I_{CC}$	Maximum Load	-	20	65	mA
Operating Temperature	$T_A$	-	-20	+25	+70	°C
			-40	-	+85	
Storage Temperature	$T_{STG}$	-	-55	-	+125	°C

### Frequency Stability

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Frequency Range	$f_O$	-		10 - 250		MHz
Frequency Stability [Note 1]	$\Delta f/f_O$	-		25, 30 or 50		±ppm
Absolute Pull Range [Note 2]	APR	-	50	-	-	±ppm
Aging	$\Delta f/f_{25}$	First Year @ +25°C, nominal $V_{CC}$	-3	-	3	ppm

1.] Inclusive of initial tolerance at time of shipment, changes in supply voltage, load, temperature and 1st year aging.

2.] Minimum guaranteed frequency shift from  $f_O$  over variations in temperature, aging, power supply and load.

### Output Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Output Type	-	-		HCMOS		-
Output Load	$C_L$	-	-	-	15	pF
Output Voltage Levels	$V_{OH}$	CMOS Load	$0.9V_{CC}$	-	-	V
	$V_{OL}$		-	-	$0.1V_{CC}$	
Output Duty Cycle	SYM	@ 50% Level	45	-	55	%
Rise and Fall Time	$T_R, T_F$	@ 20%/80% Levels, $C_L = 15pF$	-	5	10	ns
Start Up Time	$T_S$	Application of $V_{CC}$	-	3	5	ms
<b>Enable Function [Tri-State]</b>						
Enable Input Voltage	$V_{IH}$	Pin 2 Logic '1', Output Enabled	$0.7V_{CC}$	-	-	V
Disable Input Voltage	$V_{IL}$	Pin 2 Logic '0', Output Disabled	-	-	$0.3V_{CC}$	V
Disable Current	$I_{IL}$	Pin 2 Logic '0', Output Disabled	-	16	22	mA
Enable Time	$T_{PLZ}$	Pin 2 Logic '1', Output Enabled	-	-	200	ns
Phase Jitter, RMS	$t_{jrms}$	Bandwidth 12 kHz - 20 MHz	-	600	<1000	fs
Period Jitter, RMS	$p_{jrms}$	-	-	3.0	-	ps
Period Jitter, pk-pk	$p_{jpk-pk}$	-	-	30	-	ps

## Electrical Specifications

### Control Voltage

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Control Voltage	$V_C$	$V_{CC} = 2.5V$	0.2	1.25	2.3	V
		$V_{CC} = 3.3V$	0.3	1.65	3.0	
Frequency Deviation	$\Delta f/f_0$	$V_C = 0.2V$		-60 to -180		ppm
		$V_C = 2.3V$		60 to 180		
		$V_C = 0.3V$		-60 to -180		ppm
		$V_C = 3.0V$		60 to 180		
Linearity	L	Best Straight Line Fit	-	-	±15	%
Gain Transfer	$K_V$	Pull Sensitivity; @ +1.25V, +25°C Pull Sensitivity; @ +1.65V, +25°C	-	80	260	ppm/V
Input Impedance	$Z_{Vc}$	-	1	-	-	MOhms
Modulation Roll-off	-	@ -3dB	10	-	-	kHz
Transfer Function	-	-		Positive		-

### Enable Truth Table

Pin 2	Pin 4
Logic '1'	Output
Open	Output
Logic '0'	High Imp.

### Test Circuit

HCMOS



### Output Waveform

HCMOS





## Electrical Specifications

### Performance Data

#### Phase Noise [typical]

125MHz, HCMOS,  $V_{CC} = +3.3V$ ,  $V_C = +1.65V$ ,  $T_A = +25^\circ C$



#### Phase Noise Tabulated

125MHz, HCMOS,  $V_{CC} = +3.3V$ ,  $V_C = +1.65V$ ,  $T_A = +25^\circ C$

PARAMETER	SYMBOL	CONDITIONS	TYP	UNIT
<b>HCMOS @ 125.00MHz</b>				
Phase Noise		Single Side Band		
		@ 10Hz	-57.8277	
		@ 100Hz	-83.0438	
		@ 1kHz	-107.5582	
		@ 10kHz	-124.0745	dBc/Hz
		@ 100kHz	-127.7532	
		@ 1MHz	-139.0681	
		@ 10MHz	-156.3500	
	@ 20MHz	-157.3626		
Phase Jitter, RMS	tjrms	Integration Bandwidth 12kHz - 20MHz	530.5330	fs

## Mechanical Specifications

### Package Drawing



### Marking Information

1. O – Output Type; C = HCMOS.
  2. ST – Frequency Stability/Temperature Code. [Refer to Ordering Information]
  3. V – Voltage Code; 3 = 3.3V, 2 = 2.5V.
  4. D – Date Code. See Table I for codes.
  5. xxxx – Frequency Code.  
3-digits, frequencies below 100MHz  
4-digits, frequencies 100MHz or greater
- [See document 016-1454-0, Frequency Code Tables.]

### Recommended Pad Layout



### Notes

1. JEDEC termination code (e4). Barrier-plating is nickel [Ni] with gold [Au] flash plate.
2. Reflow conditions per JEDEC J-STD-020; +260°C maximum, 20 seconds.
3. MSL = 1.

### Pin Assignments

Pin	Symbol	Function
1	V <sub>C</sub>	Voltage Control
2	EOH	Enable [tri-state]
3	GND	Circuit & Package Ground
4	Output	RF Output
5	N.C.	No Connect
6	V <sub>CC</sub>	Supply Voltage

Table I - Date Code

YEAR		MONTH														
		JAN	FEB	MAR	APR	MAY	JUN	JUL	AUG	SEP	OCT	NOV	DEC			
2001	2005	2009	2013	2017	A	B	C	D	E	F	G	H	J	K	L	M
2002	2006	2010	2014	2018	N	P	Q	R	S	T	U	V	W	X	Y	Z
2003	2007	2011	2015	2019	a	b	c	d	e	f	g	h	j	k	l	m
2004	2008	2012	2016	2020	n	p	q	r	s	t	u	v	w	x	y	z





## Addendum

### Additional Developed Frequencies – MHz

FREQUENCY	FREQUENCY CODE	FREQUENCY	FREQUENCY CODE	FREQUENCY	FREQUENCY CODE	FREQUENCY	FREQUENCY CODE
25.000000	250	150.000000	1500				
62.500000	625	153.600000	1536				
106.250000	1062	250.000000	2500				
132.000000	1320						
148.500000	1485						

### Frequency Codes for Cover Page Table – MHz

FREQUENCY	FREQUENCY CODE	FREQUENCY	FREQUENCY CODE
50.000000	500	155.520000	1555
77.760000	777	156.250000	1562
100.000000	1000	200.000000	2000
122.880000	1228		
125.000000	1250		



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