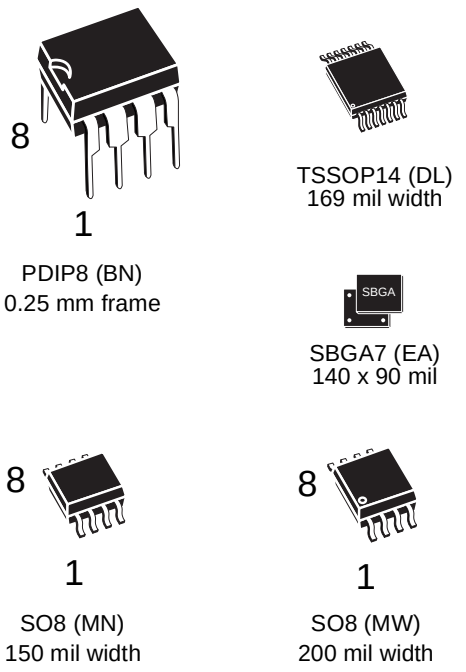
M24256-A

256 Kbit Serial I²C Bus EEPROM With Two Chip Enable Lines

NOT FOR NEW DESIGN

This device is now designated as "Not for New Design". Please use the M24256-B in all future designs (as described in application note AN1470).

- Compatible with I²C Extended Addressing
- Two Wire I²C Serial Interface
  Supports 400 kHz Protocol
- Single Supply Voltage:
  - 4.5V to 5.5V for M24256-A
  - 2.5V to 5.5V for M24256-AW
- 2 Chip Enable Inputs: up to four memories can be connected to the same I²C bus
- Hardware Write Control
- BYTE and PAGE WRITE (up to 64 Bytes)
- RANDOM and SEQUENTIAL READ Modes
- Self-Timed Programming Cycle
- Automatic Address Incrementing
- Enhanced ESD/Latch-Up Behavior
- More than 100,000 Erase/Write Cycles
- More than 40 Year Data Retention



DESCRIPTION

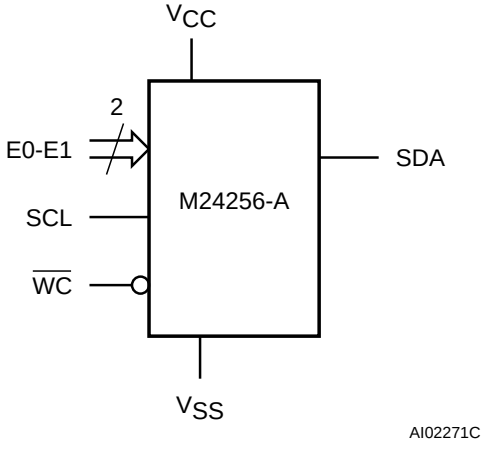
These I²C-compatible electrically erasable programmable memory (EEPROM) devices are organized as 32Kx8 bits, and operate down to 2.5 V (for the M24256-AW).

The M24256-A is available in Plastic Dual-in-Line, Plastic Small Outline and Thin Shrink Small Out-

Table 1. Signal Names

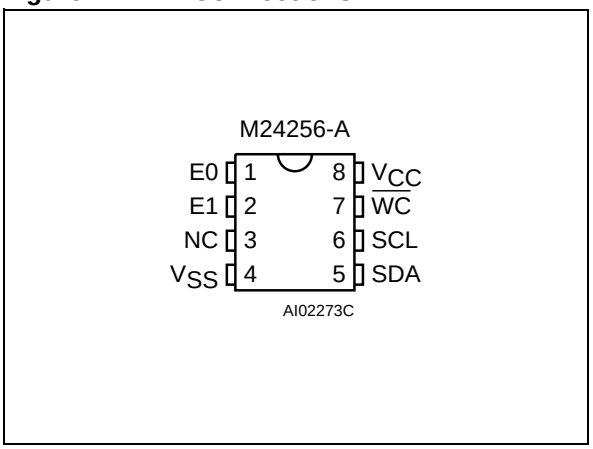
E0, E1	Chip Enable
SDA	Serial Data
SCL	Serial Clock
$\overline{WC}$	Write Control
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram



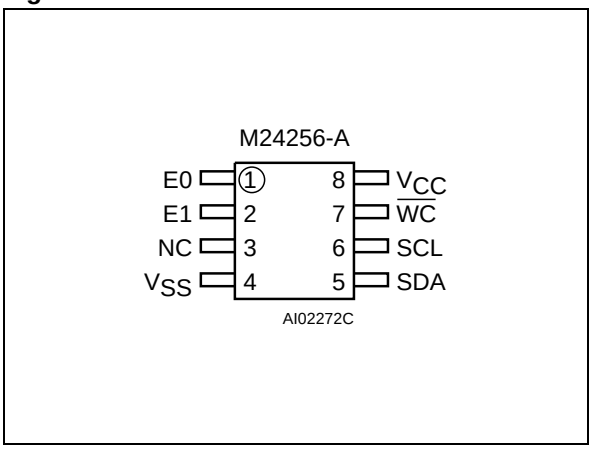
This is information on a product still in production but not recommended for new designs.

Figure 2A. DIP Connections



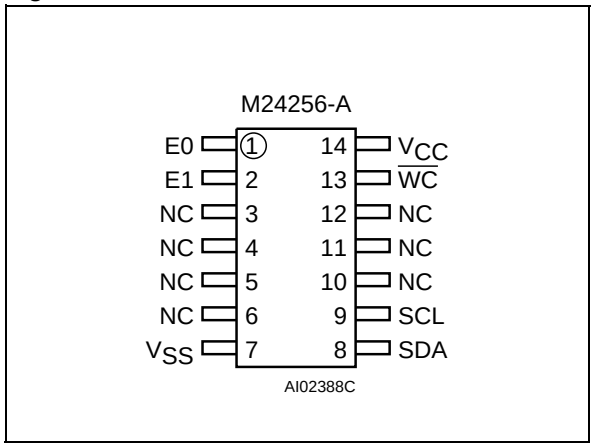
Note: 1. NC = Not Connected

Figure 2B. SO Connections



Note: 1. NC = Not Connected

Figure 2C. TSSOP Connections



Note: 1. NC = Not Connected

Figure 2D. SBGA Connections (top view)

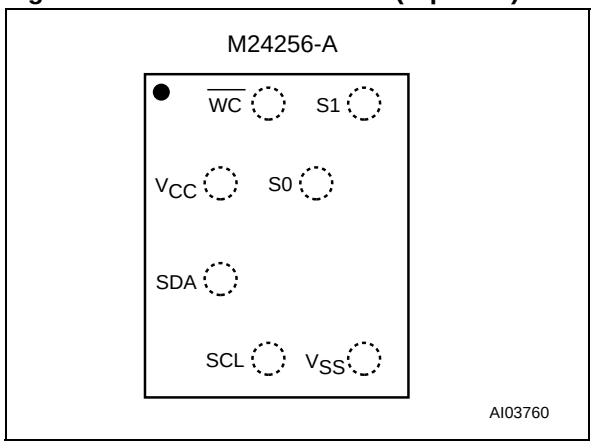


Table 2. Absolute Maximum Ratings [1]

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature		–40 to 125	°C
T_{STG}	Storage Temperature		–65 to 150	°C
T_{LEAD}	Lead Temperature during Soldering	PDIP: 10 seconds SO: 20 seconds (max) [2] TSSOP: 20 seconds (max) [2]	260 235 235	°C
V_{IO}	Input or Output range		–0.6 to 6.5	V
V_{CC}	Supply Voltage		–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) [3]		4000	V
	Electrostatic Discharge Voltage (Machine model) [4]		200	V

Note: 1. Except for the rating “Operating Temperature Range”, stresses above those listed in the Table “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the ST SURE Program and other relevant quality documents.
2. IPC/JEDEC J-STD-020A
3. JEDEC Std JESD22-A114A (C1=100 pF, R1=1500 Ω, R2=500 Ω)
4. EIAJ IC-121 (Condition C) (200 pF, 0 Ω)

line packages. The M24256-A is also available in a chip-scale (SBGA) package.

These memory devices are compatible with the I^2C extended memory standard. This is a two wire serial interface that uses a bi-directional data bus and serial clock. The memory carries a built-in 4-bit unique Device Type Identifier code (1010) in accordance with the I^2C bus definition.

The memory behaves as a slave device in the I^2C protocol, with all memory operations synchronized by the serial clock. Read and Write operations are initiated by a START condition, generated by the bus master. The START condition is followed by a Device Select Code and $\overline{RW}$ bit (as described in Table 3), terminated by an acknowledge bit.

When writing data to the memory, the memory inserts an acknowledge bit during the 9^{th} bit time, following the bus master's 8-bit transmission. When data is read by the bus master, the bus master acknowledges the receipt of the data byte in the same way. Data transfers are terminated by a STOP condition after an Ack for WRITE, and after a NoAck for READ.

Power On Reset: V_{CC} Lock-Out Write Protect

In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is included. The internal reset is held active until the V_{CC} voltage has reached the POR threshold value, and all operations are disabled – the device will not respond to any command. In the same way, when V_{CC} drops from the operating voltage, below the POR threshold value, all operations are disabled and the device will not respond to any command. A stable and valid V_{CC} must be applied before applying any logic signal.

SIGNAL DESCRIPTION

Serial Clock (SCL)

The SCL input pin is used to strobe all data in and out of the memory. In applications where this line is used by slaves to synchronize the bus to a slower clock, the master must have an open drain output, and a pull-up resistor must be connected from the SCL line to V_{CC}. (Figure 3 indicates how the value of the pull-up resistor can be calculated). In most applications, though, this method of synchronization is not employed, and so the pull-up resistor is not necessary, provided that the master has a push-pull (rather than open drain) output.

Serial Data (SDA)

The SDA pin is bi-directional, and is used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A pull up resistor must be connected from the SDA bus to V_{CC}. (Figure 3 indicates how the value of the pull-up resistor can be calculated).

Chip Enable (E1, E0)

These chip enable inputs are used to set the value that is to be looked for on the two least significant bits (b2, b1) of the 7-bit device select code. These inputs must be tied to V_{CC} or V_{SS} to establish the device select code. When unconnected, the E1 and E0 inputs are internally read as V_{IL} (see Table 7 and Table 8)

Write Control ($\overline{WC}$)

The hardware Write Control pin ($\overline{WC}$) is useful for protecting the entire contents of the memory from inadvertent erase/write. The Write Control signal is used to enable ($\overline{WC}$=V_{IL}) or disable ($\overline{WC}$=V_{IH}) write instructions to the entire memory area. When

Figure 3. Maximum R_L Value versus Bus Capacitance (C_{BUS}) for an I^2C Bus

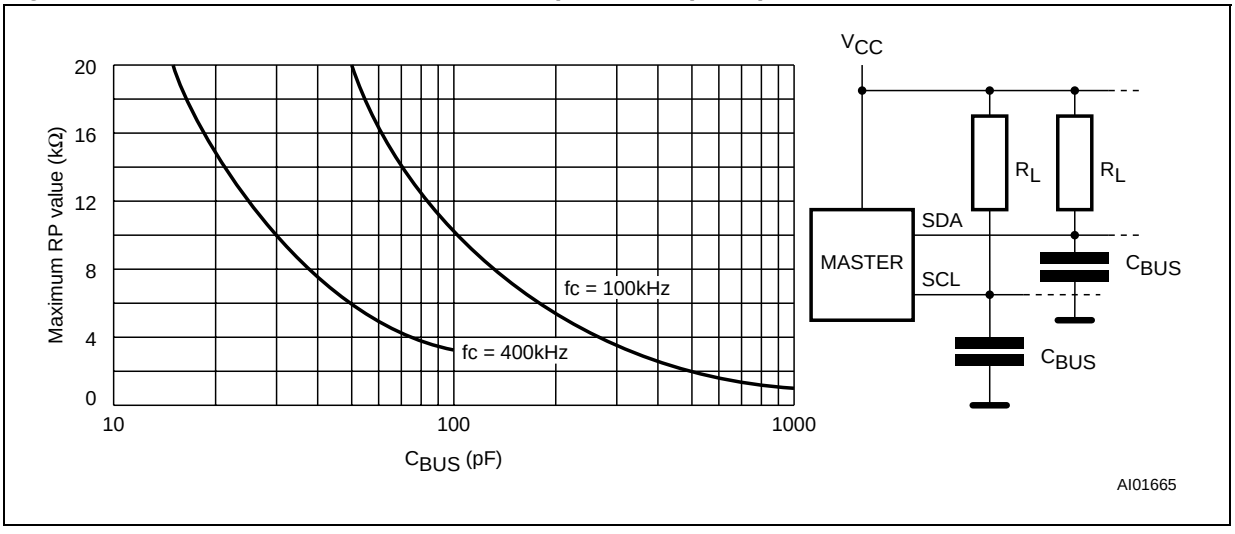
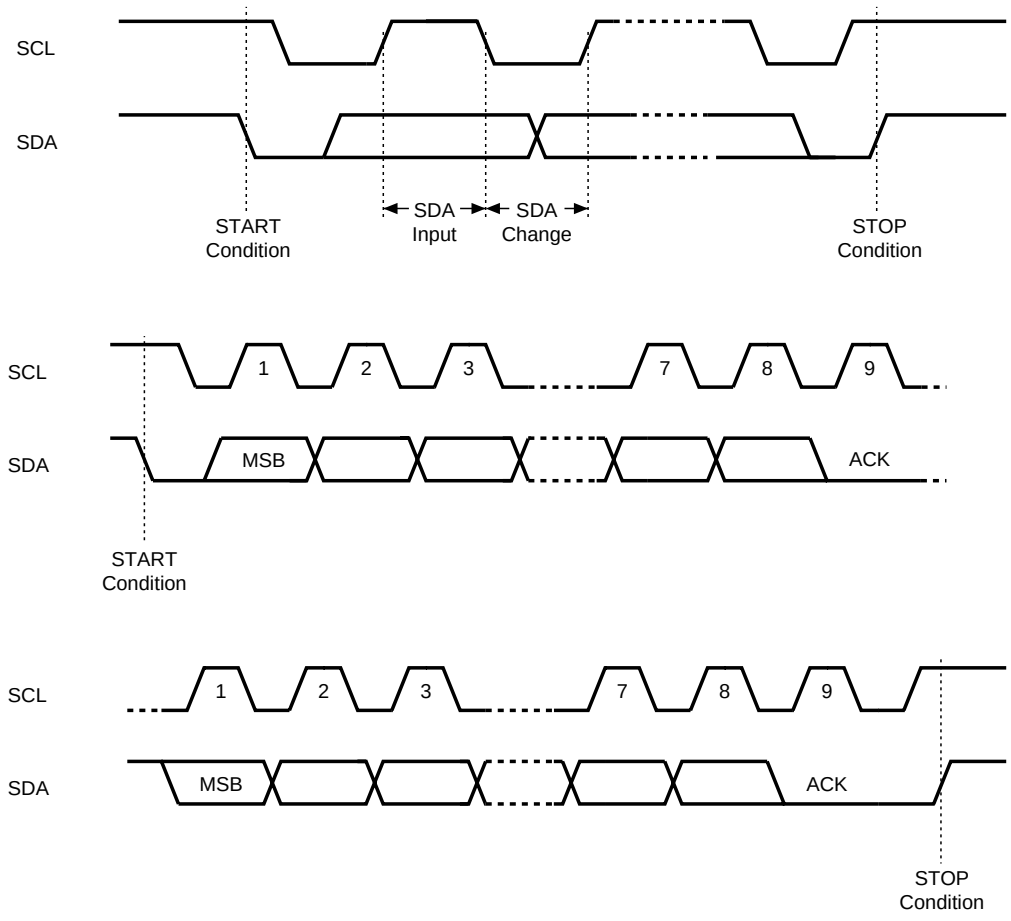


Figure 4. I²C Bus Protocol



unconnected, the $\overline{WC}$ input is internally read as V_{IL}, and write operations are allowed.

When $\overline{WC}$=1, Device Select and Address bytes are acknowledged, Data bytes are not acknowledged.

Please see the Application Note *AN404* for a more detailed description of the Write Control feature.

DEVICE OPERATION

The memory device supports the I²C protocol. This is summarized in Figure 4, and is compared with other serial bus protocols in Application Note *AN1001*. Any device that sends data on to the bus is defined to be a transmitter, and any device that reads the data to be a receiver. The device that controls the data transfer is known as the master, and the other as the slave. A data transfer can only be initiated by the master, which will also provide the serial clock for synchronization. The memory device is always a slave device in all communication.

Start Condition

START is identified by a high to low transition of the SDA line while the clock, SCL, is stable in the high state. A START condition must precede any data transfer command. The memory device continuously monitors (except during a programming cycle) the SDA and SCL lines for a START condition, and will not respond unless one is given.

Stop Condition

STOP is identified by a low to high transition of the SDA line while the clock SCL is stable in the high state. A STOP condition terminates communication between the memory device and the bus master. A STOP condition at the end of a Read command, after (and only after) a NoAck, forces the memory device into its standby state. A STOP condition at the end of a Write command triggers the internal EEPROM write cycle.

Table 3. Device Select Code [1]

	Device Type Identifier				Chip Enable			RW
	b7	b6	b5	b4	b3	b2	b1	b0
Device Select Code	1	0	1	0	0	E1	E0	RW

Note: 1. The most significant bit, b7, is sent first.

Acknowledge Bit (ACK)

An acknowledge signal is used to indicate a successful byte transfer. The bus transmitter, whether it be master or slave, releases the SDA bus after sending eight bits of data. During the 9th clock pulse period, the receiver pulls the SDA bus low to acknowledge the receipt of the eight data bits.

Data Input

During data input, the memory device samples the SDA bus signal on the rising edge of the clock, SCL. For correct device operation, the SDA signal must be stable during the clock low-to-high transition, and the data must change *only* when the SCL line is low.

Memory Addressing

To start communication between the bus master and the slave memory, the master must initiate a START condition. Following this, the master sends the 8-bit byte, shown in Table 3, on the SDA bus line (most significant bit first). This consists of the 7-bit Device Select Code, and the 1-bit Read/Write Designator (RW). The Device Select Code is further subdivided into: a 4-bit Device Type Identifier, and a 3-bit Chip Enable "Address" (0, E1, E0).

To address the memory array, the 4-bit Device Type Identifier is 1010b.

Up to four memory devices can be connected on a single I^2C bus. Each one is given a unique 2-bit code on its Chip Enable inputs. When the Device Select Code is received on the SDA bus, the memory only responds if the Chip Select Code is the same as the pattern applied to its Chip Enable pins.

Table 4. Most Significant Byte

b15	b14	b13	b12	b11	b10	b9	b8

Note: 1. b15 is treated as Don't Care on the M24256-A series.

Table 5. Least Significant Byte

b7	b6	b5	b4	b3	b2	b1	b0

The 8th bit is the RW bit. This is set to '1' for read and '0' for write operations. If a match occurs on the Device Select Code, the corresponding memory gives an acknowledgment on the SDA bus during the 9th bit time. If the memory does not match the Device Select Code, it deselects itself from the bus, and goes into stand-by mode.

There are two modes both for read and write. These are summarized in Table 6 and described later. A communication between the master and the slave is ended with a STOP condition.

Each data byte in the memory has a 16-bit (two byte wide) address. The Most Significant Byte (Table 4) is sent first, followed by the Least significant Byte (Table 5). Bits b15 to b0 form the address of the byte in memory. Bit b15 is treated as Don't Care bits on the M24256-A memory.

Write Operations

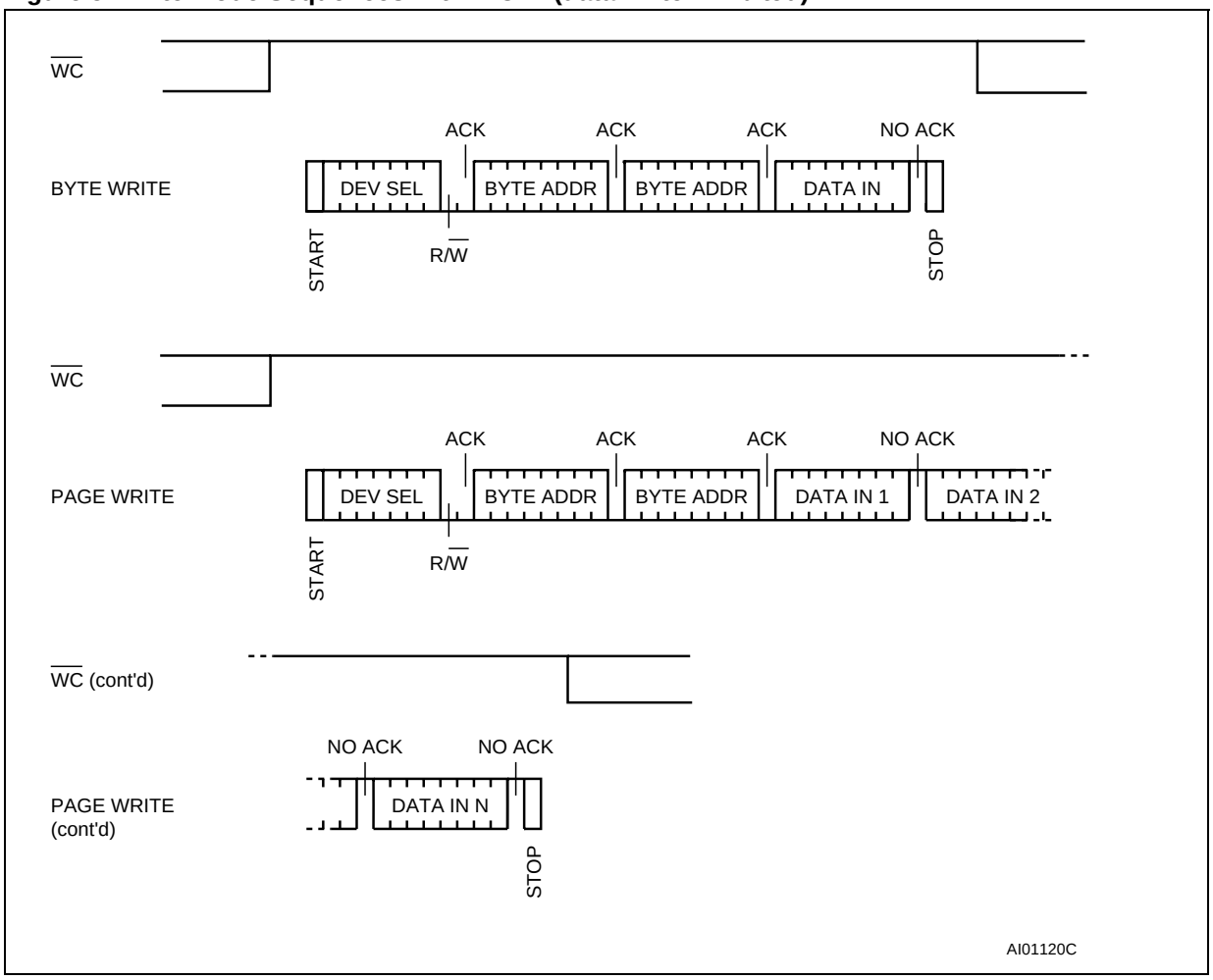
Following a START condition the master sends a Device Select Code with the RW bit set to '0', as shown in Table 6. The memory acknowledges this, and waits for two address bytes. The memory re-

Table 6. Operating Modes

Mode	RW bit	WC [1]	Data Bytes	Initial Sequence
Current Address Read	1	X	1	START, Device Select, RW = 1
Random Address Read	0	X	1	START, Device Select, RW = 0, Address
	1	X		reSTART, Device Select, RW = 1
Sequential Read	1	X	≥ 1	Similar to Current or Random Address Read
Byte Write	0	V_{IL}	1	START, Device Select, RW = 0
Page Write	0	V_{IL}	≤ 64	START, Device Select, RW = 0

Note: 1. X = V_{IH} or V_{IL}.

Figure 5. Write Mode Sequences with $\overline{WC}$=1 (data write inhibited)



sponds to each address byte with an acknowledge bit, and then waits for the data byte.

Writing to the memory may be inhibited if the $\overline{WC}$ input pin is taken high. Any write command with $\overline{WC}$=1 (during a period of time from the START condition until the end of the two address bytes) will not modify the memory contents, and the accompanying data bytes will *not* be acknowledged, as shown in Figure 5.

Byte Write

In the Byte Write mode, after the Device Select Code and the address bytes, the master sends one data byte. If the addressed location is write protected by the $\overline{WC}$ pin, the memory replies with a NoAck, and the location is not modified. If, instead, the $\overline{WC}$ pin has been held at 0, as shown in Figure 6, the memory replies with an Ack. The master terminates the transfer by generating a STOP condition.

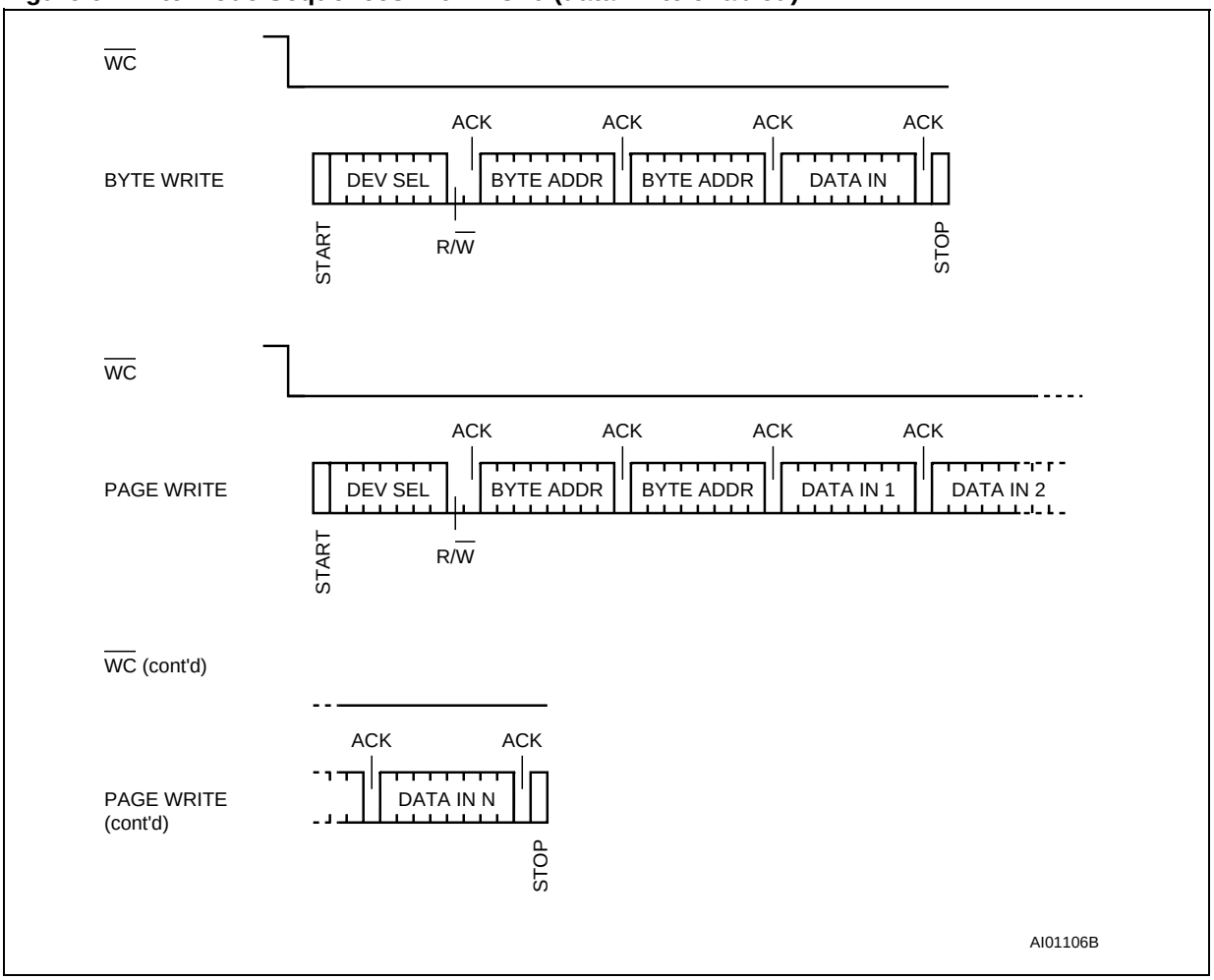
Page Write

The Page Write mode allows up to 64 bytes to be written in a single write cycle, provided that they are all located in the same 'row' in the memory: that is the most significant memory address bits (b14-b6 for the M24256-A) are the same. If more bytes are sent than will fit up to the end of the row, a condition known as 'roll-over' occurs. Data starts to become overwritten (in a way not formally specified in this data sheet).

The master sends from one up to 64 bytes of data, each of which is acknowledged by the memory if the $\overline{WC}$ pin is low. If the $\overline{WC}$ pin is high, the contents of the addressed memory location are not modified, and each data byte is followed by a NoAck. After each byte is transferred, the internal byte address counter (the 6 least significant bits only) is incremented. The transfer is terminated by the master generating a STOP condition.

When the master generates a STOP condition immediately after the Ack bit (in the "10th bit" time

Figure 6. Write Mode Sequences with $\overline{WC}$=0 (data write enabled)



slot), either at the end of a byte write or a page write, the internal memory write cycle is triggered. A STOP condition at any other time does not trigger the internal write cycle.

During the internal write cycle, the SDA input is disabled internally, and the device does not respond to any requests.

Minimizing System Delays by Polling On ACK

During the internal write cycle, the memory disconnects itself from the bus, and copies the data from its internal latches to the memory cells. The maximum write time (t_W) is shown in Table 9, but the typical time is shorter. To make use of this, an Ack polling sequence can be used by the master.

The sequence, as shown in Figure 7, is:

– Initial condition: a Write is in progress.

– Step 1: the master issues a START condition followed by a Device Select Code (the first byte of the new instruction).

– Step 2: if the memory is busy with the internal write cycle, no Ack will be returned and the master goes back to Step 1. If the memory has terminated the internal write cycle, it responds with an Ack, indicating that the memory is ready to receive the second part of the next instruction (the first byte of this instruction having been sent during Step 1).

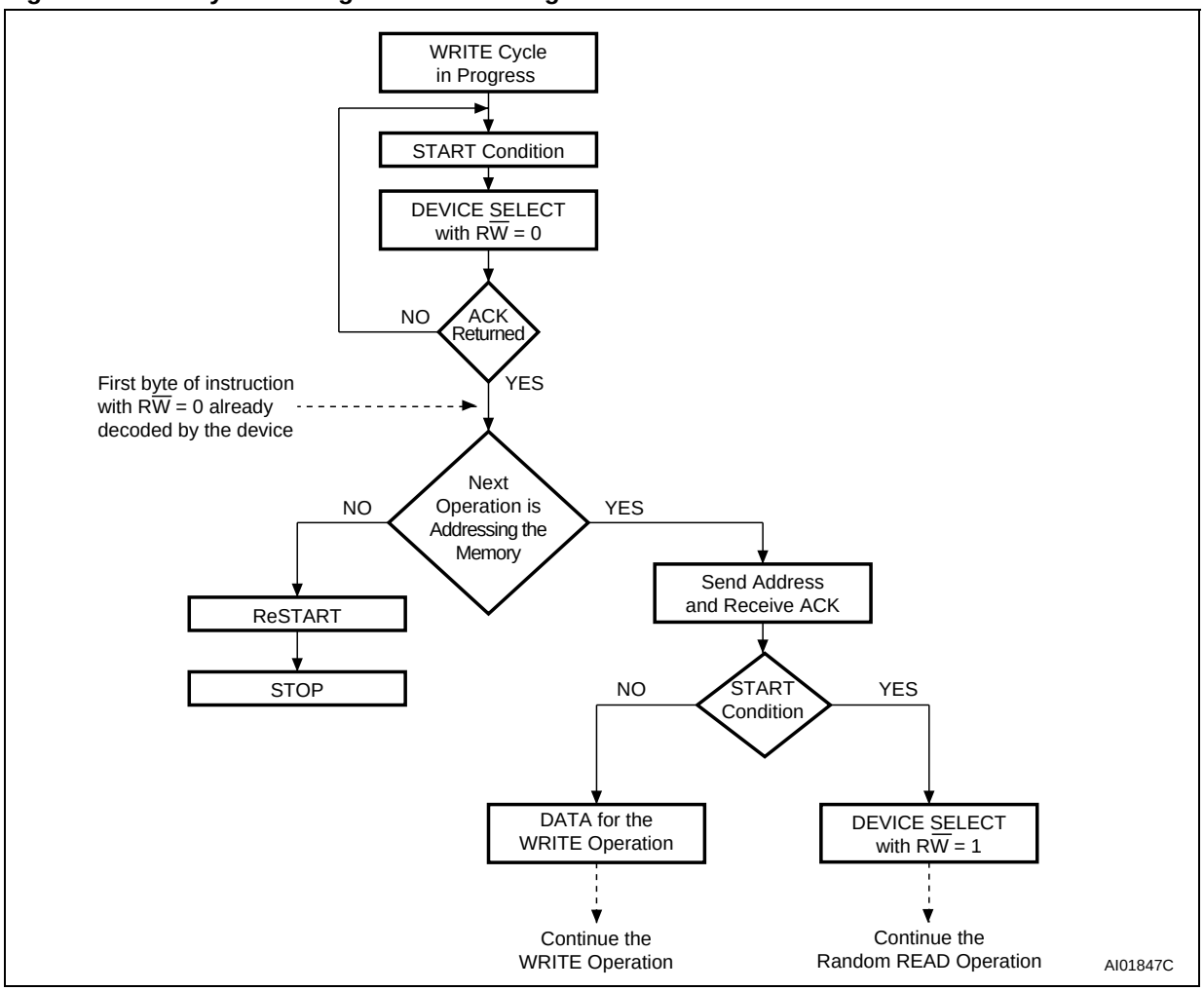
Read Operations

Read operations are performed independently of the state of the $\overline{WC}$ pin.

Random Address Read

A dummy write is performed to load the address into the address counter, as shown in Figure 8. Then, *without* sending a STOP condition, the master sends another START condition, and repeats the Device Select Code, with the $\overline{RW}$ bit set to '1'. The memory acknowledges this, and outputs the contents of the addressed byte. The master must *not* acknowledge the byte output, and terminates the transfer with a STOP condition.

Figure 7. Write Cycle Polling Flowchart using ACK



Current Address Read

The device has an internal address counter which is incremented each time a byte is read. For the Current Address Read mode, following a START condition, the master sends a Device Select Code with the RW bit set to '1'. The memory acknowledges this, and outputs the byte addressed by the internal address counter. The counter is then incremented. The master terminates the transfer with a STOP condition, as shown in Figure 8, *without* acknowledging the byte output.

Sequential Read

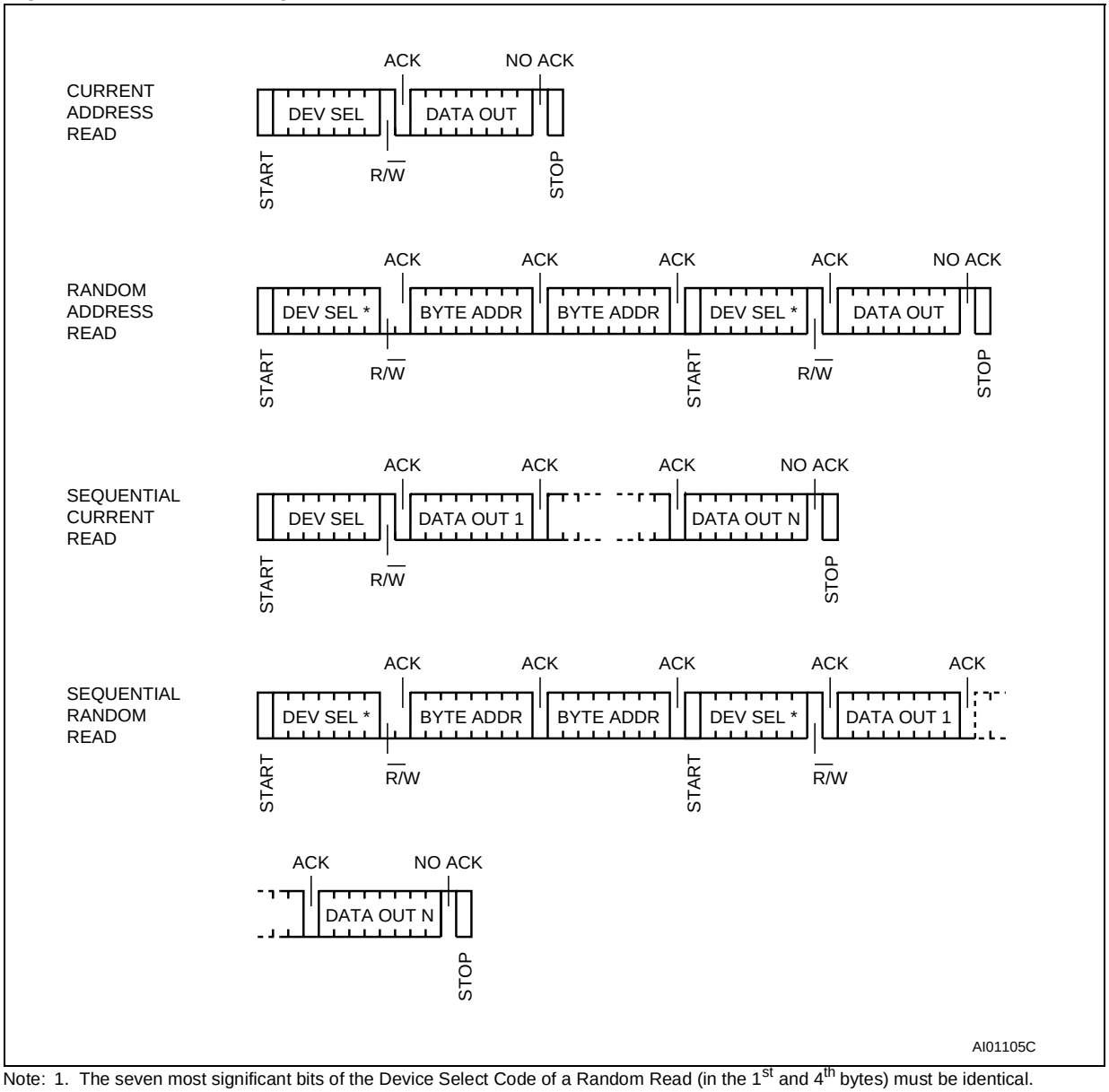
This mode can be initiated with either a Current Address Read or a Random Address Read. The master *does* acknowledge the data byte output in this case, and the memory continues to output the next byte in sequence. To terminate the stream of bytes, the master must *not* acknowledge the last byte output, and *must* generate a STOP condition.

The output data comes from consecutive addresses, with the internal address counter automatically incremented after each byte output. After the last memory address, the address counter 'rolls-over' and the memory continues to output data from memory address 00h.

Acknowledge in Read Mode

In all read modes, the memory waits, after each byte read, for an acknowledgment during the 9th bit time. If the master does not pull the SDA line low during this time, the memory terminates the data transfer and switches to its stand-by state.

Figure 8. Read Mode Sequences



Note: 1. The seven most significant bits of the Device Select Code of a Random Read (in the 1st and 4th bytes) must be identical.

Table 7. DC Characteristics
(T_A = –40 to 85 °C; V_{CC} = 4.5 to 5.5 V or 2.5 to 5.5 V)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
I_{LI}	Input Leakage Current (SCL, SDA)	$V_{IN} = V_{SS}$ or V_{CC}		± 2	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ or V_{CC}, SDA in Hi-Z		± 2	µA
I_{CC}	Supply Current	V_{CC}=5V, f_c=400kHz (rise/fall time < 30ns)		2	mA
	-W series:	V_{CC} =2.5V, f_c=400kHz (rise/fall time < 30ns)		1	mA
I_{CC1}	Supply Current (Stand-by)	$V_{IN} = V_{SS}$ or V_{CC} , V_{CC} = 5 V		10	µA
	-W series:	$V_{IN} = V_{SS}$ or V_{CC} , V_{CC} = 2.5 V		2	µA
V_{IL}	Input Low Voltage (SCL, SDA)		–0.3	$0.3V_{CC}$	V
V_{IH}	Input High Voltage (SCL, SDA)		$0.7V_{CC}$	V_{CC}+1	V
V_{IL}	Input Low Voltage (E0, E1, $\overline{WC}$)		–0.3	0.5	V
V_{IH}	Input High Voltage (E0, E1, $\overline{WC}$)		$0.7V_{CC}$	V_{CC}+1	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA, V_{CC} = 5 V		0.4	V
	-W series:	I_{OL} = 2.1 mA, V_{CC} = 2.5 V		0.4	V

Table 8. Input Parameters[1] (T_A = 25 °C, f = 400 kHz)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF
Z_L	Input Impedance (E1, E0, $\overline{WC}$)	$V_{IN} \leq 0.5$ V	50		kΩ
Z_H	Input Impedance (E1, E0, $\overline{WC}$)	$V_{IN} \geq 0.7V_{CC}$	500		kΩ
t_{NS}	Pulse width ignored (Input Filter on SCL and SDA)	Single glitch		100	ns

Note: 1. Sampled only, not 100% tested.

Table 9. AC Characteristics

Symbol	Alt.	Parameter	M24256-A				Unit
			V_{CC}=4.5 to 5.5 V T_A=–40 to 85°C		V_{CC}=2.5 to 5.5 V T_A=–40 to 85°C		
			Min	Max	Min	Max	
t_{CH1CH2}	t_R	Clock Rise Time		300		300	ns
t_{CL1CL2}	t_F	Clock Fall Time		300		300	ns
t_{DH1DH2} [2]	t_R	SDA Rise Time	20	300	20	300	ns
t_{DL1DL2} [2]	t_F	SDA Fall Time	20	300	20	300	ns
t_{CHDX} [1]	$t_{SU:STA}$	Clock High to Input Transition	600		600		ns
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	600		600		ns
t_{DLCL}	$t_{HD:STA}$	Input Low to Clock Low (START)	600		600		ns
t_{CLDX}	$t_{HD:DAT}$	Clock Low to Input Transition	0		0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	1.3		1.3		µs
t_{DXCX}	$t_{SU:DAT}$	Input Transition to Clock Transition	100		100		ns
t_{CHDH}	$t_{SU:STO}$	Clock High to Input High (STOP)	600		600		ns
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	1.3		1.3		µs
t_{CLQV} [3]	t_{AA}	Clock Low to Data Out Valid	200	900	200	900	ns
t_{CLQX}	t_{DH}	Data Out Hold Time After Clock Low	200		200		ns
f_C	f_{SCL}	Clock Frequency		400		400	kHz
t_W	t_{WR}	Write Time		10		10	ms

Note: 1. For a reSTART condition, or following a write cycle.
2. Sampled only, not 100% tested.
3. To avoid spurious START and STOP conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA.

Table 10. AC Measurement Conditions

Input Rise and Fall Times	≤ 50 ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Reference Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Figure 9. AC Testing Input Output Waveforms

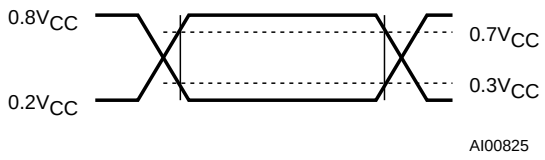


Figure 10. AC Waveforms

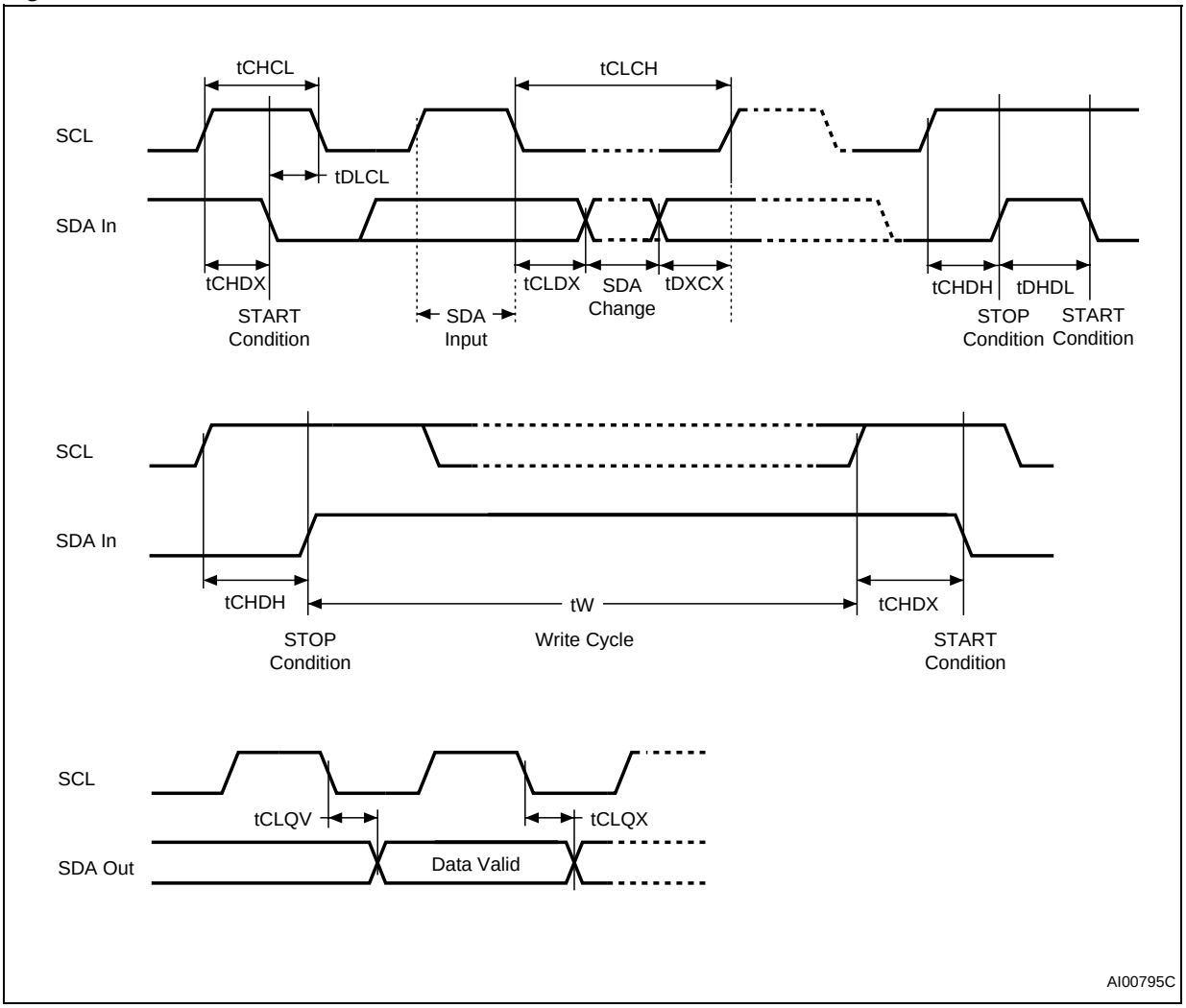
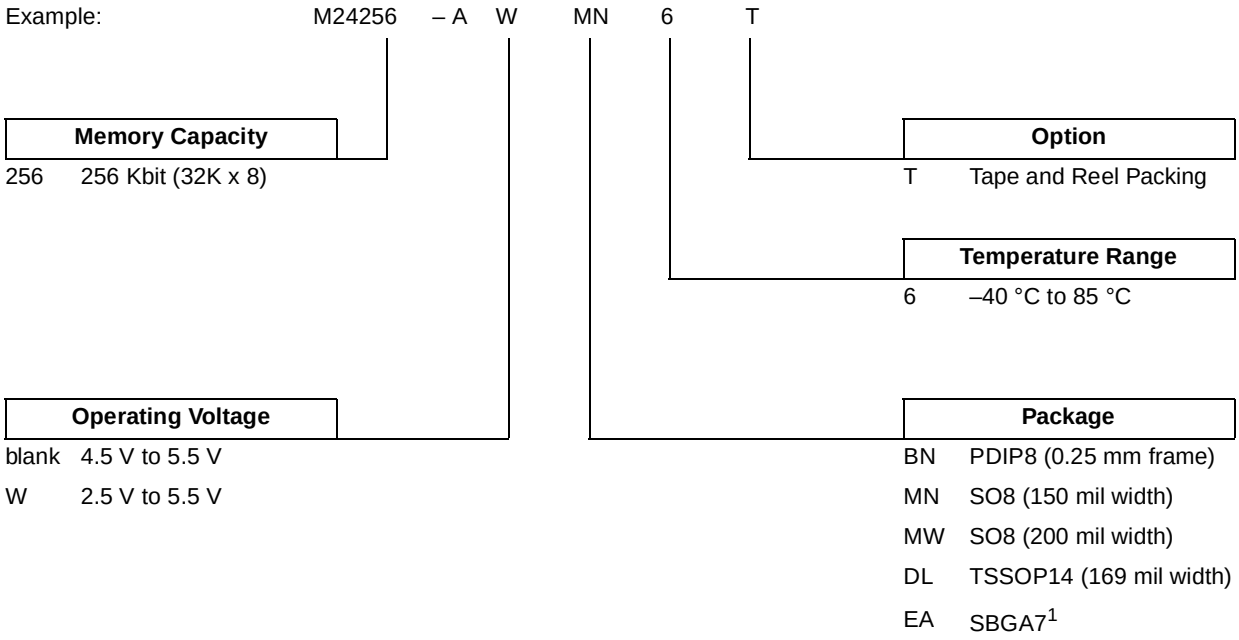


Table 11. Ordering Information Scheme



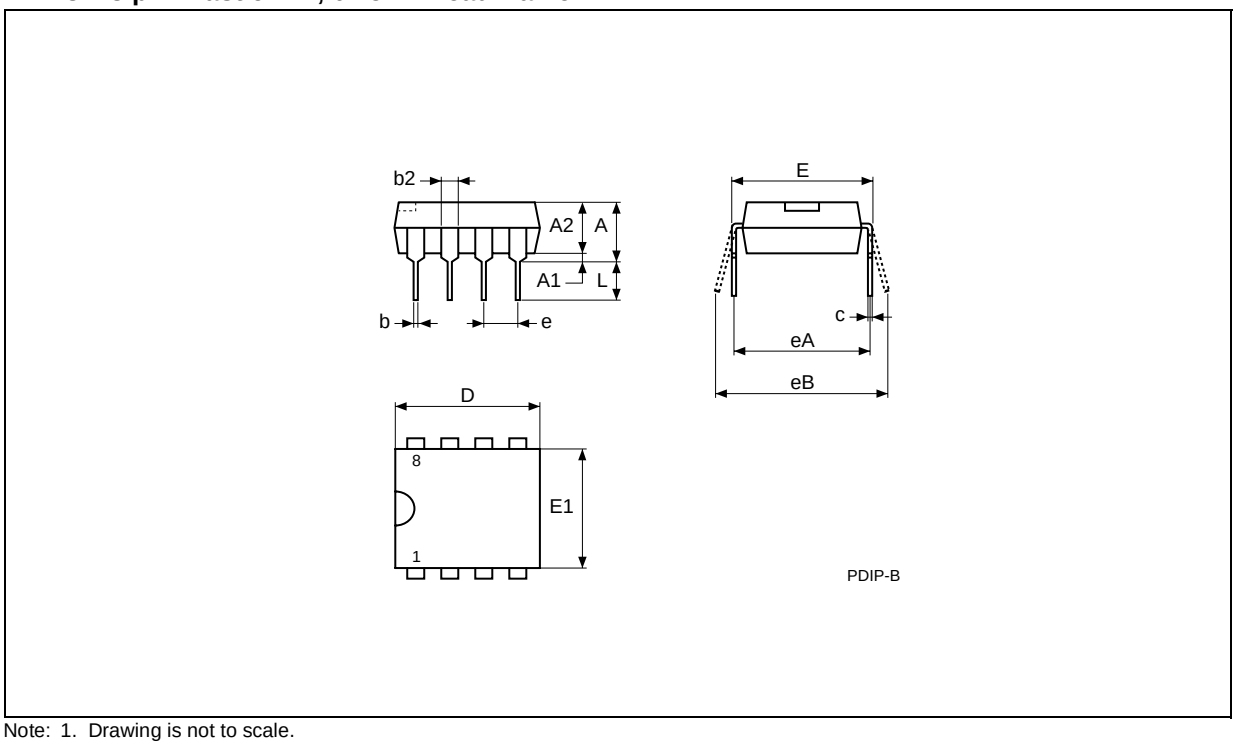
Note: 1. SBGA7 package available only for the “M24256-A W EA 6 T”

ORDERING INFORMATION

Devices are shipped from the factory with the memory content set at all 1s (FFh).

The notation used for the device number is as shown in Table 11. For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST Sales Office.

PDIP8 – 8 pin Plastic DIP, 0.25mm lead frame

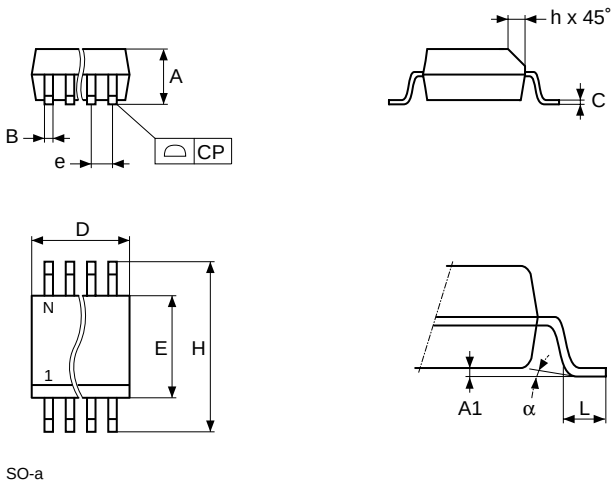


Note: 1. Drawing is not to scale.

PDIP8 – 8 pin Plastic DIP, 0.25mm lead frame

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			5.33			0.210
A1		0.38			0.015	
A2	3.30	2.92	4.95	0.130	0.115	0.195
b	0.46	0.36	0.56	0.018	0.014	0.022
b2	1.52	1.14	1.78	0.060	0.045	0.070
c	0.25	0.20	0.36	0.010	0.008	0.014
D	9.27	9.02	10.16	0.365	0.355	0.400
E	7.87	7.62	8.26	0.310	0.300	0.325
E1	6.35	6.10	7.11	0.250	0.240	0.280
e	2.54	–	–	0.100	–	–
eA	7.62	–	–	0.300	–	–
eB			10.92			0.430
L	3.30	2.92	3.81	0.130	0.115	0.150

SO8 narrow – 8 lead Plastic Small Outline, 150 mils body width



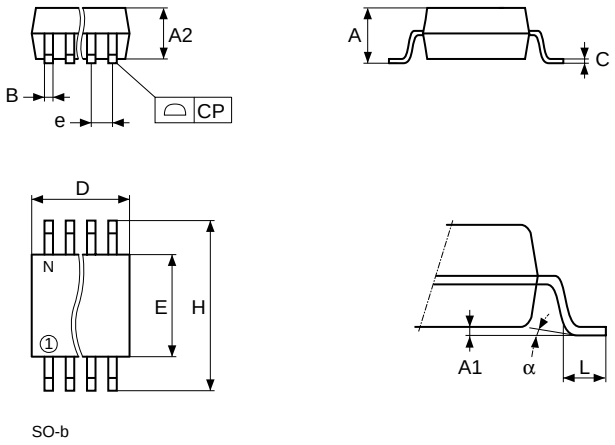
SO-a

Note: Drawing is not to scale.

SO8 narrow – 8 lead Plastic Small Outline, 150 mils body width

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N	8			8		
CP			0.10			0.004

SO8 wide – 8 lead Plastic Small Outline, 200 mils body width

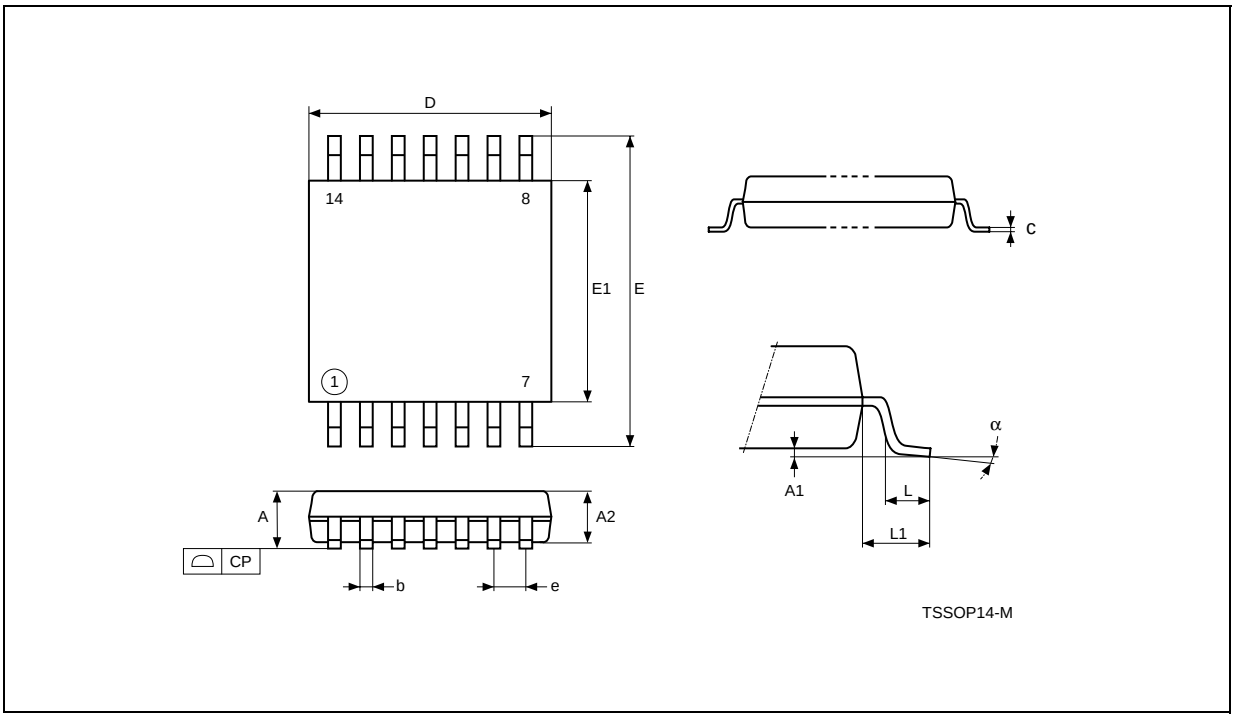


Note: Drawing is not to scale.

SO8 wide – 8 lead Plastic Small Outline, 200 mils body width

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			2.03			0.080
A1		0.10	0.25		0.004	0.010
A2			1.78			0.070
B		0.35	0.45		0.014	0.018
C	0.20	–	–	0.008	–	–
D		5.15	5.35		0.203	0.211
E		5.20	5.40		0.205	0.213
e	1.27	–	–	0.050	–	–
H		7.70	8.10		0.303	0.319
L		0.50	0.80		0.020	0.031
α		0°	10°		0°	10°
N	8			8		
CP			0.10			0.004

TSSOP14 - 14 lead Thin Shrink Small Outline

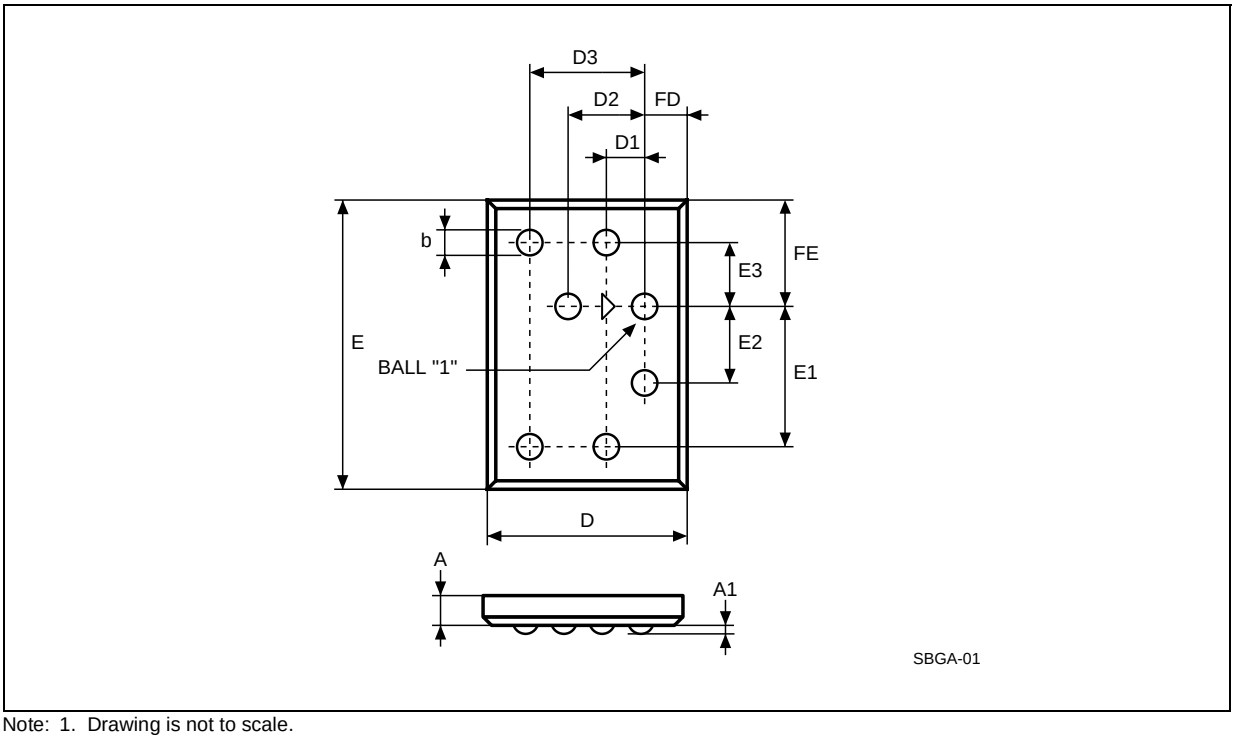


Note: 1. Drawing is not to scale.

TSSOP14 - 14 lead Thin Shrink Small Outline

Symbol	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			1.200			0.0472
A1		0.050	0.150		0.0020	0.0059
A2	1.000	0.800	1.050	0.0394	0.0315	0.0413
b		0.190	0.300		0.0075	0.0118
c		0.090	0.200		0.0035	0.0079
CP			0.100			0.0039
D	5.000	4.900	5.100	0.1969	0.1929	0.2008
e	0.650	–	–	0.0256	–	–
E	6.400	6.200	6.600	0.2520	0.2441	0.2598
E1	4.400	4.300	4.500	0.1732	0.1693	0.1772
L	0.600	0.500	0.750	0.0236	0.0197	0.0295
L1	1.000			0.0394		
α		0°	8°		0°	8°

SBGA7 – 7 ball Shell Ball Grid Array – Underside view (ball side)



Note: 1. Drawing is not to scale.

SBGA7 – 7 ball Shell Ball Grid Array

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A	0.430	0.380	0.480	0.017	0.015	0.019
A1	0.180	0.150	0.210	0.007	0.006	0.008
b	0.350	0.320	0.380	0.014	0.013	0.015
D	3.555	3.525	3.585	0.140	0.138	0.142
D2 [1]	1.000	0.970	1.030	0.039	0.038	0.041
E	2.275	2.245	2.305	0.090	0.088	0.091
FD	1.278	—	—	0.050	—	—
FE	0.388	—	—	0.015	—	—
N	7			7		

Note: 1. No ball is closer than D2 to any other ball, thus giving an arrangement of equilateral triangles in which:
E1 = D2/2 ; E2 = D2 ; E3 = 3xD2/2
D3 = √3xD2/2 ; D1 = D2 + √3xD2/2

Table 12. Revision History

Date	Rev	Description of Revision
17-Apr-2000	1.2	SBGA7(EA) package added on pp 1, 2, OrderInfo, PackageData E1 and E0 are specified as having to be tied either to V_{CC} or V_{SS}
22-May-2001	1.3	-R voltage range removed Lead Soldering Temperature in the Absolute Maximum Ratings table amended Depiction of Start and Stop condition on timing illustrations revised Write Mode Sequences with $\overline{WC}$=1 (data write inhibited) illustration updated Write Cycle Polling Flow Chart using ACK illustration updated References to PSDIP8 changed to PDIP8, and Package Mechanical data updated Document promoted from Preliminary Data to Full Data Sheet
09-Oct-2001	1.4	Document moved from Full Data Sheet to Not for New Design (please see the M24256-B data sheet for a suitable replacement device)
09-Nov-2001	1.5	Reference made to AN1470, on replacing the M24256-A by the M24256-B Specification of Test Condition for Leakage Currents in the DC Characteristics table improved

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