8-Bit, 40/80/100 MSPS Dual A/D Converter

AD9288

FEATURES

Dual 8-bit, 40 MSPS, 80 MSPS, and 100 MSPS ADC
Low power: 90 mW at 100 MSPS per channel
On-chip reference and track-and-hold
475 MHz analog bandwidth each channel
SNR = 47 dB @ 41 MHz
1 V p-p analog input range each channel
Single 3.0 V supply operation (2.7 V to 3.6 V)
Standby mode for single-channel operation
Twos complement or offset binary output mode
Output data alignment mode
Pin-compatible 10-bit upgrade available

APPLICATIONS

Battery-powered instruments
Hand-held scopemeters
Low cost digital oscilloscopes
I and Q communications

FUNCTIONAL BLOCK DIAGRAM

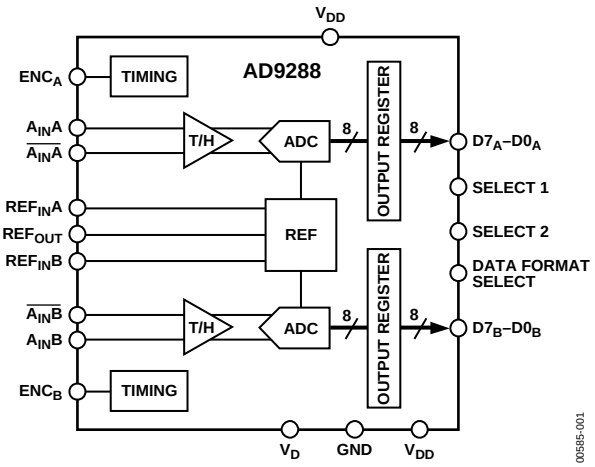

Figure 1.

GENERAL DESCRIPTION

The AD9288 is a dual 8-bit monolithic sampling analog-to-digital converter with on-chip track-and-hold circuits. It is optimized for low cost, low power, small size, and ease of use. The product operates at a 100 MSPS conversion rate with outstanding dynamic performance over its full operating range. Each channel can be operated independently.

The ADC requires only a single 3.0 V (2.7 V to 3.6 V) power supply and an Encode clock for full-performance operation. No external reference or driver components are required for many applications. The digital outputs are TTL/CMOS-compatible, and a separate output power supply pin supports interfacing with 3.3 V or 2.5 V logic.

The Encode input is TTL/CMOS-compatible, and the 8-bit digital outputs can be operated from 3.0 V (2.5 V to 3.6 V) supplies. User-selectable options offer a combination of standby modes, digital data formats, and digital data timing schemes. In standby mode, the digital outputs are driven to a high impedance state.

Fabricated on an advanced CMOS process, the AD9288 is available in a 48-lead surface-mount plastic package (7 mm × 7 mm, 1.4 mm LQFP) specified over the industrial temperature range (–40°C to +85°C). The AD9288 is pin-compatible with the 10-bit AD9218, facilitating future system migrations.

Rev. C
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REVISION HISTORY

12/04—Rev. B to Rev. C

Change to Absolute Maximum Ratings ... 7
Replaced Evaluation Board Section ... 16
Updated Outline Dimensions ... 21
Changes to Ordering Guide ... 21

2/02—Rev. A to Rev. B

Edits to ABSOLUTE MAXIMUM RATINGS ... 3

1/01—Rev. 0 to Rev. A

2/99—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 3.0 V; V_D = 3.0 V, differential input; external reference, unless otherwise noted.

Table 1.

Parameter	Temp	Test Level	AD9288BST-100 Min	AD9288BST-100 Typ	AD9288BST-100 Max	AD9288BST-80 Min	AD9288BST-80 Typ	AD9288BST-80 Max	AD9288BST-40 Min	AD9288BST-40 Typ	AD9288BST-40 Max	Unit
RESOLUTION				8			8			8		Bits
DC ACCURACY												
Differential Nonlinearity	25°C	I		± 0.5	+1.25		± 0.5	+1.25		± 0.5	+1.25	LSB
	Full	VI			1.50			1.50			1.50	LSB
Integral Nonlinearity	25°C	I		± 0.50	+1.25		± 0.50	+1.25		± 0.50	+1.25	LSB
	Full	VI			1.50			1.50			1.50	LSB
No Missing Codes	Full	VI		Guaranteed			Guaranteed			Guaranteed		
Gain Error[1]	25°C	I	–6	± 2.5	+6	–6	± 2.5	+6	–6	± 2.5	+6	% FS
	Full	VI	–8		+8	–8		+8	–8		+8	% FS
Gain Tempco[1]	Full	VI		80			80			80		ppm/°C
Gain Matching	25°C	V		±1.5			±1.5			±1.5		% FS
Voltage Matching	25°C	V		±15			±15			±15		mV
ANALOG INPUT												
Input Voltage Range (with Respect to $\overline{A_{IN}}$)	Full	V		±512			±512			±512		mV p-p
Common-Mode Voltage	Full	V	0.3 × VD	0.3 × VD	0.3 × VD	0.3 × VD	0.3 × VD	0.3 × VD	0.3 × VD	0.3 × VD	0.3 × VD	V
			–0.2		+0.2	–0.2		+0.2	–0.2		+0.2	
Input Offset Voltage	25°C	I	–35	±10	+35	–35	± 10	+35	–35	± 10	+35	mV
	Full	VI	–40		+40	–40		+40	–40		+40	mV
Reference Voltage	Full	VI	1.2	1.25	1.3	1.2	1.25	1.3	1.2	1.25	1.3	V
Reference Tempco	Full	VI		± 130			± 130			± 130		ppm/°C
Input Resistance	25°C	I	7	10	13	7	10	13	7	10	13	kΩ
	Full	VI	5		16	5		16	5		16	
Input Capacitance	25°C	V		2			2			2		pF
Analog Bandwidth, Full Power	25°C	V		475			475			475		MHz
SWITCHING PERFORMANCE												
Maximum Conversion Rate	Full	VI	100			80			40			MSPS
Minimum Conversion Rate	25°C	IV			1			1			1	MSPS
Encode Pulse Width High (t_{EH})	25°C	IV	4.3		1000	5.0		1000	8.0		1000	ns
Encode Pulse Width Low (t_{EL})	25°C	IV	4.3		1000	5.0		1000	8.0		1000	ns
Aperture Delay (t_A)	25°C	V		300			300			300		ps
Aperture Uncertainty (Jitter)	25°C	V		5			5			5		ps rms
Output Valid Time (t_V)[2]	Full	VI	2	3.0		2	3.0		2	3.0		ns
Output Propagation Delay (t_{PD})[2]	Full	VI		4.5	6.0		4.5	6.0		4.5	6.0	ns
DIGITAL INPUTS												
Logic 1 Voltage	Full	VI	2.0			2.0			2.0			V
Logic 0 Voltage	Full	VI			0.8			0.8			0.8	V
Logic 1 Current	Full	VI			± 1			± 1			± 1	µA
Logic 0 Current	Full	VI			± 1			± 1			± 1	µA
Input Capacitance	25°C	V		2.0			2.0			2.0		pF
DIGITAL OUTPUTS[3]												
Logic 1 Voltage	Full	VI	2.45			2.45			2.45			V
Logic 0 Voltage	Full	VI			0.05			0.05			0.05	V
POWER SUPPLY												
Power Dissipation[4]	Full	VI		180	218		171	207		156	189	mW
Standby Dissipation[4, 5]	Full	VI		6	11		6	11		6	11	mW
Power Supply Rejection Ratio (PSRR)	25°C	I		8	20		8	20		8	20	mV/V

Parameter	Temp	Test Level	AD9288BST-100 Min	AD9288BST-100 Typ	AD9288BST-100 Max	AD9288BST-80 Min	AD9288BST-80 Typ	AD9288BST-80 Max	AD9288BST-40 Min	AD9288BST-40 Typ	AD9288BST-40 Max	Unit
DYNAMIC PERFORMANCE[6]												
Transient Response	25°C	V		2			2			2		ns
Overvoltage Recovery Time	25°C	V		2			2			2		ns
Signal-to-Noise Ratio (SNR) (without Harmonics)												
f_{IN} = 10.3 MHz	25°C	I		47.5			47.5		44	47.5	dB	
fl_N = 26 MHz	25°C	I		47.5		44	47				dB	
f_{IN} = 41 MHz	25°C	I	44	47.0							dB	
Signal-to-Noise Ratio (SINAD) (with Harmonics)												
f_{IN} = 10.3 MHz	25°C	I		47			47		44	47		dB
f_{IN} = 26 MHz	25°C	I		47		44	47					dB
f_{IN} = 41 MHz	25°C	I	44	47			47					dB
Effective Number of Bits												
f_{IN} = 10.3 MHz	25°C	I		7.5			7.5		7.0	7.5		Bits
f_{IN} = 26 MHz	25°C	I		7.5		7.0	7.5					Bits
f_{IN} = 41 MHz	25°C	I	7.0	7.5			7.5					Bits
Second Harmonic Distortion												
f_{IN} = 10.3 MHz	25°C	I		70			70		55	70		dBc
f_{IN} = 26 MHz	25°C	I		70		55	70					dBc
f_{IN} = 41 MHz	25°C	I	55	70			70					dBc
Third Harmonic Distortion												
f_{IN} = 10.3 MHz	25°C	I		60			60		55	60		dBc
f_{IN} = 26 MHz	25°C	I		60		55	60					dBc
f_{IN} = 41 MHz	25°C	I	52	60			60					dBc
Two-Tone Intermod Distortion (IMD)												
f_{IN} = 10.3 MHz	25°C	V		60			60		60			dBc

[1] Gain error and gain temperature coefficient are based on the ADC only (with a fixed 1.25 V external reference).
[2] t_V and t_{PD} are measured from the 1.5 V level of the Encode input to the 10%/90% levels of the digital outputs swing. The digital output load during test is not to exceed an ac load of 10 pF or a dc current of ±40 µA.
[3] Digital supply current based on V_{DD} = 3.0 V output drive with < 10 pF loading under dynamic test conditions.
[4] Power dissipation measured under the following conditions: f_S = 100 MSPS, analog input is –0.7 dBFS, both channels in operation.
[5] Standby dissipation calculated with Encode clock in operation.
[6] SNR/harmonics based on an analog input voltage of –0.7 dBFS referenced to a 1.024 V full-scale input range.

EXPLANATION OF TEST LEVELS

Level	Description
I	100% production tested.
II	100% production tested at 25°C and sample tested at specified temperatures.
III	Sample tested only.
IV	Parameter is guaranteed by design and characterization testing.
V	Parameter is a typical value only.
VI	100% production tested at 25°C; guaranteed by design and characterization testing for industrial temperature range; 100% production tested at temperature extremes for military devices.

TIMING DIAGRAMS

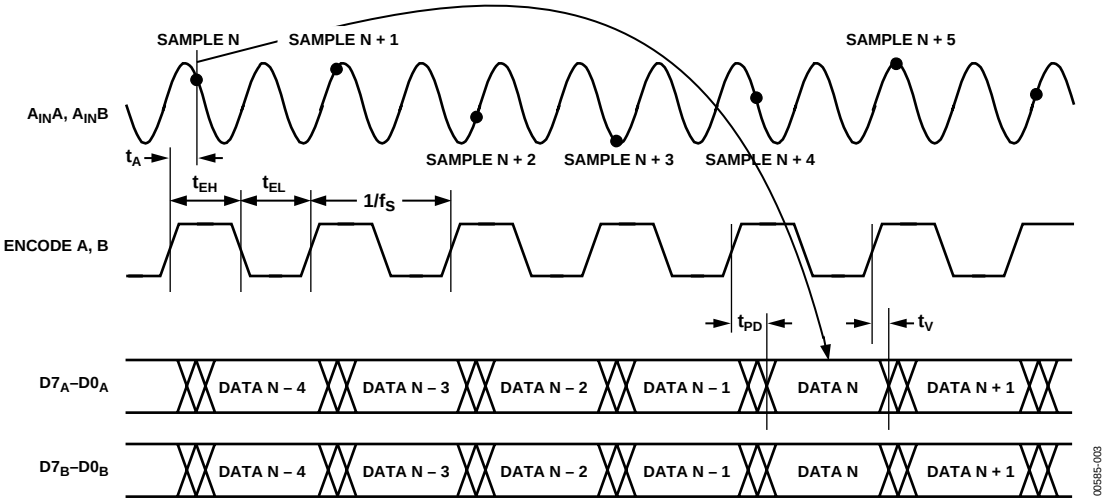

Figure 2. Normal Operation, Same Clock (S1 = 1, S2 = 0) Channel Timing

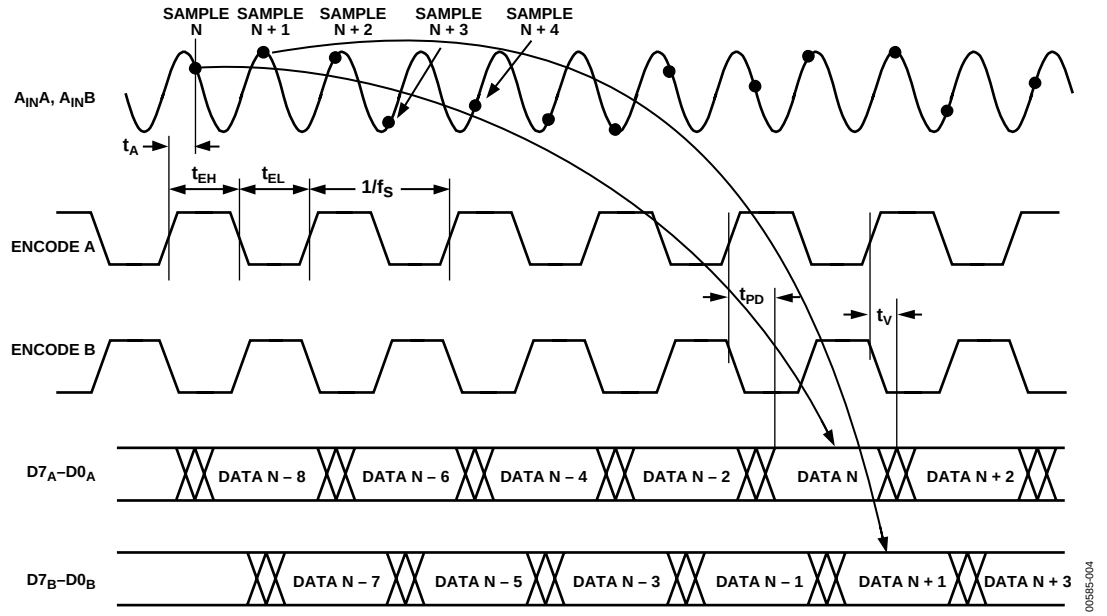

Figure 3. Normal Operation with Two Clock Sources (S1 = 1, S2 = 0) Channel Timing

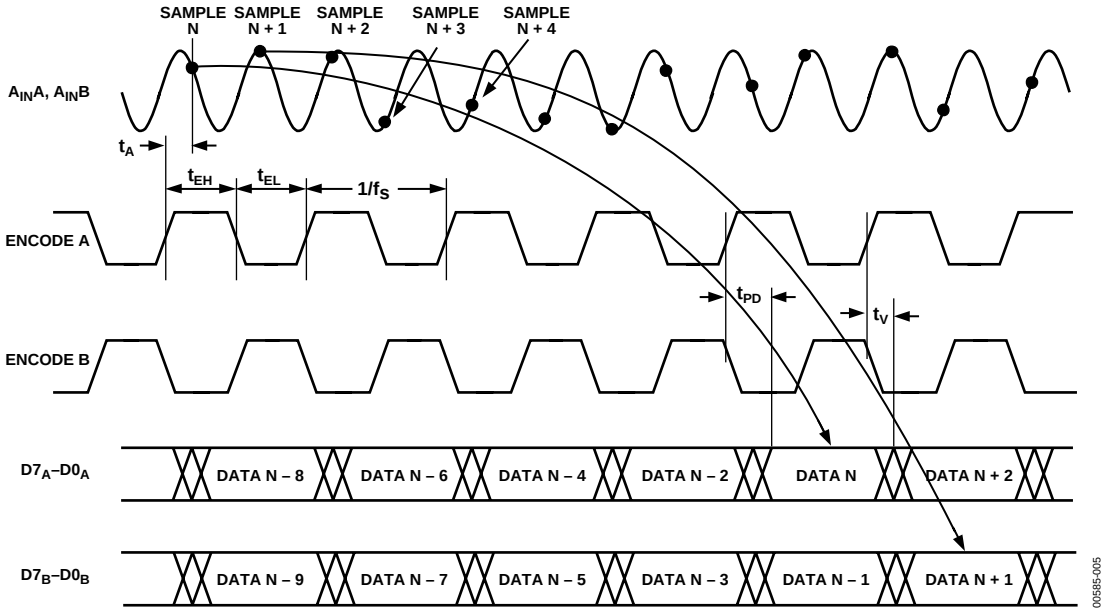

Figure 4. Data Align with Two Clock Sources (S1 = 1, S2 = 1) Channel Timing

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
V_D, V_{DD}	4 V
Analog Inputs	–0.5 V to V_D + 0.5 V
Digital Inputs	–0.5 V to V_{DD} + 0.5 V
VREF IN	–0.5 V to V_D + 0.5 V
Digital Output Current	20 mA
Operating Temperature	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Maximum Junction Temperature	150°C
Maximum Case Temperature	150°C
Thermal Impedance θ_{ja}	57°C/W

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

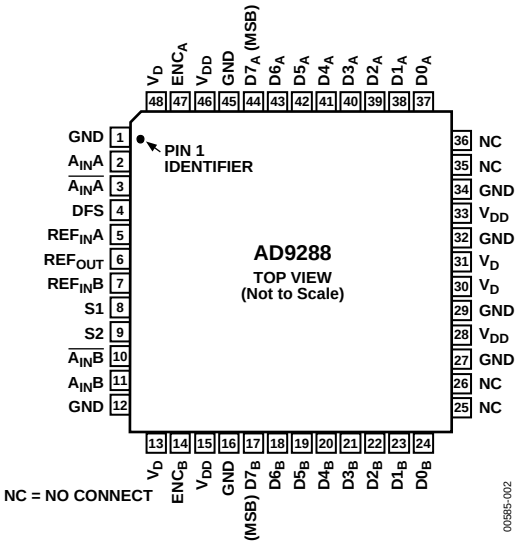

Figure 5. Pin Configuration

Table 3.

Pin No.	Name	Description
1, 12, 16, 27, 29, 32, 34, 45	GND	Ground
2	$A_{IN}A$	Analog Input for Channel A.
3	$\overline{A_{IN}A}$	Analog Input for Channel A (Complementary).
4	DFS	Data Format Select. Offset binary output available if set low. Twos complement output available if set high.
5	$REF_{IN}A$	Reference Voltage Input for Channel A.
6	REF_{OUT}	Internal Reference Voltage.
7	$REF_{IN}B$	Reference Voltage Input for Channel B.
8	S1	User Select 1. Refer to Table 4. Tied with respect to V_D.
9	S2	User Select 2. Refer to Table 4. Tied with respect to V_D.
10	$\overline{A_{IN}B}$	Analog Input for Channel B (Complementary).
11	$A_{IN}B$	Analog Input for Channel B.
13, 30, 31, 48	V_D	Analog Supply (3 V).
14	ENC_B	Clock Input for Channel B.
15, 28, 33, 46	V_{DD}	Digital Supply (3 V).
17–24	$D7_B$–$D0_B$	Digital Output for Channel B.
25, 26, 35, 36	NC	Do Not Connect.
37–44	$D0_A$–$D7_A$	Digital Output for Channel A.
47	ENC_A	Clock Input for Channel A.

TYPICAL PERFORMANCE CHARACTERISTICS

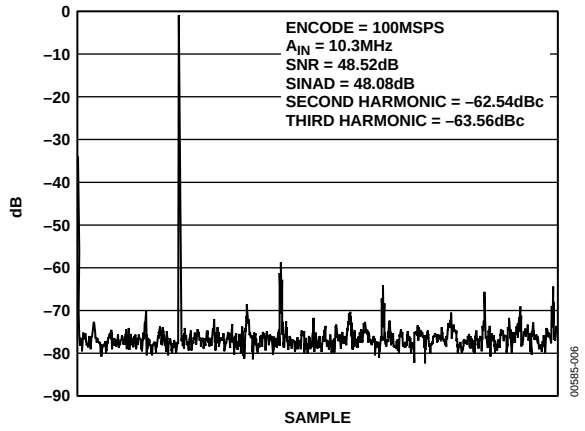

Figure 6. Spectrum: f_S = 100 MSPS, f_{IN} = 10 MHz, Single-Ended Input

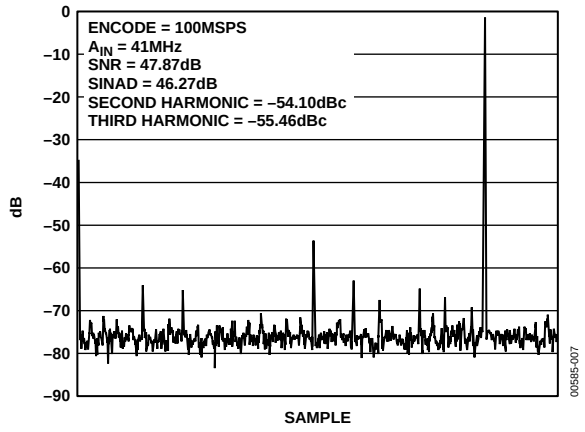

Figure 7. Spectrum: f_S = 100 MSPS, f_{IN} = 41 MHz, Single-Ended Input

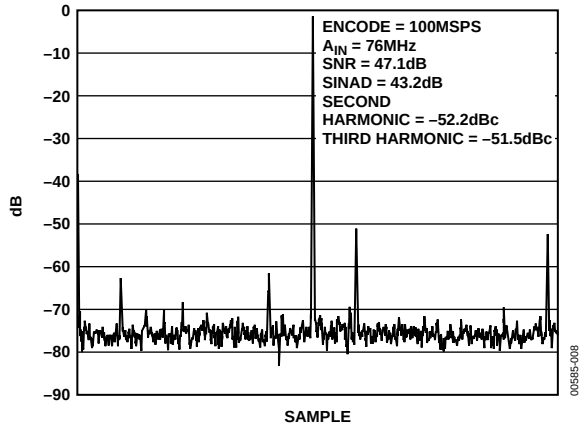

Figure 8. Spectrum: f_S = 100 MSPS, f_{IN} = 76 MHz, Single-Ended Input

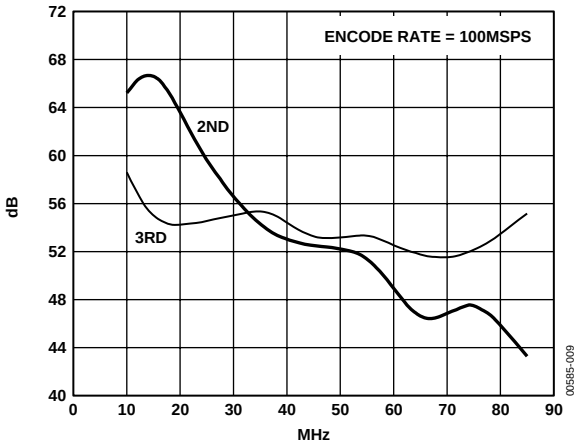

Figure 9. Harmonic Distortion vs. A_{IN} Frequency

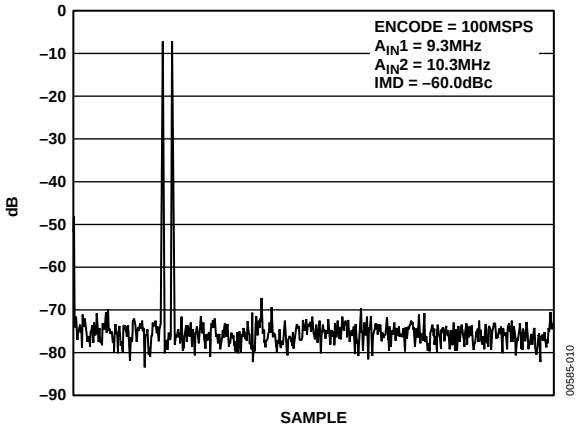

Figure 10. Two-Tone Intermodulation Distortion

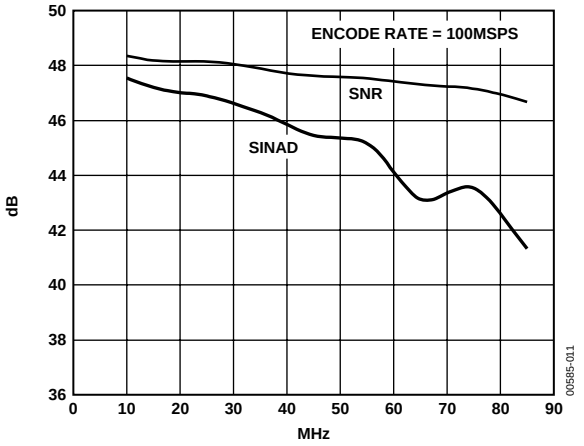

Figure 11. SINAD/SNR vs. A_{IN} Frequency

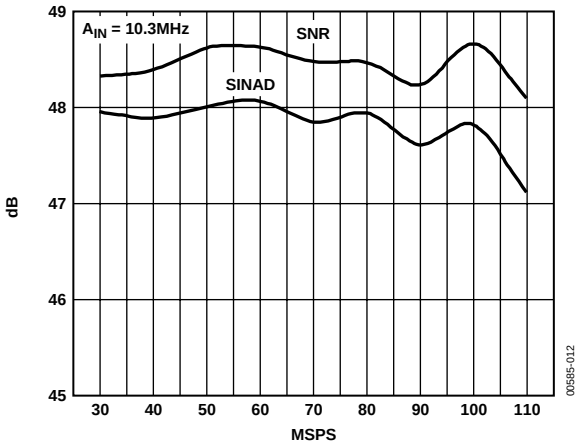

Figure 12. SINAD/SNR vs. Encode Rate

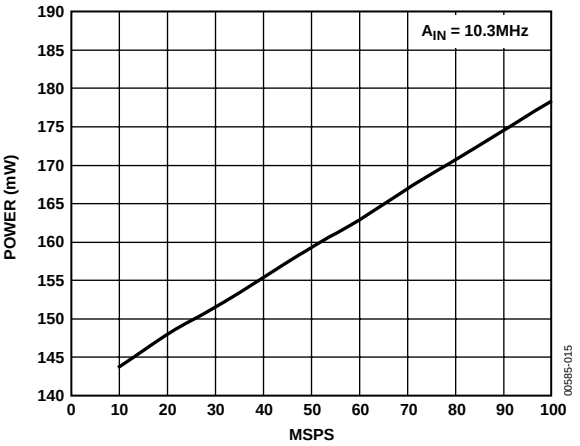

Figure 15. Analog Power Dissipation vs. Encode Rate

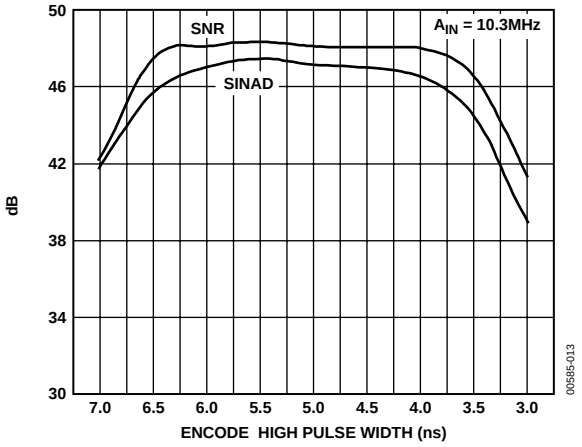

Figure 13. SINAD/SNR vs. Encode Pulse Width High

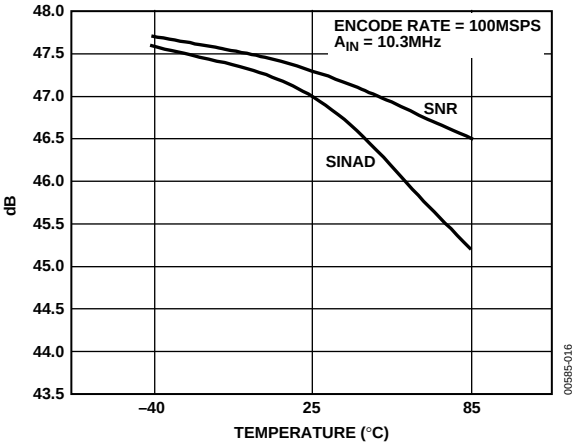

Figure 16. SINAD/SNR vs. Temperature

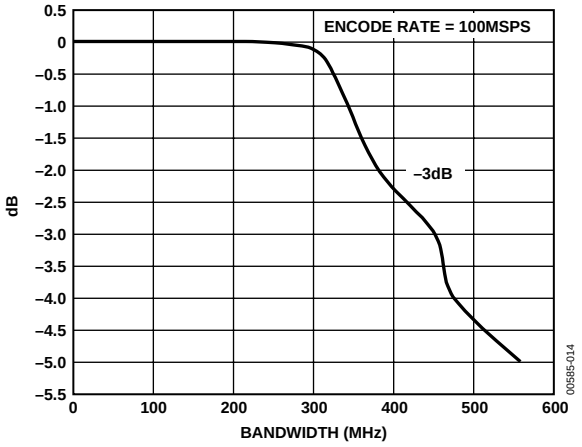

Figure 14. ADC Frequency Response: f_S = 100 MSPS

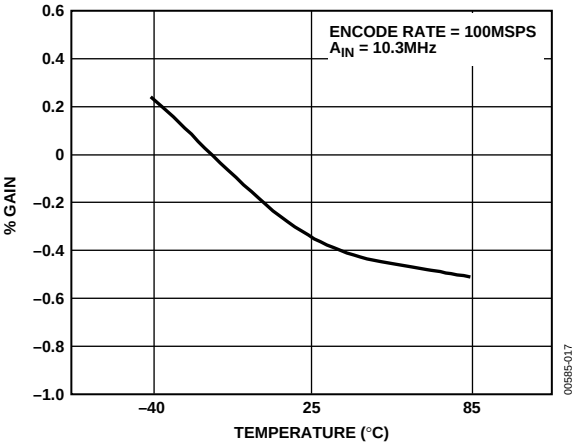

Figure 17. ADC Gain vs. Temperature (with External 1.25 V Reference)

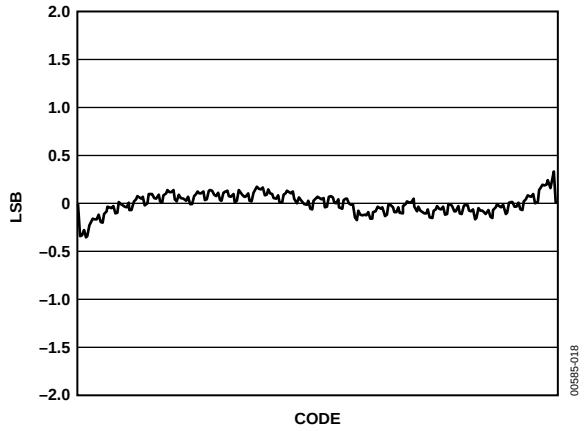

Figure 18. Integral Nonlinearity

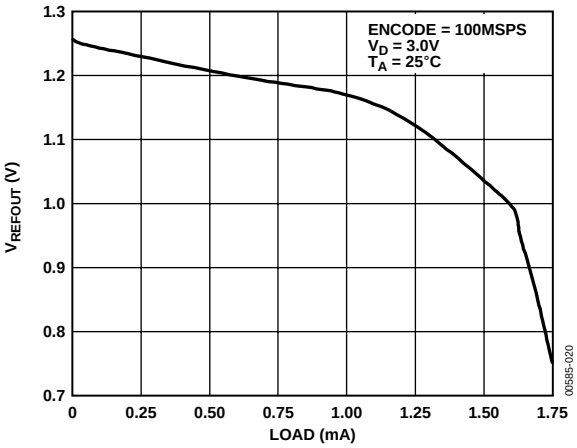

Figure 20. Voltage Reference Out vs. Current Load

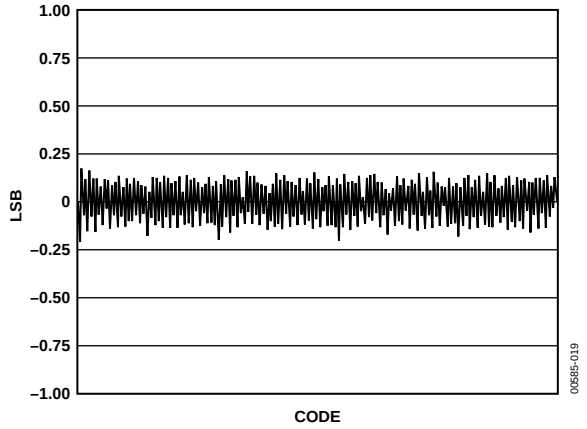

Figure 19. Differential Nonlinearity

TEST CIRCUITS

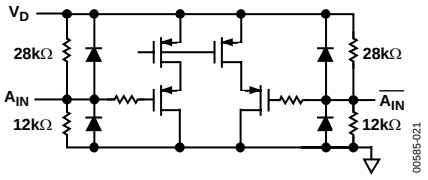

Figure 21. Equivalent Analog Input Circuit

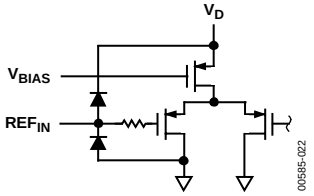

Figure 22. Equivalent Reference Input Circuit

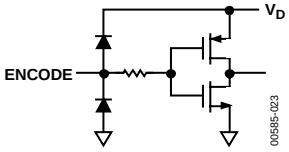

Figure 23. Equivalent Encode Input Circuit

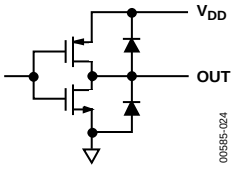

Figure 24. Equivalent Digital Output Circuit

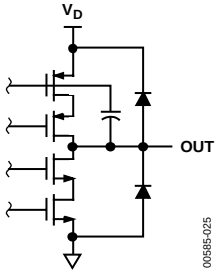

Figure 25. Equivalent Reference Output Circuit

TERMINOLOGY

Analog Bandwidth (Small Signal)
The analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB.

Aperture Delay
The delay between a 50% crossing of Encode and the instant at which the analog input is sampled.

Aperture Uncertainty (Jitter)
The sample-to-sample variation in aperture delay.

Differential Nonlinearity

The deviation of any code from an ideal 1 LSB step.

Encode Pulse Width/Duty Cycle
Pulse width high is the minimum amount of time that the Encode pulse should be left in Logic 1 state to achieve rated performance; pulse width low is the minimum time Encode pulse should be left in low state. At a given clock rate, these specs define an acceptable Encode duty cycle.

Integral Nonlinearity
The deviation of the transfer function from a reference line measured in fractions of 1 LSB using a "best straight line" determined by a least square curve fit.

Minimum Conversion Rate
The Encode rate at which the SNR of the lowest analog signal frequency drops by no more than 3 dB below the guaranteed limit.

Maximum Conversion Rate
The Encode rate at which parametric testing is performed.

Output Propagation Delay
The delay between a 50% crossing of Encode and the time when all output data bits are within valid logic levels.

Power Supply Rejection Ratio
The ratio of a change in input offset voltage to a change in power supply voltage.

Signal-to-Noise-and-Distortion (SINAD)
The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, including harmonics but excluding dc.

Signal-to-Noise Ratio (SNR)
The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, excluding the first five harmonics and dc.

Spurious-Free Dynamic Range (SFDR)
The ratio of the rms signal amplitude to the rms value of the peak spurious spectral component. The peak spurious component may or may not be a harmonic. May be reported in dBc (i.e., degrades as signal level is lowered), or in dBFS (always related back to converter full scale).

Two-Tone Intermodulation Distortion Rejection
Two-Tone SFDR
The ratio of the rms value of either input tone to the rms value of the peak spurious component. The peak spurious component may or may not be an IMD product. May be reported in dBc (i.e., degrades as signal level is lowered), or in dBFS (always related back to converter full scale).

Worst Harmonic
The ratio of the rms value of either input tone to the rms value of the worst third order intermodulation product; reported in dBc.

THEORY OF OPERATION

The AD9288 ADC architecture is a bit-per-stage pipeline-type converter utilizing switch capacitor techniques. These stages determine the 5 MSBs and drive a 3-bit flash. Each stage provides sufficient overlap and error correction, allowing optimization of comparator accuracy. The input buffers are differential, and both sets of inputs are internally biased. This allows the most flexible use of ac or dc and differential or single-ended input modes. The output staging block aligns the data, carries out the error correction, and feeds the data to output buffers. The set of output buffers are powered from a separate supply, allowing adjustment of the output voltage swing. There is no discernible difference in performance between the two channels.

USING THE AD9288

Good high speed design practices must be followed when using the AD9288. To obtain maximum benefit, decoupling capacitors should be physically as close as possible to the chip, minimizing trace and via inductance between chip pins and capacitor (0603 surface-mount capacitors are used on the AD9288/PCB evaluation board). It is recommended to place a 0.1 µF capacitor at each power-ground pin pair for high frequency decoupling, and to include one 10 µF capacitor for local low frequency decoupling. The VREF IN pin should also be decoupled by a 0.1 µF capacitor. It is also recommended to use a split power plane and a contiguous ground plane (see the Evaluation Board section). Data output traces should be short (< 1 inch), minimizing on-chip noise at switching.

ENCODE INPUT

Any high speed A/D converter is extremely sensitive to the quality of the sampling clock provided by the user. A track-and-hold circuit is essentially a mixer. Any noise, distortion, or timing jitter on the clock is combined with the desired signal at the A/D output. For that reason, considerable care has been taken in the design of the Encode (Clock) input of the AD9288, and the user is advised to give commensurate thought to the clock source. The Encode input is fully TTL/CMOS-compatible.

DIGITAL OUTPUTS

The digital outputs are TTL/CMOS-compatible for lower power consumption. During standby, the output buffers transition to a high impedance state. A data format selection option supports either twos complement (set high) or offset binary output (set low) formats.

ANALOG INPUT

The analog input to the AD9288 is a differential buffer. For best dynamic performance, impedance at A_{IN} and $\overline{A_{IN}}$ should match. Special care was taken in the design of the analog input stage of the AD9288 to prevent damage and corruption of data when the input is overdriven. The nominal input range is 1.024 V p-p centered at $V_D \times 0.3$.

VOLTAGE REFERENCE

A stable and accurate 1.25 V voltage reference is built into the AD9288 (REF_{OUT}). In normal operation, the internal reference is used by strapping Pins 5 ($REF_{IN}A$) and 7 ($REF_{IN}B$) to Pin 6 (REFOUT). The input range can be adjusted by varying the reference voltage applied to the AD9288. No appreciable degradation in performance occurs when the reference is adjusted ±5%. The full-scale range of the ADC tracks reference voltage, which changes linearly.

TIMING

The AD9288 provides latched data outputs, with four pipeline delays. Data outputs are available one propagation delay (t_{PD}) after the rising edge of the Encode command (see Figure 2, Figure 3, and Figure 4). The length of the output data lines and loads placed on them must be minimized to reduce transients within the AD9288. These transients can detract from the converter's dynamic performance.

The minimum guaranteed conversion rate of the AD9288 is 1 MSPS. At clock rates below 1 MSPS, dynamic performance degrades. Typical power-up recovery time after standby mode is 15 clock cycles.

USER-SELECTABLE OPTIONS

Two pins are available for a combination of operational modes. These options allow the user to place both channels, excluding the reference, into standby mode, or just the B channel. Both modes place the output buffers and clock inputs into high impedance states.

The other option allows the user to skew the B channel output data by 1/2 of a clock cycle. In other words, if two clocks are fed to the AD9288 and are 180° out of phase, enabling the data align allows Channel B output data to be available at the rising edge of Clock A. If the same Encode clock is provided to both channels and the data align pin is enabled, then output data from Channel B is 180° out of phase with respect to Channel A. If the same Encode clock is provided to both channels and the data align pin is disabled, both outputs are delivered on the same rising edge of the clock.

Table 4. User-Selectable Options

S1	S2	Option
0	0	Standby Both Channels A and B.
0	1	Standby Channel B Only.
1	0	Normal Operation (Data Align Disabled).
1	1	Data Align Enabled (data from both channels available on rising edge of Clock A. Channel B data is delayed a 1/2 clock cycle).

AD9218/AD9288 CUSTOMER PCB BOM

Table 5. Bill of Materials

No.	Qty.	Reference Designator	Device	Package	Value	Comments
1	29	C1, C3-C15, C20, C21, C24, C25, C27, C30–C35, C39–C42	Capacitor	0603	0.1 µF	
2	2	C2, C36	Capacitor	0603	15 pF	8138 out
3	7	C16–C19, C26, C37, C38	Capacitor	TAJD	10 µF	
4	28	E1, E2, E3, E4, E12–E30, E34–E38	W-HOLE	W-HOLE		
5	4	H1, H2, H3, H4	MTHOLE	MTHOLE		
6	5	J1, J2, J3, J4, J5	SMA	SMA		J2, J3, not placed
7	3	P1, P4, P11	4-pin power connector	Post	Z5.531.3425.0	Wieland
8	3	P1, P4, P11	4-pin power connector	Detachable Connector	25.602.5453.0	Wieland
9	1	P2, P3[1]	80-pin rt. angle male		TSW-140-08-L-D-RA	Samtec
10	4	R1, R2, R32, R34	Resistor	0603	36 Ω	R1, R2, R32, R34, not placed
11	9	R3, R7, R11, R14, R22, R23, R24, R30, R51	Resistor	0603	50 Ω	R11, R22, R23, R24, R30, R51 not placed
12	17	R4, R5, R8, R9, R10, R12, R13, R20, R33, R35, R36, R37, R40, R42, R43, R50, R53	Resistor	0603	Zero Ω	R43, R50 not placed
13	2	R6, R38	Resistor	0603	25 Ω	R6, R38 not placed
14	6	R15, R16, R18, R26, R29, R31	Resistor	0603	500 Ω	R16, R29 not placed
15	2	R17, R25	Resistor	0603	525 Ω	
16	2	R19, R27	Resistor	0603	4 kΩ	
17	12	R21, R28, R39, R41, R44, R46–R49, R52, R54, R55	Resistor	0603	1 kΩ	
18	2	T1, T2	Transformer	ADT1-1WT		Minicircuits
19	1	U1	AD9288[2]	LQFP48		
20	2	U2, U3	74LCX821			
21	2	U5, U6	SN74VCX86			
22	4	U7, U8, U9, U10	Resistor array	CTS	47 Ω	768203470G
23	2	U11, U12	AD8138 op amp[3]			

[1] P2, P3 are implemented as one physical 80-pin connector SAMTEC TSW-140-08-L-D-RA.
[2] AD9288/PCB populated with AD9288-100.
[3] To use optional amp: place R22, R23, R30, R24, R16, R29, remove R4, R36.

EVALUATION BOARD

The AD9218/AD9288 customer evaluation board offers an easy way to test the AD9218 or the AD9288. The compatible pinout of the two parts facilitates the use of one PCB for testing either part. The PCB requires power supplies, a clock source, and a filtered analog source for most ADC testing required.

POWER CONNECTOR

Power is supplied to the board via a detachable 12-lead power strip. The minimum 3 V supplies required to run the board are V_{DD}, V_{DL}, and V_{DD}. To allow the use of the optional amplifier path, ±5 V supplies are required.

ANALOG INPUTS

Each channel has an independent analog path that uses a wideband transformer to drive the ADC differentially from a single-ended sine source at the input SMAs. The transformer paths can be bypassed to allow the use of a dc-coupled path by using two AD8138 op amps with a simple board modification. The analog input should be band-pass filtered to remove any harmonics in the input signal and to minimize aliasing.

VOLTAGE REFERENCE

The AD9288 has an internal 1.25 V voltage reference; an external reference for each channel can be used instead by connecting two external voltage references at the power connector and setting jumpers at E18 and E19. The evaluation board is shipped configured for internal reference mode.

CLOCKING

Each channel can be clocked by a common clock input at SMA input ENCODE A/B. The channels can also be clocked independently by a simple board modification. The clock input should be a low jitter sine source for maximum performance.

DATA OUTPUTS

The data outputs are latched on-board by two 10-bit latches and drive an 8-pin connector which is compatible with the dual-channel FIFO board available from Analog Devices. This board, together with ADC analyzer software, can greatly simplify ADC testing.

DATA FORMAT/GAIN

The DFS/Gain pin can be biased for desired operation at the DFS jumper located at the S1, S2 jumpers.

TIMING

Timing on each channel can be controlled if needed on the PCB. Clock signals at the latches or the data ready signals that go to the output 80-pin connector can be inverted if required. Jumpers also allow for biasing of Pins S1 and S2 for power-down and timing alignment control.

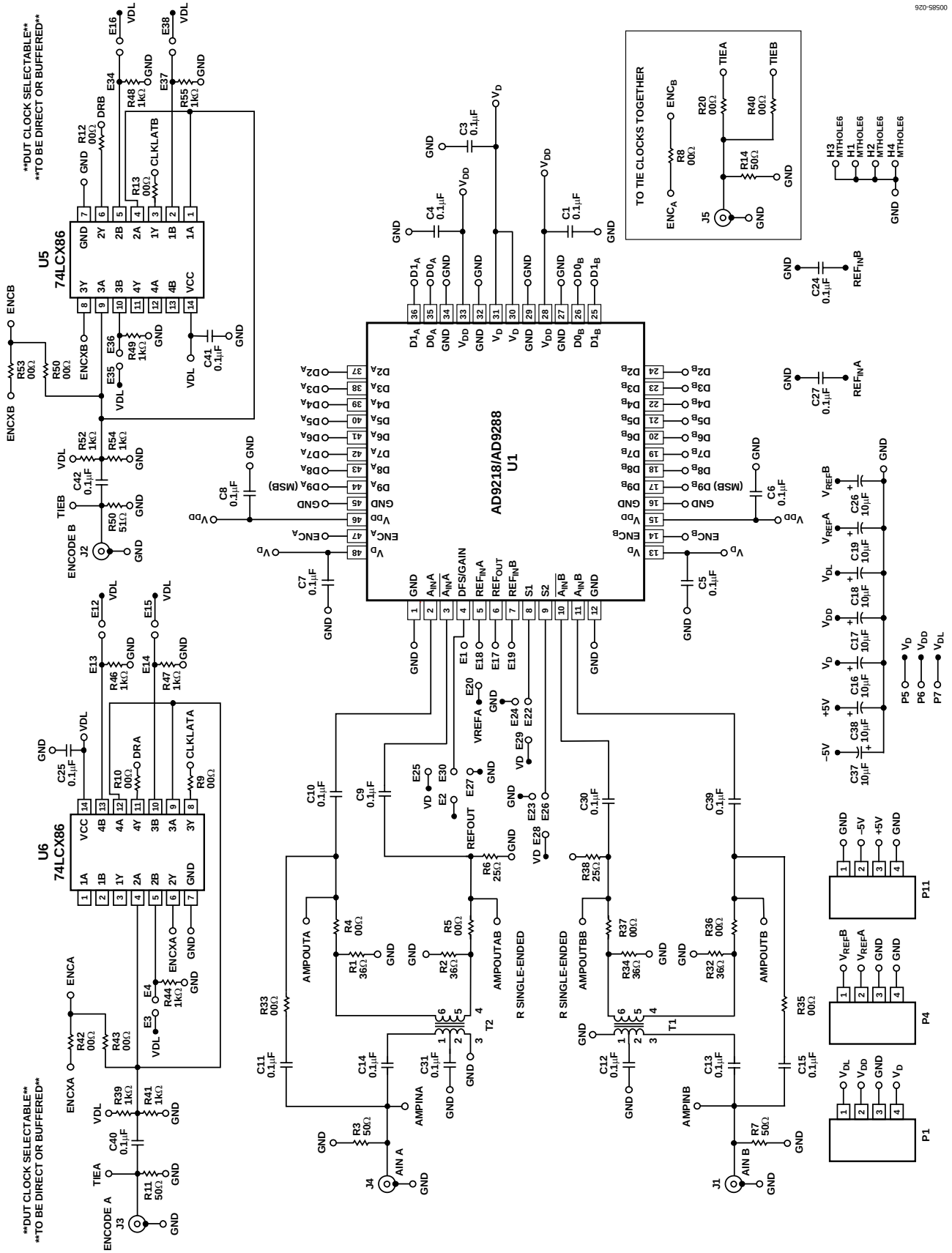

Figure 26. PCB Schematic

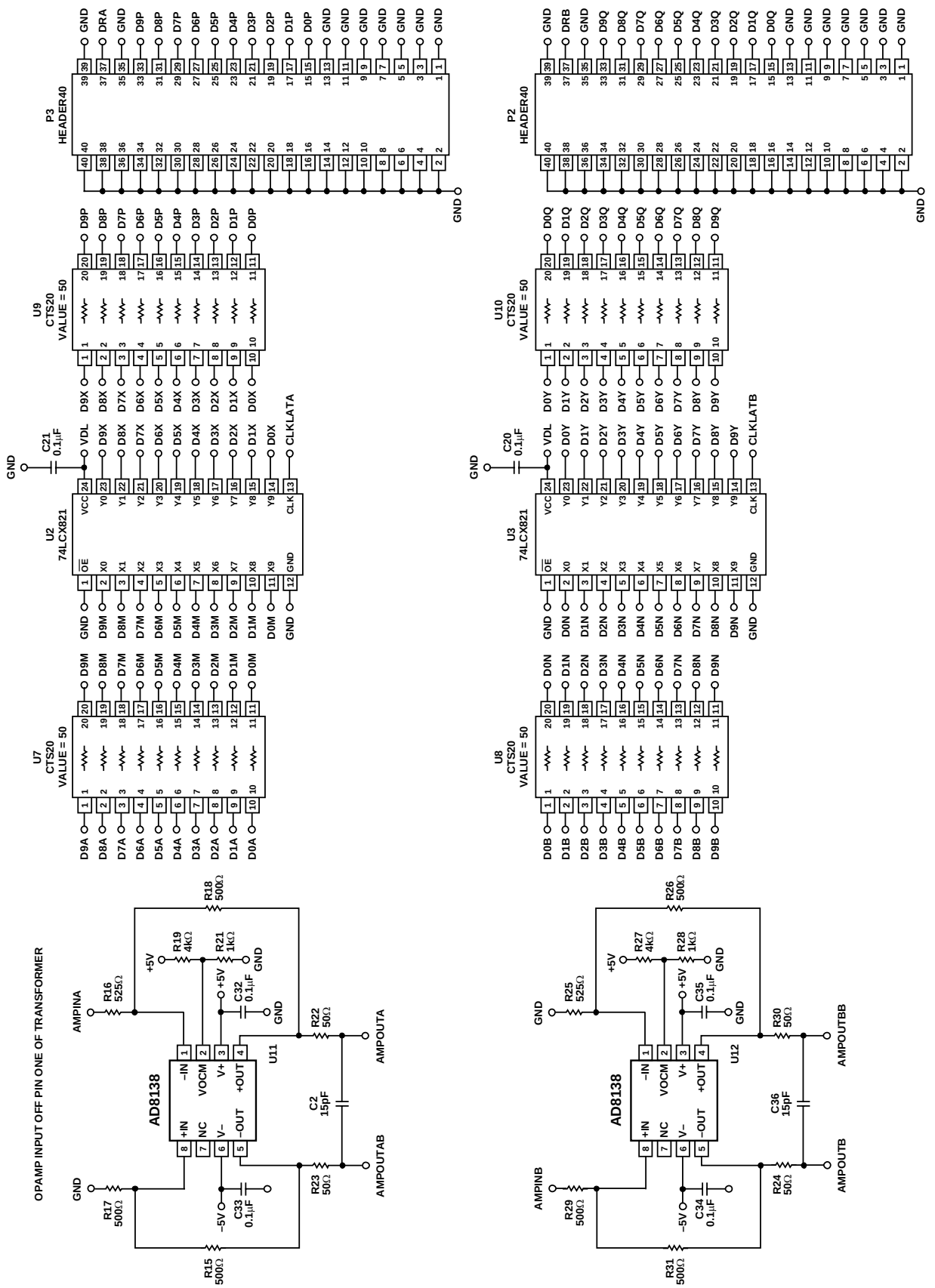

Figure 27. PCB Schematic (Continued)

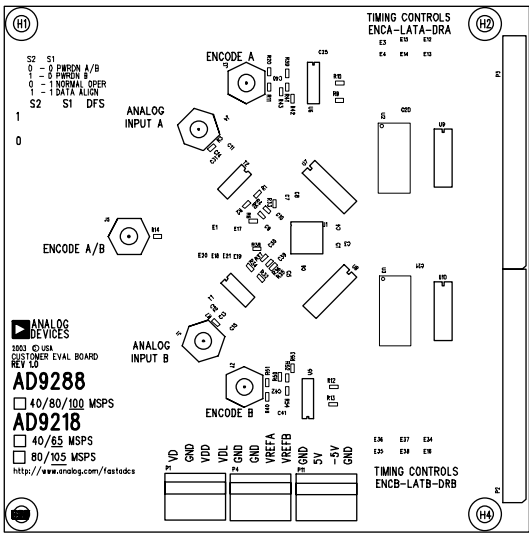

Figure 28. Top Silkscreen

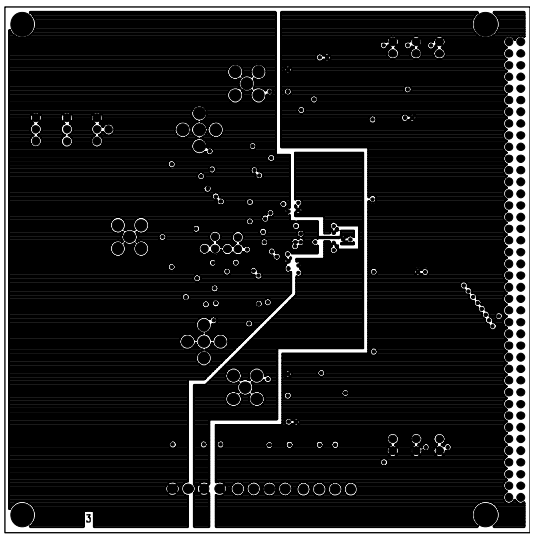

Figure 31. Split Power Plane

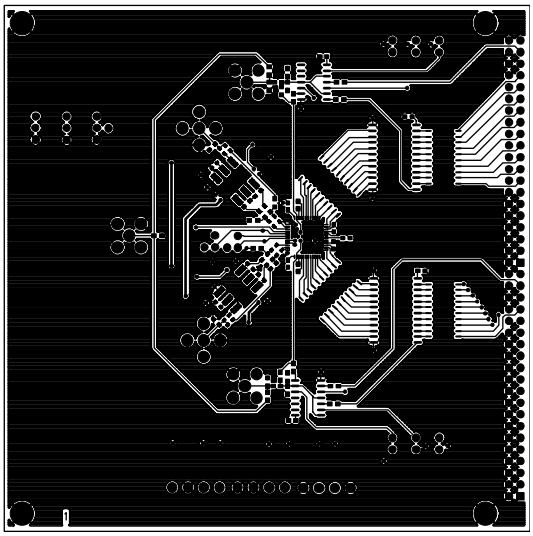

Figure 29. Top Routing

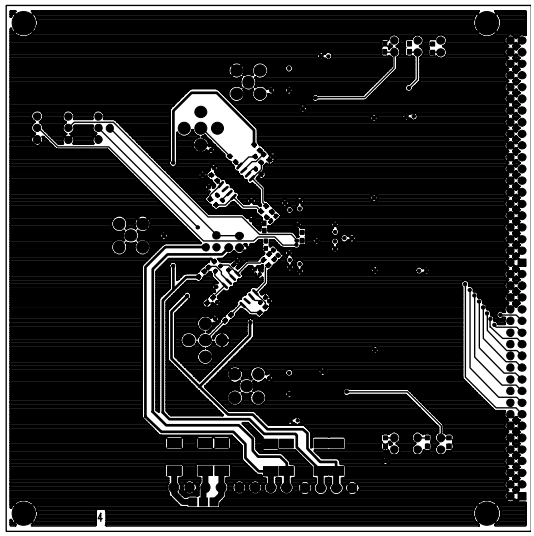

Figure 32. Bottom Routing

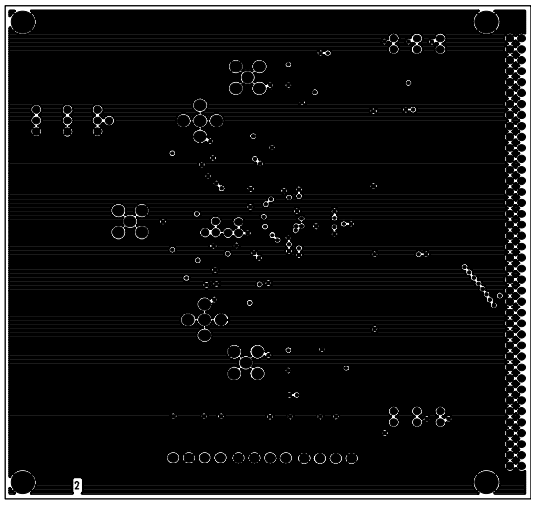

Figure 30. Ground Plane

Figure 33. Bottom Silkscreen

TROUBLESHOOTING

If the board does not seem to be working correctly, try the following:

- Verify power at the IC pins.
- Check that all jumpers are in the correct position for the desired mode of operation.
- Verify that V_{REF} is at 1.23 V.
- Try running Encode clock and analog inputs at low speeds (20 MSPS/1 MHz) and monitor LCX821 outputs, DAC outputs, and ADC outputs for toggling.

The AD9218/AD9288 evaluation board is provided as a design example for customers of Analog Devices, Inc. ADI makes no warranties, express, statutory, or implied, regarding merchantability or fitness for a particular purpose.

OUTLINE DIMENSIONS

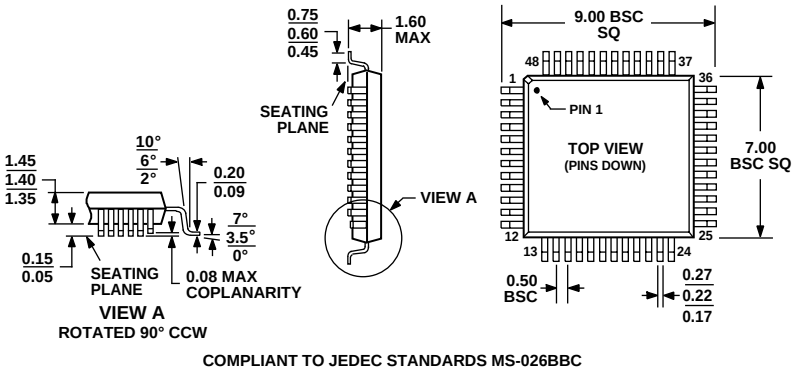

Figure 34. 48-Lead Low Profile Quad Flat Package [LQFP]
(ST-48)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Options
AD9288BST-40	–40°C to +85°C	48-Lead Low Profile Quad Flat Package	ST-48
AD9288BSTZ-40[1]	–40°C to +85°C	48-Lead Low Profile Quad Flat Package	ST-48
AD9288BSTZRL-40[1]	–40°C to +85°C	48-Lead Low Profile Quad Flat Package	ST-48
AD9288BST-80	–40°C to +85°C	48-Lead Low Profile Quad Flat Package	ST-48
AD9288BSTZ-80[1]	–40°C to +85°C	48-Lead Low Profile Quad Flat Package	ST-48
AD9288BST-100	–40°C to +85°C	48-Lead Low Profile Quad Flat Package	ST-48
AD9288BSTZ-100[1]	–40°C to +85°C	48-Lead Low Profile Quad Flat Package	ST-48
AD9288/PCB		Evaluation Board	

[1] Z = Pb-free part.

NOTES

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NOTES

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C00585–0–12/04(C)

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