CY7C107D
CY7C1007D

1-Mbit (1M x 1) Static RAM

Features

- Pin- and function-compatible with CY7C107B/CY7C1007B
- High speed
  - t_{AA} = 10 ns
- Low active power
  - I_{CC} = 80 mA @ 10 ns
- Low complementary metal oxide semiconductor (CMOS) standby power
  - I_{SB2} = 3 mA
- 2.0 V data retention
- Automatic power-down when deselected
- CMOS for optimum speed/power
- Transistor transistor logic (TTL) compatible inputs and outputs
- CY7C107D available in Pb-free 28-pin 400-Mil wide Molded SOJ package. CY7C1007D available in Pb-free 28-pin 300-Mil wide Molded SOJ package

Functional Description [1]

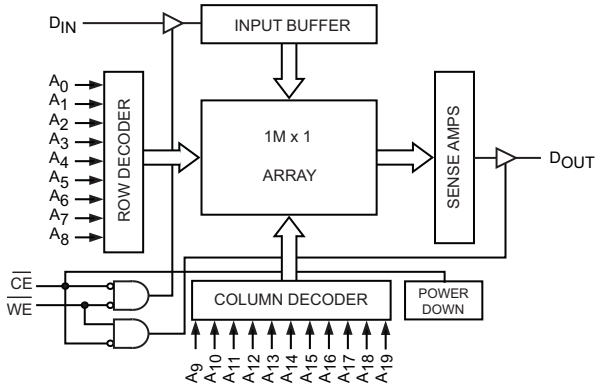
The CY7C107D and CY7C1007D are high-performance CMOS static RAMs organized as 1,048,576 words by 1 bit. Easy memory expansion is provided by an active LOW Chip Enable ($\overline{CE}$) and tri-state drivers. These devices have an automatic power-down feature that reduces power consumption by more than 65% when deselected. The output pin (D_{OUT}) is placed in a high-impedance state when:

- Deselected ($\overline{CE}$ HIGH)
- When the write operation is active ($\overline{CE}$ and $\overline{WE}$ LOW)

Write to the device by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. Data on the input pin (D_{IN}) is written into the memory location specified on the address pins (A_0 through A_{19}).

Read from the device by taking Chip Enable ($\overline{CE}$) LOW while while forcing Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins appears on the data output (D_{OUT}) pin.

Logic Block Diagram



Note
1. For guidelines on SRAM system design, please refer to the 'System Design Guidelines' Cypress application note, available on the internet at www.cypress.com.

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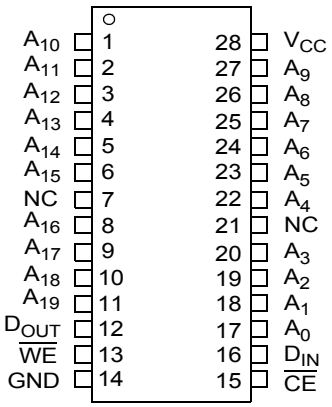
Pin Configuration [2]

SOJ
Top View



Selection Guide

	CY7C107D-10 CY7C1007D-10	Unit
Maximum access time	10	ns
Maximum operating current	80	mA
Maximum CMOS standby current, I_{SB2}	3	mA

Note
2. NC pins are not connected on the die.

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Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied..... –55 °C to +125 °C

Supply voltage on V_{CC} relative to GND [3] ... –0.5 V to +6.0 V

DC voltage applied to outputs in High-Z state [3]..... –0.5 V to V_{CC} + 0.5 V

DC input voltage [3] ..... –0.5 V to V_{CC} + 0.5 V

Current into outputs (LOW) ..... 20 mA

Static discharge voltage..... > 2001 V (per MIL-STD-883, Method 3015)

Latch-up current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}	Speed
Industrial	–40 °C to +85 °C	5 V ± 0.5 V	10 ns

Electrical Characteristics (Over the Operating Range)

Parameter	Description	Test Conditions		7C107D-10 7C1007D-10 Min	7C107D-10 7C1007D-10 Max	Unit
V_{OH}	Output HIGH voltage	I_{OH} = –4.0 mA		2.4	–	V
V_{OL}	Output LOW voltage	I_{OL} = 8.0 mA		–	0.4	V
V_{IH}	Input HIGH voltage			2.2	V_{CC} + 0.5	V
V_{IL}	Input LOW voltage [3]			–0.5	0.8	V
I_{IX}	Input leakage current	GND ≤ V_I ≤ V_{CC}		–1	+1	µA
I_{OZ}	Output leakage current	GND ≤ V_I ≤ V_{CC}, output disabled		–1	+1	µA
I_{CC}	V_{CC} operating supply current	V_{CC} = Max, I_{OUT} = 0 mA, f = f_{max} = $1/t_{RC}$	100 MHz	–	80	mA
			83 MHz	–	72	mA
			66 MHz	–	58	mA
			40 MHz	–	37	mA
I_{SB1}	Automatic $\overline{CE}$ Power-down current— TTL Inputs	Max V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{max}		–	10	mA
I_{SB2}	Automatic $\overline{CE}$ Power-down current— CMOS Inputs	Max V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3V, V_{IN} ≥ V_{CC} – 0.3V or V_{IN} ≤ 0.3V, f = 0		–	3	mA

Note
3. V_{IL} (min) = –2.0 V and V_{IH}(max) = V_{CC} + 1 V for pulse durations of less than 5 ns.

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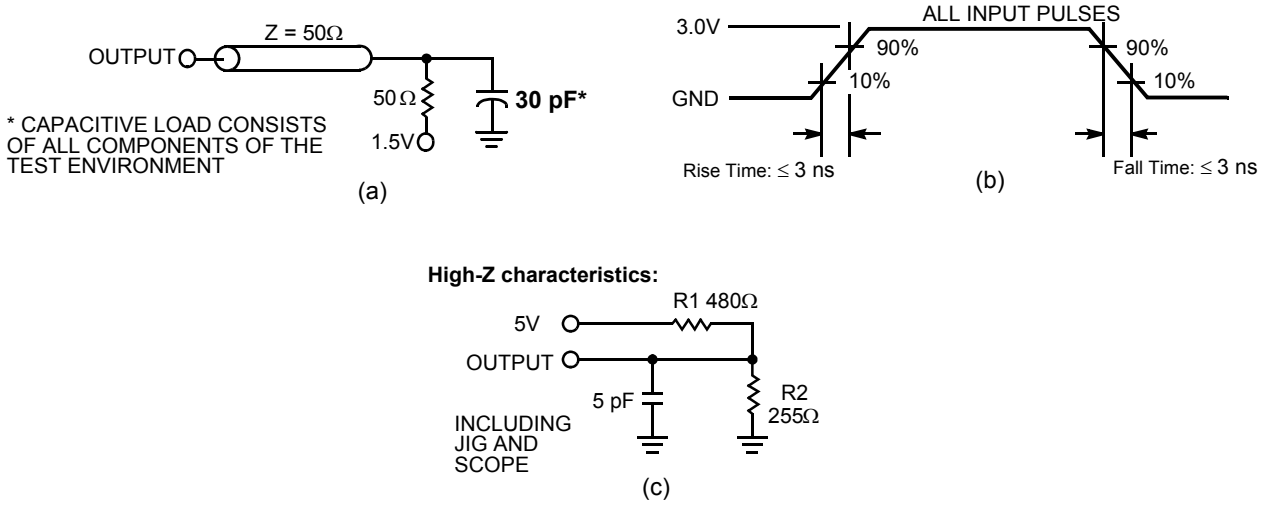
Capacitance [4]

Parameter	Description	Test Conditions	Max	Unit
C_{IN}: Addresses	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 5.0 V	7	pF
C_{IN}: Controls			10	pF
C_{OUT}	Output capacitance		10	pF

Thermal Resistance [4]

Parameter	Description	Test Conditions	300-Mil Wide SOJ	400-Mil Wide SOJ	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	59.16	58.76	°C/W
Θ_{JC}	Thermal resistance (junction to case)		40.84	40.54	°C/W

AC Test Loads and Waveforms [5]



Notes
4. Tested initially and after any design or process changes that may affect these parameters.
5. AC characteristics (except High-Z) are tested using the load conditions shown in Figure (a). High-Z characteristics are tested for all speeds using the test load shown in Figure (c).

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Switching Characteristics (Over the Operating Range) [6]

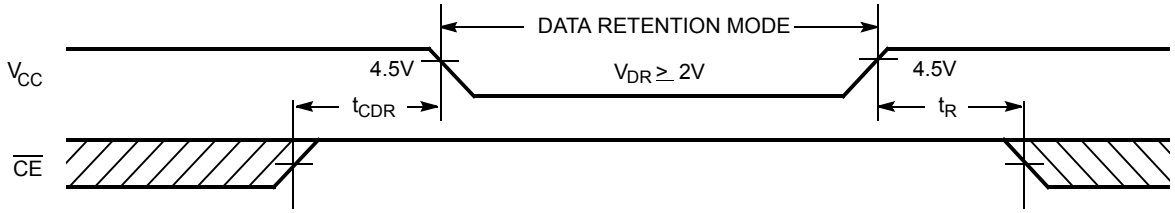
Parameter	Description	7C107D-10 7C1007D-10		Unit
		Min	Max	
Read Cycle				
t_{power} [7]	V_{CC}(typical) to the first access	100	–	µs
t_{RC}	Read cycle time	10	–	ns
t_{AA}	Address to data valid	–	10	ns
t_{OHA}	Data hold from address change	3		ns
t_{ACE}	$\overline{CE}$ LOW to data valid	–	10	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z [8]	3	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z [8, 9]	–	5	ns
t_{PU} [10]	$\overline{CE}$ LOW to power-up	0	–	ns
t_{PD} [10]	$\overline{CE}$ HIGH to power-down	–	10	ns
Write Cycle [11]				
t_{WC}	Write cycle time	10	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	7	–	ns
t_{AW}	Address set-up to write end	7	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address set-up to write start	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	7	–	ns
t_{SD}	Data set-up to write end	6	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z [8]	3	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High Z [8, 9]	–	6	ns

Notes
6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
7. t_{POWER} gives the minimum amount of time that the power supply should be at typical V_{CC} values until the first memory access can be performed.
8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} and t_{HZWE} is less than t_{LZWE} for any given device.
9. t_{HZCE} and t_{HZWE} are specified with a load capacitance of 5 pF as in part (c) of "AC Test Loads and Waveforms [5]" on page 5. Transition is measured when the outputs enter a high impedance state.
10. This parameter is guaranteed by design and is not tested.
11. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions	Min	Max	Unit
V_{DR}	V_{CC} for data retention		2.0	–	V
I_{CCDR}	Data retention current	$V_{CC} = V_{DR} = 2.0$ V, $\overline{CE} \geq V_{CC} - 0.3$ V, $V_{IN} \geq V_{CC} - 0.3$ V or $V_{IN} \leq 0.3$ V	–	3	mA
t_{CDR} [12]	Chip deselect to data retention time		0	–	ns
t_R [13]	Operation recovery time		t_{RC}	–	ns

Data Retention Waveform



Switching Waveforms

Figure 1. Read Cycle No. 1 (Address Transition Controlled) [14, 15]

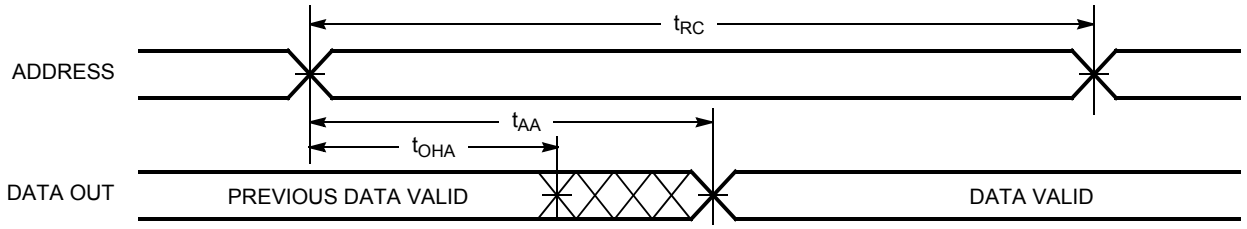
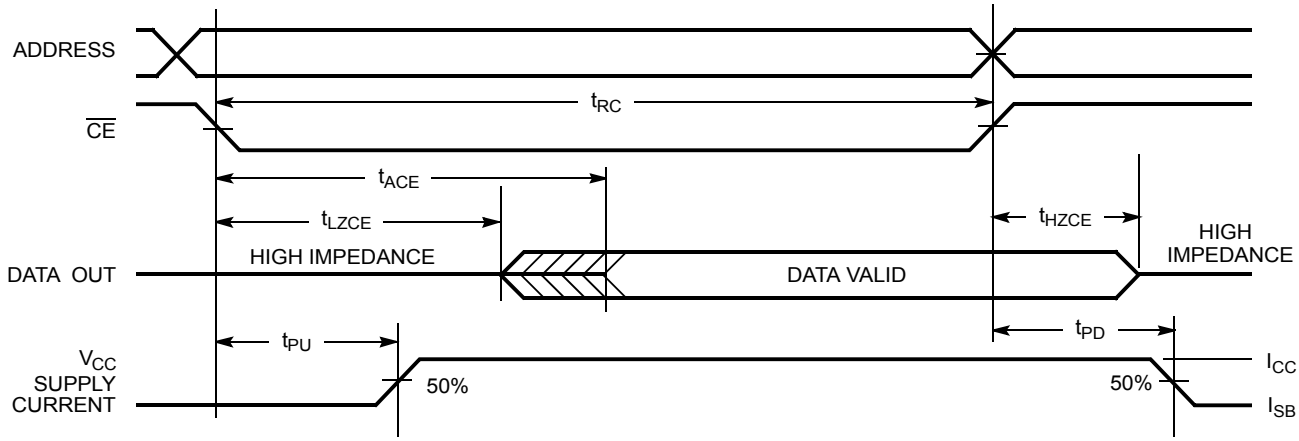


Figure 2. Read Cycle No. 2 [15, 16]



Notes
12. AC characteristics (except High-Z) are tested using the load conditions shown in Figure (a). High-Z characteristics are tested for all speeds using the test load shown in Figure (c)
13. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 50$ µs or stable at $V_{CC(min)} \geq 50$ µs.
14. Device is continuously selected, $\overline{CE} = V_{IL}$.
15. $\overline{WE}$ is HIGH for read cycle.
16. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

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Switching Waveforms(continued)

Figure 3. Write Cycle No. 1 ($\overline{CE}$ Controlled) [17]

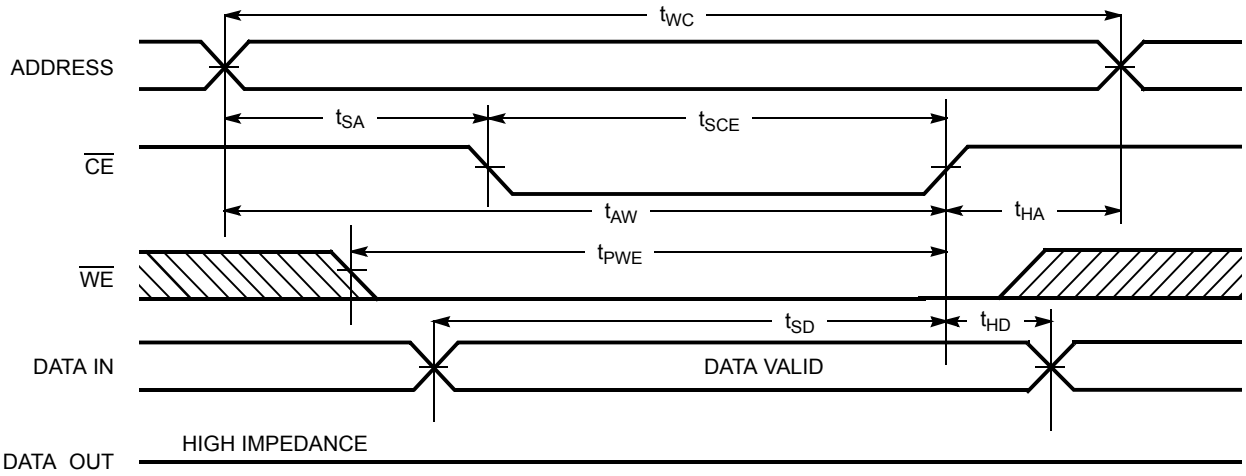
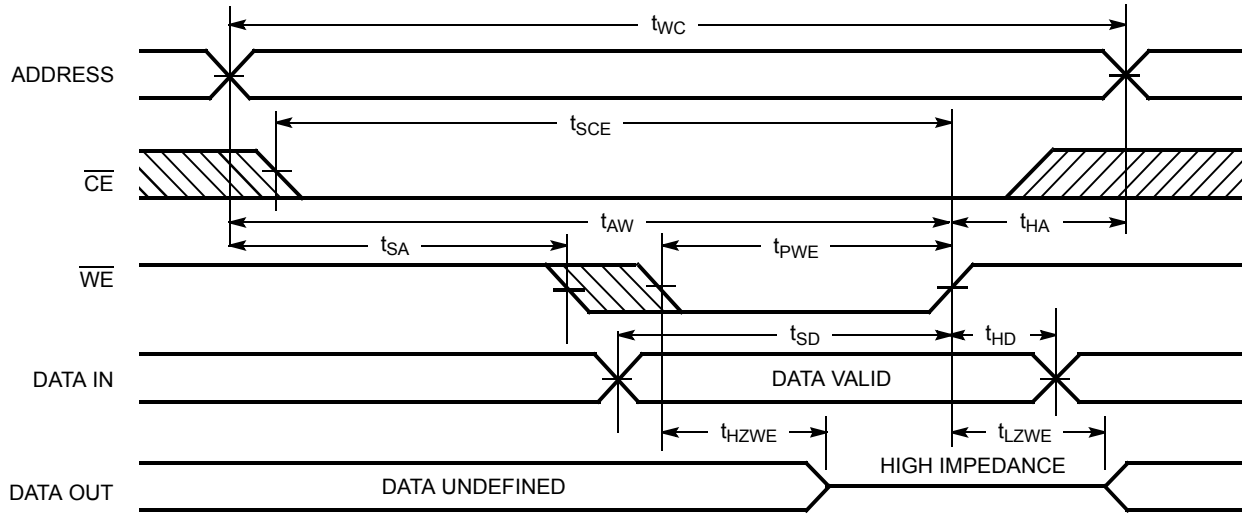


Figure 4. Write Cycle No. 2 ($\overline{WE}$ Controlled) [17]



Truth Table

$\overline{CE}$	$\overline{WE}$	D_{OUT}	Mode	Power
H	X	High Z	Power-down	Standby (I_{SB})
L	H	Data out	Read	Active (I_{CC})
L	L	High Z	Write	Active (I_{CC})

Note
17. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.

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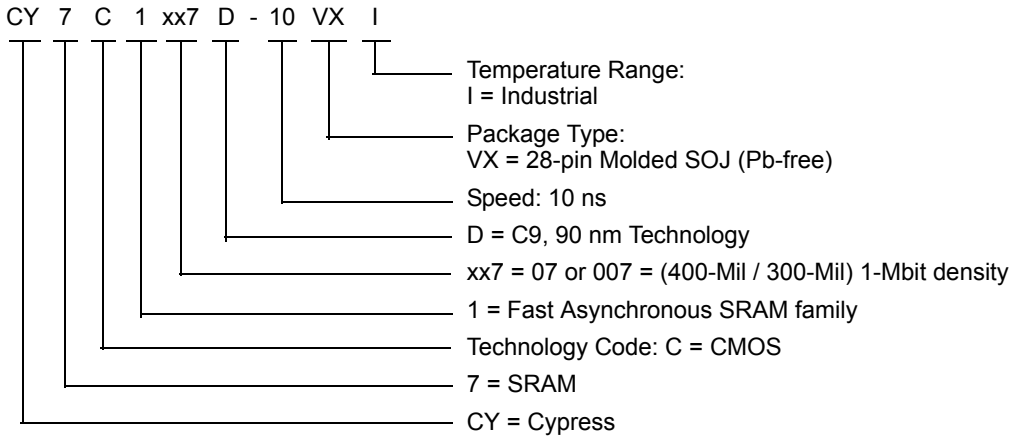
Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C107D-10VXI	51-85032	28-pin (400-Mil) Molded SOJ (Pb-free)	Industrial
	CY7C1007D-10VXI	51-85031	28-pin (300-Mil) Molded SOJ (Pb-free)	

Ordering Code Definitions



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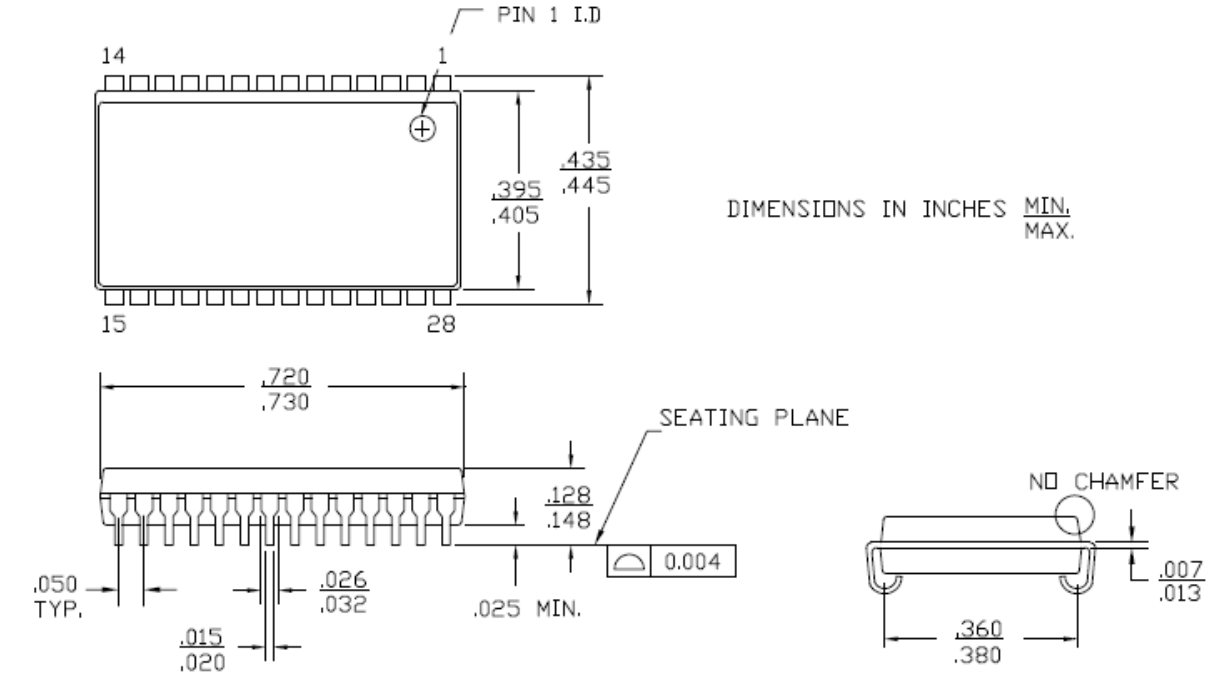
Package Diagrams

Figure 5. 28-pin (400-Mil) Molded SOJ, 51-85032



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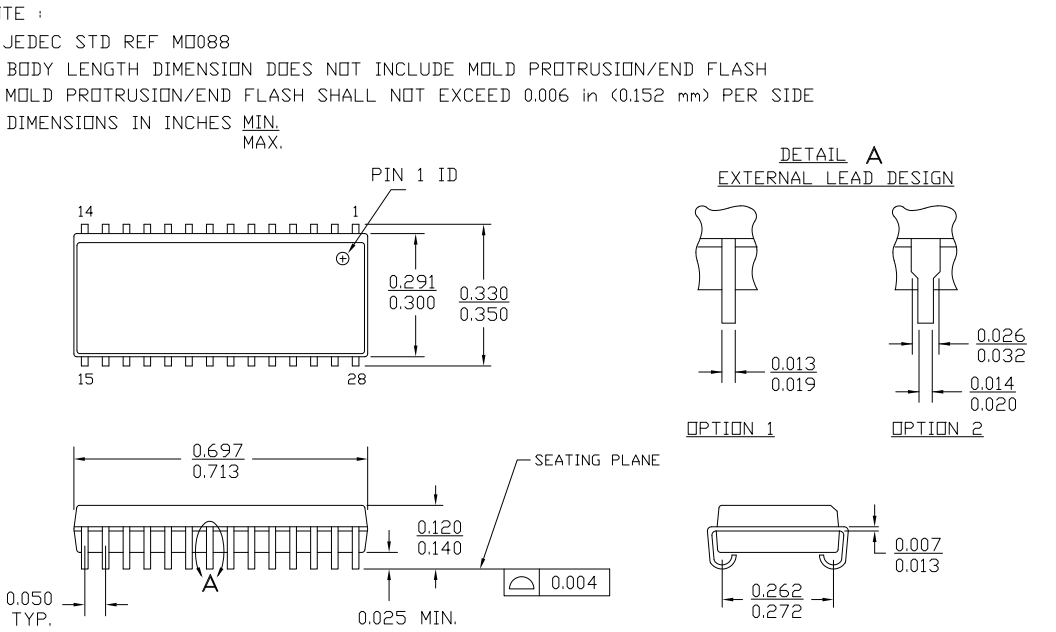
Package Diagrams(continued)

Figure 6. 28-pin (300-Mil) Molded SOJ, 51-85031



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Acronyms

Acronym	Description
BGA	ball grid array
CMOS	complementary metal oxide semiconductor
FBGA	very fine ball gird array
I/O	input/output
JTAG	joint test action group
SRAM	static random access memory
TTL	Transistor transistor logic

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
µA	microamperes
mA	milliampere
MHz	megahertz
ns	nanoseconds
pF	picofarads
V	volts
Ω	ohms
W	watts

Document History Page

Document Title: CY7C107D/CY7C1007D, 1-Mbit (1M x 1) Static RAM Document Number: 38-05469				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	201560	See ECN	SWI	Advance Information data sheet for C9 IPP
*A	233722	See ECN	RKF	DC parameters modified as per EROS (Spec # 01-02165) Pb-free offering in Ordering Information
*B	263769	See ECN	RKF	Added Data Retention Characteristics table Added T_{power} Spec in Switching Characteristics Table Shaded Ordering Information
*C	307601	See ECN	RKF	Reduced Speed bins to –10 and –12 ns
*D	560995	See ECN	VKN	Converted from Preliminary to Final Removed Commercial Operating range Removed 12 ns speed bin Added I_{CC} values for the frequencies 83MHz, 66MHz and 40MHz Updated Thermal Resistance table Updated Ordering Information Table Changed Overshoot spec from V_{CC}+2V to V_{CC}+1V in footnote #3
*E	802877	See ECN	VKN	Changed I_{CC} specs from 60 mA to 80 mA for 100MHz, 55 mA to 72 mA for 83MHz, 45 mA to 58 mA for 66MHz, 30 mA to 37 mA for 40MHz
*F	2898399	03/24/2010	AJU	Updated Package Diagrams
*G	3104943	12/08/2010	AJU	Added Ordering Code Definitions.
*H	3218989	04/07/2011	PRAS	Added TOC Added Acrnyms and Units of Measure table. Updated Package diagrams from *C to *D (51-85032)

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