

ADS5102/3 EVM

User's Guide

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

EVM IMPORTANT NOTICE

Texas Instruments (TI) provides the enclosed product(s) under the following conditions:

This evaluation kit being sold by TI is intended for use for **ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY** and is not considered by TI to be fit for commercial use. As such, the goods being provided may not be complete in terms of required design-, marketing-, and/or manufacturing-related protective considerations, including product safety measures typically found in the end product incorporating the goods. As a prototype, this product does not fall within the scope of the European Union directive on electromagnetic compatibility and therefore may not meet the technical requirements of the directive.

Should this evaluation kit not meet the specifications indicated in the EVM User's Guide, the kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE.

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods. Please be aware that the products received may not be regulatory compliant or agency certified (FCC, UL, CE, etc.). Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge.

EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

TI currently deals with a variety of customers for products, and therefore our arrangement with the user **is not exclusive**.

TI assumes **no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein**.

Please read the EVM User's Guide and, specifically, the EVM Warnings and Restrictions notice in the EVM User's Guide prior to handling the product. This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact the TI application engineer.

Persons handling the product must have electronics training and observe good laboratory practice standards.

No license is granted under any patent right or other intellectual property right of TI covering or relating to any machine, process, or combination in which such TI products or services might be or are used.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the specified input and output ranges as described in the EVM user's guide.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

Preface

Read This First

About This Manual

This user's guide is to assist the user with the operation of the EVM using the ADS5102/3 devices.

How to Use This Manual

This document contains the following chapters:

- ☐ Chapter 1—Overview
- ☐ Chapter 2—Physical Description
- ☐ Chapter 3—Circuit Description

Information About Cautions and Warnings

This book may contain cautions and warnings.

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software or equipment.

This is an example of a warning statement.

A warning statement describes a situation that could potentially cause harm to you.

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

FCC Warning

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

Contents

1	Overview	1-1
1.1	Purpose	1-2
1.2	EVM Basic Functions	1-2
1.3	Power Requirements	1-2
1.4	ADS5102/3 EVM Operational Procedure	1-3
2	Physical Description	2-1
2.1	PCB Layout	2-2
2.2	Bill of Materials	2-5
3	Circuit Description	3-1
3.1	Circuit Function	3-2
3.1.1	Analog Inputs	3-2
3.1.2	External Reference Inputs	3-2
3.1.3	Clock Inputs	3-3
3.1.4	Control Inputs	3-3
3.1.5	Power	3-3
3.1.6	Outputs	3-3
3.2	Schematic Diagram	3-4

Figures

2-1	Top Layer	2-2
2-2	Inner Layer 1, Ground Plane	2-3
2-3	Inner Layer 2, Power Plane	2-4
2-4	Bottom Layer	2-5

Tables

1-1	Two Pin Jumper List	1-3
1-2	Three Pin Jumper List	1-3
2-1	Bill of Materials	2-5
3-1	Reference Voltage Adjustment Ranges	3-2
3-2	Output Connector J15	3-4

Notes, Cautions, and Warnings

Voltage Limits	1-2
----------------------	-----

Overview

This user's guide gives a general overview of the ADS5102/3 evaluation module (EVM) and provides a general description of the features and functions to be considered while using this module.

Topic	Page
1.1 Purpose	1-2
1.2 EVM Basic Functions	1-2
1.3 Power Requirements	1-2
1.4 ADS5102/3 EVM Operational Procedure	1-3

1.1 Purpose

The ADS5102/3 EVM provides a platform for evaluating the ADS5102/3 analog-to-digital converter (ADC) under various signal, reference, and supply conditions. Use this document in combination with the EVM schematic diagram supplied.

1.2 EVM Basic Functions

Analog input to the ADC is provided via two external SMA connectors. The single-ended input the user provides is converted into a differential signal at the input of the device. One input uses a differential amplifier, while the other input is transformer coupled.

The EVM provides an external SMA connection for input of the ADC clock. The user can send this clock to the output connector with the digital data or provide a second clock source to be sent in place of the ADC clock. This allows the user to provide the required setup and hold times of the output data with respect to the output clock. See the *Clock Inputs* section for the proper configuration and operation.

Digital output from the EVM is via a 40-pin connector. The digital lines from the ADC are buffered before going to this connector. More information on this connector can be found in the ADC output section.

Power connections to the EVM are via banana jack sockets. Separate sockets are provided for the analog and digital supply.

In addition to the internal reference provided by the ADS5102/3 device, options are provided on the EVM to allow adjustment of the ADC references via an onboard reference circuit. A precision voltage reference source, a resistor network, and an operational amplifier (op amp) provide the ADS5102/3 device reference voltages REFT and REFB.

1.3 Power Requirements

The EVM can be powered directly with a single 1.8-V supply if using the module with transformer coupled input, internal reference source, and 1.8-V logic outputs.

A voltage of 3.3 V is required for the DRVDD power input to provide 3.3-V logic outputs. A voltage of ± 5 V is required if using external references and/or differential amplifier input. Provision has also been made to allow the EVM to be powered with independent 1.8-V analog and digital supplies to provide higher performance.

Voltage Limits

Exceeding the maximum input voltages can damage EVM components. Undervoltage may cause improper operation of some or all of the EVM components.

1.4 ADS5102/3 EVM Operational Procedure

The ADS5102/3 EVM provides a flexible means of evaluating the ADS5102/3 in a number of modes of operation. A basic setup procedure that can be used as a board confidence check is as follows:

- 1) Verify all jumper settings against the schematic jumper list in Table 1–1 and Table 1–2:

Table 1–1. Two Pin Jumper List

Jumper	Function	Installed	Removed	Default
W10	External REFT feed	External	Internal	Removed
W11	External REFB feed	External	Internal	Removed
R39	Positive analog input	Transformer coupled	No connection	Installed
R37	Negative analog input	Transformer coupled	No connection	Installed
R38	Positive analog input	Differential amplifier	No connection	Removed
R36	Negative analog input	Differential amplifier	No connection	Removed
R43, R44	Output clock option	ADC clock at output connector	Buff clock at output connector	Removed
R42	Optional output clock parallel termination	Provides pullup termination	No pullup termination	Removed
R14	Optional ADC clock parallel termination	Provides pullup termination	No pullup termination	Removed

Table 1–2. Three Pin Jumper List

Jumper	Function	Location: Pins 1–2	Location: Pins 2–3	Default
W1	Band gap input voltage (power down reference mode)	REFT voltage to bandgap pin	1.25 V to bandgap pin	Removed
W3	Transformer and diff amp common mode select	ADC output common mode voltage	External common mode voltage	1–2
W4	Power down select	Operate mode	Power down mode	1–2
W5	Output enable select	Data bus tristate	Data bus enable	2–3
W6	Reference select	External reference	Internal reference	2–3

- 2) Connect supplies to the EVM as follows:

- 1.8-V analog supply to J6 and return to J5
- 1.8-V digital supply to J9 and return to J10
- 3.3-V driver supply to J13 and return to J14
- 5-V analog supply to J7 and return to J8
- –5-V analog supply to J11 and return to J8

- 3) Switch power supplies on.
- 4) Use a function generator with 50- Ω output to input a 40-MHz, 1.5-V offset, 3-V_(p-p) amplitude square wave signal into J3 to be used as the ADC clock.

Note:

The frequency of the clock must be within the specification for the device speed grade.

- 5) Use a function generator with 50- Ω output to input a 1.5-V offset, 3-V_(p-p) amplitude square wave signal into J4 to be used as the buffered output clock.

Note:

This signal must be the same frequency and synchronized with the ADC clock.

- 6) Use a frequency generator with 50- Ω output to input a 1.5-MHz, 0-V offset, 0.4-V_(p-p) amplitude sine wave signal into J2. This provides a transformer coupled differential signal to the ADC.
- 7) The digital pattern on the output connector J15 now represents a sine wave and can be monitored using a logic analyzer.

Physical Description

This chapter describes the physical characteristics and PCB layout of the EVM and lists the components used on the module.

Topic	Page
2.1 PCB Layout	2-2
2.2 Bill of Materials	2-5

2.1 PCB Layout

The EVM is constructed on a 4-layer, 104 mm (4.1 inch) x 114 mm (4.5 inch) x 1,57 mm (0.062 inch) thick PCB using FR-4 material. Figure 2–1 through Figure 2–4 show the individual layers.

Figure 2–1. Top Layer

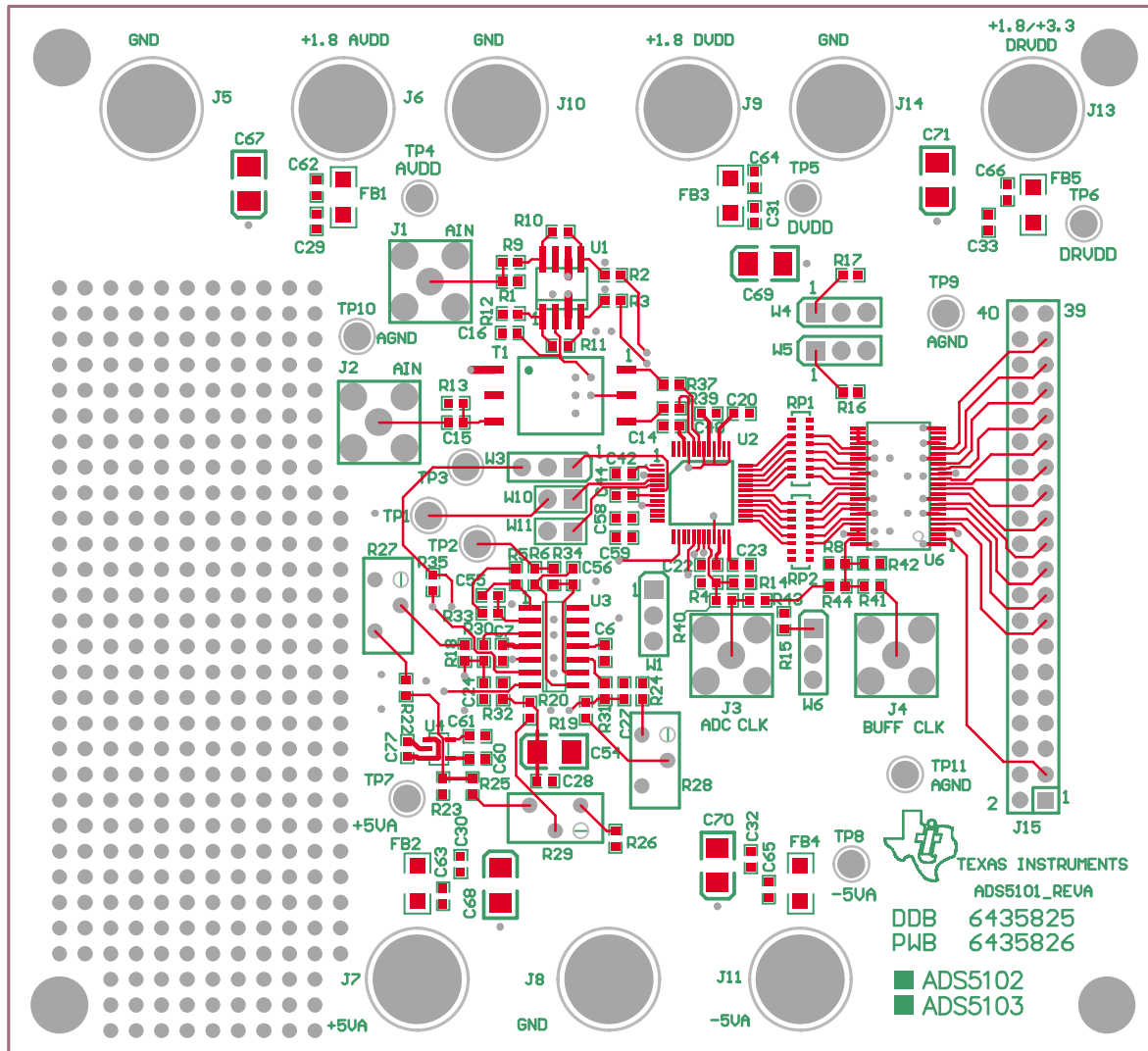


Figure 2–2. Inner Layer 1, Ground Plane

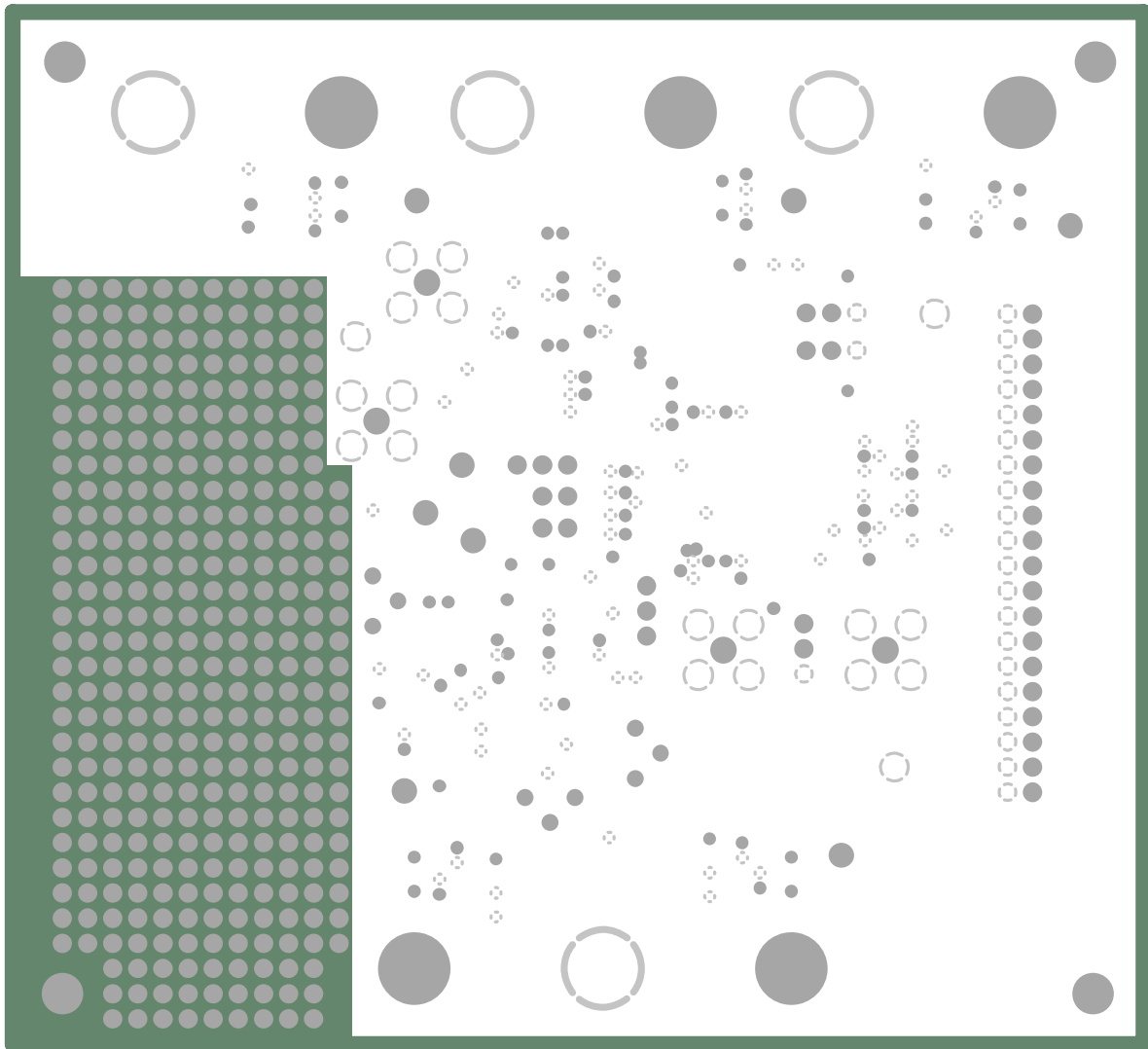


Figure 2–3. Inner Layer 2, Power Plane

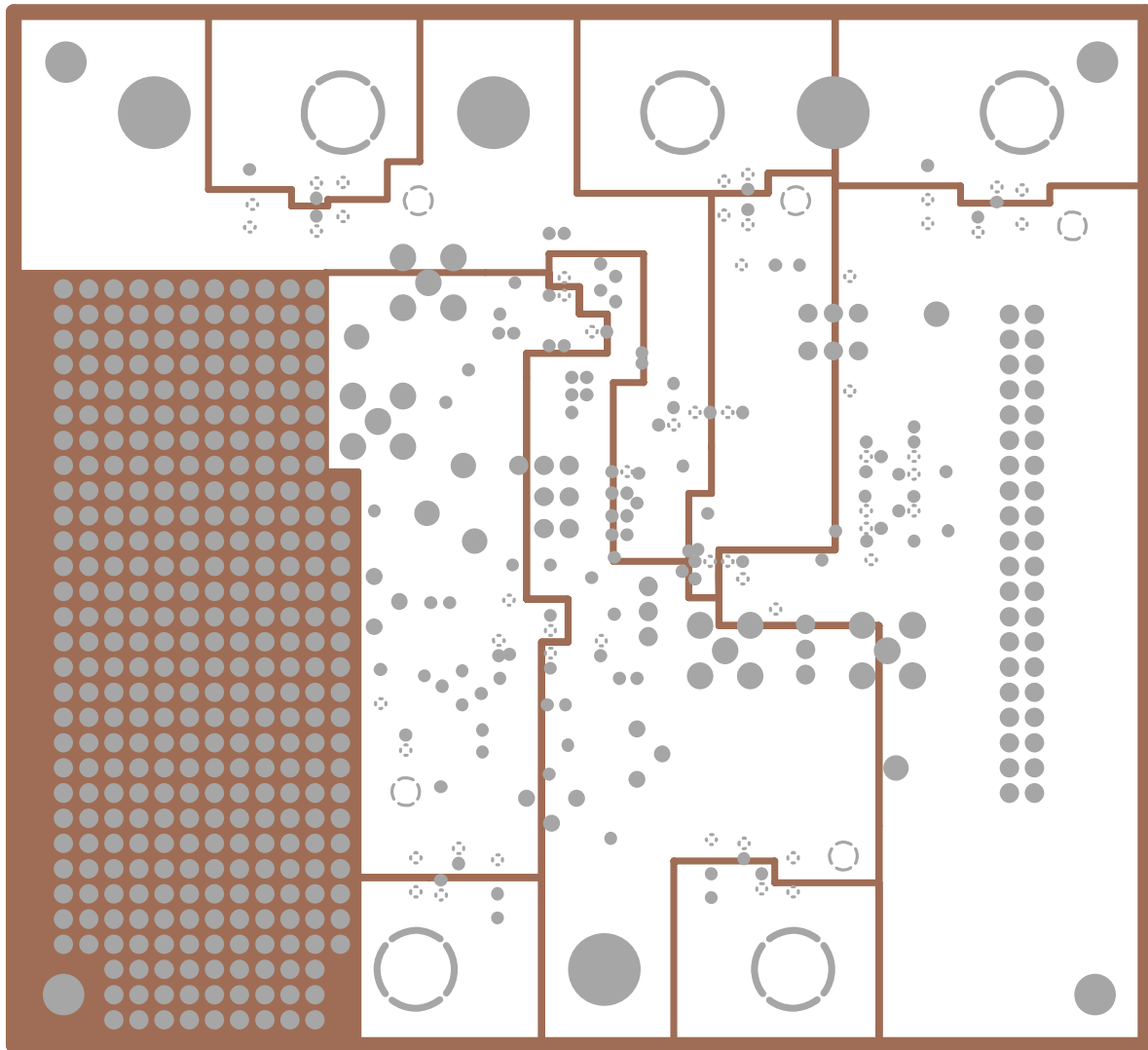
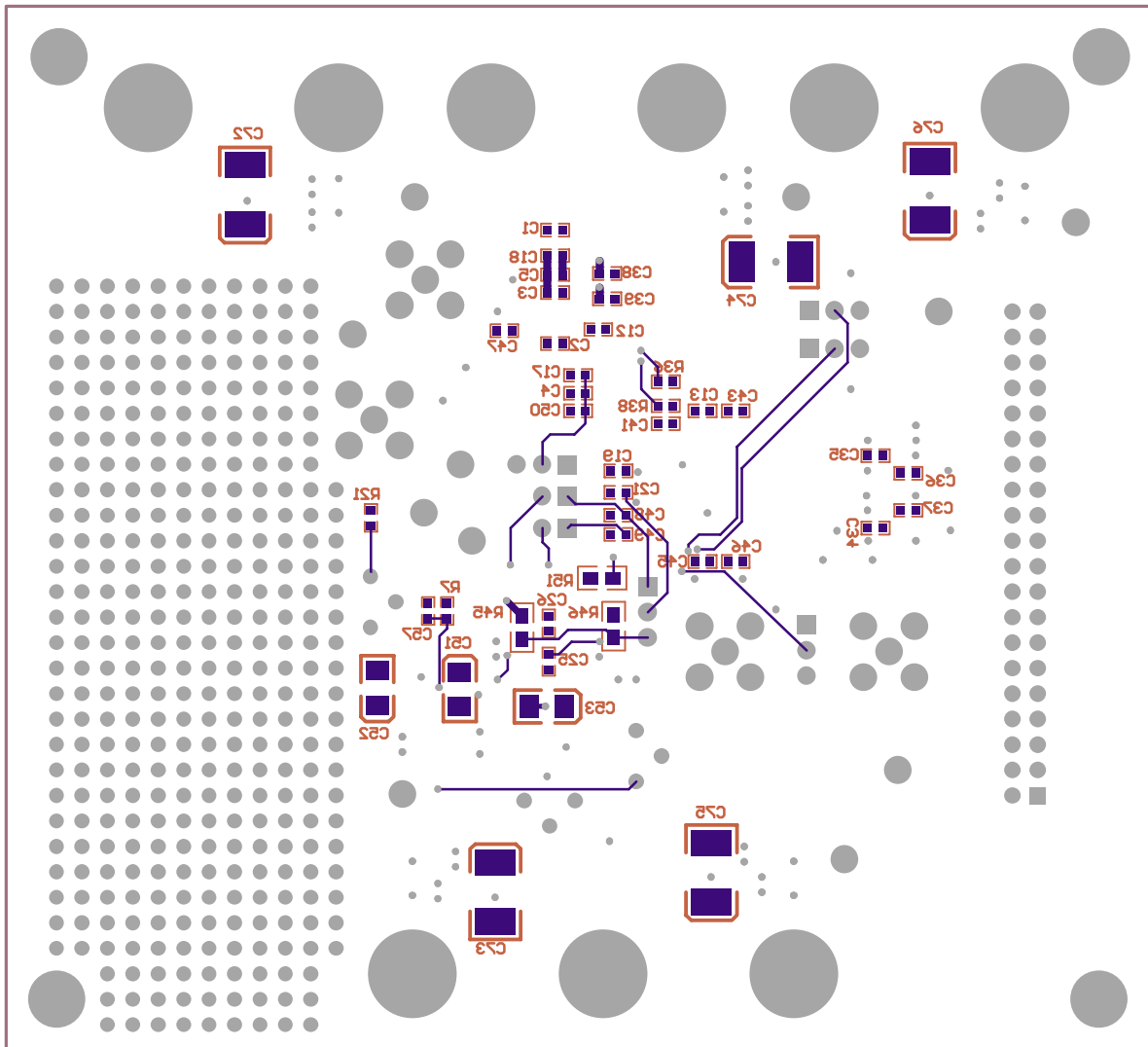


Figure 2–4. Bottom Layer



2.2 Bill of Materials

Table 2–1 lists the parts used in constructing the EVM.

Table 2–1. Bill of Materials

Description	QTY	Part Number	MFG.	REF DES
47 μ F, tantalum, 10%, 10 V	5	10TPA47M	SANYO	C72–C76
0.1 μ F, 16 V, 10% capacitor	31	ECJ–1VB1C104K	Panasonic	C12–C37, C62–C66
10 μ F, 10 V, 10% capacitor	9	GRM42X5R106K10	Murata	C51–C54, C67–C71
0.01 μ F, 50 V, 10% capacitor	4		AVX	C47–C49 C60
1.0 μ F, 10 V, 10% capacitor	10		AVX	C40–C46, C58, C59, C77
22 pF, 50 V, 5%, capacitor	2	06035A220JAT2A	AVX	C38, C39
0.001 μ F, 16 V, 10% capacitor	1			C50
0.047 μ F, 16 V, 10% capacitor	3			C55–C57
1.8 pF, 16 V, 10% capacitor	2			C1, C2

Table 2–1. Bill of Materials (Continued)

Description	Qty.	Part Number	Mfg.	Ref. Des.
470 pF, 16 V, 10% capacitor	5			C3–C7
2.2 μ F, 16 V, 10% capacitor	1			C61
Ferrite bead	5			FB1–FB5
499- Ω resistor, 1/16 W, 1%	3	ERJ-3EKF499R0V	Panasonic	R9–R11
523- Ω resistor, 1/16 W, 1%	1	ERJ-3EKF523R0V	Panasonic	R12
49.9- Ω resistor, 1/16 W, 1%	9	ERJ-3EKF49R9V	Panasonic	R1–R8, R13
1-k Ω resistor, 1/16 W, 1%	2			R21, R22
2.49-k Ω resistor, 1/16 W, 1%	1			R23
475- Ω resistor, 1/16 W, 1%	2			R24, R26
953- Ω resistor, 1/16 W, 1%	1			R25
2-k Ω resistor, 1/16 W, 1%	3			R33–R35
10-k Ω resistor, 1/16 W, 1%	6			R15–R20
100- Ω resistor, 1/16 W, 1%	3			R30–R32
0- Ω resistor, 1/16 W, 1%	4	ERJ-3EKF0R00V	Panasonic	R37–R41
				NOT INSTALLED: R14, R36, R38, R42–R44
1-k Ω resistor, 1/16 W, 1%	1		Panasonic	R46
100-k Ω resistor, 1/16 W, 1%	1	P100KHCT–ND	Panasonic	R47
3.01-k Ω resistor, 1/16 W, 1%	1		Panasonic	R45
9.53-k Ω resistor, 1/16 W, 1%	1	ERJ-6GEY0R00V	Panasonic	R51
1K Pot	3	3296Y–102	Bourns	R27–R29
Transformer	1	T1–1T–KK81	Mini-Circuits	T1
SMA connectors	4	2262–0000–09	Macom	J1–J4
Black test point	3	5011K	Keystone	TP9–TP11
Red test point	8	5000K	Keystone	TP1–TP8
2POS_header	2	TSW–150–07–L–S	Samtec	W10, W11
3POS_header	5	TSW–150–07–L–S	Samtec	W1, W3–W6
2-circuit jumpers	6	863–3285	Allied (molex)	
40-pin header	1	TSW–120–07–L–D	Samtec	J15
Red banana jacks	5	ST–351A	ALLIED	J6, J7, J9, J1, J13
Black banana jacks	4	ST351B	ALLIED	J5, J8, J10, J14
ADS51002/3	1	ADS5102/3	TI	U2
TPS79225	1	TPS79225DBVT	TI	U4
24- Ω R-Pack	2	742C163101JCT	Bourns	RP1, RP2
SN74AVC16244	1	SN74AVC16244DGGR	TI	U6
THS4141	1	THS4141ID	TI	U1
OPA4227	1	OPA4227UA	TI	U3
Stand off hex (1/4 x 1")	4	219–2063	Allied	

Circuit Description

This chapter describes the circuit function and shows the schematic for the EVM.

Topic	Page
3.1 Circuit Function	3-2
3.2 Schematic Diagram	3-4

3.1 Circuit Function

The following paragraphs describe the function of the individual circuits. See the data sheet for device operating characteristics.

3.1.1 Analog Inputs

The ADC has either transformer-coupled inputs or differential-amplifier inputs from a single-ended source. The inputs are provided via the SMA connectors J1 and J2 on the EVM, which must be configured as follows:

- ☐ For a differential amplifier input to the ADC, a single ended source is connected to J1. R36 and R38 must be installed, and R37 and R39 must be removed. The input has a 50- Ω terminator.
- ☐ For a 1:1 transformer coupled input to the ADC, a single ended source is connected to J2. R36 and R38 must be removed, and R37 and R39 must be installed. The input is ac-coupled and has a 50- Ω terminator.

3.1.2 External Reference Inputs

In addition to being able to use the internal reference of the ADC, a reference circuit has been included on the EVM. This circuit uses a precision 2.5-V, low-noise linear regulator as the primary source, and allows adjustment of the REFT and REFB signals to the ADC using potentiometers R27 and R28, respectively. A third source, CML, is also generated to provide an adjustable common mode voltage to be used by the transformer and differential amplifier during external reference operation. CML is adjusted by potentiometer R29. In order to use the ADC with external references, install jumpers W10 and W11, install jumper W3 between pins 2 and 3, jumper W6 between pins 1 and 2, and jumper W1 between pins 1 and 2. If REFT is set to any voltage other than 1.25 V, jumper W1 must be installed between pins 2 and 3 for optimal ADC performance. The ranges of the external reference signals are shown in Table 3–1.

Table 3–1. Reference Voltage Adjustment Ranges

Signal	Minimum Voltage	Typical Voltage	Maximum Voltage
REFT	0.9	1.25	1.6
REFB	0.3	0.75	0.9
CML	0.5	1.0	1.25

3.1.3 Clock Inputs

The EVM provides separate inputs for the ADC clock and output buffer clock. This allows the user to send a modified version of the ADC clock (inverted, delayed, etc.) with the output data to generate the required setup and hold times for the user interface. The ADC clock input is SMA connector J3 and has provisions for serial and/or parallel termination. The buffered output clock input is SMA connector J4 and has provisions for serial and/or parallel termination. The clock inputs must be 50- Ω square wave signals, 1.8-V or 3.3-V referenced to ground, with a duty cycle of 50 $\pm$ 5%. The EVM can operate with only one clock input by installing R43 and R44, and removing R41 and R8 to prevent double termination.

3.1.4 Control Inputs

The ADC has three discrete inputs to control the operation of the device.

3.1.4.1 Standby

With jumper W4 installed between pins 2 and 3, the ADC is in power-down mode. The device is in operate mode with jumper W4 installed between pin 1 and pin 2.

3.1.4.2 Output Enable

With jumper W5 installed between pins 1 and 2, the ADC data outputs are in a 3-state mode. The data outputs are enabled with jumper W5 installed between pins 2 and 3.

3.1.4.3 Power Down Reference

With jumper W6 installed between pins 1 and 2, the ADC internal reference is disabled and the device is in external reference mode. The ADC is in internal reference mode with jumper W6 installed between pins 2 and 3.

3.1.5 Power

Power is supplied to the EVM via banana jack sockets. A separate connection is provided for a 1.8-V analog supply (J6 and J5), a 1.8-V digital supply (J9 and J10), a 1.8/3.3-V digital driver supply (J13 and J14), and a $\pm$ 5-V analog supply (J7, J8, and J11).

3.1.6 Outputs

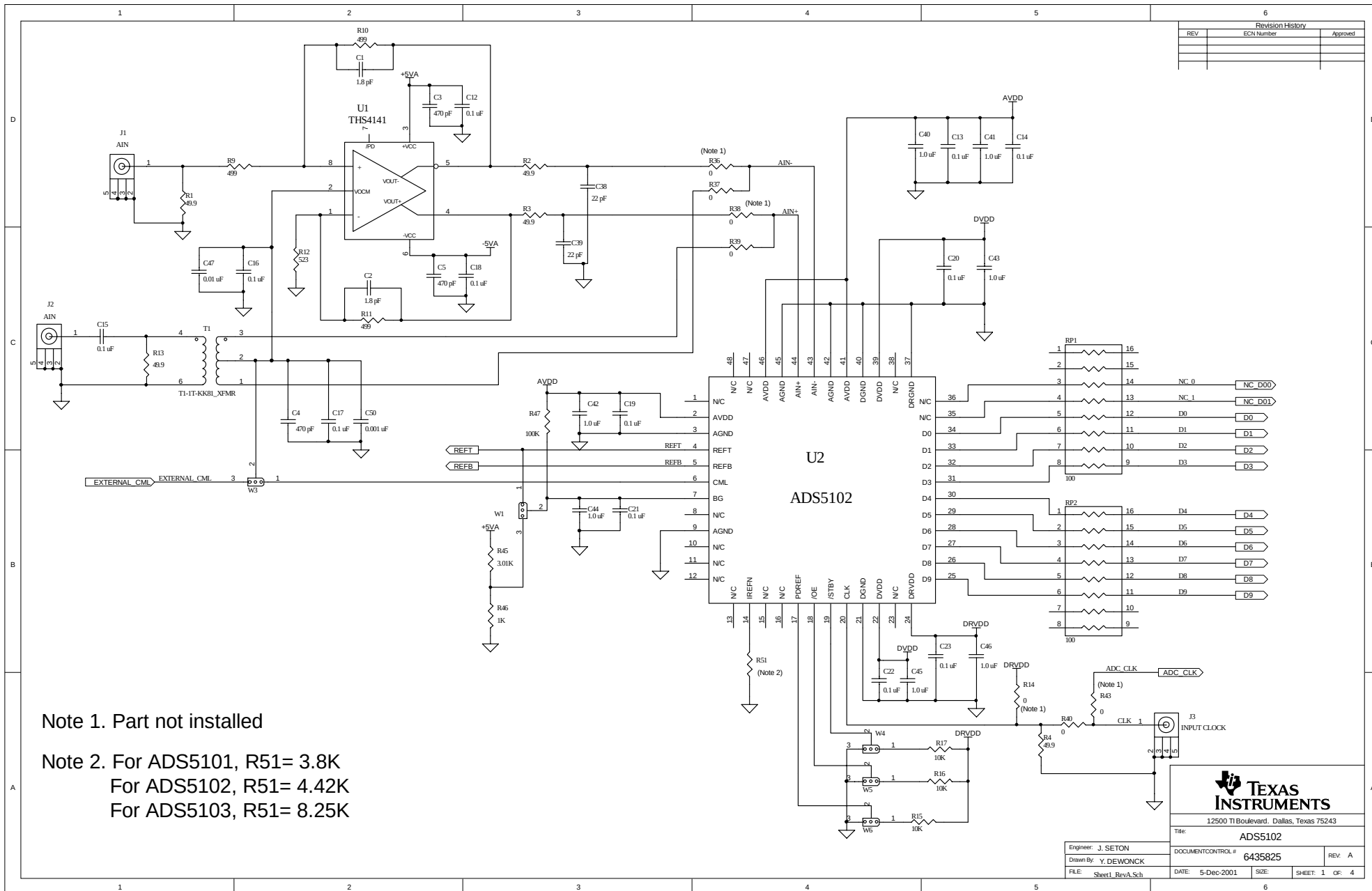
The data outputs from the ADC are buffered using a SN74AVC16244 before going to header J15. The ADC and output buffer can provide 1.8-V or 3.3-V output levels. The voltage placed at the driver power inputs (J13 and J14) selects this. J15 is a standard 40-pin header on a 100-mil grid, and allows easy connection to a logic analyzer. The connector pin out is listed in Table 3–2.

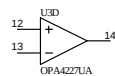
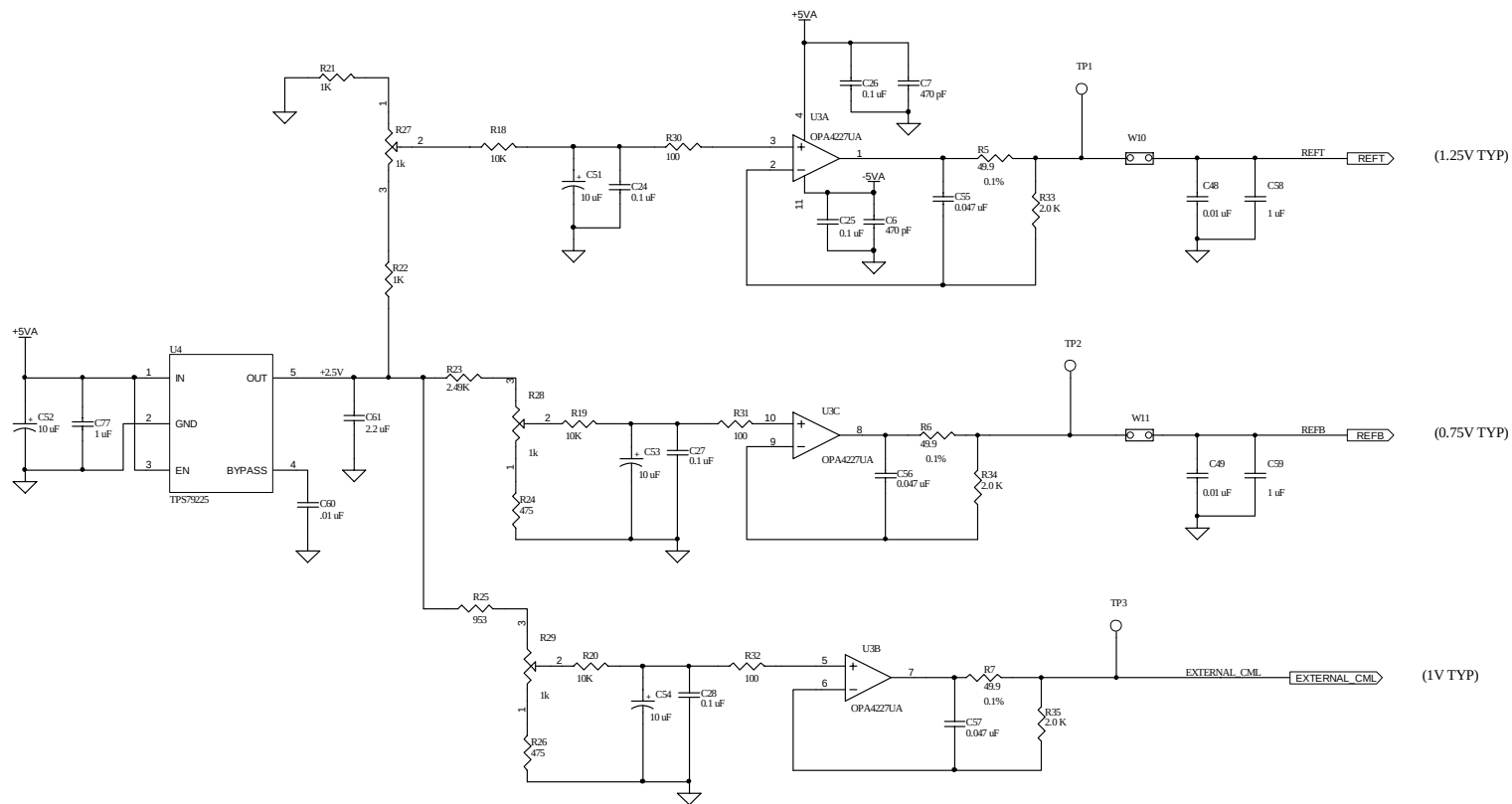
Table 3–2. Output Connector J15

J15 Pin	Description	J15 Pin	Description
1	NC	21	Data Bit 6
2	GND	22	GND
3	Output clock	23	Data Bit 5
4	GND	24	GND
5	NC	25	Data Bit 4
6	GND	26	GND
7	NC	27	Data Bit 3
8	GND	28	GND
9	NC	29	Data Bit 2
10	GND	30	GND
11	NC	31	Data Bit 1
12	GND	32	GND
13	NC	33	Data Bit 0 (MSB)
14	GND	34	GND
15	Data Bit 9 (MSB)	35	NC
16	GND	36	GND
17	Data Bit 8	37	NC
18	GND	38	GND
19	Data Bit 7	39	NC
20	GND	40	GND

3.2 Schematic Diagram

The following figures show the schematic diagram for the EVM.



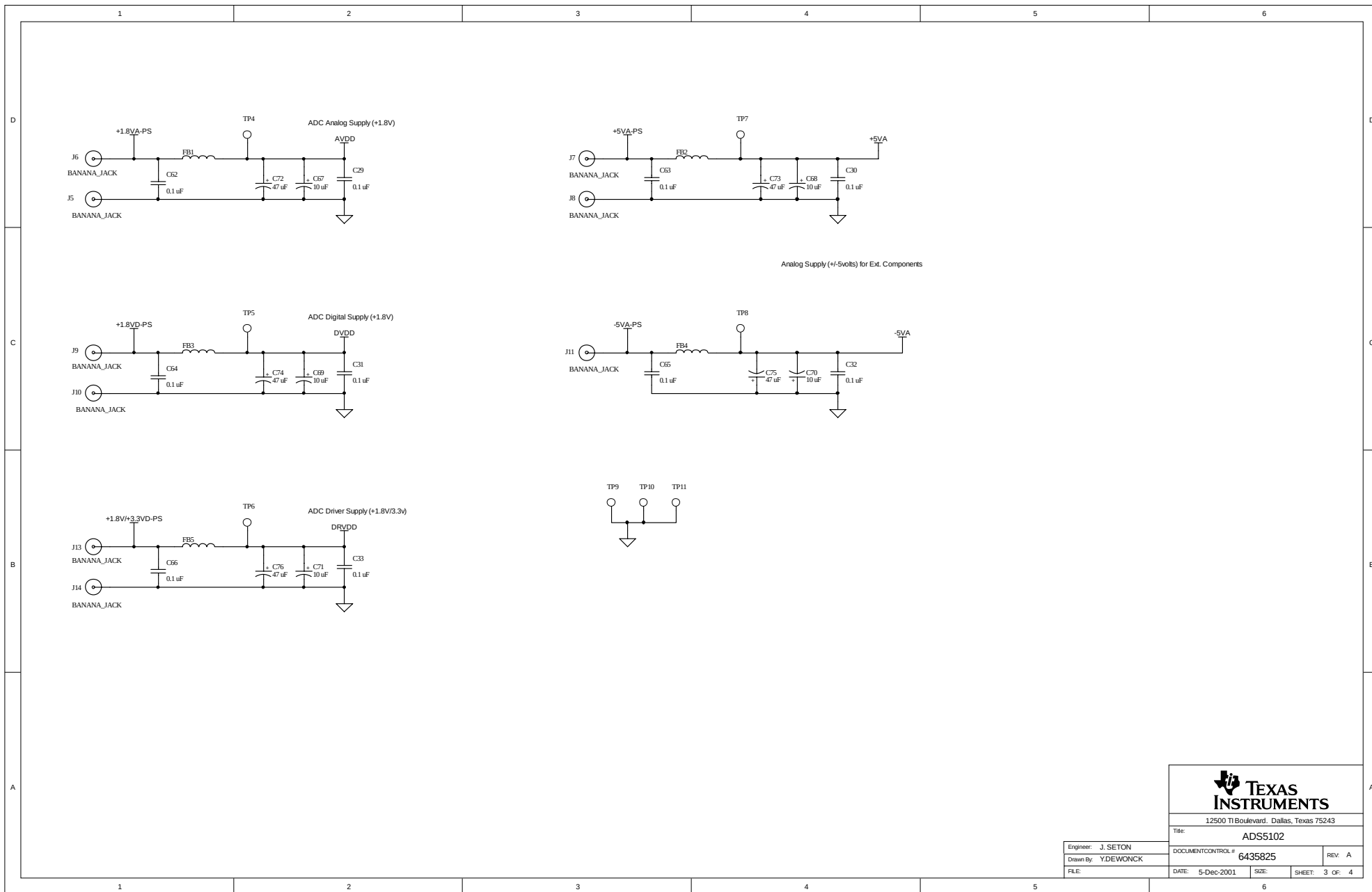


12500 TI Boulevard, Dallas, Texas 75243

Title:		ADS5102	
DOCUMENT CONTROL #		6435825	
DATE:		5-Dec-2001	SIZE: SHEET: 2 OF: 4

Engineer: J. SETON
Drawn By: Y.DEWONCK
FILE:

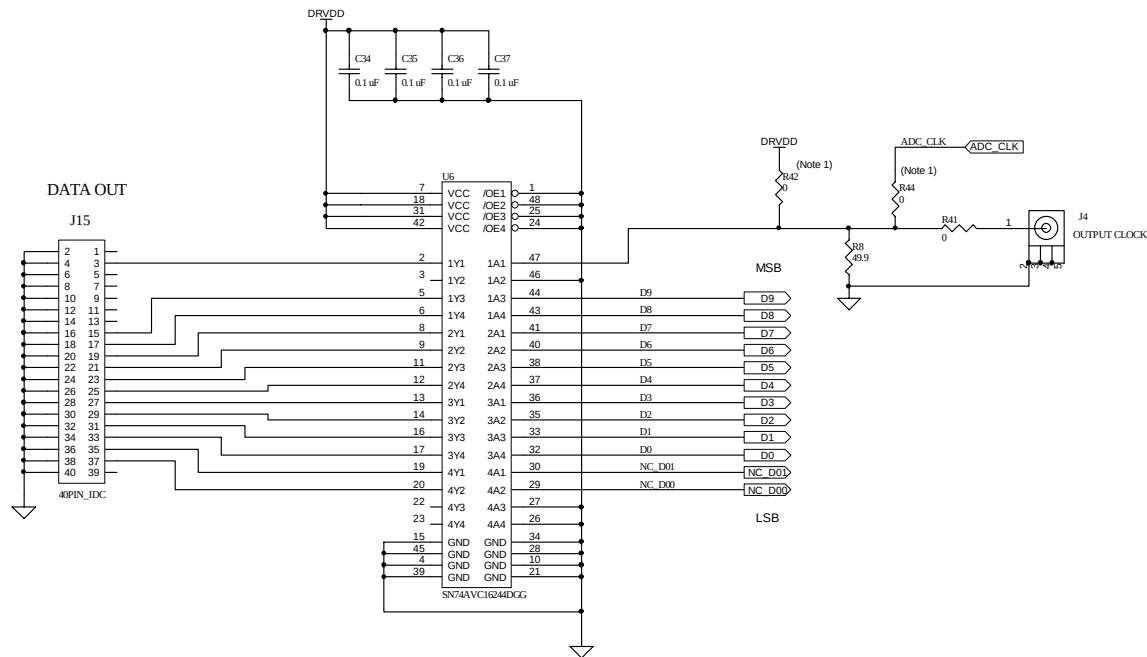
REV. A



12500 TI Boulevard, Dallas, Texas 75243

Title:		ADS5102	
DOCUMENT CONTROL #		6435825	REV. A
DATE:	5-Dec-2001	SIZE:	SHEET: 3 OF 4

Engineer:	J. SETON
Drawn By:	YDEWONCK
FILE:	



Note 1. Part not installed

Title: ADS5102			
12500 TI Boulevard, Dallas, Texas 75243			
Engineer: J. SETON Drawn By: Y. DEWONCK FILE:	DOCUMENT CONTROL # 6435825	REV. A	DATE: 5-Dec-2001 SIZE: 4 SHEET: 4 OF 4



**Стандарт
Электрон
Связь**

Мы молодая и активно развивающаяся компания в области поставок электронных компонентов. Мы поставляем электронные компоненты отечественного и импортного производства напрямую от производителей и с крупнейших складов мира.

Благодаря сотрудничеству с мировыми поставщиками мы осуществляем комплексные и плановые поставки широчайшего спектра электронных компонентов.

Собственная эффективная логистика и склад в обеспечивает надежную поставку продукции в точно указанные сроки по всей России.

Мы осуществляем техническую поддержку нашим клиентам и предпродажную проверку качества продукции. На все поставляемые продукты мы предоставляем гарантию .

Осуществляем поставки продукции под контролем ВП МО РФ на предприятия военно-промышленного комплекса России , а также работаем в рамках 275 ФЗ с открытием отдельных счетов в уполномоченном банке. Система менеджмента качества компании соответствует требованиям ГОСТ ISO 9001.

Минимальные сроки поставки, гибкие цены, неограниченный ассортимент и индивидуальный подход к клиентам являются основой для выстраивания долгосрочного и эффективного сотрудничества с предприятиями радиоэлектронной промышленности, предприятиями ВПК и научно-исследовательскими институтами России.

С нами вы становитесь еще успешнее!

Наши контакты:

Телефон: +7 812 627 14 35

Электронная почта: sales@st-electron.ru

Адрес: 198099, Санкт-Петербург,
Промышленная ул, дом № 19, литера Н,
помещение 100-Н Офис 331