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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

FAIRCHILD SEMICONDUCTOR®

July 2007

FDS9958

Dual P-Channel PowerTrench® MOSFET
-60V, -2.9A, 105mΩ

Features

- Max $r_{DS(on)}$ =105mΩ at V_{GS} = -10V, I_D = -2.9A
- Max $r_{DS(on)}$ =135mΩ at V_{GS} = -4.5V, I_D = -2.5A
- RoHS Compliant

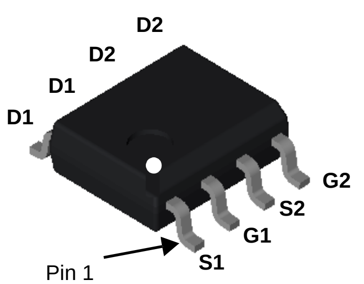
General Description

These P-channel logic level specified MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench® process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance.

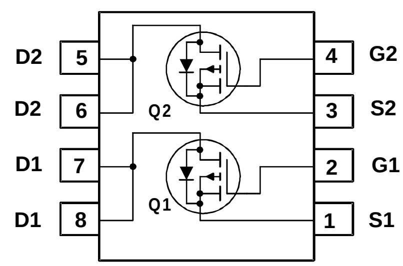
These devices are well suited for portable electronics applications: load switching and power management, battery charging and protection circuits.

Applications

- Load Switch
- Power Management



SO-8



MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DS}	Drain to Source Voltage		-60	V
V_{GS}	Gate to Source Voltage		±20	V
I_D	Drain Current -Continuous	(Note 1a)	-2.9	A
	-Pulsed		-12	
E_{AS}	Single Pulse Avalanche Energy	(Note 3)	54	mJ
P_D	Power Dissipation for Dual Operation		2	W
	Power Dissipation	(Note 1a)	1.6	
	Power Dissipation	(Note 1b)	0.9	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case		40	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	78	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDS9958	FDS9958	SO-8	330mm	12mm	2500units

Electrical Characteristics T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units

Off Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = -250μA, V_{GS} = 0V	-60			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = -250μA, referenced to 25°C		-52		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -48V, V_{GS} = 0V			-1	μA
		V_{DS} = -48V, V_{GS} = 0V, T_J = 125°C			-100	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20V, V_{DS} = 0V			±100	nA

On Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = -250μA	-1.0	-1.6	-3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = -250μA, referenced to 25°C		4		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = -10V, I_D = -2.9A		82	105	mΩ
		V_{GS} = -4.5V, I_D = -2.5A		103	135	mΩ
		V_{GS} = -10V, I_D = -2.9A, T_J= 125°C		131	190	mΩ
g_{FS}	Forward Transconductance	V_{DD} = -5V, I_D = -2.9A		7.7		S

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
C_{iss}	Input Capacitance	V_{DS} = -30V, V_{GS} = 0V, f = 1MHz		765	1020	pF
C_{oss}	Output Capacitance			90	120	pF
C_{rss}	Reverse Transfer Capacitance			40	65	pF

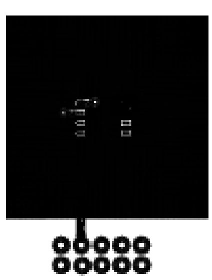
Switching Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = -30V, I_D = -2.9A, V_{GS} = -10V, R_{GEN} = 6Ω		6	12	ns
t_r	Rise Time			3	10	ns
$t_{d(off)}$	Turn-Off Delay Time			27	43	ns
t_f	Fall Time			6	12	ns
Q_g	Total Gate Charge	V_{GS} = 0V to -10V, V_{DD} = -30V, I_D = -2.9A		16	23	nC
Q_g	Total Gate Charge	V_{GS} = 0V to -4.5V, V_{DD} = -30V, I_D = -2.9A		8	12	nC
Q_{gs}	Gate to Source Charge	V_{DD} = -30V, I_D = -2.9A		2		nC
Q_{gd}	Gate to Drain "Miller" Charge			3		nC

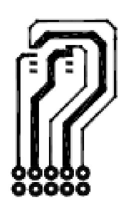
Drain-Source Diode Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0V, I_S = -1.3A (Note 2)		-0.8	-1.2	V
t_{rr}	Reverse Recovery Time	I_F = -2.9A, di/dt = 100A/μs		26	42	ns
Q_{rr}	Reverse Recovery Charge			21	35	nC

NOTES:
1. $R_{\theta JA}$ is determined with the device mounted on a 1in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 78°C/W when mounted on a 1 in^2 pad of 2 oz copper



b) 135°C/W when mounted on a minimun pad

2. Pulse Test: Pulse Width < 300μs, Duty cycle < 2.0%.

3. UIL condition: Starting T_J = 25°C, L = 3mH, I_{AS} = 6A, V_{DD} = 60V, V_{GS} = 10V.

Typical Characteristics T_J = 25°C unless otherwise noted

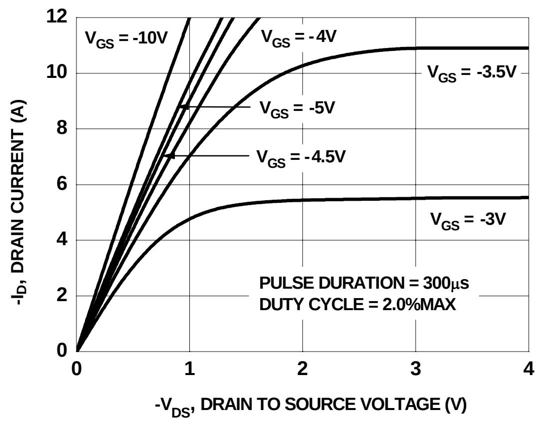


Figure 1. On-Region Characteristics

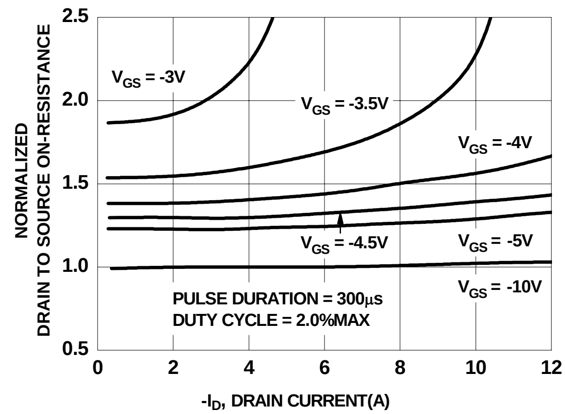


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

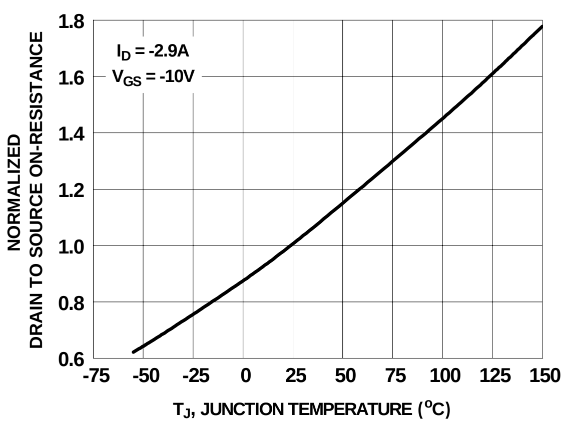


Figure 3. Normalized On-Resistance vs Junction Temperature

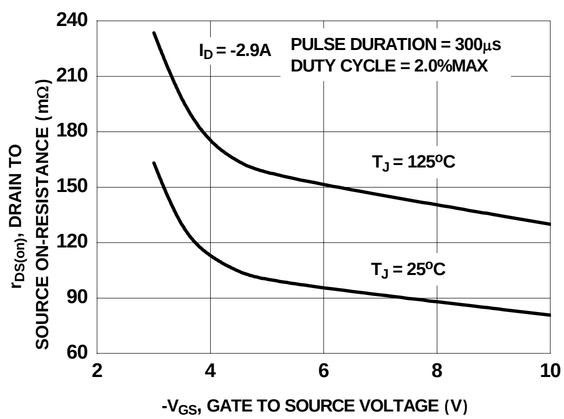


Figure 4. On-Resistance vs Gate to Source Voltage

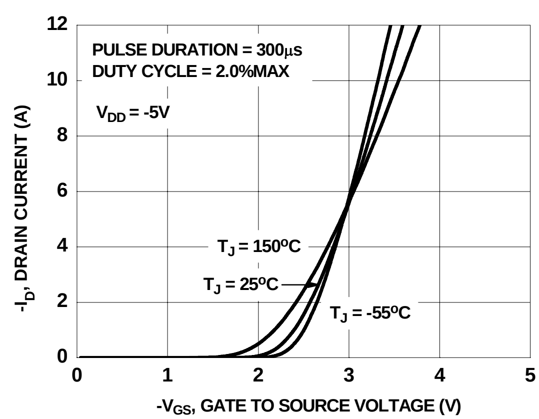


Figure 5. Transfer Characteristics

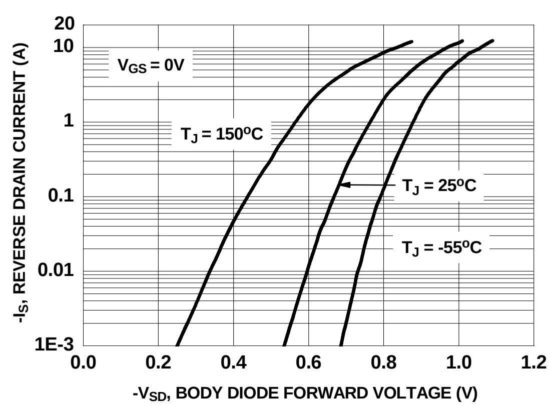


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25°C unless otherwise noted

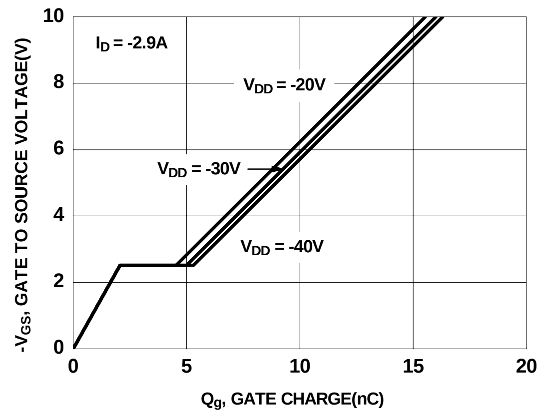


Figure 7. Gate Charge Characteristics

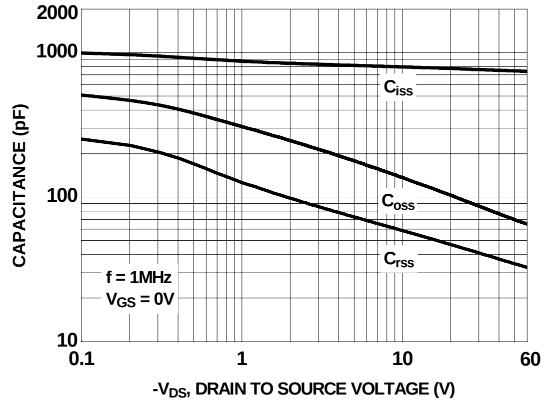


Figure 8. Capacitance vs Drain to Source Voltage

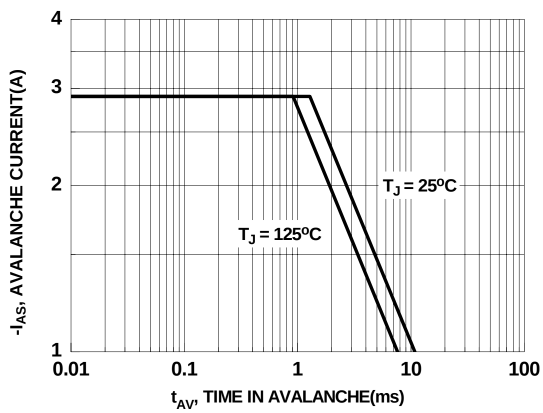


Figure 9. Unclamped Inductive Switching Capability

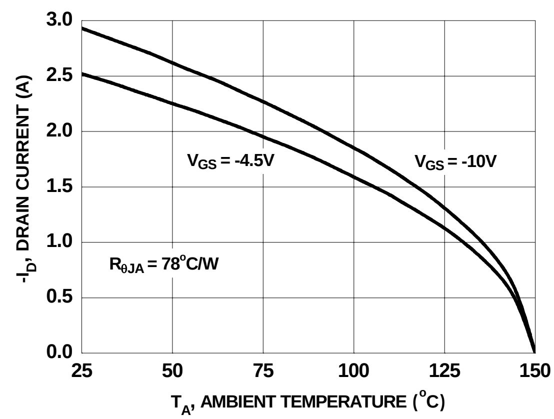


Figure 10. Maximum Continuous Drain Current vs Ambient Temperature

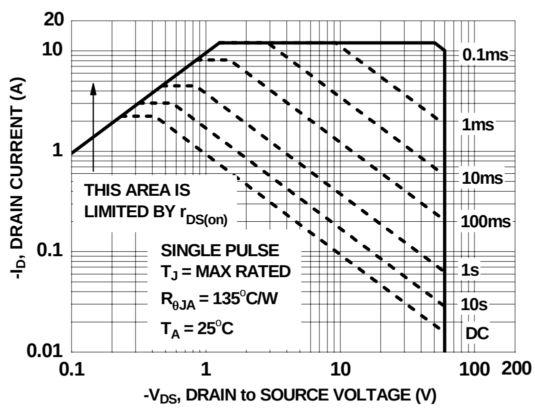


Figure 11. Forward Bias Safe Operating Area

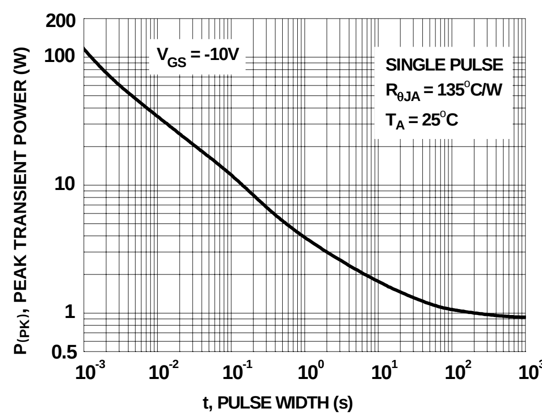


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25°C unless otherwise noted

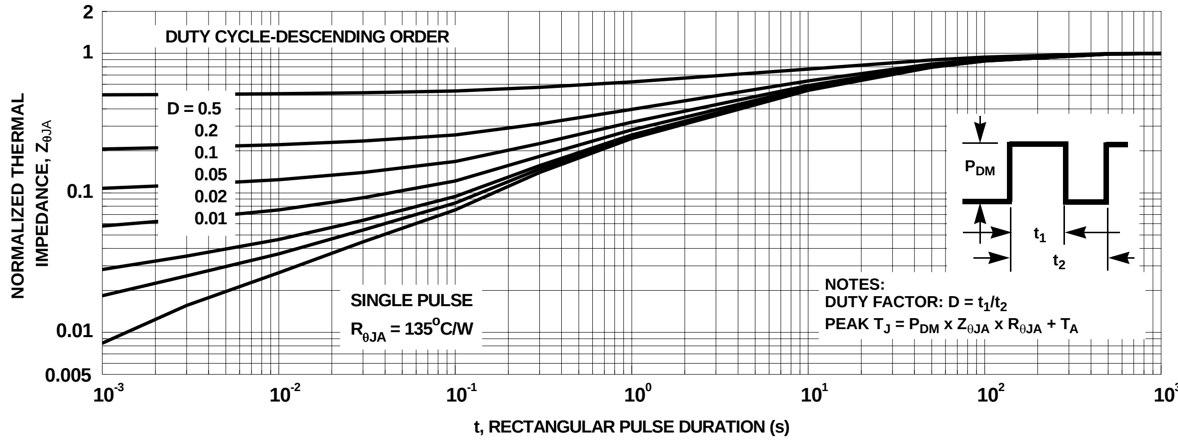


Figure 13. Transient Thermal Response Curve

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Rev. I30

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Наши контакты:

Телефон: +7 812 627 14 35

Электронная почта: sales@st-electron.ru

Адрес: 198099, Санкт-Петербург, Промышленная ул, дом № 19, литера Н, помещение 100-Н Офис 331