Low Cost 270 MHz Differential Receiver Amplifiers

AD8129/AD8130

FEATURES

High speed
- **AD8130: 270 MHz, 1090 V/µs @ G = +1**
- **AD8129: 200 MHz, 1060 V/µs @ G = +10**

High CMRR
- **94 dB min, dc to 100 kHz**
- **80 dB min @ 2 MHz**
- **70 dB @ 10 MHz**

High input impedance: 1 MΩ differential
Input common-mode range ±10.5 V
Low noise
- **AD8130: 12.5 nV/√Hz**
- **AD8129: 4.5 nV/√Hz**

Low distortion, 1 V p-p @ 5 MHz
- **AD8130, –79 dBc worst harmonic @ 5 MHz**
- **AD8129, –74 dBc worst harmonic @ 5 MHz**

User-adjustable gain
- **No external components for G = +1**

Power supply range +4.5 V to ±12.6 V
Power-down

APPLICATIONS

High speed differential line receivers
Differential-to-single-ended converters
High speed instrumentation amps
Level shifting

GENERAL DESCRIPTION

The AD8129/AD8130 are designed as receivers for the transmission of high speed signals over twisted-pair cables to work with the AD8131 or AD8132 drivers. Either can be used for analog or digital video signals and for high speed data transmission.

Figure 2. AD8129 CMRR vs. Frequency

CONNECTION DIAGRAM

Figure 1.

The AD8129/AD8130 are differential-to-single-ended amplifiers with extremely high CMRR at high frequency. Therefore, they can also be effectively used as high speed instrumentation amps or for converting differential signals to single-ended signals.

The AD8129 is a low noise, high gain (10 or greater) version intended for applications over very long cables, where signal attenuation is significant. The AD8130 is stable at a gain of 1 and can be used for applications where lower gains are required. Both have user-adjustable gain to help compensate for losses in the transmission line. The gain is set by the ratio of two resistor values. The AD8129/AD8130 have very high input impedance on both inputs, regardless of the gain setting.

The AD8129/AD8130 have excellent common-mode rejection (70 dB @ 10 MHz), allowing the use of low cost, unshielded twisted-pair cables without fear of corruption by external noise sources or crosstalk. The AD8129/AD8130 have a wide power supply range from single +5 V to ±12 V, allowing wide common-mode and differential-mode voltage ranges while maintaining signal integrity. The wide common-mode voltage range enables the driver-receiver pair to operate without isolation transformers in many systems where the ground potential difference between drive and receive locations is many volts. The AD8129/AD8130 have considerable cost and performance improvements over op amps and other multiamplifier receiving solutions.

Figure 3. Typical Connection Configuration

Rev. C
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REVISION HISTORY

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Revision 0: Initial Version

AD8129/AD8130 SPECIFICATIONS

5 V SPECIFICATIONS

AD8129 G = +10, AD8130 G = +1, T_A = 25°C, $+V_S$ = 5 V, $-V_S$ = 0 V, REF = 2.5 V, $\overline{PD} \geq V_{IH}$, R_L = 1 kΩ, C_L = 2 pF, unless otherwise noted. T_{MIN} to T_{MAX} = −40°C to +125°C, unless otherwise noted.

Table 1.

Model		AD8129			AD8130			
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
DYNAMIC PERFORMANCE								
−3 dB Bandwidth	V_{OUT} ≤ 0.3 V p-p	160	185		220	250		MHz
	V_{OUT} = 1 V p-p	160	185		180	205		MHz
Bandwidth for 0.1 dB Flatness	V_{OUT} ≤ 0.3 V p-p, SOIC/MSOP		25/40			25		MHz
Slew Rate	V_{OUT} = 2 V p-p, 25% to 75%	810	930		810	930		V/µs
Settling Time	V_{OUT} = 2 V p-p, 0.1%		20			20		ns
Rise and Fall Times	V_{OUT} ≤ 1 V p-p, 10% to 90%		1.8			1.5		ns
Output Overdrive Recovery			20			30		ns
NOISE/DISTORTION								
Second Harmonic/Third Harmonic	V_{OUT} = 1 V p-p, 5 MHz		−68/−75			−72/−79		dBc
	V_{OUT} = 2 V p-p, 5 MHz		−62/−64			−65/−71		dBc
	V_{OUT} = 1 V p-p, 10 MHz		−63/−70			−60/−62		dBc
	V_{OUT} = 2 V p-p, 10 MHz		−56/−58			−68/−68		dBc
IMD	V_{OUT} = 2 V p-p, 10 MHz		−67			−70		dBc
Output IP3	V_{OUT} = 2 V p-p, 10 MHz		25			26		dBm
Input Voltage Noise (RTI)	f ≥ 10 kHz		4.5			12.3		nV/√Hz
Input Current Noise (+IN, −IN)	f ≥ 100 kHz		1			1		pA/√Hz
Input Current Noise (REF, FB)	f ≥ 100 kHz		1.4			1.4		pA/√Hz
Differential Gain Error	AD8130, G = +2, NTSC 100 IRE, R_L ≥ 150 Ω		0.3			0.13		%
Differential Phase Error	AD8130, G = +2, NTSC 100 IRE, R_L ≥ 150 Ω		0.1			0.15		Degrees
INPUT CHARACTERISTICS								
Common-Mode Rejection Ratio	DC to 100 kHz, V_{CM} = 1.5 V to 3.5 V	86	96		86	96		dB
	V_{CM} = 1 V p-p @ 1 MHz	80			80			dB
	V_{CM} = 1 V p-p @ 10 MHz		70			70		dB
CMRR with V_{OUT} = 1 V p-p	V_{CM} = 1 V p-p @ 1 kHz, V_{OUT} = ±0.5 V dc		80			72		dB
Common-Mode Voltage Range	$V_{+IN} - V_{-IN}$ = 0 V		1.25 to 3.7			1.25 to 3.8		V
Differential Operating Range			±0.5			±2.5		V
Differential Clipping Level		±0.6	±0.75	±0.85	±2.3	±2.8	±3.3	V
Resistance	Differential		1			6		MΩ
	Common mode		4			4		MΩ
Capacitance	Differential		3			3		pF
	Common mode		4			4		pF

Model		AD8129			AD8130			
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
DC PERFORMANCE								
Closed-Loop Gain Error	V_{OUT} = ±1 V, R_L ≥ 150 Ω		±0.25	±1.25		±0.1	±0.6	%
	T_{MIN} to T_{MAX}		20			20		ppm/°C
Open-Loop Gain	V_{OUT} = ±1 V		86			71		dB
Gain Nonlinearity	V_{OUT} = ±1 V		250			200		ppm
Input Offset Voltage			0.2	0.8		0.4	1.8	mV
	T_{MIN} to T_{MAX}		2			20		μV/°C
	T_{MIN} to T_{MAX}			1.4			3.5	mV
Input Offset Voltage vs. Supply	$+V_S$ = 5 V, $-V_S$ = −0.5 V to +0.5 V		−88	−80		−74	−70	dB
	$-V_S$ = 0 V, $+V_S$ = +4.5 V to +5.5 V		−100	−86		−90	−76	dB
Input Bias Current (+IN, −IN)			±0.5	±2		±0.5	±2	μA
Input Bias Current (REF, FB)			±1	±3.5		±1	±3.5	μA
	T_{MIN} to T_{MAX} (+IN, −IN, REF, FB)		5			5		nA/°C
Input Offset Current	(+IN, −IN, REF, FB)		±0.08	±0.4		±0.08	±0.4	μA
	T_{MIN} to T_{MAX}		0.2			0.2		nA/°C
OUTPUT PERFORMANCE								
Voltage Swing	R_{LOAD} ≥ 150 Ω	1.1		3.9	1.1		3.9	V
Output Current			35			35		mA
Short-Circuit Current	To common		−60/+55			−60/+55		mA
	T_{MIN} to T_{MAX}		−240			−240		μA/°C
Output Impedance	$\overline{PD}$ ≤ V_{IL}, in power-down mode		10			10		pF
POWER SUPPLY								
Operating Voltage Range	Total supply voltage	±2.25		±12.6	±2.25		±12.6	V
Quiescent Supply Current			9.9	10.6		9.9	10.6	mA
	T_{MIN} to T_{MAX}		33			33		μA/°C
	$\overline{PD}$ ≤ V_{IL}		0.65	0.85		0.65	0.85	mA
	$\overline{PD}$ ≤ V_{IL}, T_{MIN} to T_{MAX}			1			1	mA
$\overline{PD}$ PIN								
V_{IH}		$+V_S$ − 1.5			$+V_S$ − 1.5			V
V_{IL}				$+V_S$ − 2.5			$+V_S$ − 2.5	V
I_{IH}	$\overline{PD}$ = min V_{IH}			−30			−30	μA
I_{IL}	$\overline{PD}$ = max V_{IL}			−50			−50	μA
Input Resistance	$\overline{PD}$ ≤ $+V_S$ − 3 V		12.5			12.5		kΩ
	$\overline{PD}$ ≥ $+V_S$ − 2 V		100			100		kΩ
Enable Time			0.5			0.5		μs
OPERATING TEMPERATURE RANGE		−40		+125	−40		+125	°C

±5 V SPECIFICATIONS

AD8129 G = +10, AD8130 G = +1, T_A = 25°C, V_S = ±5 V, REF = 0 V, $\overline{PD}$ ≥ V_{IH}, R_L = 1 kΩ, C_L = 2 pF, unless otherwise noted. T_{MIN} to T_{MAX} = −40°C to +125°C, unless otherwise noted.

Table 2.

		AD8129			AD8130			
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
DYNAMIC PERFORMANCE								
−3 dB Bandwidth	V_{OUT} ≤ 0.3 V p-p	175	200		240	270		MHz
	V_{OUT} = 2 V p-p	170	190		140	155		MHz
Bandwidth for 0.1 dB Flatness	V_{OUT} ≤ 0.3 V p-p, SOIC/MSOP		30/50			45		MHz
Slew Rate	V_{OUT} = 2 V p-p, 25% to 75%	925	1060		950	1090		V/µs
Settling Time	V_{OUT} = 2 V p-p, 0.1%		20			20		ns
Rise and Fall Times	V_{OUT} ≤ 1 V p-p, 10% to 90%		1.7			1.4		ns
Output Overdrive Recovery			30			40		ns
NOISE/DISTORTION								
Second Harmonic/Third Harmonic	V_{OUT} = 1 V p-p, 5 MHz		−74/−84			−79/−86		dBc
	V_{OUT} = 2 V p-p, 5 MHz		−68/−74			−74/−81		dBc
	V_{OUT} = 1 V p-p, 10 MHz		−67/−81			−74/−80		dBc
	V_{OUT} = 1 V p-p, 10 MHz		−61/−70			−74/−76		dBc
IMD	V_{OUT} = 2 V p-p, 10 MHz		−67			−70		dBc
Output IP3	V_{OUT} = 2 V p-p, 10 MHz		25			26		dBm
Input Voltage Noise (RTI)	f ≥ 10 kHz		4.5			12.5		nV/√Hz
Input Current Noise (+IN, −IN)	f ≥ 100 kHz		1			1		pA/√Hz
Input Current Noise (REF, FB)	f ≥ 100 kHz		1.4			1.4		pA/√Hz
Differential Gain Error	AD8130, G = +2, NTSC 200 IRE, R_L ≥ 150 Ω		0.3			0.13		%
Differential Phase Error	AD8130, G = +2, NTSC 200 IRE, R_L ≥ 150 Ω		0.1			0.15		Degrees
INPUT CHARACTERISTICS								
Common-Mode Rejection Ratio	DC to 100 kHz, V_{CM} = −3 V to +3.5 V	94	110		90	110		dB
	V_{CM} = 1 V p-p @ 2 MHz	80			80			dB
	V_{CM} = 1 V p-p @ 10 MHz		70			70		dB
CMRR with V_{OUT} = 1 V p-p	V_{CM} = 2 V p-p @ 1 kHz, V_{OUT} = ±0.5 V dc		100			83		dB
Common-Mode Voltage Range	V_{+IN} − V_{-IN} = 0 V		±3.5			±3.8		V
Differential Operating Range			±0.5			±2.5		V
Differential Clipping Level		±0.6	±0.75	±0.85	±2.3	±2.8	±3.3	V
Resistance	Differential		1			6		MΩ
	Common mode		4			4		MΩ
Capacitance	Differential		3			3		pF
	Common mode		4			4		pF

Parameter	Conditions	AD8129 Min	AD8129 Typ	AD8129 Max	AD8130 Min	AD8130 Typ	AD8130 Max	Unit
DC PERFORMANCE								
Closed-Loop Gain Error	V_{OUT} = ±1 V, R_L ≥ 150 Ω		±0.4	±1.5		±0.15	±0.6	%
	T_{MIN} to T_{MAX}		20			10		ppm/°C
Open-Loop Gain	V_{OUT} = ±1 V		88			74		dB
Gain Nonlinearity	V_{OUT} = ±1 V		250			200		ppm
Input Offset Voltage			0.2	0.8		0.4	1.8	mV
	T_{MIN} to T_{MAX}		2			20		µV/°C
	T_{MIN} to T_{MAX}			1.4			3.5	mV
Input Offset Voltage vs. Supply	$+V_S$ = +5 V, $-V_S$ = −4.5 V to −5.5 V		−90	−84		−78	−74	dB
	$-V_S$ = −5 V, $+V_S$ = +4.5 V to +5.5 V		−94	−86		−80	−74	dB
Input Bias Current (+IN, −IN)			±0.5	±2		±0.5	±2	µA
Input Bias Current (REF, FB)			±1	±3.5		±1	±3.5	µA
	T_{MIN} to T_{MAX} (+IN, −IN, REF, FB)		5			5		nA/°C
Input Offset Current	(+IN, −IN, REF, FB)		±0.08	±0.4		±0.08	±0.4	µA
	T_{MIN} to T_{MAX}		0.2			0.2		nA/°C
OUTPUT PERFORMANCE								
Voltage Swing	R_{LOAD} = 150 Ω/1 kΩ	3.6/4.0			3.6/4.0			±V
Output Current			40			40		mA
Short-Circuit Current	To common		−60/+55			−60/+55		mA
	T_{MIN} to T_{MAX}		−240			−240		µA/°C
Output Impedance	$\overline{PD}$ ≤ V_{IL}, in power-down mode		10			10		pF
POWER SUPPLY								
Operating Voltage Range	Total supply voltage	±2.25		±12.6	±2.25		±12.6	V
Quiescent Supply Current			10.8	11.6		10.8	11.6	mA
	T_{MIN} to T_{MAX}		36			36		µA/°C
	$\overline{PD}$ ≤ V_{IL}		0.68	0.85		0.68	0.85	mA
	$\overline{PD}$ ≤ V_{IL}, T_{MIN} to T_{MAX}			1			1	mA
$\overline{PD}$ PIN								
V_{IH}		$+V_S$ − 1.5			$+V_S$ − 1.5			V
V_{IL}				$+V_S$ − 2.5			$+V_S$ − 2.5	V
I_{IH}	$\overline{PD}$ = min V_{IH}			−30			−30	µA
I_{IL}	$\overline{PD}$ = max V_{IL}			−50			−50	µA
Input Resistance	$\overline{PD}$ ≤ $+V_S$ − 3 V		12.5			12.5		kΩ
	$\overline{PD}$ ≥ $+V_S$ − 2 V		100			100		kΩ
Enable Time			0.5			0.5		µs
OPERATING TEMPERATURE RANGE		−40		+125	−40		+125	°C

±12 V SPECIFICATIONS

AD8129 G = +10, AD8130 G = +1, T_A = 25°C, V_S = ±12 V, REF = 0 V, $\overline{PD}$ ≥ V_{IH}, R_L = 1 kΩ, C_L = 2 pF, unless otherwise noted. T_{MIN} to T_{MAX} = −40°C to +85°C, unless otherwise noted.

Table 3.

		AD8129			AD8130			
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
DYNAMIC PERFORMANCE								
−3 dB Bandwidth	V_{OUT} ≤ 0.3 V p-p	175	200		250	290		MHz
	V_{OUT} = 2 V p-p	170	195		150	175		MHz
Bandwidth for 0.1 dB Flatness	V_{OUT} ≤ 0.3 V p-p, SOIC/MSOP		50/70			110		MHz
Slew Rate	V_{OUT} = 2 V p-p, 25% to 75%	935	1070		960	1100		V/µs
Settling Time	V_{OUT} = 2 V p-p, 0.1%		20			20		ns
Rise and Fall Times	V_{OUT} ≤ 1 V p-p, 10% to 90%		1.7			1.4		ns
Output Overdrive Recovery			40			40		ns
NOISE/DISTORTION								
Second Harmonic/Third Harmonic	V_{OUT} = 1 V p-p, 5 MHz		−71/−84			−79/−86		dBc
	V_{OUT} = 2 V p-p, 5 MHz		−65/−74			−74/−81		dBc
	V_{OUT} = 1 V p-p, 10 MHz		−65/−82			−74/−80		dBc
	V_{OUT} = 2 V p-p, 10 MHz		−59/−70			−74/−74		dBc
IMD	V_{OUT} = 2 V p-p, 10 MHz		−67			−70		dBc
Output IP3	V_{OUT} = 2 V p-p, 10 MHz		25			26		dBm
Input Voltage Noise (RTI)	f ≥ 10 kHz		4.6			13		nV/√Hz
Input Current Noise (+IN, −IN)	f ≥ 100 kHz		1			1		pA/√Hz
Input Current Noise (REF, FB)	f ≥ 100 kHz		1.4			1.4		pA/√Hz
Differential Gain Error	AD8130, G = +2, NTSC 200 IRE, R_L ≥ 150 Ω		0.3			0.13		%
Differential Phase Error	AD8130, G = +2, NTSC 200 IRE, R_L ≥ 150 Ω		0.1			0.2		Degrees
INPUT CHARACTERISTICS								
Common-Mode Rejection Ratio	DC to 100 kHz, V_{CM} = ±10 V	92	105		88	105		dB
	V_{CM} = 1 V p-p @ 2 MHz	80			80			dB
	V_{CM} = 1 V p-p @ 10 MHz		70			70		dB
CMRR with V_{OUT} = 1 V p-p	V_{CM} = 4 V p-p @ 1 kHz, V_{OUT} = ±0.5 V dc		93			80		dB
Common-Mode Voltage Range	V_{+IN} − V_{-IN} = 0 V		±10.3			±10.5		V
Differential Operating Range			±0.5			±2.5		V
Differential Clipping Level		±0.6	±0.75	±0.85	±2.3	±2.8	±3.3	V
Resistance	Differential		1			6		MΩ
	Common mode		4			4		MΩ
Capacitance	Differential		3			3		pF
	Common mode		4			4		pF

Parameter	Conditions	AD8129 Min	AD8129 Typ	AD8129 Max	AD8130 Min	AD8130 Typ	AD8130 Max	Unit
DC PERFORMANCE								
Closed-Loop Gain Error	V_{OUT} = ±1 V, R_L ≥ 150 Ω		±0.8	±1.8		±0.15	±0.6	%
	T_{MIN} to T_{MAX}		20			10		ppm/°C
Open-Loop Gain	V_{OUT} = ±1 V		87			73		dB
Gain Nonlinearity	V_{OUT} = ±1 V		250			200		ppm
Input Offset Voltage			0.2	0.8		0.4	1.8	mV
	T_{MIN} to T_{MAX}		2			20		μV/°C
	T_{MIN} to T_{MAX}			1.4			3.5	mV
Input Offset Voltage vs. Supply	$+V_S$ = +12 V, $-V_S$ = −11.0 V to −13.0 V		−88	−82		−77	−70	dB
	$-V_S$ = −12 V, $+V_S$ = +11.0 V to +13.0 V		−92	−84		−88	−70	dB
Input Bias Current (+IN, −IN)			±0.25	±2		±0.25	±2	μA
Input Bias Current (REF, FB)			±0.5	±3.5		±0.5	±3.5	μA
	T_{MIN} to T_{MAX} (+IN, −IN, REF, FB)		2.5			2.5		nA/°C
Input Offset Current	(+IN, −IN, REF, FB)		±0.08	±0.4		±0.08	±0.4	μA
	T_{MIN} to T_{MAX}		0.2			0.2		nA/°C
OUTPUT PERFORMANCE								
Voltage Swing	R_{LOAD} = 700 Ω	±10.8			±10.8			V
Output Current			40			40		mA
Short-Circuit Current	To common		−60/+55			−60/+55		mA
	T_{MIN} to T_{MAX}		−240			−240		μA/°C
Output Impedance	$\overline{PD}$ ≤ V_{IL}, in power-down mode		10			10		pF
POWER SUPPLY								
Operating Voltage Range	Total supply voltage	±2.25		±12.6	±2.25		±12.6	V
Quiescent Supply Current			13	13.9		13	13.9	mA
	T_{MIN} to T_{MAX}		43			43		μA°C
	$\overline{PD}$ ≤ V_{IL}		0.73	0.9		0.73	0.9	mA
	$\overline{PD}$ ≤ V_{IL}, T_{MIN} to T_{MAX}			1.1			1.1	mA
$\overline{PD}$ PIN								
V_{IH}		$+V_S$ − 1.5			$+V_S$ − 1.5			V
V_{IL}				$+V_S$ − 2.5			$+V_S$ − 2.5	V
I_{IH}	$\overline{PD}$ = min V_{IH}			−30			−30	μA
I_{IL}	$\overline{PD}$ = max V_{IL}			−50			−50	μA
Input Resistance	$\overline{PD}$ ≤ $+V_S$ − 3 V		3			3		kΩ
	$\overline{PD}$ ≥ $+V_S$ − 2 V		100			100		kΩ
Enable Time			0.5			0.5		μs
OPERATING TEMPERATURE RANGE		−40		+85	−40		+85	°C

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	26.4 V
Power Dissipation	Refer to Figure 4
Input Voltage (Any Input)	$-V_S - 0.3$ V to $+V_S + 0.3$ V
Differential Input Voltage (AD8129)	
$V_S \geq \pm 11.5$ V	±0.5 V
Differential Input Voltage (AD8129)	
$V_S < \pm 11.5$ V	±6.2 V
Differential Input Voltage (AD8130)	±8.4 V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, θ_{JA} is specified for the device soldered in a circuit board in still air.

Table 5. Thermal Resistance

Package Type	θ_{JA}	Unit
8-Lead SOIC/4-Layer	121	°C/W
8-Lead MSOP/4-Layer	142	°C/W

Maximum Power Dissipation

The maximum safe power dissipation in the AD8129/AD8130 packages is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit can change the stresses that the package exerts on the die, permanently shifting the parametric performance of the AD8129/AD8130. Exceeding a junction temperature of 150°C for an extended period can result in changes in the silicon devices, potentially causing failure.

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S). The power dissipated due to the load drive depends upon the particular application. The power due to load drive is calculated by multiplying the load current by the associated voltage drop across the device. RMS voltages and currents must be used in these calculations.

Airflow reduces θ_{JA}. In addition, more metal directly in contact with the package leads from metal traces through holes, ground, and power planes reduces the θ_{JA}.

Figure 4 shows the maximum safe power dissipation in the package vs. the ambient temperature for the 8-lead SOIC (121°C/W) and MSOP (θ_{JA} = 142°C/W) packages on a JEDEC standard 4-layer board. θ_{JA} values are approximations.

Figure 4. Maximum Power Dissipation vs. Temperature

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

AD8130 FREQUENCY RESPONSE CHARACTERISTICS

G = +1, R_L = 1 kΩ, C_L = 2 pF, V_{OUT} = 0.3 V p-p, T_A = 25°C, unless otherwise noted.

Figure 5. AD8130 Frequency Response vs. Supply, V_{OUT} = 0.3 V p-p

Figure 6. AD8130 Frequency Response vs. Supply, V_{OUT} = 1 V p-p

Figure 7. AD8130 Frequency Response vs. Supply, V_{OUT} = 2 V p-p

Figure 8. AD8130 Frequency Response vs. Load Capacitance

Figure 9. AD8130 Fine Scale Response vs. Supply, R_L = 1 kΩ

Figure 10. AD8130 Fine Scale Response vs. Supply, R_L = 150 Ω

Figure 11. AD8130 Frequency Response vs. Supply, R_L = 150 Ω

Figure 12. AD8130 Frequency Response vs. Supply, G = +2, V_{OUT} = 0.3 V p-p

Figure 13. AD8130 Frequency Response vs. Supply, G = +2, V_{OUT} = 2 V p-p

Figure 14. AD8130 Frequency Response for Various R_F/R_G

Figure 15. AD8130 Fine Scale Response vs. Supply, G = +2, R_L = 1 kΩ

Figure 16. AD8130 Fine Scale Response vs. Supply, G = +2, R_L = 150 Ω

Figure 17. AD8130 Frequency Response vs. Supply, G = +2, R_L = 150 Ω

Figure 18. AD8130 Fine Scale Response vs. Supply, G = +5, G = +10, V_{OUT} = 2 V p-p

Figure 19. AD8130 Frequency Response vs. Supply, G = +5, G = +10, V_{OUT} = 2 V p-p

Figure 20. AD8130 Frequency Response vs. Supply, G = +5, G = +10, R_L = 150 Ω

Figure 21. AD8130 Frequency Response for Various Output Levels

G	R_F	R_G
1	0Ω	–
2	499Ω	499Ω
5	8.06kΩ	2kΩ
10	4.99kΩ	549Ω

Figure 22. AD8130 Basic Frequency Response Test Circuit

AD8129 FREQUENCY RESPONSE CHARACTERISTICS

G = +10, R_L = 1 kΩ, C_L = 2 pF, V_{OUT} = 0.3 V p-p, T_A = 25°C, unless otherwise noted.

Figure 23. AD8129 Frequency Response vs. Supply, V_{OUT} = 0.3 V p-p

Figure 24. AD8129 Frequency Response vs. Supply, V_{OUT} = 1 V p-p

Figure 25. AD8129 Frequency Response vs. Supply, V_{OUT} = 2 V p-p

Figure 26. AD8129 Frequency Response vs. Load Capacitance

Figure 27. AD8129 Fine Scale Response vs. Supply, R_L = 1 kΩ

Figure 28. AD8129 Fine Scale Response vs. Supply, R_L = 150 Ω

Figure 29. AD8129 Frequency Response vs. Supply, R_L = 150 Ω

Figure 30. AD8129 Frequency Response vs. Supply, G = +20, V_{OUT} = 0.3 V p-p

Figure 31. AD8129 Frequency Response vs. Supply, G = +20, V_{OUT} = 2 V p-p

Figure 32. AD8129 Fine Scale Response vs. SOIC and MSOP for Various R_F/R_G

Figure 33. AD8129 Fine Scale Response vs. Supply

Figure 34. AD8129 Fine Scale Response vs. Supply

Figure 35. AD8129 Frequency Response vs. Supply, G = +20, R_L = 150 Ω

Figure 36. AD8129 Fine Scale Response vs. Supply, G = +50, G = +100, V_{OUT} = 2 V p-p

Figure 37. AD8129 Frequency Response vs. Supply, G = +50, G = +100, V_{OUT} = 2 V p-p

Figure 38. AD8129 Frequency Response vs. Supply, G = +50, G = +100, R_L = 150 Ω

Figure 39. AD8129 Frequency Response for Various Output Levels

G	R_F	R_G
10	2kΩ	221Ω
20	2kΩ	105Ω
50	2kΩ	41.2Ω
100	2kΩ	20Ω

Figure 40. AD8129 Basic Frequency Response Test Circuit

AD8130 HARMONIC DISTORTION CHARACTERISTICS

R_L = 1 kΩ, C_L = 2 pF, T_A = 25°C, unless otherwise noted.

Figure 41. AD8130 Second Harmonic Distortion vs. Frequency

Figure 42. AD8130 Second Harmonic Distortion vs. Frequency

Figure 43. AD8130 Second Harmonic Distortion vs. Output Voltage

Figure 44. AD8130 Third Harmonic Distortion vs. Frequency

Figure 45. AD8130 Third Harmonic Distortion vs. Frequency

Figure 46. AD8130 Third Harmonic Distortion vs. Output Voltage

Figure 47. AD8130 Second Harmonic Distortion vs. Frequency

Figure 49. AD8130 Harmonic Distortion vs. Output Voltage

Figure 48. AD8130 Third Harmonic Distortion vs. Frequency

AD8129 HARMONIC DISTORTION CHARACTERISTICS

R_L = 1 kΩ, C_L = 2 pF, T_A = 25°C, unless otherwise noted.

Figure 50. AD8129 Second Harmonic Distortion vs. Frequency

Figure 51. AD8129 Second Harmonic Distortion vs. Frequency

Figure 52. AD8129 Second Harmonic Distortion vs. Output Voltage

Figure 53. AD8129 Third Harmonic Distortion vs. Frequency

Figure 54. AD8129 Third Harmonic Distortion vs. Frequency

Figure 55. AD8129 Third Harmonic Distortion vs. Output Voltage

Figure 56. AD8129 Second Harmonic Distortion vs. Frequency

Figure 57. AD8129 Third Harmonic Distortion vs. Frequency

Figure 58. AD8129 Harmonic Distortion vs. Output Voltage

Figure 59. AD8130 Harmonic Distortion vs. Common-Mode Voltage

Figure 60. AD8130 Harmonic Distortion vs. Load Resistance

Figure 61. AD8130 Harmonic Distortion vs. Load Resistance

Figure 62. AD8129 Harmonic Distortion vs. Common-Mode Voltage

Figure 63. AD8129 Harmonic Distortion vs. Load Resistance

Figure 64. AD8129 Harmonic Distortion vs. Load Resistance

MINI-CIRCUITS®:
T4-6T, $f_C \leq 10MHz$
TC4-1W, $f_C > 10MHz$

G	R_F	R_G
1	0Ω	–
2	499Ω	499Ω
10	2kΩ	221Ω
20	2kΩ	105Ω

Figure 65. AD8129/AD8130 Basic Distortion Test Circuit, V_{CM} = 0 V, Unless Otherwise Noted

Figure 66. AD8129/AD8130 Input Current Noise vs. Frequency

Figure 67. AD8129/AD8130 Input Voltage Noise vs. Frequency

Figure 68. AD8130 Common-Mode Rejection vs. Frequency

Figure 69. AD8130 Positive Power Supply Rejection vs. Frequency

Figure 70. AD8130 Negative Power Supply Rejection vs. Frequency

Figure 71. AD8139 Common-Mode Rejection vs. Frequency

Figure 72. AD8129 Positive Power Supply Rejection vs. Frequency

Figure 73. AD8129 Negative Power Supply Rejection vs. Frequency

Figure 74. AD8130 Open-Loop Gain and Phase vs. Frequency

Figure 75. AD8129 Open-Loop Gain and Phase vs. Frequency

Figure 76. Closed-Loop Output Impedance vs. Frequency

AD8130 TRANSIENT RESPONSE CHARACTERISTICS

G = +1, R_L = 1 kΩ, C_L = 2 pF, V_S = ±5 V, T_A = 25°C, unless otherwise noted.

Figure 77. AD8130 Transient Response, V_S = ±2.5 V, V_{OUT} = 1 V p-p

Figure 78. AD8130 Transient Response, V_S = ±5 V, V_{OUT} = 1 V p-p

Figure 79. AD8130 Transient Response, V_S = ±12 V, V_{OUT} = 1 V p-p

Figure 80. AD8130 Transient Response vs. Supply, V_{OUT} = 0.2 V p-p

Figure 81. AD8130 Transient Response vs. Supply, V_{OUT} = 1 V p-p, C_L = 5 pF

Figure 82. AD8130 Transient Response vs. Supply, V_{OUT} = 2 V p-p, C_L = 5 pF

Figure 83. AD8130 Transient Response vs. Load Capacitance, V_{OUT} = 0.2 V p-p

Figure 84. AD8130 Transient Response vs. Output Amplitude, V_{OUT} = 0.5 V p-p, 1 V p-p, 2 V p-p

Figure 85. AD8130 Transient Response vs. Output Amplitude, V_{OUT} = 1 V p-p, 2 V p-p, 4 V p-p

Figure 86. AD8130 Transient Response vs. Load Capacitance, V_{OUT} = 1 V p-p, G = +2

Figure 87. AD8130 Transient Response vs. Supply, V_{OUT} = 2 V p-p, G = +2

Figure 88. AD8130 Transient Response vs. Load Capacitance, V_{OUT} = 8 V p-p

Figure 89. AD8130 Transient Response with +3 V Common-Mode Input

Figure 90. AD8130 Transient Response with −3 V Common-Mode Input

Figure 91. AD8130 Transient Response, V_{OUT} = 10 V p-p, G = +2, V_S = ±12 V

Figure 92. AD8130 Transient Response vs. Output Amplitude

Figure 93. AD8130 Transient Response, V_{OUT} = 8 V p-p, G = +5, V_S = ±5 V

Figure 94. AD8130 Transient Response, V_{OUT} = 20 V p-p, G = +5, V_S = ±12 V

AD8129 TRANSIENT RESPONSE CHARACTERISTICS

G = +10, R_F = 2 kΩ, R_G = 221 Ω, R_L = 1 kΩ, C_L = 1 pF, V_S = ±5 V, T_A = 25°C, unless otherwise noted.

Figure 95. AD8129 Transient Response, V_S = ±2.5 V, V_{OUT} = 1 V p-p

Figure 96. AD8129 Transient Response, V_S = ±5 V, V_{OUT} = 1 V p-p

Figure 97. AD8129 Transient Response, V_S = ±12 V, V_{OUT} = 1 V p-p

Figure 98. AD8129 Transient Response vs. Supply, V_{OUT} = 0.4 V p-p

Figure 99. AD8129 Transient Response vs. Supply, V_{OUT} = 1 V p-p, C_L = 5 pF

Figure 100. AD8129 Transient Response vs. Supply, V_{OUT} = 2 V p-p, C_L = 5 pF

Figure 101 Transient Response vs. Load Capacitance, V_{OUT} = 0.4 V p-p

Figure 102. Transient Response vs. Output Amplitude, V_{OUT} = 0.5 V p-p, 1 V p-p, 2 V p-p

Figure 103. Transient Response vs. Output Amplitude, V_{OUT} = 1 V p-p, 2 V p-p, 4 V p-p

Figure 104. AD8129 Transient Response, V_{OUT} = 1 V p-p, V_S = ±2.5 V to ±12 V

Figure 105. AD8129 Transient Response, V_{OUT} = 2 V p-p, V_S = ±5 V

Figure 106. AD8129 Transient Response, V_{OUT} = 8 V p-p, V_S = ±5 V

Figure 107. AD8129 Transient Response with +3.5 V Common-Mode Input

Figure 108. AD8129 Transient Response with −3.5 V Common-Mode Input

Figure 109. AD8129 Transient Response, V_{OUT} = 10 V p-p, G = +20

Figure 110. AD8129 Transient Response vs. Output Amplitude, V_{OUT} = 1 V p-p, 2 V p-p, 4 V p-p

Figure 111. AD8129 Transient Response, V_{OUT} = 8 V p-p, G = +50, V_S = ±5 V

Figure 112. AD8129 Transient Response, V_{OUT} = 20 V p-p, G = +50, V_S = ±12 V

Figure 113. AD8130 DC Power Supply Current vs. Differential Input Voltage

Figure 114. AD8129 DC Power Supply Current vs. Differential Input Voltage

Figure 115. AD8129/AD8130 Input Differential Voltage Range vs. Temperature, 1% Gain Compression

Figure 116. AD8130 Gain Nonlinearity, V_{OUT} = 2 V p-p

Figure 117. AD8130 Gain Nonlinearity, V_{OUT} = 5 V p-p

Figure 118. AD8130 Differential Input Clipping Level

Figure 119. AD8129 Gain Nonlinearity, V_{OUT} = 2 V p-p

Figure 120. AD8129 Gain Nonlinearity, V_{OUT} = 10 V p-p

Figure 121. AD8129 Differential Input Clipping Level

Figure 122. Quiescent Power Supply Current vs. Total Supply Voltage

Figure 123. Quiescent Power Supply Current vs. Temperature

Figure 124. Input Bias Current and Input Offset Current vs. Temperature

Figure 125. Common-Mode Voltage Range vs. Temperature, Typical 1% Gain Compression

Figure 126. Common-Mode Voltage Range vs. Temperature, Typical 1% Gain Compression

Figure 127. Common-Mode Voltage Range vs. Temperature, Typical 1% Gain Compression

Figure 128. Output Voltage Range vs. Output Current, Typical 1% Gain Compression

Figure 129. Output Voltage Range vs. Output Current, Typical 1% Gain Compression

Figure 130. Output Voltage Range vs. Output Current, Typical 1% Gain Compression

THEORY OF OPERATION

The AD8129/AD8130 use an architecture called active feedback, which differs from that of conventional op amps. The most obvious differentiating feature is the presence of two separate pairs of differential inputs compared with a conventional op amp's single pair. Typically, for the active feedback architecture, one of these input pairs is driven by a differential input signal, while the other is used for the feedback. This active stage in the feedback path is where the term *active feedback* is derived.

The active feedback architecture offers several advantages over a conventional op amp in many types of applications. Among these are excellent common-mode rejection, wide input common-mode range, and a pair of inputs that are high impedance and completely balanced in a typical application. In addition, while an external feedback network establishes the gain response as in a conventional op amp, its separate path makes it completely independent of the signal input. This eliminates any interaction between the feedback and input circuits, which traditionally causes problems with CMRR in conventional differential-input op amp circuits.

Another advantage is the ability to change the polarity of the gain merely by switching the differential inputs. A high input-impedance inverting amplifier can be made. Besides a high input impedance, a unity-gain inverter with the AD8130 has a noise gain of unity. This produces lower output noise and higher bandwidth than op amps that have noise gain equal to 2 for a unity-gain inverter.

The two differential input stages of the AD8129/AD8130 are each transconductance stages that are well matched. These stages convert the respective differential input voltages to internal currents. The currents are then summed and converted to a voltage, which is buffered to drive the output. The compensation capacitor is in the summing circuit.

When the feedback path is closed around the part, the output drives the feedback input to the voltage that causes the internal currents to sum to 0. This occurs when the two differential inputs are equal and opposite; that is, their algebraic sum is 0.

In a closed-loop application, a conventional op amp has its differential input voltage driven to near 0 under nontransient conditions. The AD8129/AD8130 generally has differential input voltages at each of its input pairs, even under equilibrium conditions. As a practical consideration, it is necessary to limit the differential input voltage internally with a clamp circuit.

Therefore, the input dynamic ranges are limited to about 2.5 V for the AD8130 and 0.5 V for the AD8129 (see the AD8129/AD8130 Specifications section for more detail). For this and other reasons, it is not recommended to reverse the input and feedback stages of the AD8129/AD8130, even though some apparently normal functionality may be observed under some conditions. A few simple circuits can illustrate how the active feedback architecture of the AD8129/AD8130 operates.

OP AMP CONFIGURATION

If only one of the input stages of the AD8129/AD8130 is used, it functions very much like a conventional op amp (see Figure 131). Classical inverting and noninverting op amps circuits can be created, and the basic governing equations are the same as for a conventional op amp. The unused input pins form the second input and should be shorted together and tied to ground or a midsupply voltage when they are not used.

Figure 131. With Both Inputs Grounded, the Feedback Stage Functions like an Op Amp: $V_{OUT} = V_{IN} (1 + R_F/R_G)$.

With the unused pair of inputs shorted, there is no differential voltage between them. This dictates that the differential input voltage of the used inputs is also 0 for closed-loop applications. Because this is the governing principle of conventional op amp circuits, an active feedback amplifier can function as a conventional op amp under these conditions.

Note that this circuit is presented only for illustration purposes to show the similarities of the active feedback architecture functionality to conventional op amp functionality. If it is desired to design a circuit that can be created from a conventional op amp, it is recommended to choose a conventional op amp with specifications that are better suited to that application. These op amp principles are the basis for offsetting the output, as described in the Output Offset/Level Translator section.

APPLICATIONS

BASIC GAIN CIRCUITS

The gain of the AD8129/AD8130 can be set with a pair of feedback resistors. The basic configuration is shown in Figure 132. The gain equation is the same as that of a conventional op amp: $G = 1 + R_F/R_G$. For unity-gain applications using the AD8130, R_F can be set to 0 (short circuit), and R_G can be removed (see Figure 133). The AD8129 is compensated to operate at gains of 10 and higher; therefore, shorting the feedback path to obtain unity gain causes oscillation.

Figure 132. Basic Gain Circuit: $V_{OUT} = V_{IN}(1 + R_F/R_G)$

Figure 133. An AD8130 with Unity Gain

The input signal can be applied either differentially or in a single-ended fashion—all that matters is the magnitude of the differential signal between the two inputs. For single-ended input applications, applying the signal to the +IN with –IN grounded creates a noninverting gain, while reversing these connections creates an inverting gain. Because the two inputs are high impedance and matched, both of these conditions provide the same high input impedance. Thus, an advantage of the active feedback architecture is the ability to make a high input impedance inverting op amp. If conventional op amps are used, a high impedance buffer followed by an inverting stage is needed. This requires two op amps.

TWISTED-PAIR CABLE, COMPOSITE VIDEO RECEIVER WITH EQUALIZATION USING AN AD8130

The AD8130 has excellent common-mode rejection at its inputs. This makes it an ideal candidate for a receiver for signals that are transmitted over long distances on twisted-pair cables. Category 5 cables are very common in office settings and are extensively used for data transmission. These cables can also be used for the analog transmission of signals such as video.

These long cables pick up noise from the environment they pass through. This noise does not favor one conductor over another and therefore is a common-mode signal. A receiver that rejects the common-mode signal on the cable can greatly enhance the signal-to-noise ratio performance of the link.

The AD8130 is also very easy to use as a differential receiver, because the differential inputs and the feedback inputs are entirely separate. This means that there is no interaction between the feedback network and the termination network, as there would be in conventional op amp types of receivers.

Another issue with long cables is that there is more attenuation of the signal at longer distances. Attenuation is also a function of frequency; it increases to roughly the square root of frequency.

For good fidelity of video circuits, the overall frequency response of the transmission channel should be flat vs. frequency. Because the cable attenuates the high frequencies, a frequency-selective boost circuit can be used to undo this effect. These circuits are called equalizers.

An equalizer uses frequency-dependent elements (Ls and Cs) to create a frequency response that is the opposite of the rest of the channel's response to create an overall flat response. There are many ways to create such circuits, but a common technique is to put the frequency-selective elements in the feedback path of an op amp circuit. The AD8130 in particular makes this easier than other circuits, because, once again, the feedback path is completely independent of the input path and there is no interaction.

The circuit in Figure 134 was developed as a receiver/equalizer for transmitting composite video over 300 meters of Category 5 cable. This cable has an attenuation of approximately 20 dB at 10 MHz for 300 meters. At 100 MHz, the attenuation is approximately 60 dB (see Figure 135).

Figure 134. An Equalizer Circuit for Composite Video Transmissions over 300 Meters of Category-5 Cable

Figure 135. Transmission Response of 300 Meters of Category-5 Cable

The feedback network is between Pin 6 and Pin 5 and from Pin 5 to ground. C1 and R_F create a corner frequency of about 800 kHz. The gain increases to provide about 15 dB of boost at 8 MHz. The response of this circuit is shown in Figure 136.

Figure 136. Frequency Response of Equalizer Circuit

It is difficult to calculate the exact component values via strictly mathematical means, because the equations for the cable attenuation are approximate and have functions that are not simply related to the responses of RC networks. The method used in this design was to approximate the required response via graphical means from the frequency response and then select components that would approximate this response. The circuit was then built, measured, and finally adjusted to obtain an acceptable response—in this case, flat to 9 MHz to within approximately 1 dB (see Figure 137).

Figure 137. Combined Response of Cable Plus Equalizer

OUTPUT OFFSET/LEVEL TRANSLATOR

The circuit in Figure 133 has the reference input (Pin 4) tied to ground, which produces a ground-referenced output signal. If it is desired to offset the output voltage from ground, the REF input can be used (see Figure 138). The level V_{OFFSET} appears at the output with unity gain.

Figure 138. The Voltage Applied to Pin 4 to the Unity-Gain Output Voltage Produced by V_{IN}

If the circuit has a gain higher than unity, the gain must be factored in. If R_G is connected to ground, the voltage applied to REF is multiplied by the gain of the circuit and appears at the output—just like a noninverting conventional op amp. This situation is not always desirable; the user may want V_{OFFSET} to appear at the output with unity gain.

One way to accomplish this is to drive both REF and R_G with the desired offset signal (see Figure 139). Superposition can be used to solve this circuit. First, break the connection between V_{OFFSET} and R_G. With R_G grounded, the gain from Pin 4 to V_{OUT} is $1 + R_F/R_G$. With Pin 4 grounded, the gain though R_G to V_{OUT} is $-R_F/R_G$. The sum of these is 1. If V_{REF} is delivered from a low impedance source, this works fine. However, if the delivered offset voltage is derived from a high impedance source, such as a voltage divider, its impedance affects the gain equation. This makes the circuit more complicated because it creates an interaction between the gain and offset voltage.

Figure 139. In this Circuit, V_{OFFSET} Appears at the Output with Unity Gain. This Circuit Works Well if the V_{OFFSET} Source Impedance Is Low.

A way around this is to apply the offset voltage to a voltage divider whose attenuation factor matches the gain of the amplifier and then apply this voltage to the high impedance REF input. This circuit first divides the desired offset voltage by the gain, and the amplifier multiplies it back up to unity (see Figure 140).

Figure 140. Adding an Attenuator at the Offset Input Causes It to Appear at the Output with Unity Gain.

RESISTORLESS GAIN OF 2

The voltage applied to the REF input (Pin 4) can also be a high bandwidth signal. If a unity-gain AD8130 has both +IN and REF driven with the same signal, there is unity gain from V_{IN} and unity gain from V_{REF}. Thus, the circuit has a gain of 2 and requires no resistors (see Figure 141).

Figure 141. Gain-of-2 Connections with No Resistors

SUMMER

A general summing circuit can be made by the previous technique. A unity-gain configured AD8130 has one signal applied to +IN, while the other signal is applied to REF. The output is the sum of the two input signals (see Figure 142).

Figure 142. A Summing Circuit that is Noninverting with High Input Impedance

This circuit offers several advantages over a conventional op amp inverting summing circuit. First, the inputs are both high impedance and the circuit is noninverting. It would require significant additional circuitry to make an op amp summing circuit that has high input impedance and is noninverting.

Another advantage is that the AD8130 circuit still preserves the full bandwidth of the part. In a conventional summing circuit, the noise gain is increased for each additional input, so the bandwidth response decreases accordingly. By this technique, four signals can be summed by applying them to two AD8130s and then summing the two outputs by a third AD8130.

CABLE-TAP AMPLIFIER

It is often desirable to have a video signal drive several pieces of equipment. However, the cable should only be terminated once at its endpoint; therefore, it is not appropriate to have a termination at each device. A loop-through connection allows a device to tap the video signal while not disturbing it by any excessive loading.

Such a connection, also referred to as a cable-tap amplifier, can be simply made with an AD8130 (see Figure 143). The circuit is configured with unity gain, and if no output offset is desired, the REF pin is grounded. The negative differential input is connected directly to the shield of the cable (or an associated connector) at the point at which it wants to be tapped.

Figure 143. The AD8130 Can Tap the Video Signal at Any Point Along the Cable Without Loading the Signal.

The center conductor connects to the positive differential input of the AD8130. The amplitude of the video signal at this point is unity, because it is between the two termination resistors. The AD8130 provides a high impedance to this signal so that the signal is not disturbed. A buffered unity-gain version of the video signal appears at the output.

POWER-DOWN

The AD8129/AD8130 have a power-down pin that can be used to lower the quiescent current when the amplifier is not being used. A logic low level on the $\overline{PD}$ pin causes the part to power down. Because there is no ground pin on the AD8129/AD8130, there is no logic reference to interface to standard logic levels. For this reason, the reference level for the $\overline{PD}$ input is V_S. If the AD8129/AD8130 are run with V_S = 5 V, there is direct compatibility with logic families. However, if V_S is higher than this, a level-shift circuit is needed to interface to conventional logic levels. A simple level-shifting circuit that is compatible with common logic families is presented in Figure 144.

Figure 144. Circuit that Shifts the Logic Level When V_S Is Not Equal to Approximately 5 V.

EXTREME OPERATING CONDITIONS

The AD8129/AD8130 are designed to provide high performance over a wide range of supply voltages. However, there are some extremes of operating conditions that have been observed to produce suboptimal results. One of these conditions occurs when the AD8130 is operated at unity gain with low supply voltage—less than approximately ±4 V.

At unity gain, the output drives FB directly. With supplies of $\pm V_S$ less than approximately ±4 V at unity gain, the output can drive FB's voltage too close to the rail for the circuit to stay properly biased. This can lead to a parasitic oscillation.

A way to prevent this is to limit the input signal swing with clamp diodes. Common silicon-junction signal diodes like the 1N4148 have a forward bias of approximately 0.7 V when about 1 mA of current flows through them. Two series pairs of such diodes connected antiparallel across the differential inputs can be used to clamp the input signal and prevent this condition. It should be noted that the REF input can also shift the output signal; therefore, this technique only works when REF is at ground or close to it (see Figure 145).

Figure 145. Clamping Diodes at the Input Limits the Input Swing Amplitude

Another problem can occur with the AD8129 operating at a supply voltage of greater than or equal to ±12 V. The architecture causes the supply current to increase as the input differential voltage increases. If the AD8129 differential inputs are overdriven too far, excessive current can flow into the device and potentially cause permanent damage.

A practical means to prevent this from occurring is to clamp the inputs differentially with a pair of antiparallel Schottky diodes (see Figure 146). These diodes have a lower forward voltage of approximately 0.4 V. If the differential voltage across the inputs is restricted to these conditions, no excess current is drawn by the AD8129 under these operating conditions.

If the supply voltage is restricted to less than ±11 V, the internal clamping circuit limits the differential voltage and excessive supply current is not drawn. The external clamp circuit is not needed.

Figure 146. Schottky Diodes Across the Inputs Limits the Input Differential Voltage

In both circuits, the input series resistors function to limit the current through the diodes when they are forward biased. As a practical matter, these resistors must be matched so that the CMRR is preserved at high frequencies. These resistors have minimal effect on the CMRR at low frequency.

POWER DISSIPATION

The AD8129/AD8130 can operate with supply voltages from +5 V to ±12 V. The major reason for such a wide supply range is to provide a wide input common-mode range for systems that can require this. This would be encountered when significant common-mode noise couples into the input path. For applications that do not require a wide dynamic range for the input or output, it is recommended to operate with lower supply voltages.

The AD8129/AD8130 is also available in a very small 8-lead MSOP package. This package has higher thermal impedance than larger packages and operates at a higher temperature with the same amount of power dissipation. Certain operating conditions that are within the specifications range of the parts can cause excess power dissipation. Caution should be exercised.

The power dissipation is a function of several operating conditions, including the supply voltage, the input differential voltage, the output load, and the signal frequency.

A basic starting point is to calculate the quiescent power dissipation with no signal and no differential input voltage. This is just the product of the total supply voltage and the quiescent operating current. The maximum operating supply voltage is 26.4 V, and the quiescent current is 13 mA. This causes a quiescent power dissipation of 343 mW. For the MSOP package, the θ_{JA} specification is 142°C/W. Therefore, the quiescent power causes about a 49°C rise above ambient in the MSOP package.

The current consumption is also a function of the differential input voltage (see Figure 113 and Figure 114). This current should be added onto the quiescent current and then multiplied by the total supply voltage to calculate the power.

The AD8129/AD8130 can directly drive loads of as low as 100 Ω, such as a terminated 50 Ω cable. The worst-case power dissipation in the output stage occurs when the output is at midsupply. As an example, for a 12 V supply with the output driving a 250 Ω load to ground, the maximum power dissipation in the output occurs when the output voltage is 6 V. The load current is 6 V/250 Ω = 24 mA. This same current flows through the output across a 6 V drop from V_S. It dissipates 144 mW. For the 8-lead MSOP package, this causes a temperature rise of 20°C above ambient. Although this is a worst-case number, it is apparent that this can be a considerable additional amount of power dissipation.

Several changes can be made to alleviate this. One is to use the standard 8-lead SOIC package. This lowers the thermal impedance to 121°C/W, which is a 15% improvement. Another is to use a lower supply voltage unless absolutely necessary.

Finally, do not use the AD8129/AD8130 when it is operating on high supply voltages to directly drive a heavy load. It is best to use a second op amp after the output stage. Some of the gain can be shifted to this stage so that the signal swing at the output of the AD8129/AD8130 is not too large.

LAYOUT, GROUNDING, AND BYPASSING

The AD8129/AD8130 are very high speed parts that can be sensitive to the PCB environment in which they operate. Realizing their superior specifications requires attention to various details of standard high speed PCB design practice.

The first requirement is for a good solid ground plane that covers as much of the board area around the AD8129/AD8130 as possible. The only exception to this is that the ground plane around the FB pin should be kept a few millimeters away, and the ground should be removed from the inner layers and the opposite side of the board under this pin. This minimizes the stray capacitance on this node and helps preserve the gain flatness vs. frequency.

The power supply pins should be bypassed as close as possible to the device to the nearby ground plane. Good high frequency ceramic chip capacitors should be used, and the bypassing should be done with a capacitance value of 0.01 μF to 0.1 μF for each supply. Farther away, low frequency bypassing should be provided with 10 μF tantalum capacitors from each supply to ground.

The signal routing should be short and direct to avoid parasitic effects. Where possible, signals should be run over ground planes to avoid radiating or to avoid being susceptible to other radiation sources.

OUTLINE DIMENSIONS

COMPLIANT TO JEDEC STANDARDS MS-012-AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 147. 8-Lead Standard Small Outline Package [SOIC] Narrow Body (R-8) Dimensions shown in millimeters and (inches)

COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 148. 8-Lead Mini Small Outline Package [MSOP] (RM-8) Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range[1]	Package Description	Package Option	Branding
AD8129AR	−40°C to +85°C	8-Lead SOIC	R-8	
AD8129AR-REEL	−40°C to +85°C	8-Lead SOIC, 13" Tape and Reel	R-8	
AD8129AR-REEL7	−40°C to +85°C	8-Lead SOIC, 7" Tape and Reel	R-8	
AD8129ARZ[2]	−40°C to +85°C	8-Lead SOIC	R-8	
AD8129ARZ-REEL[2]	−40°C to +85°C	8-Lead SOIC, 13" Tape and Reel	R-8	
AD8129ARZ-REEL7[2]	−40°C to +85°C	8-Lead SOIC, 7" Tape and Reel	R-8	
AD8129ARM	−40°C to +85°C	8-Lead MSOP	RM-8	HQA
AD8129ARM-REEL	−40°C to +85°C	8-Lead MSOP, 13" Tape and Reel	RM-8	HQA
AD8129ARM-REEL7	−40°C to +85°C	8-Lead MSOP, 7" Tape and Reel	RM-8	HQA
AD8129ARMZ[2]	−40°C to +85°C	8-Lead MSOP	RM-8	HQA#
AD8129ARMZ-REEL[2]	−40°C to +85°C	8-Lead MSOP, 13" Tape and Reel	RM-8	HQA#
AD8129ARMZ-REEL7[2]	−40°C to +85°C	8-Lead MSOP, 7" Tape and Reel	RM-8	HQA#
AD8130AR	−40°C to +85°C	8-Lead SOIC	R-8	
AD8130AR-REEL	−40°C to +85°C	8-Lead SOIC, 13" Tape and Reel	R-8	
AD8130AR-REEL7	−40°C to +85°C	8-Lead SOIC, 7" Tape and Reel	R-8	
AD8130ARZ[2]	−40°C to +85°C	8-Lead SOIC	R-8	
AD8130ARZ-REEL[2]	−40°C to +85°C	8-Lead SOIC, 13" Tape and Reel	R-8	
AD8130ARZ-REEL7[2]	−40°C to +85°C	8-Lead SOIC, 7" Tape and Reel	R-8	
AD8130ARM	−40°C to +85°C	8-Lead MSOP	RM-8	HPA
AD8130ARM-REEL	−40°C to +85°C	8-Lead MSOP, 13" Tape and Reel	RM-8	HPA
AD8130ARM-REEL7	−40°C to +85°C	8-Lead MSOP, 7" Tape and Reel	RM-8	HPA
AD8130ARMZ[2]	−40°C to +85°C	8-Lead MSOP	RM-8	HPA#
AD8130ARMZ-REEL[2]	−40°C to +85°C	8-Lead MSOP, 13" Tape and Reel	RM-8	HPA#
AD8130ARMZ-REEL7[2]	−40°C to +85°C	8-Lead MSOP, 7" Tape and Reel	RM-8	HPA#

[1] Operating temperature range for ±5 V or +5 V operation is −40°C to +125°C.
[2] Z = Pb-free part; # indicates lead-free, may be top or bottom marked.

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