

Automotive Dual N-Channel 40 V (D-S) 175 °C MOSFETs

PRODUCT SUMMARY

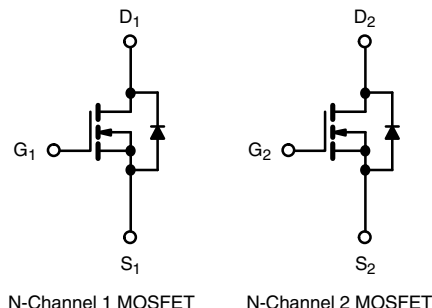
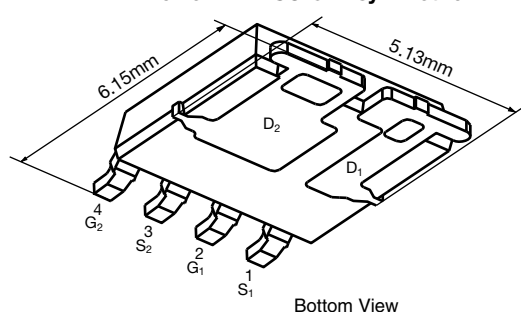
	N-CHANNEL 1	N-CHANNEL 2
V_{DS} (V)	40	40
$R_{DS(on)}$ (Ω) at $V_{GS} = 10$ V	0.022	0.011
$R_{DS(on)}$ (Ω) at $V_{GS} = 4.5$ V	0.026	0.013
I_D (A)	15	45
Configuration	Dual N	

FEATURES

- TrenchFET® Power MOSFET
- AEC-Q101 Qualified^d
- 100 % R_g and UIS Tested
- Material categorization:
For definitions of compliance please see www.vishay.com/doc?99912



PowerPAK® SO-8L Asymmetric



ORDERING INFORMATION

Package	PowerPAK SO-8L Dual Asymmetric
Lead (Pb)-free and Halogen-free	SQJ942EP-T1-GE3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER		SYMBOL	N-CHANNEL 1	N-CHANNEL 2	UNIT
Drain-Source Voltage		V _{DS}	40	40	V
Gate-Source Voltage		V _{GS}	± 20		
Continuous Drain Current ^a	T _C = 25 °C	I _D	15	45	A
	T _C = 125 °C		15	32	
Continuous Source Current (Diode Conduction) ^a		I _S	15	44	
Pulsed Drain Current ^b		I _{DM}	60	180	
Single Pulse Avalanche Current	L = 0.1 mH	I _{AS}	19	27	
Single Pulse Avalanche Energy		E _{AS}	18.5	36.5	mJ
Maximum Power Dissipation ^b	T _C = 25 °C	P _D	17	48	W
	T _C = 125 °C		6	16	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to + 175		°C
Soldering Recommendations (Peak Temperature) ^{e, f}			260		

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	N-CHANNEL 1	N-CHANNEL 2	UNIT
Junction-to-Ambient	R_{thJA}	75	70	°C/W
Junction-to-Case (Drain)	R_{thJC}	9	3.1	

Notes

- Package limited.
- Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %.
- When mounted on 1" square PCB (FR4 material).
- Parametric verification ongoing.
- See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.



SPECIFICATIONS (T _C = 25 °C, unless otherwise noted)								
PARAMETER	SYMBOL	TEST CONDITIONS			MIN.	TYP.	MAX.	UNIT
Static								
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		N-Ch 1	40	-	-	V
		V _{GS} = 0 V, I _D = 250 μA		N-Ch 2	40	-	-	
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		N-Ch 1	1.3	1.8	2.3	
		V _{DS} = V _{GS} , I _D = 250 μA		N-Ch 2	1.3	1.8	2.3	
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V		N-Ch 1	-	-	± 100	nA
				N-Ch 2	-	-	± 100	
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V	V _{DS} 40 V	N-Ch 1	-	-	1	μA
		V _{GS} = 0 V	V _{DS} = - 40 V	N-Ch 2	-	-	1	
		V _{GS} = 0 V	V _{DS} = 40 V, T _J = 125 °C	N-Ch 1	-	-	50	
		V _{GS} = 0 V	V _{DS} = 40 V, T _J = 125 °C	N-Ch 2	-	-	50	
		V _{GS} = 0 V	V _{DS} = 40 V, T _J = 175 °C	N-Ch 1	-	-	150	
		V _{GS} = 0 V	V _{DS} = 40 V, T _J = 175 °C	N-Ch 2	-	-	150	
On-State Drain Current ^a	I _{D(on)}	V _{GS} = 10 V	V _{DS} ≥ 5 V	N-Ch 1	30	-	-	A
		V _{GS} = 10 V	V _{DS} ≥ 5 V	N-Ch 2	30	-	-	
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V	I _D = 7.8 A	N-Ch 1	-	0.018	0.022	Ω
		V _{GS} = 10 V	I _D = 10.1 A	N-Ch 2	-	0.009	0.011	
		V _{GS} = 10 V	I _D = 7.8 A, T _J = 125 °C	N-Ch 1	-	-	0.032	
		V _{GS} = 10 V	I _D = 10.1 A, T _J = 125 °C	N-Ch 2	-	-	0.017	
		V _{GS} = 10 V	I _D = 7.8 A, T _J = 175 °C	N-Ch 1	-	-	0.038	
		V _{GS} = 10 V	I _D = 10.1 A, T _J = 175 °C	N-Ch 2	-	-	0.020	
		V _{GS} = 4.5 V	I _D = 7.1 A	N-Ch 1	-	0.022	0.026	
		V _{GS} = 4.5 V	I _D = 9.3 A	N-Ch 2	-	0.011	0.013	
Forward Transconductance ^b	g _{fs}	V _{DS} = 15 V, I _D = 7.8 A		N-Ch 1	-	46	-	S
		V _{DS} = 15 V, I _D = 10.1 A		N-Ch 2	-	73	-	
Dynamic ^b								
Input Capacitance	C _{iss}	V _{GS} = 0 V	V _{DS} = 20 V, f = 1 MHz	N-Ch 1	-	647	809	pF
		V _{GS} = 0 V	V _{DS} = 20 V, f = 1 MHz	N-Ch 2	-	1161	1451	
Output Capacitance	C _{oss}	V _{GS} = 0 V	V _{DS} = 20 V, f = 1 MHz	N-Ch 1	-	105	131	
		V _{GS} = 0 V	V _{DS} = 20 V, f = 1 MHz	N-Ch 2	-	178	222	
Reverse Transfer Capacitance	C _{rss}	V _{GS} = 0 V	V _{DS} = 20 V, f = 1 MHz	N-Ch 1	-	42	53	
		V _{GS} = 0 V	V _{DS} = 20 V, f = 1 MHz	N-Ch 2	-	68	85	
Total Gate Charge ^c	Q _g	V _{GS} = 10 V	V _{DS} = 20 V, I _D = 16 A	N-Ch 1	-	13.1	19.7	nC
		V _{GS} = 10 V	V _{DS} = 20 V, I _D = 6 A	N-Ch 2	-	22.5	33.8	
Gate-Source Charge ^c	Q _{gs}	V _{GS} = 10 V	V _{DS} = 20 V, I _D = 16 A	N-Ch 1	-	2.12	-	
		V _{GS} = 10 V	V _{DS} = 20 V, I _D = 6 A	N-Ch 2	-	3.35	-	
Gate-Drain Charge ^c	Q _{gd}	V _{GS} = 10 V	V _{DS} = 20 V, I _D = 16 A	N-Ch 1	-	1.84	-	
		V _{GS} = 10 V	V _{DS} = 20 V, I _D = 6 A	N-Ch 2	-	3.14	-	
Gate Resistance	R _g	f = 1 MHz		N-Ch 1	1.5	3.02	5	Ω
				N-Ch 2	2.05	4.11	7	

Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.
c. Independent of operating temperature.

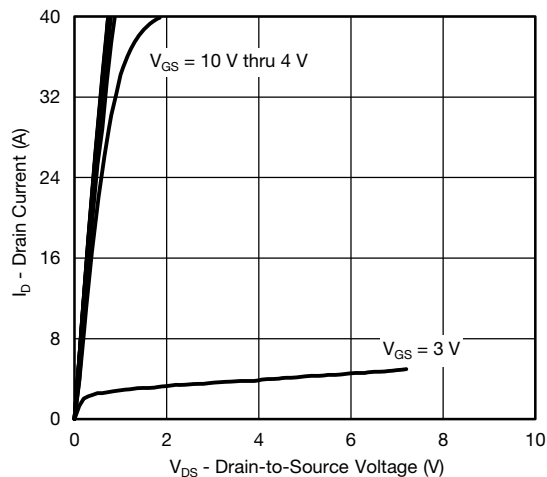
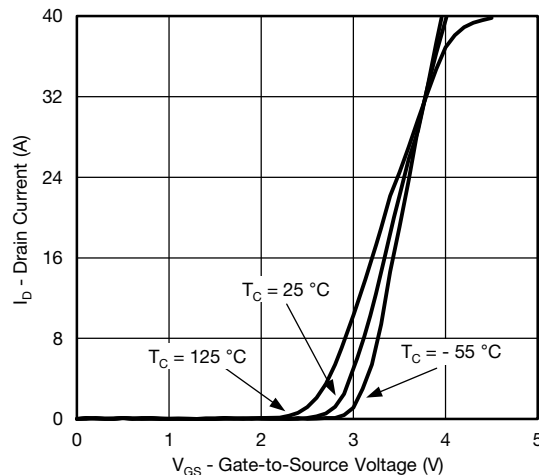
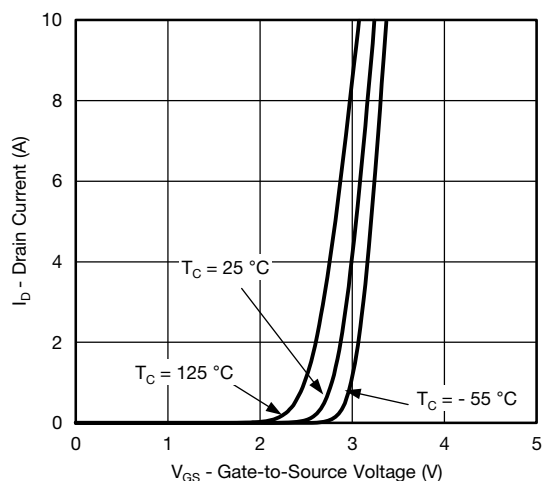
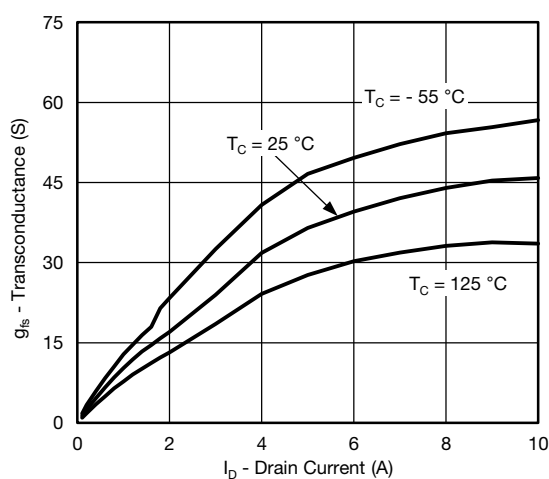
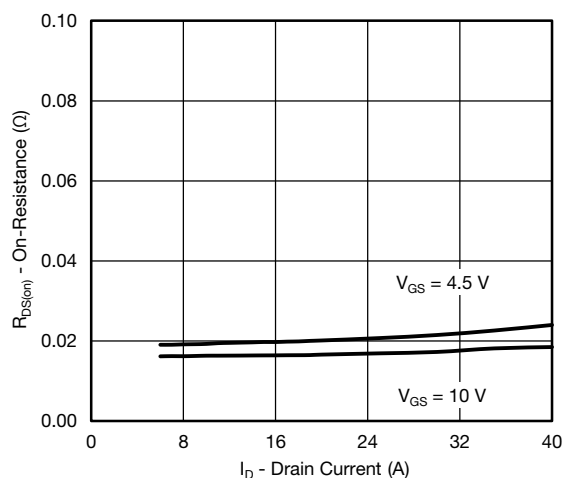
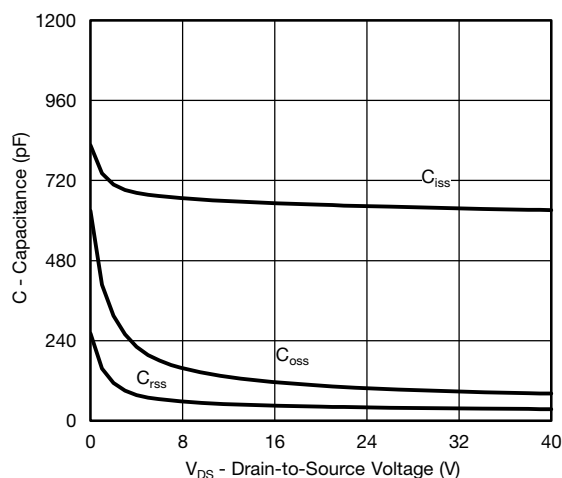


SPECIFICATIONS (T _C = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Turn-On Delay Time ^c	t _{d(on)}	V _{DD} = 20 V, R _L = 20 Ω I _D ≡ 1 A, V _{GEN} = 10 V, R _g = 1 Ω	N-Ch 1	-	33	50	ns
		V _{DD} = 20 V, R _L = 20 Ω I _D ≡ 1 A, V _{GEN} = 10 V, R _g = 1 Ω	N-Ch 2	-	40	60	
Rise Time ^c	t _r	V _{DD} = 20 V, R _L = 20 Ω I _D ≡ 1 A, V _{GEN} = 10 V, R _g = 1 Ω	N-Ch 1	-	25	38	
		V _{DD} = 20 V, R _L = 20 Ω I _D ≡ 1 A, V _{GEN} = 10 V, R _g = 1 Ω	N-Ch 2	-	31	46	
Turn-Off Delay Time ^c	t _{d(off)}	V _{DD} = 20 V, R _L = 20 Ω I _D ≡ 1 A, V _{GEN} = 10 V, R _g = 1 Ω	N-Ch 1	-	29	43	
		V _{DD} = 20 V, R _L = 20 Ω I _D ≡ 1 A, V _{GEN} = 10 V, R _g = 1 Ω	N-Ch 2	-	52	78	
Fall Time ^c	t _f	V _{DD} = 20 V, R _L = 20 Ω I _D ≡ 1 A, V _{GEN} = 10 V, R _g = 1 Ω	N-Ch 1	-	12	18	
		V _{DD} = 20 V, R _L = 20 Ω I _D ≡ 1 A, V _{GEN} = 10 V, R _g = 1 Ω	N-Ch 2	-	16	24	
Source-Drain Diode Ratings and Characteristics ^b							
Pulsed Current ^a	I _{SM}		N-Ch 1	-	-	60	A
			N-Ch 2	-	-	180	
Forward Voltage	V _{SD}	I _S = 5.2 A	N-Ch 1	-	0.8	1.2	V
		I _S = 6.8 A	N-Ch 2	-	0.8	1.2	

Notes

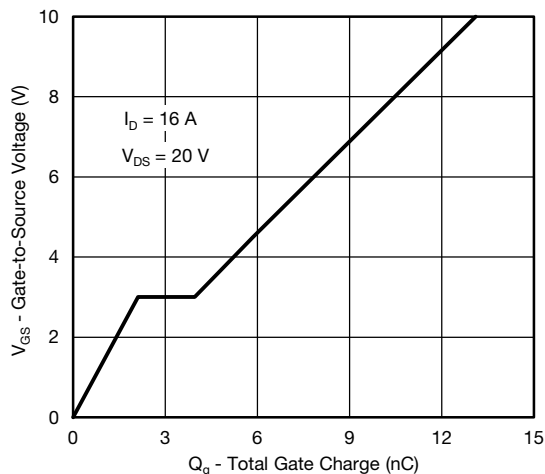
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.
c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

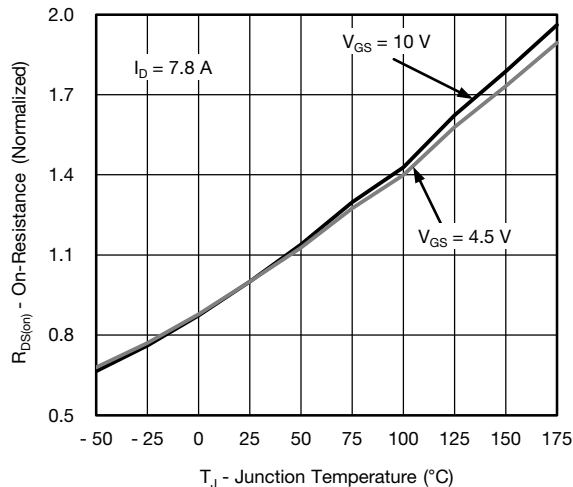
N-CHANNEL 1 TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Output Characteristics

Transfer Characteristics

Transfer Characteristics

Transconductance

On-Resistance vs. Drain Current

Capacitance



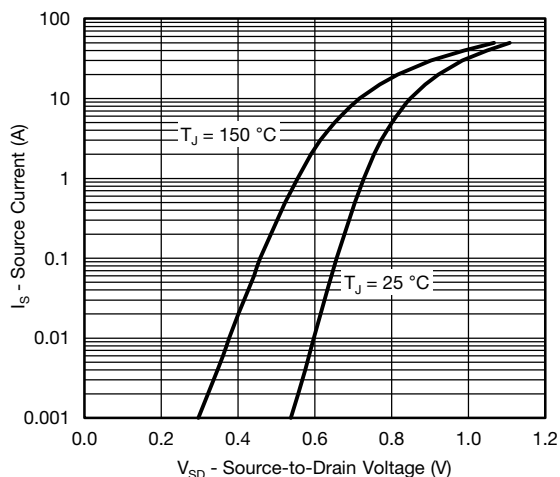
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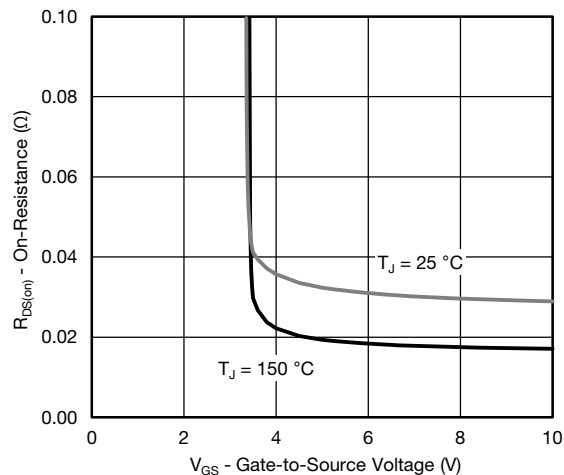
Gate Charge



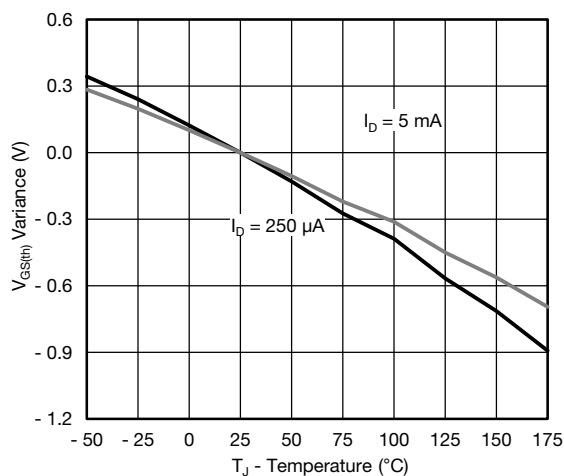
On-Resistance vs. Junction Temperature



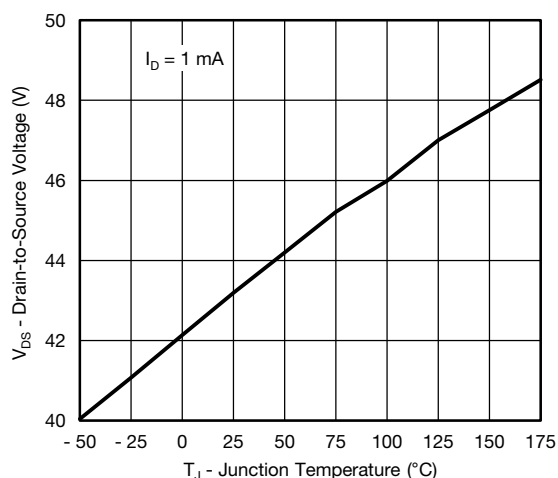
Source Drain Diode Forward Voltage



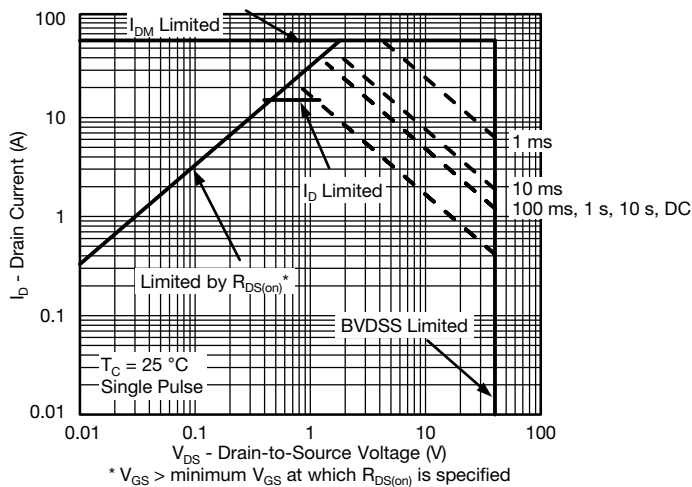
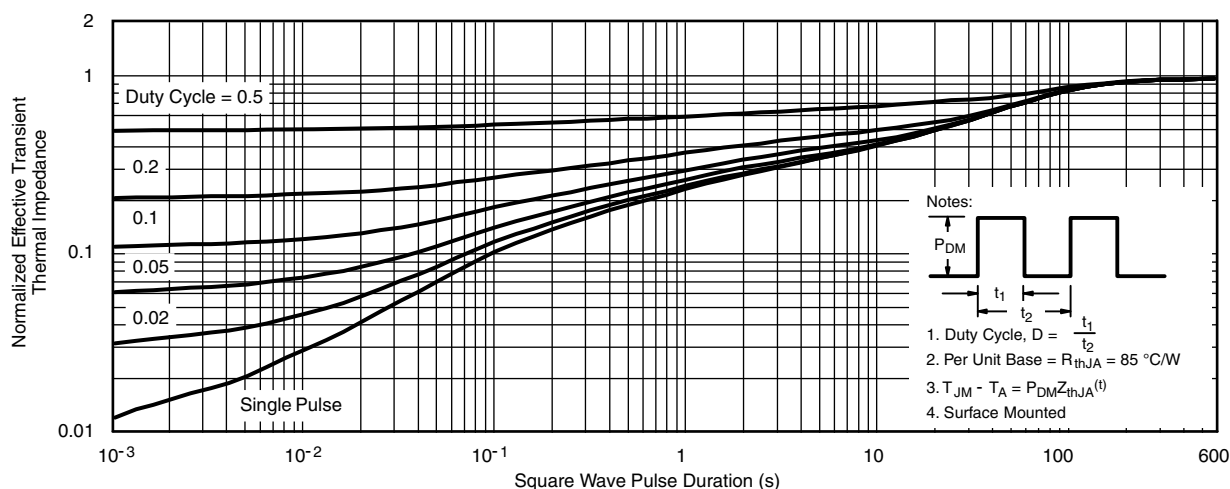
On-Resistance vs. Gate-to-Source Voltage

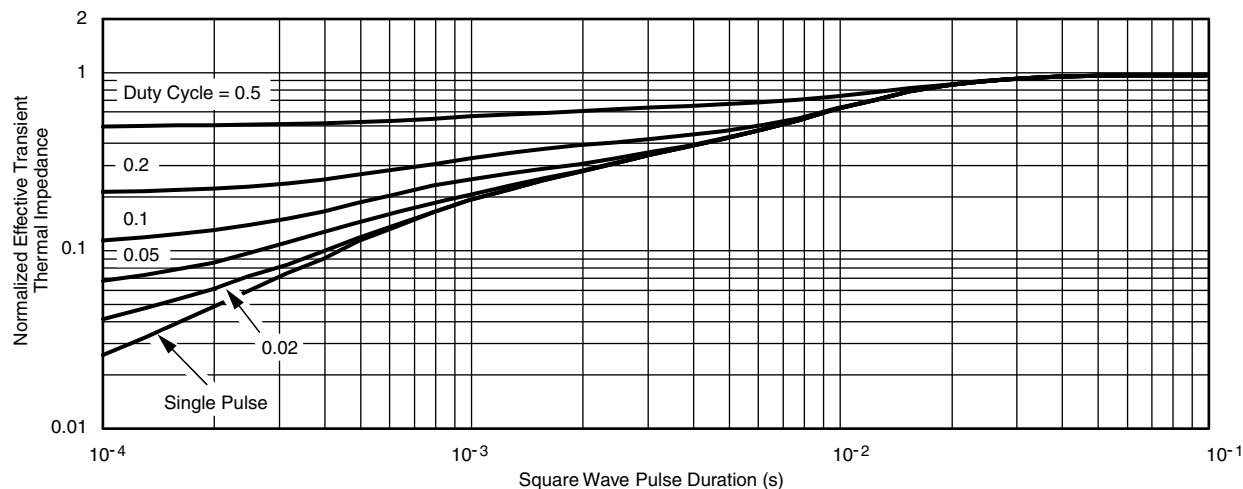


Threshold Voltage



Drain Source Breakdown vs. Junction Temperature

N-CHANNEL 1 TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Safe Operating Area

Normalized Thermal Transient Impedance, Junction-to-Ambient

N-CHANNEL 1 TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)


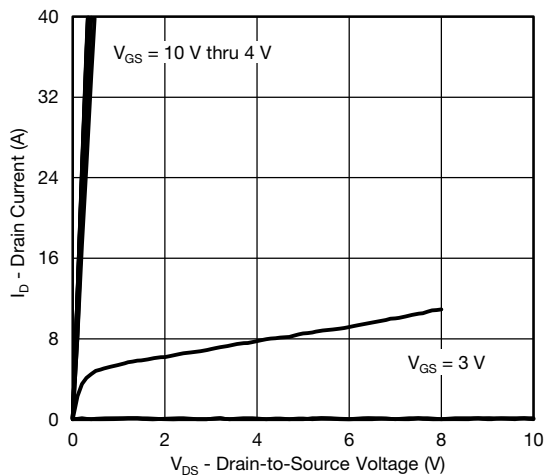
Normalized Thermal Transient Impedance, Junction-to-Case

Note

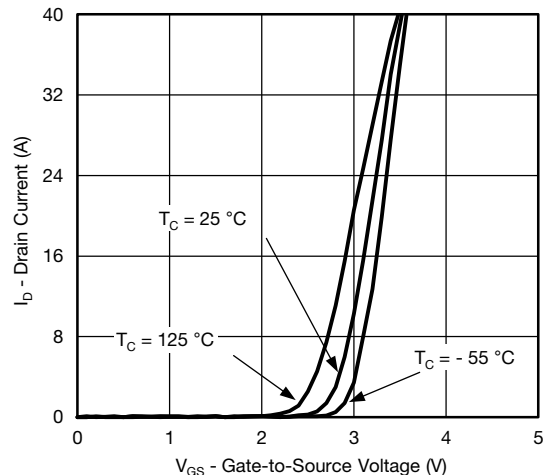
- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient ($25\text{ }^{\circ}\text{C}$)
 - Normalized Transient Thermal Impedance Junction-to-Case ($25\text{ }^{\circ}\text{C}$)
 are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.



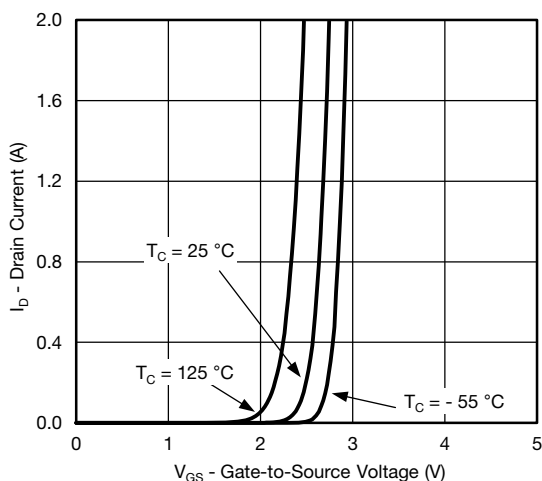
N-CHANNEL 2 TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)



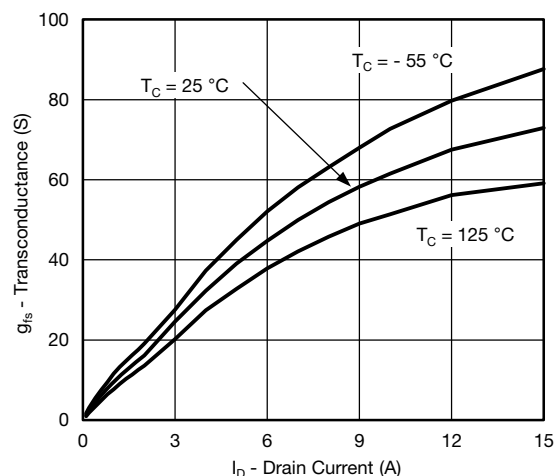
Output Characteristics



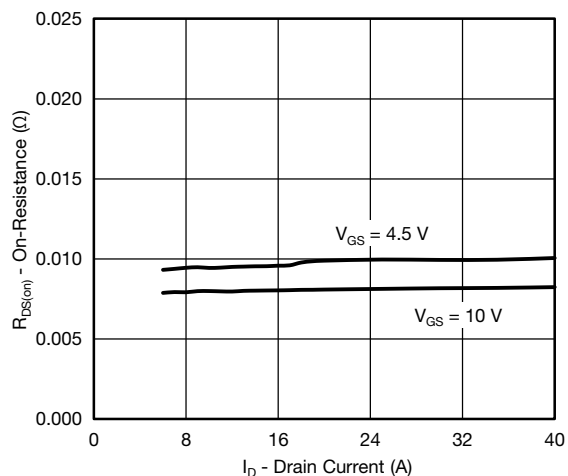
Transfer Characteristics



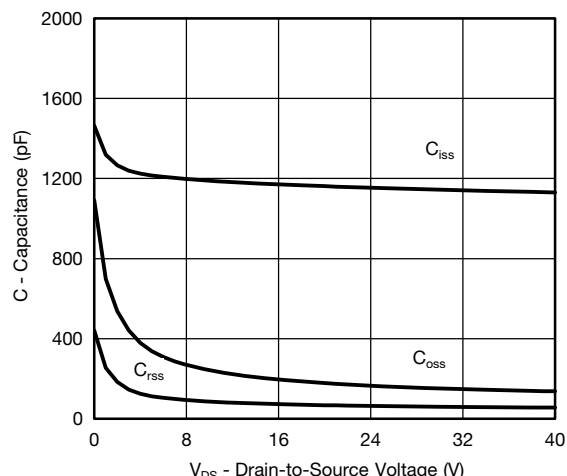
Transfer Characteristics



Transconductance



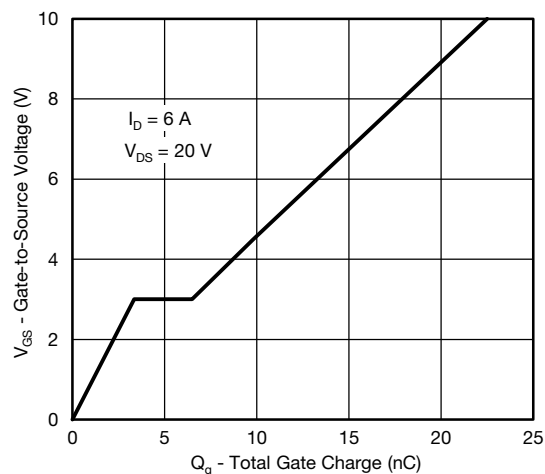
On-Resistance vs. Drain Current



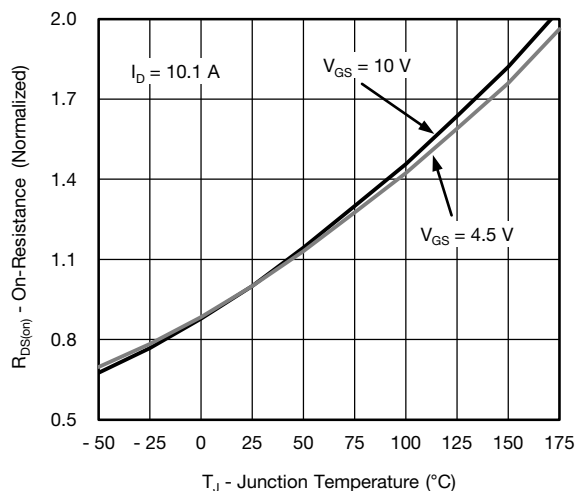
Capacitance



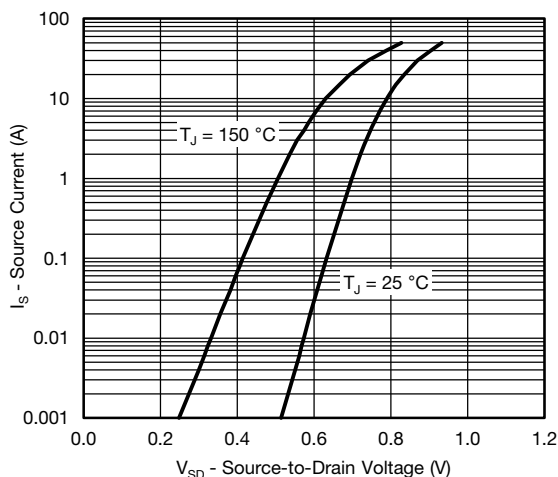
N-CHANNEL 2 TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)



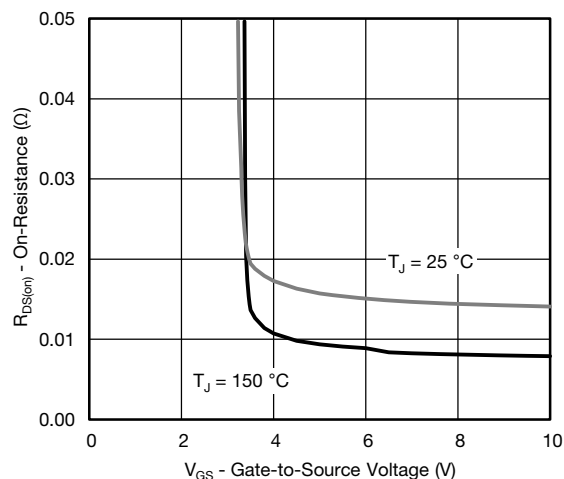
Gate Charge



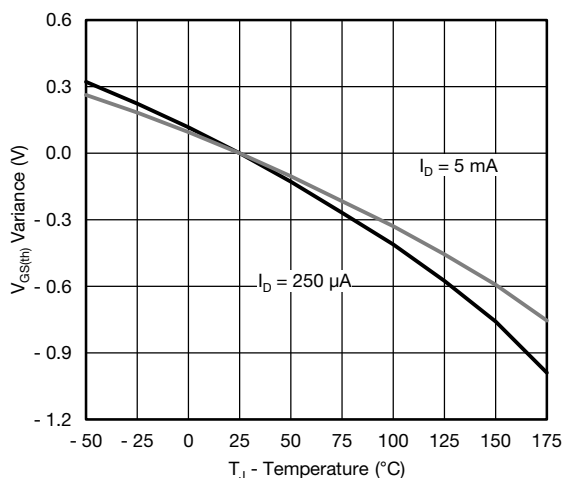
On-Resistance vs. Junction Temperature



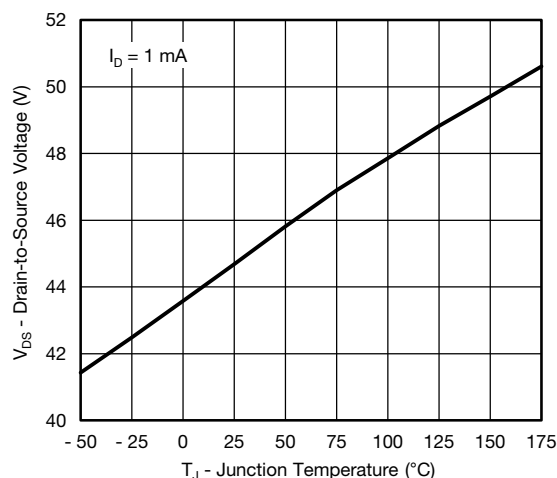
Source Drain Diode Forward Voltage



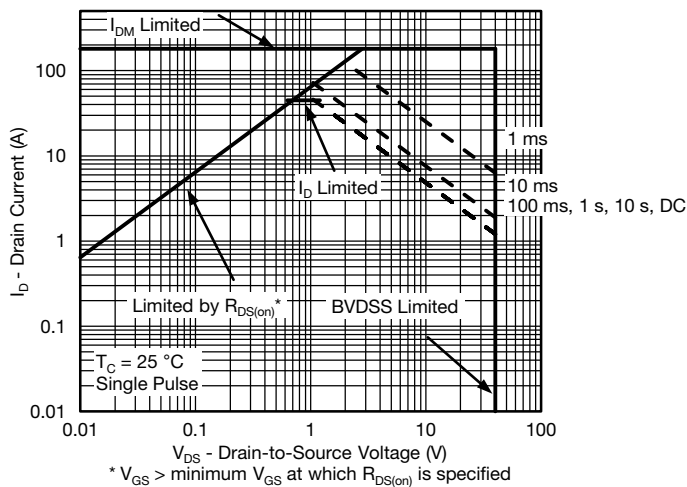
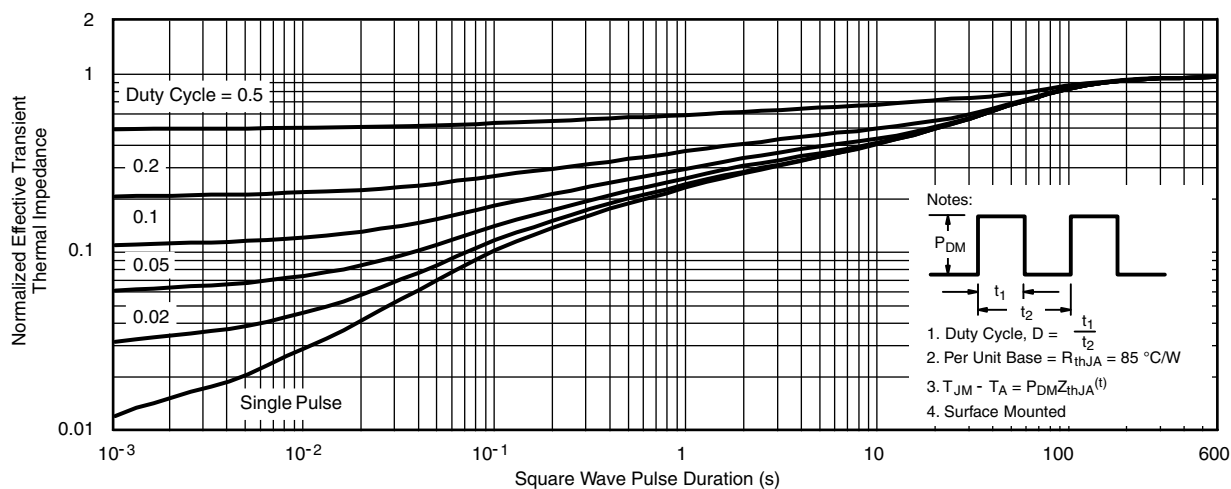
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

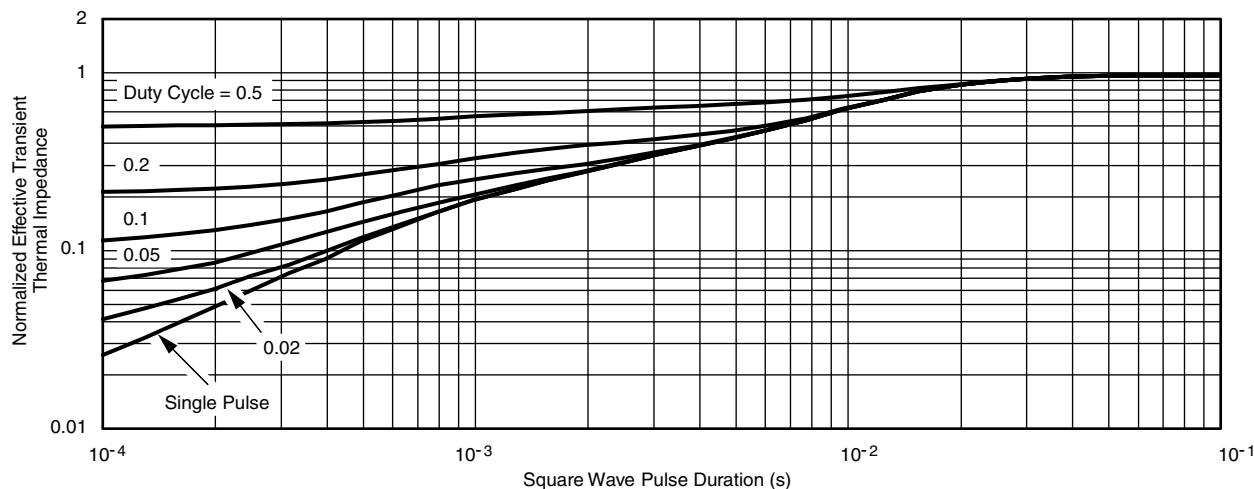


Drain Source Breakdown vs. Junction Temperature

N-CHANNEL 2 TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Safe Operating Area

Normalized Thermal Transient Impedance, Junction-to-Ambient



N-CHANNEL 2 TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient ($25\text{ }^{\circ}\text{C}$)
 - Normalized Transient Thermal Impedance Junction-to-Case ($25\text{ }^{\circ}\text{C}$)are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?62669.

**PowerPAK® SO-8L**

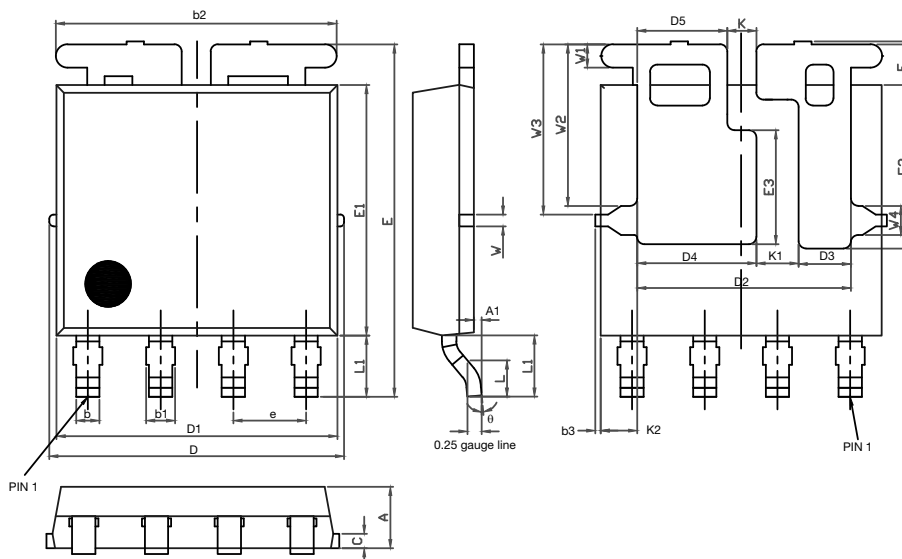
Ordering codes for the SQ rugged series power MOSFETs in the PowerPAK SO-8L package:

DATASHEET PART NUMBER	OLD ORDERING CODE ^a	NEW ORDERING CODE
SQJ200EP	-	SQJ200EP-T1_GE3
SQJ202EP	-	SQJ202EP-T1_GE3
SQJ401EP	SQJ401EP-T1-GE3	SQJ401EP-T1_GE3
SQJ402EP	SQJ402EP-T1-GE3	SQJ402EP-T1_GE3
SQJ403EEP	SQJ403EEP-T1-GE3	SQJ403EEP-T1_GE3
SQJ403EP	-	SQJ403EP-T1_GE3
SQJ410EP	SQJ410EP-T1-GE3	SQJ410EP-T1_GE3
SQJ412EP	SQJ412EP-T1-GE3	SQJ412EP-T1_GE3
SQJ422EP	SQJ422EP-T1-GE3	SQJ422EP-T1_GE3
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SQJ459EP	-	SQJ459EP-T1_GE3
SQJ460AEP	-	SQJ460AEP-T1_GE3
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SQJ840EP	SQJ840EP-T1-GE3	SQJ840EP-T1_GE3
SQJ844AEP	SQJ844AEP-T1-GE3	SQJ844AEP-T1_GE3
SQJ850EP	SQJ850EP-T1-GE3	SQJ850EP-T1_GE3
SQJ858AEP	SQJ858AEP-T1-GE3	SQJ858AEP-T1_GE3
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SQJ951EP	SQJ951EP-T1-GE3	SQJ951EP-T1_GE3
SQJ952EP	-	SQJ952EP-T1_GE3
SQJ956EP	SQJ956EP-T1-GE3	SQJ956EP-T1_GE3
SQJ960EP	SQJ960EP-T1-GE3	SQJ960EP-T1_GE3
SQJ963EP	SQJ963EP-T1-GE3	SQJ963EP-T1_GE3
SQJ968EP	SQJ968EP-T1-GE3	SQJ968EP-T1_GE3
SQJ980AEP	SQJ980AEP-T1-GE3	SQJ980AEP-T1_GE3
SQJ992EP	SQJ992EP-T1-GE3	SQJ992EP-T1_GE3

Note

a. Old ordering code is obsolete and no longer valid for new orders

PowerPAK® SO-8L Assymmetric Case Outline



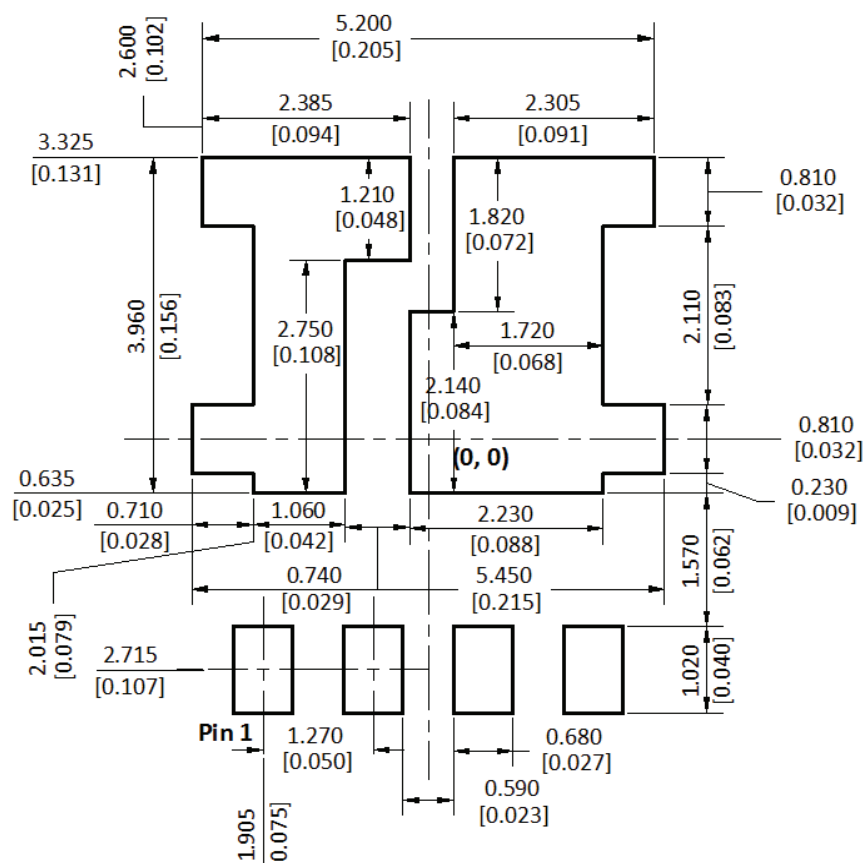
DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00	1.07	1.14	0.039	0.042	0.045
A1	0.00	0.06	0.13	0.000	0.003	0.005
b	0.33	0.41	0.48	0.013	0.016	0.019
b1	0.44	0.51	0.58	0.017	0.020	0.023
b2	4.80	4.90	5.00	0.189	0.193	0.197
b3	0.04	0.12	0.20	0.002	0.005	0.008
c	0.20	0.25	0.30	0.008	0.010	0.012
D	5.00	5.13	5.25	0.197	0.202	0.207
D1	4.80	4.90	5.00	0.189	0.193	0.197
D2	3.63	3.73	3.83	0.143	0.147	0.151
D3	0.81	0.91	1.01	0.032	0.036	0.040
D4	1.98	2.08	2.18	0.078	0.082	0.086
D5	1.47	1.57	1.67	0.058	0.062	0.066
e	1.20	1.27	1.34	0.047	0.050	0.053
E	6.05	6.15	6.25	0.238	0.242	0.246
E1	4.27	4.37	4.47	0.168	0.172	0.176
E2	2.75	2.85	2.95	0.108	0.112	0.116
E3	1.89	1.99	2.09	0.074	0.078	0.082
F	0.05	0.12	0.19	0.002	0.005	0.007
L	0.62	0.72	0.82	0.024	0.028	0.032
L1	0.92	1.07	1.22	0.036	0.042	0.048
K	0.41	0.51	0.61	0.016	0.020	0.024
K1	0.64	0.74	0.84	0.025	0.029	0.033
K2	0.54	0.64	0.74	0.021	0.025	0.029
W	0.13	0.23	0.33	0.005	0.009	0.013
W1	0.31	0.41	0.51	0.012	0.016	0.020
W2	2.72	2.82	2.92	0.107	0.111	0.115
W3	2.86	2.96	3.06	0.113	0.117	0.120
W4	0.41	0.51	0.61	0.016	0.020	0.024
θ	5°	10°	12°	5°	10°	12°

DWG: 6009

Note

- Millimeters will govern

RECOMMENDED MINIMUM PADs FOR PowerPAK® SO-8L DUAL ASYMMETRIC



Recommended Minimum Pads
Dimensions in mm [inches]



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