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# ***THS4211/15EVM***

## *User's Guide*

| DEVICE  | EVM TITLE     | USER'S GUIDE           | DESCRIPTION                                | SHUTDOWN |
|---------|---------------|------------------------|--|----------|
| THS4211 | THS4211EVM    | THS4211/15EVM          | Configurable for gains $\geq +2/-1$        | No       |
| THS4215 | THS4215EVM    | THS4211/15EVM          | Configurable for gains $\geq +2/-1$        | Yes      |
| THS4211 | THS4211EVM-UG | THS4211 Unity Gain EVM | Noninverting unity gain configuration only | No       |

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## **EVM WARNINGS AND RESTRICTIONS**

It is important to operate this EVM within the specified input and output ranges described in the EVM User's Guide. The input supply voltage ( $\pm V_S$ ) should be no greater than  $\pm 7.5$  V for dual supply ( $V_S$  should be no greater than 15 V for single supply operation). The output current ( $I_O$ ) should be no greater than 100 mA.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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# Read This First

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### *Information About Cautions and Warnings*

This book may contain cautions and warnings.

**This is an example of a caution statement.**

**A caution statement describes a situation that could potentially damage your software or equipment.**

**This is an example of a warning statement.**

**A warning statement describes a situation that could potentially cause harm to you.**

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### *FCC Warning*

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.



This EVM contains components that can potentially be damaged by electrostatic discharge. Always transport and store the EVM in its supplied ESD bag when not in use. Handle using an antistatic wristband. Operate on an antistatic work surface. For more information on proper handling, refer to SSYA008.

### **Related Documentation From Texas Instruments**

The URLs below are correct as of the date of publication of this manual. Texas Instruments applications apologizes if they change over time.

- THS4211/THS4215 data sheet (SLOS400)
- Application report (SLMA002), *PowerPAD Thermally Enhanced Package*, <http://www-s.ti.com/sc/psheets/slma004/slma002.pdf>
- Application report (SLMA004), *PowerPAD Made Easy*, <http://www-s.ti.com/sc/psheets/slma004/slma004.pdf>
- Application report (SSYA008), *Electrostatic Discharge (ESD)*, <http://www-s.ti.com/sc/psheets/ssya008/ssya008.pdf>
- Application report (SLOA102), *High Speed PCB Layout Tips*, <http://www-s.ti.com/sc/psheets/sloa102/sloa102.pdf>

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# Introduction and Description

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This EVM provides a platform for testing the THS4211 and THS4215 in 8-pin MSOP (DGN) and 8-pin LLP (DRB) with and without power down. It contains the high-speed op amp, a number of passive components, and various features and footprints that enable the user to experiment, test, and verify various operational amplifier circuit implementations.

If the user wants to evaluate a unity gain noninverting buffer, that configuration is not recommended with this EVM. The user needs to obtain a THS4211 unity gain EVM, THS4211EVM-UG. See Section 3.2.

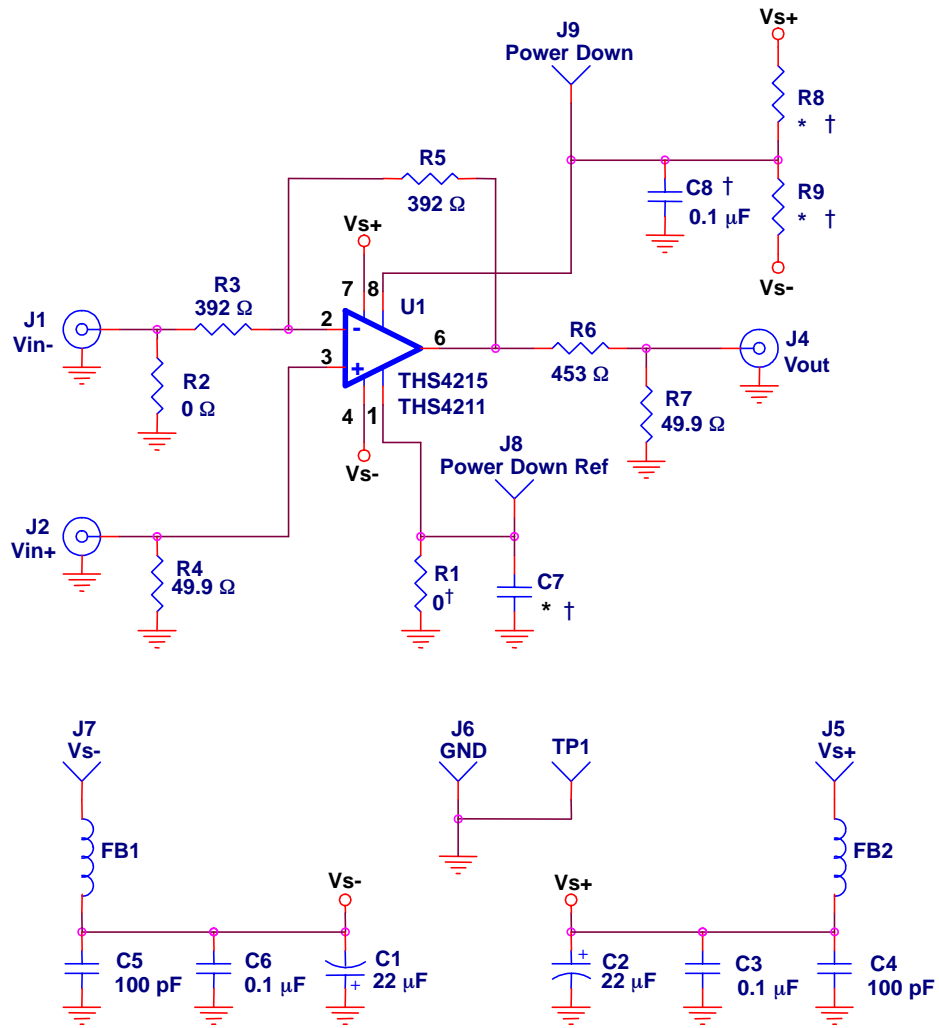
## 1.1 Evaluation Schematic

As delivered, the EVM has a fully functional example circuit—just add power supplies, a signal source, and monitoring instrument. See Figure 1–1 for a complete schematic diagram. EVM features include:

- Wide operating supply voltage range: single supply 4.5 Vdc to dual supply  $\pm 7.5$  Vdc operation (see the device data sheet). Single supply operation is obtained by connecting both J6 (GND) and J7 (VS-) to ground.
- Nominal 50- $\Omega$  input impedance (R4). Termination can be configured according to the application requirement.
- 50- $\Omega$  impedance traces on Vin-, Vin+, and Vout (see Figure 4-1—the vias provide the impedance)
- Power-down input for the THS4215 (J9).
- Power-down reference for the THS4215 can be changed by removing R1 and supplying the desired reference level to J8.
- Convenient GND test point (TP1).
- 453- $\Omega$  series matching resistor (R6)—produces a 500- $\Omega$  load in combination with resistor R7. 500  $\Omega$  is the standard data sheet load impedance.
- Power supply ripple rejection capacitors (C1 and C2).
- Decoupling capacitors (C3, C4, C5, C6).
- PowerPAD™ heatsinking capability.
- User customizable/configurable component choice.
- A good example of high-speed amplifier PCB design and layout.



Figure 1-1. Schematic of the THS4211/15EVM

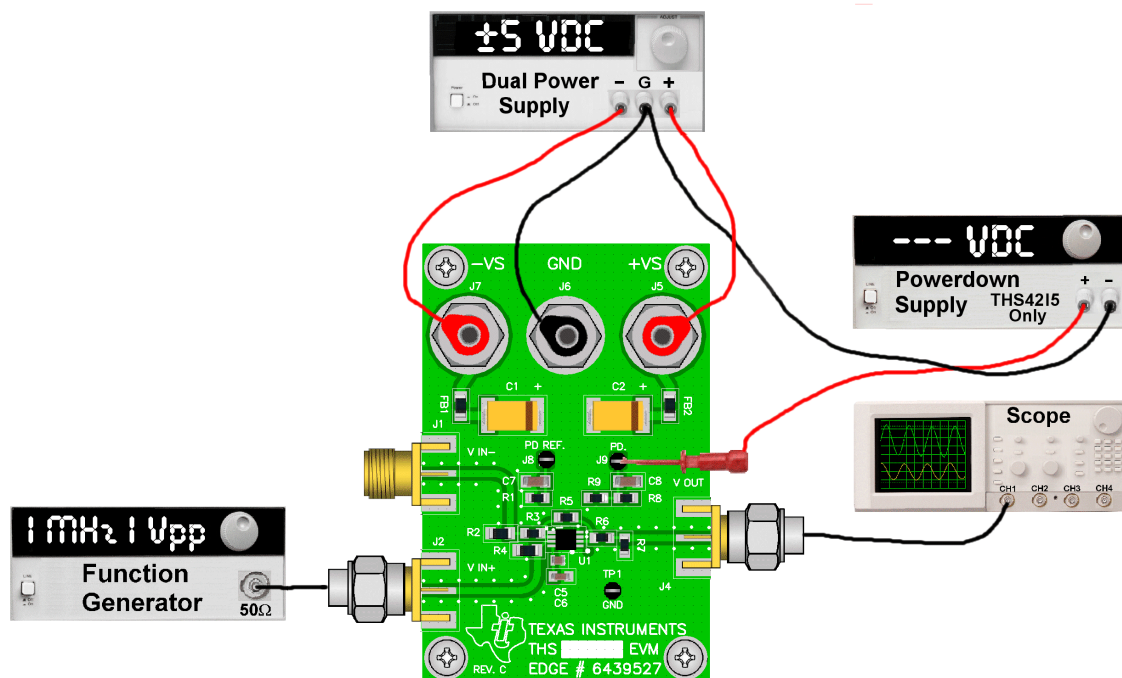


\* Not Installed on the THS4215 EVM  
 † Not Installed on the THS4211 EVM

## Using the EVM

Figure 2-1 shows how to connect power supplies, signal source and monitoring instrument. It is recommended that the user connect the EVM as shown to avoid damage to the EVM or the op amp installed on the board.

Figure 2-1. Test Equipment Connections

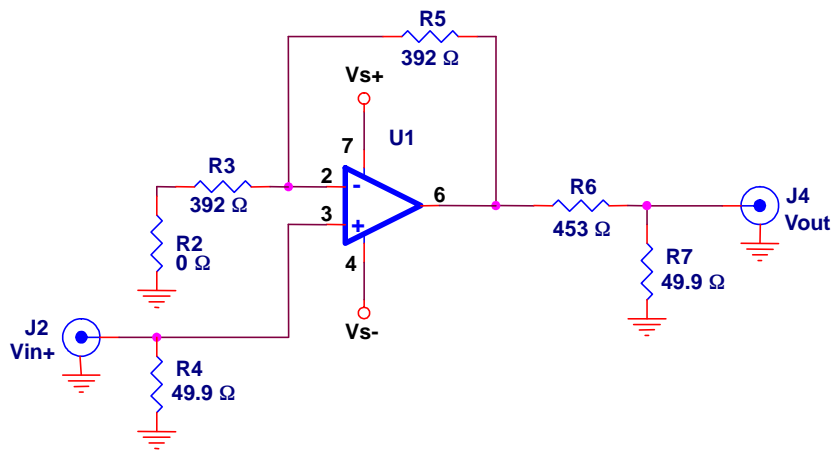


# EVM Applications

Example applications are presented in this chapter. These applications demonstrate the most popular circuits, but many other circuits can be constructed. The purpose of the EVM board is for the user to experiment with different circuits, exploring new and creative design techniques, which is the function of an evaluation board.

## 3.1 Default Configuration

Figure 3-1. Default Configuration



**Note:** This schematic reflects the default THS4211EVM configuration. Power supply decoupling not shown.

The EVM output provides a 500- $\Omega$  load to the output of the EVM to provide optimum performance (per the data sheet). The load is implemented as a 453- $\Omega$  resistor (R6) in series with the output to J4 ( $V_{out}$ ), and a 49.9- $\Omega$  output load resistor (R7) from J4 to ground. The total of these two resistors is close to 500  $\Omega$ , which is the standard load impedance.

When the EVM is monitored with a high input impedance instrument, R7 can remain on the board, and the EVM provides a 10:1 attenuation of the input signal.

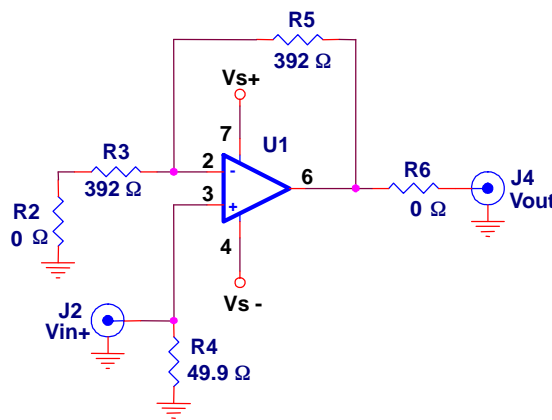
When the EVM is monitored with an instrument that has an input impedance of 50  $\Omega$ , R7 must be removed. The EVM again provides a 10:1 attenuation.

If the user provides an external load, R7 may be removed, and R6 replaced with a 0-Ω jumper. The EVM then provides a gain of 2 (6 dB) at the output connector J4. A gain of 2 is often used to compensate for the voltage division effect when series and termination resistors are used for stage impedance matching.

### 3.2 Noninverting Gain Stage

The default configuration of the EVM is a noninverting gain stage with a voltage divider on the output. If a gain of 2 is desired, the user should change R6 to 0 Ω, and remove R7 as shown in Figure 3-2:

Figure 3-2. Noninverting Gain Stage



**Note:** Power supply decoupling not shown.

Gain for this circuit is:

$$\frac{V_O}{V_I} = 1 + \frac{R5}{R3}$$

for  $R2 = 0$ , when the input voltage is measured at J2.

Changing R6 to 49.9 Ω in this and the subsequent section, allows the EVM to connect to a 50-Ω load. This amplifier is designed to attain optimum performance driving 500-Ω loads, but also drives 100-Ω loads—refer to data sheet characteristics.

**Note:**

The unity gain noninverting buffer configuration can be implemented by removing R3 and R2. This configuration, however, requires a 392-Ω resistor to be installed in location R5 on the EVM. A resistor less than the recommended value may cause the EVM to become unstable due to inductance on the PCB trace. Texas Instruments manufactures a different EVM for customers who wish to evaluate the noninverting buffer configuration. This EVM is optimized for low inductance traces on the op amp output. It is implemented on THS4211EVM-UG.

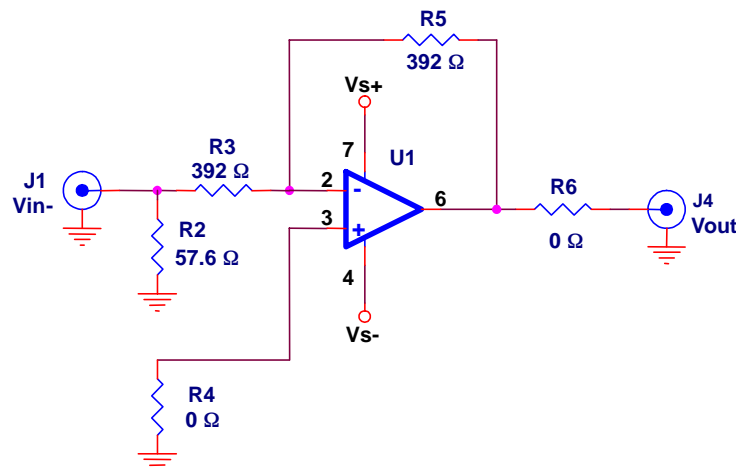
### 3.3 Inverting Gain Stage

If unity gain inverting operation is desired, the user should:

- Change R6 to 0 Ω
- Remove R7
- Change R4 to 0 Ω
- Change R2 to 57.6 Ω (R3 in parallel with R2 equals 50 Ω for termination of the input)

as shown in Figure 3-3.

Figure 3-3. Inverting Gain Stage



The gain for this circuit with a 50-Ω source is:

$$\frac{V_O}{V_I} = -\frac{R_5}{R_3}$$

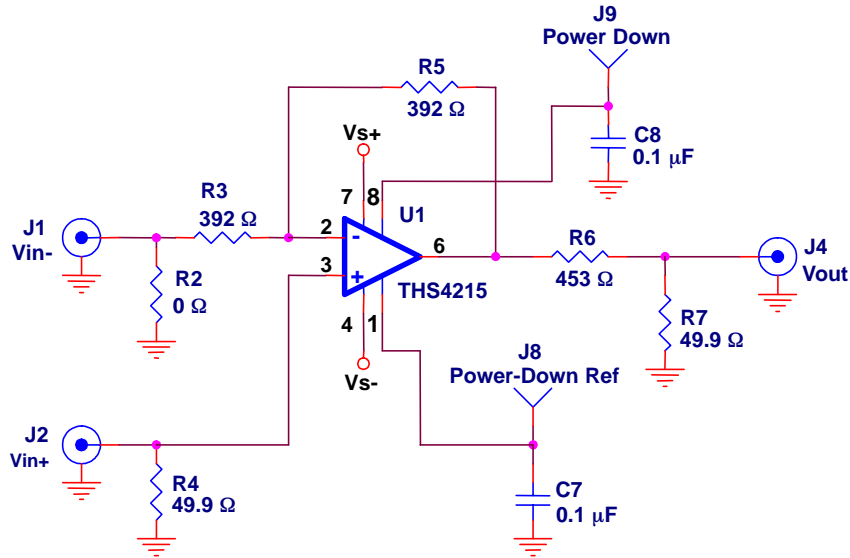
when the input voltage is measured at J1.

The input impedance of the stage is 50 Ω, as determined by R2 in parallel with R3.

### 3.4 Power-Down Reference Operation—THS4215EVM Only

For the default EVM configuration, power-down reference level is set to ground through R1. This reference can be set to a different level if R1 is removed and an external voltage is supplied to J8 as shown in Figure 3-4.

Figure 3-4. Power-Down Reference Operation



**Note:** This schematic reflects the default THS4215EVM configuration.

The reference pin allows the user to control the logic levels of the power-down pin. The reference pin is mainly designed for systems with supply voltages higher than 5 V; however, it works with any voltage within the amplifier's voltage range. In most cases, the reference pin is connected to a digital ground or to ground. For example, a customer is using a 3-V microcontroller to control the power-down pin of an amplifier that is operating from a  $\pm 5$  V power supply. Using the traditional power-down circuit, the customer has to buffer/boost the 3-V signal from the microcontroller to a higher level to ensure the proper voltage level for the amplifier to toggle between enable and disable. With the reference circuit, the customer can connect the 3-V signal directly to the power-down pin.

When the reference pin is connected to ground, the power-down voltage applied to the power-down pin must be greater than  $\text{Ref} + 1.8$  V ( $\text{GND} + 1.8$  V) for the amplifier to be active (enable). To place the device into power-down mode (disable) the voltage applied to the power-down pin must be less than  $\text{Ref} + 1$  V ( $\text{GND} + 1$  V).

Now, when the reference pin is connected to the positive supply or allowed to float, the power-down logic levels are referenced to the positive supply. Therefore, if a system is operating on a split supply of 5 V and the reference pin is left floating (not connected), the power-down pin voltage must be greater than  $\text{Ref} - 1$  V ( $5$  V  $- 1$ ;  $V = 4$  V) for the amplifier to be active (enable). To place the device into power-down mode (disable) the voltage applied to the power-down pin must be less than  $\text{Ref} - 1.5$  V ( $5$  V  $- 1.5$ ;  $V = 3.5$  V).

# EVM Hardware Description

This chapter describes the EVM hardware. It includes the EVM parts list, and printed circuit board layout.

Table 4-1. THS4211EVM Bill of Materials

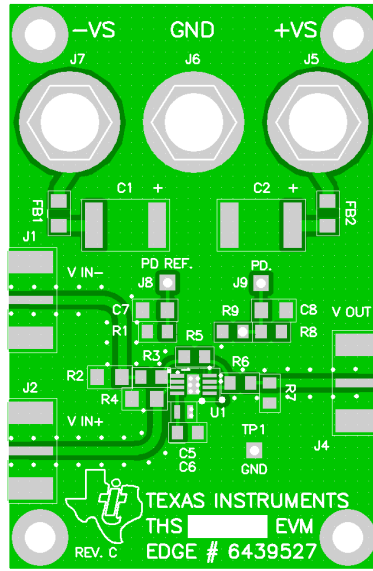
| Item | Description                                  | SMD Size | Reference Designator | PCB QTY | Manufacturer's Part Number     | Distributor's Part Number      |
|------|--|----------|----------------------|---------|--------------------------------|--------------------------------|
| 1    | Bead, ferrite, 3A, 80 $\Omega$               | 1206     | FB1, FB2             | 2       | (Steward)<br>HI1206N800R-00    | (Digi-Key)<br>240-1010-1-ND    |
| 2    | Cap., 22 $\mu$ F, tantalum, 25 V, 10%        | D        | C1, C2               | 2       | (AVX) TAJD226K025R             | (Garrett)<br>TAJD226K025R      |
| 3    | Cap., 100 pF, ceramic, 5%, 150 V             | AQ12     | C4, C5               | 2       | (AVX)<br>AQ12EM101JAJME        | (TTI)<br>AQ12EM101JAJME        |
| 4    | Cap., 0.1 $\mu$ F, ceramic, X7R, 50 V        | 0805     | C3, C6               | 2       | (AVX)<br>08055C104KAT2A        | (Garrett)<br>08055C104KAT2A    |
| 6    | Open   | 0805     | R1, R8, R9           | 2       |                                |                                |
| 7    | Resistor, 49.9 $\Omega$ , 1/8 W, 1%          | 0805     | R7                   | 1       | (PHYCOMP)<br>9C08092A49R9FKHFT | (Garrett)<br>9C08052A49R9FKHFT |
| 8    | Resistor, 392 $\Omega$ , 1/8 W, 1%           | 0805     | R3, R5               | 2       | (PHYCOMP)<br>9C08052A3920FKHFT | (Garrett)<br>9C08052A3920FKHFT |
| 9    | Resistor, 453 $\Omega$ , 1/8 W, 1%           | 0805     | R6                   | 1       | (PHYCOMP)<br>9C08052A4530FKHFT | (Garrett)<br>9C08052A4530FKHFT |
| 10   | Open   | 1206     | C7, C8               | 2       |                                |                                |
| 11   | Resistor, 0 $\Omega$ , 1/4 W                 | 1206     | R2                   | 1       | (PHYCOMP)<br>9C12063A0R00JLHFT | (Garrett)<br>9C12063A0R00JLHFT |
| 12   | Resistor, 49.9 $\Omega$ , 1/4 W, 1%          | 1206     | R4                   | 1       | (PHYCOMP)<br>9C12063A49R9FKRFT | (Garrett)<br>9C12063A49R9FKRFT |
| 13   | Test point, black                            |          | TP1                  | 1       | (Keystone) 5001                | (Allied) 839-3601              |
| 14   | Open   |          | J8, J9               | 2       |                                |                                |
| 15   | Jack, banana receptacle, 0.25" diameter hole |          | J5, J6, J7           | 3       | (HH Smith) 101                 | (Newark) 35F865                |
| 16   | Connector, edge, SMA PCB jack                |          | J1, J2, J4           | 3       | (Johnson)<br>142-0701-801      | (Allied) 528-0238              |
| 17   | Standoff, 4-40 hex, 0.625" length            |          |                      | 4       | (Keystone) 1804                | (Allied) 839-2089              |
| 18   | Screw, Phillips, 4-40, .250"                 |          |                      | 4       | SHR-0440-016-SN                |                                |
| 19   | IC, THS4211                                  |          | U1                   | 1       | (TI) THS4211DGN                |                                |
| 20   | Board, printed circuit                       |          |                      | 1       | (TI) Edge #6439527 Rev.C       |                                |

Table 4-2. THS4215EVM Bill of Materials

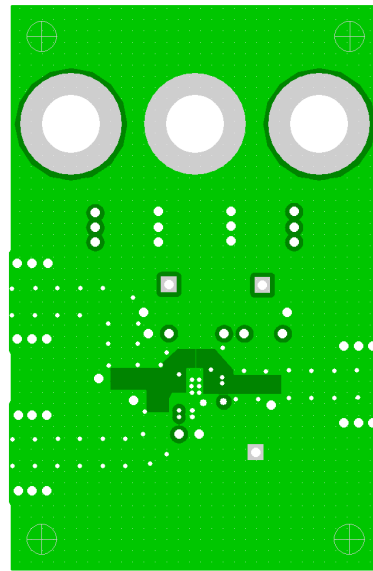
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|------|--|----------|----------------------|---------|--------------------------------|--------------------------------|
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| 2    | Capacitor, 22 μF, tantalum, 25 V, 10%        | D        | C1, C2               | 2       | (AVX) TAJD226K025R             | (Garrett)<br>TAJD226K025R      |
| 3    | Capacitor, 100 pF, ceramic, 150 V, 5%,       | AQ12     | C4, C5               | 2       | (AVX)<br>AQ12EM101JAJME        | (TTI)<br>AQ12EM101JAJME        |
| 4    | Open   | 1206     | C7                   | 1       |                                |                                |
| 5    | Capacitor, 0.1 μF, ceramic, X7R, 50 V        | 0805     | C3, C6               | 2       | (AVX)<br>08055C104KAT2A        | (Garrett)<br>08055C104KAT2A    |
| 6    | Capacitor, 0.1 μF, ceramic, X7R, 50 V        | 1206     | C8                   | 1       | (AVX)<br>12065C104KAT2A        | (Garrett)<br>12065C104KAT2A    |
| 7    | Open   | 0805     | R8, R9               | 2       |                                |                                |
| 8    | Resistor, 0 Ω, 1/8W, 1%                      | 0805     | R1                   | 1       | (Phycomp)<br>9C08052A0R00JLHFT | (Garrett)<br>9C08052A0R00JLHFT |
| 9    | Resistor, 49.9 Ω, 1/8W, 1%                   | 0805     | R7                   | 1       | (Phycomp)<br>9C08052A49R9FKHFT | (Garrett)<br>9C08052A49R9FKHFT |
| 10   | Resistor, 392 Ω, 1/8W, 1%                    | 0805     | R3, R5               | 2       | (Phycomp)<br>9C08052A3920FKHFT | (Garrett)<br>9C08052A3920FKHFT |
| 11   | Resistor, 453 Ω, 1/8W, 1%                    | 0805     | R6                   | 1       | (Phycomp)<br>9C08052A4530FKHFT | (Garrett)<br>9C08052A4530FKHFT |
| 12   | Resistor, 0 Ω, 1/4W                          | 1206     | R2                   | 1       | (Phycomp)<br>9C12063A0R00JLHFT | (Garrett)<br>9C12063A0R00JLHFT |
| 13   | Resistor, 49.9 Ω, 1/4W, 1%                   | 1206     | R4                   | 1       | (Phycomp)<br>9C12063A49R9FKRFT | (Garrett)<br>9C12063A49R9FKRFT |
| 14   | Test point, black                            |          | TP1, J8, J9          | 3       | (Keystone) 5001                | (Allied) 839-3601              |
| 15   | Jack, banana receptacle, 0.25" diameter hole |          | J5, J6, J7           | 3       | (HH Smith) 101                 | (Newark) 35F865                |
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| 17   | Standoff, 4-40 Hex, 0.625" length            |          |                      | 4       | (Keystone) 1804                | (Allied) 839-2089              |
| 18   | Screw, Phillips, 4-40, .250"                 |          |                      | 4       | SHR-0440-016-SN                |                                |
| 19   | IC, THS4215                                  |          | U1                   | 1       | (TI) THS4215DGN                |                                |
| 20   | Board, printed circuit                       |          |                      | 1       | (TI) Edge #6439527 Rev.C       |                                |



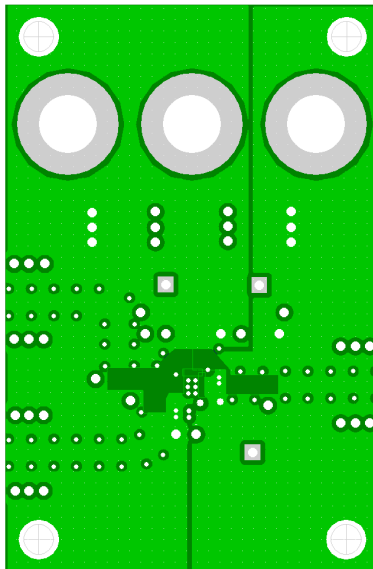
Figure 4-1. Board Layout Views



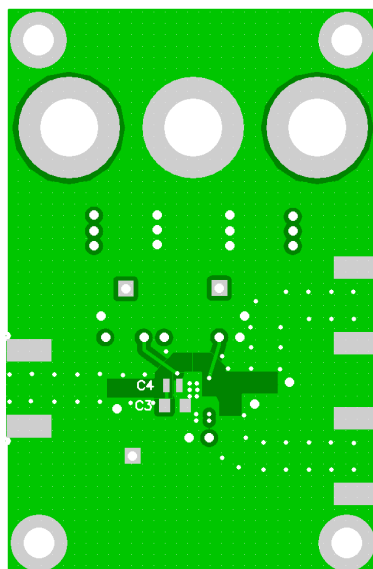
Top



Layer 2 - Ground



Layer 3 - Power



Bottom



## Стандарт Электрон Связь

Мы молодая и активно развивающаяся компания в области поставок электронных компонентов. Мы поставляем электронные компоненты отечественного и импортного производства напрямую от производителей и с крупнейших складов мира.

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Собственная эффективная логистика и склад в обеспечивает надежную поставку продукции в точно указанные сроки по всей России.

Мы осуществляем техническую поддержку нашим клиентам и предпродажную проверку качества продукции. На все поставляемые продукты мы предоставляем гарантию .

Осуществляем поставки продукции под контролем ВП МО РФ на предприятия военно-промышленного комплекса России , а также работаем в рамках 275 ФЗ с открытием отдельных счетов в уполномоченном банке. Система менеджмента качества компании соответствует требованиям ГОСТ ISO 9001.

Минимальные сроки поставки, гибкие цены, неограниченный ассортимент и индивидуальный подход к клиентам являются основой для выстраивания долгосрочного и эффективного сотрудничества с предприятиями радиоэлектронной промышленности, предприятиями ВПК и научно-исследовательскими институтами России.

С нами вы становитесь еще успешнее!

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