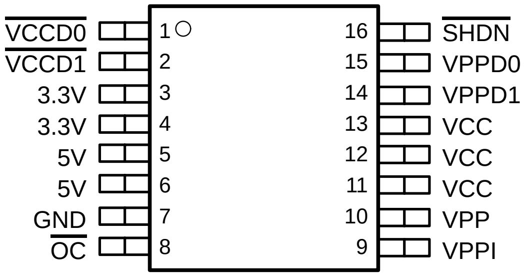
TPS2212
SINGLE-SLOT, PARALLEL INTERFACE POWER SWITCH FOR LOW POWER PC CARD SLOTS

SLVS193A – APRIL 1999 – REVISED JANUARY 2001

- **Fully Integrated V_{CC} and V_{pp} Switching for Low Power Single-Slot PC Card™ Interface**
- **Low $r_{DS(on)}$ (160-mΩ V_{CC} Switches)**
- **Low Current Limit, 450 mA (V_{CC}) Typ**
- **3.3-V Low-Voltage Mode**
- **12-V Supply Can Be Disabled Except During 12-V Flash Programming**
- **Short-Circuit and Thermal Protection**
- **Space-Saving 16-Pin SSOP (DB)**
- **Compatible With 3.3-V, 5-V, and 12-V PC Cards**
- **Break-Before-Make Switching**
- **Typical Applications Include: PCMCIA PC Card Sockets in PDAs, PBXs, Bar Code Scanners, Compact Flash and Smart Cards**

DB PACKAGE
(TOP VIEW)



description

The TPS2212 PC Card power-interface switch provides an integrated power-management solution for a single low power PC Card. All of the discrete power MOSFETs, a logic section, current limiting, and thermal protection for PC Card control are combined on a single integrated circuit, using the Texas Instruments LinBiCMOS™ process. The circuit allows the distribution of 3.3-V, 5-V, and/or 12-V card power, and is compatible with many PCMCIA controllers. The current-limiting feature eliminates the need for fuses, which reduces component count and improves reliability. Current-limit reporting can help the user isolate a system fault to the PC Card.

The TPS2212 features a 3.3-V low-voltage mode that allows for 3.3-V switching without the need for 5 V. Bias power can be derived from either the 3.3-V or 5-V inputs. This facilitates low-power system designs such as sleep mode and pager mode, where only 3.3 V is available.

End equipment for the TPS2212 includes notebook computers, desktop computers, personal digital assistants (PDAs), digital cameras, and bar-code scanners. This device is well suited for those applications that need to limit the power provided to the PC card because of power-supply constraints. In many applications, such as palm computers, the system cannot allocate more than 200 mA of current to a PC card slot. For these lower-power applications, the TPS2212 provides the same advanced level of protection that the TPS2211 provides for higher-power applications.

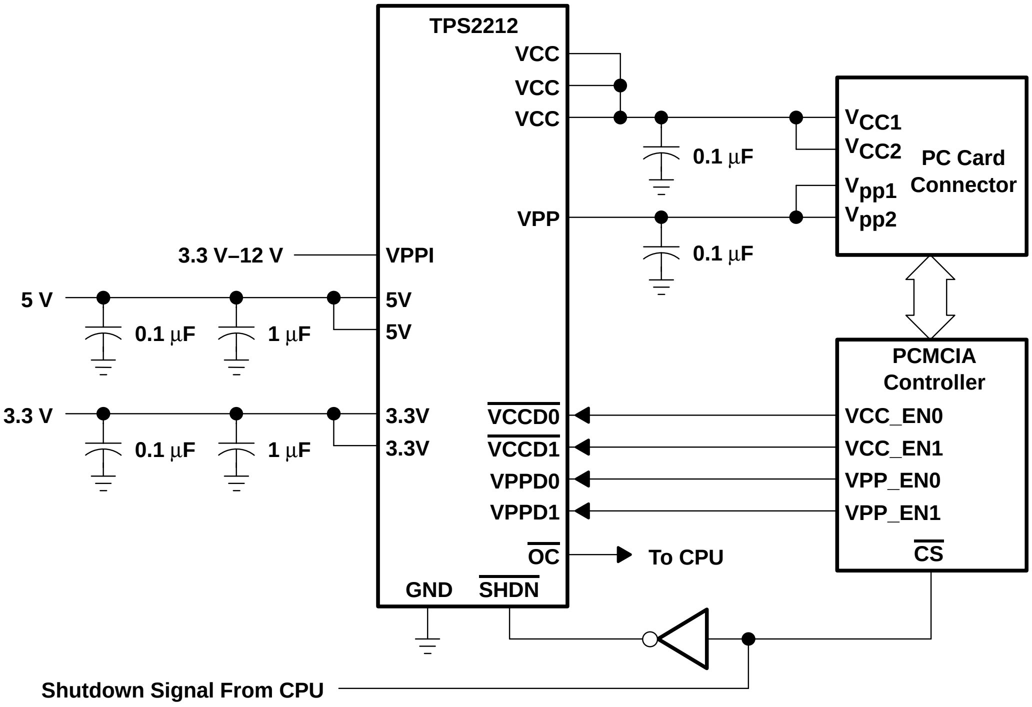
AVAILABLE OPTIONS

T_A	PACKAGED DEVICE
	SMALL OUTLINE (DB)
–40°C to 85°C	TPS2212IDB

The DB package is available taped and reeled. Add an R suffix to the device type (e.g., TPS2212IDBR) for taped and reeled.

PC Card is a trademark of PCMCIA (Personal Computer Memory Card International Association).
LinBiCMOS is a trademark of Texas Instruments.

typical PC-card power-distribution application



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
3.3V	3, 4	I	3.3-V V_{CC} input for card power and/or chip power if 5 V is not present
5V	5, 6	I	5-V V_{CC} input for card power and/or chip power
VPPI	9	I	Main V_{pp} input, typically 12 V, allows 3.3 V–12 V.
VCC	11, 12, 13	O	Switched output that delivers 0 V, 3.3-V, 5-V, or high impedance to card
VPP	10	O	Switched output that delivers 0 V 3.3-V, 5-V, VPPI (12V), or high impedance to card
GND	7		Ground
$\overline{\text{OC}}$	8	O	Logic-level overcurrent reporting output that goes low when an overcurrent conditions exists
$\overline{\text{SHDN}}$	16	I	Logic input that shuts down the TPS2212 and sets all power outputs to high-impedance state
$\overline{\text{VCCD0}}$	1	I	Logic input that controls voltage of VCC (see control-logic table)
$\overline{\text{VCCD1}}$	2	I	Logic input that controls voltage of VCC (see control-logic table)
VPPD0	15	I	Logic input that controls voltage of VPP (see control-logic table)
VPPD1	14	I	Logic input that controls voltage of VPP (see control-logic table)

absolute maximum ratings over operating free-air temperature (unless otherwise noted)[†]

Input voltage range for card power:	$V_{I(5V)}$	–0.3 V to 7 V
	$V_{I(3.3V)}$	–0.3 V to 7 V
	$V_{I(VPPI)}$	–0.3 V to 14 V
Logic input voltage		–0.3 V to 7 V
Continuous total power dissipation		See Dissipation Rating Table
Output current (each card):	$I_{O(VCC)}$	internally limited
	$I_{O(VPP)}$	internally limited
Operating virtual junction temperature range, T_J		–40°C to 150°C
Operating free-air temperature range, T_A		–40°C to 85°C
Storage temperature range, T_{stg}		–55°C to 150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds		260°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DB	775 mW	6.2 mW/°C	496 mW	403 mW

These devices are mounted on an FR4 board with no special thermal considerations.

recommended operating conditions

		MIN	MAX	UNIT
Input voltage, V_I	$V_{I(5V)}$	0	5.25	V
	$V_{I(3.3V)}$	0	5.25	V
	$V_{I(VPPI)}$	0	13.5	V
Output current	$I_{O(VCC)}$		250	mA
	$I_{O(VPP)}$		150	mA
Operating virtual junction temperature, T_J		–40	125	°C

electrical characteristics, T_A = –40°C to 85°C (unless otherwise noted)

power switch

PARAMETER			TEST CONDITIONS[†]	MIN	TYP	MAX	UNIT
	Switch resistance	5 V to VCC	$V_{I(5V)} = 5$ V		160	210	mΩ
		3.3 V to VCC	$V_{I(5V)} = 5$ V, $V_{I(3.3V)} = 3.3$ V		160	210	
		3.3 V to VCC	$V_{I(5V)} = 0$ V, $V_{I(3.3V)} = 3.3$ V		160	210	
		5 V to VPP	T_J=25°C			6	Ω
		3.3 V to VPP	T_J=25°C			6	
		12 V to VPP	T_J=25°C			1	
$V_{O(VPP)}$	Clamp low voltage		I_{pp} at 10 mA			0.8	V
$V_{O(VCC)}$	Clamp low voltage		I_{CC} at 10 mA			0.8	V
I_{lkg}	Leakage current	I_{pp} high-impedance state	T_A = 25°C		1	10	μA
			T_A= 85°C			50	
		I_{CC} high-impedance state	T_A = 25°C		1	10	
			T_A=85°C			50	
I_I	Input current	$V_{I(5V)} = 5$ V	$V_{O(VCC)} = 5$ V, $V_{O(VPP)} = 12$ V		40	150	μA
		$V_{I(5V)} = 0$ V, $V_{I(3.3V)} = 3.3$ V	$V_{O(VCC)} = 3.3$ V, $V_{O(VPP)} = 12$ V		40	150	
		Shutdown mode	$V_{O(VCC)} = V_{O(VPP)}$ = Hi-Z			1	
I_{OS}	Short-circuit output-current limit	$I_{O(VCC)}$	T_J = 85°C, output powered into a short to GND	300		600	mA
		$I_{O(VPP)}$		120		400	mA

[†] Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

logic section

PARAMETER	TEST CONDITIONS[†]	MIN	MAX	UNIT
Logic input current			1	μA
Logic input high level		2		V
Logic input low level			0.8	V
Logic output high level	$V_{I(5V)} = 5$ V, $I_O = 1$ mA	$V_{I(5V)} - 0.4$		V
	$V_{I(5V)} = 0$ V, $I_O = 1$ mA, $V_{I(3.3V)} = 3.3$ V	$V_{I(3.3V)} - 0.4$		
Logic output low level	$I_O = 1$ mA		0.4	V

[†] Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

switching characteristics[‡]

PARAMETER		TEST CONDITIONS[§]		MIN	TYP	MAX	UNIT
t_r	Rise times, output	$V_{O(VCC)}$			2.8		ms
		$V_{O(VPP)}$			6.4		
t_f	Fall times, output	$V_{O(VCC)}$			4.5		
		$V_{O(VPP)}$			12		
t_{pd}	Propagation delay (see Figure1)	$V_{I(VPPD0)}$ to $V_{O(VPP)}$	t_{on}		6.8		ms
			t_{off}		18		
		$V_{I(\overline{VCCD1})}$ to $V_{O(VCC)}$ (3.3V)	t_{on}		4		
			t_{off}		17		
		$V_{I(\overline{VCCD0})}$ to $V_{O(VCC)}$ (5V)	t_{on}		6.6		
			t_{off}		17		

[‡] Switching Characteristics are with C_L = 150 μF.
[§] Refer to Parameter Measurement Information

PARAMETER MEASUREMENT INFORMATION

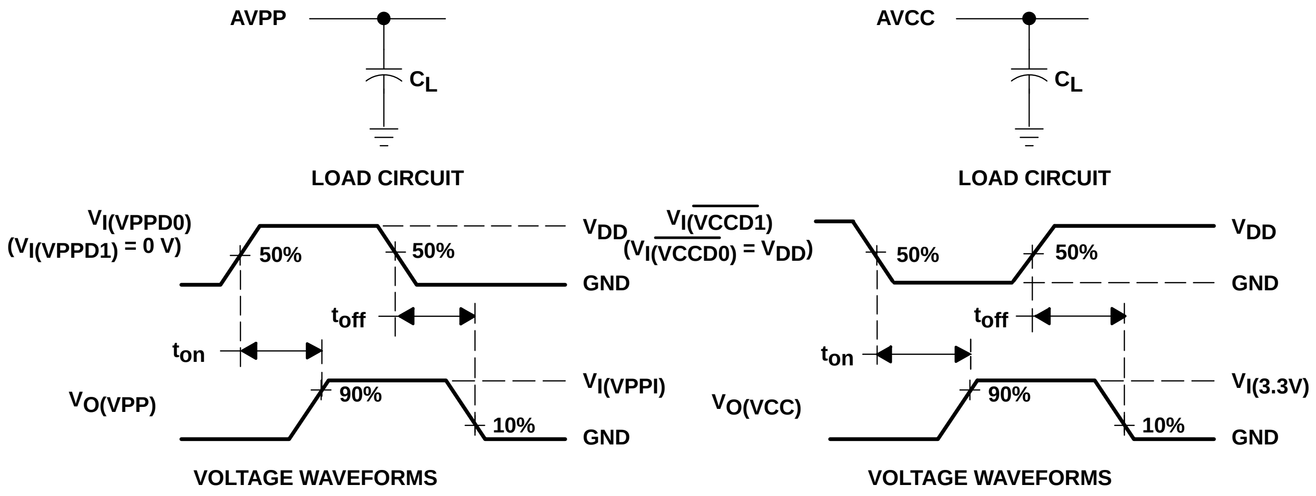


Figure 1. Test Circuits and Voltage Waveforms

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PARAMETER MEASUREMENT INFORMATION

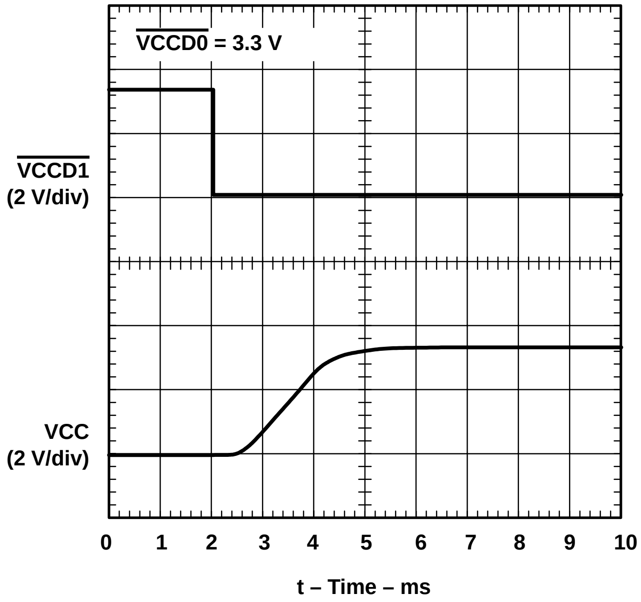

Figure 2. VCC Propagation Delay and Rise Time With 1-μF Load, 3.3-V Switch

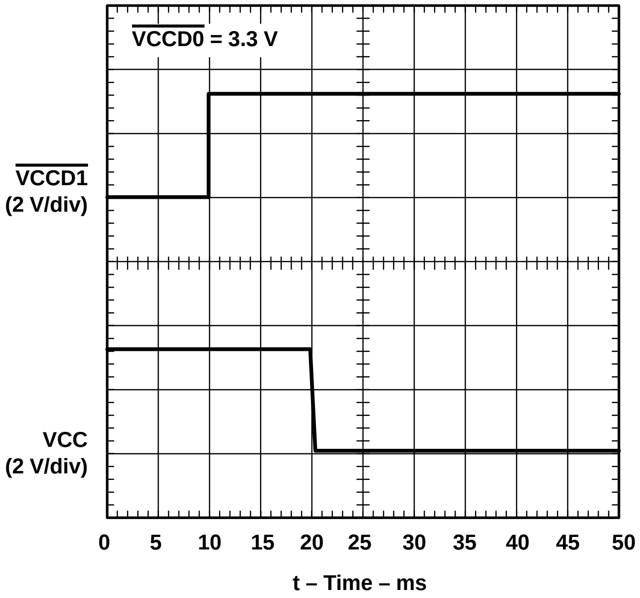

Figure 3. VCC Propagation Delay and Fall Time With 1-μF Load, 3.3-V Switch

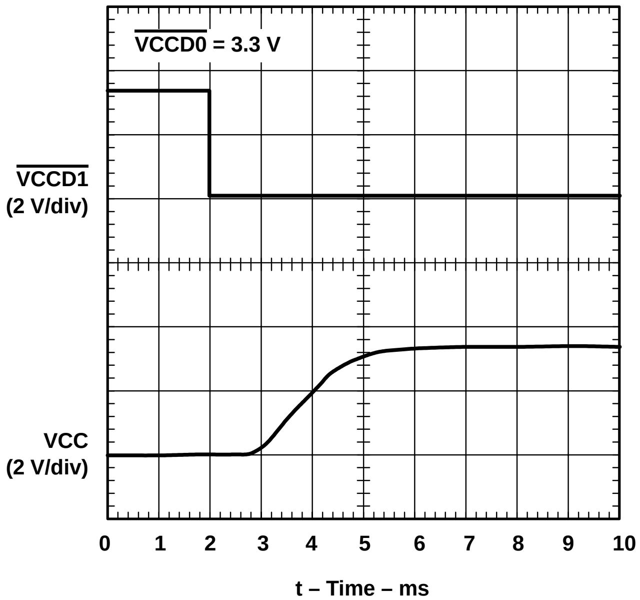

Figure 4. VCC Propagation Delay and Rise Time With 150-μF Load, 3.3-V Switch

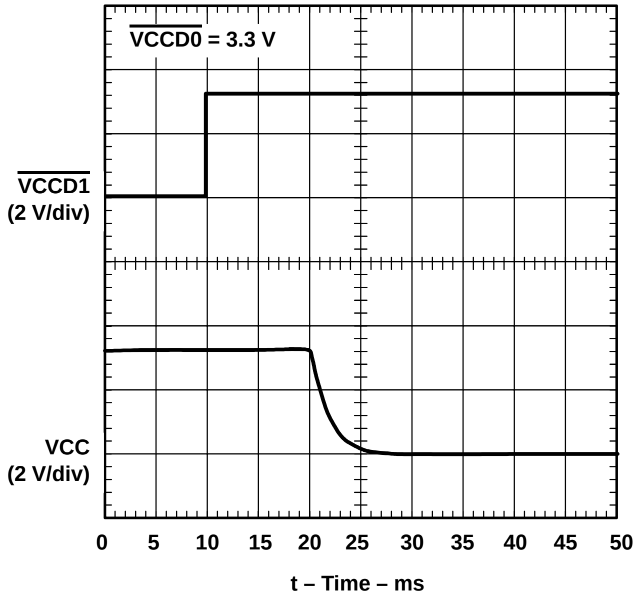

Figure 5. VCC Propagation Delay and Fall Time With 150-μF Load, 3.3-V Switch

PARAMETER MEASUREMENT INFORMATION

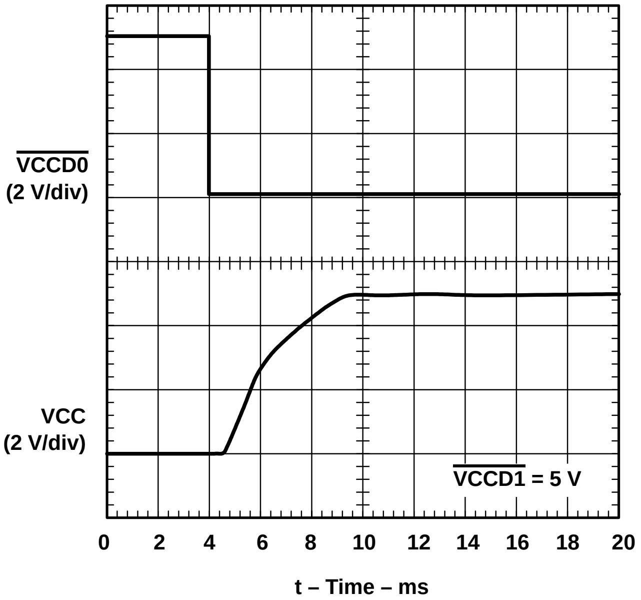

Figure 6. VCC Propagation Delay and Rise Time With 1-µF Load, 5-V Switch

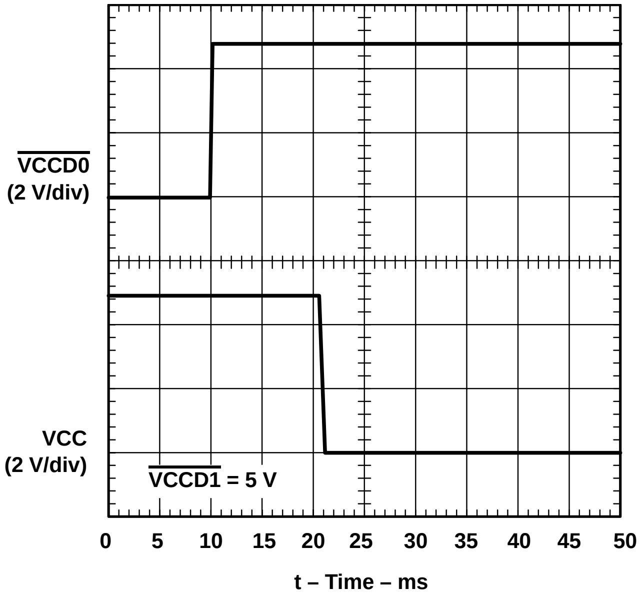

Figure 7. VCC Propagation Delay and Fall Time With 1-µF Load, 5-V Switch

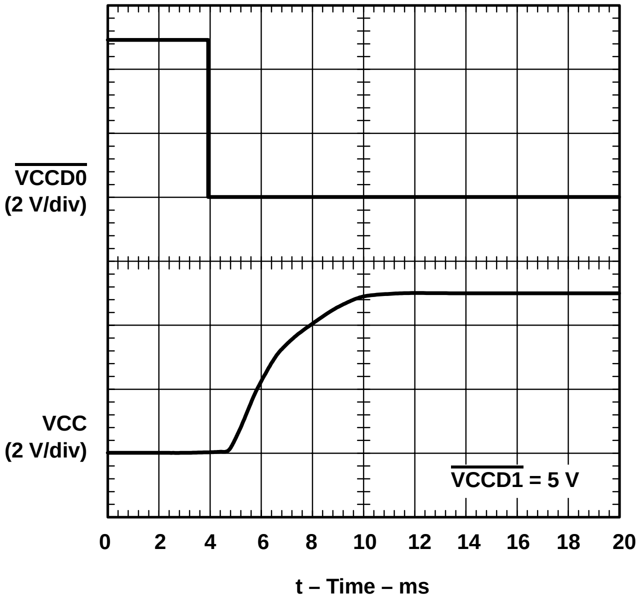

Figure 8. VCC Propagation Delay and Rise Time With 150-µF Load, 5-V Switch

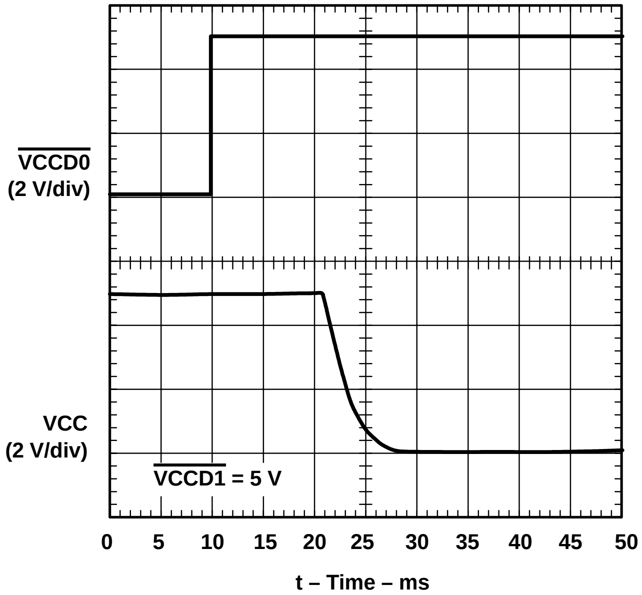

Figure 9. VCC Propagation Delay and Fall Time With 150-µF Load, 5-V Switch

PARAMETER MEASUREMENT INFORMATION

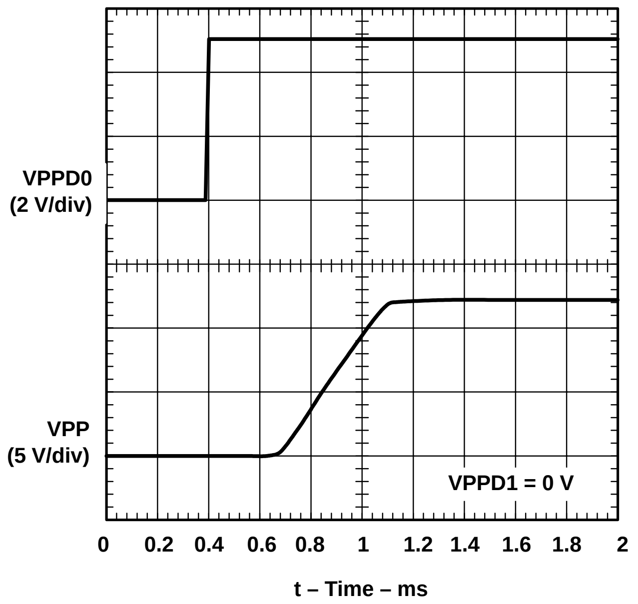

Figure 10. VPP Propagation Delay and Rise Time With 1-µF Load, 12-V Switch

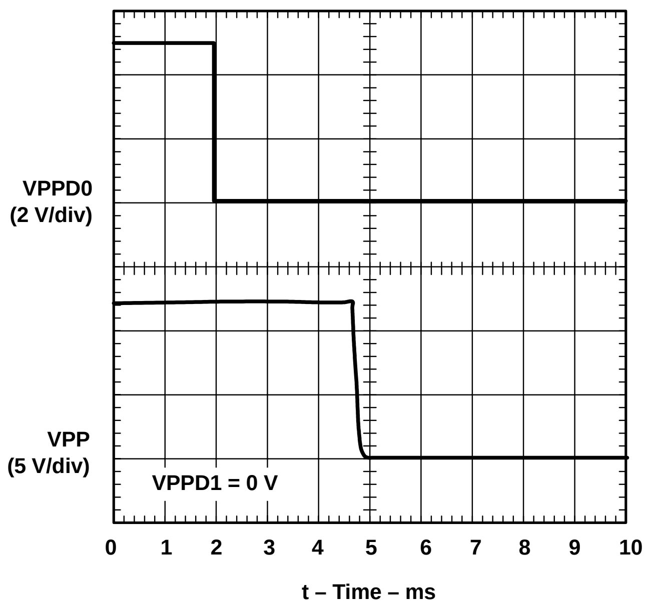

Figure 11. VPP Propagation Delay and Fall Time With 1-µF Load, 12-V Switch

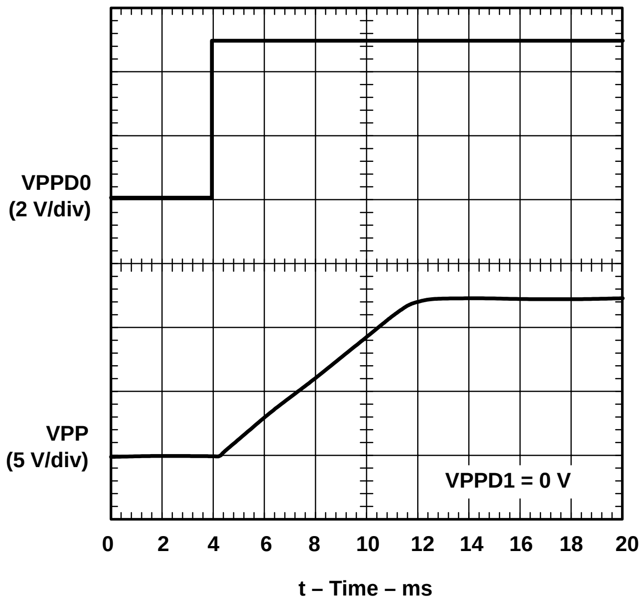

Figure 12. VPP Propagation Delay and Rise Time With 150-µF Load, 12-V Switch

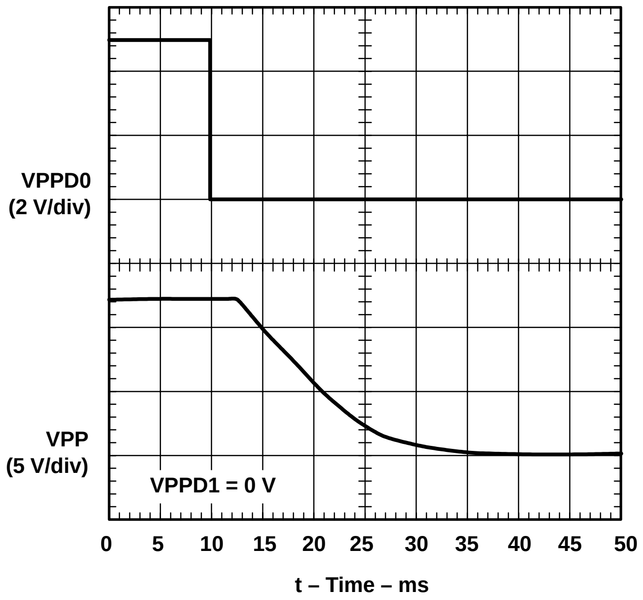

Figure 13. VPP Propagation Delay and Fall Time With 150-µF Load, 12-V Switch

TYPICAL CHARACTERISTICS

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$r_{DS(on)}$	Static drain-source on-state resistance, 3.3-V VCC switch	vs Junction Temperature	17
$r_{DS(on)}$	Static drain-source on-state resistance, 12-V VPP switch	vs Junction Temperature	18
$V_{O(VCC)}$	Output voltage, 5-V VCC switch	vs Output current	19
$V_{O(VCC)}$	Output voltage, 3.3-V VCC switch	vs Output current	20
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$I_{OS(VPP)}$	Short-circuit current, 12-V VPP switch	vs Junction Temperature	24

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs JUNCTION TEMPERATURE

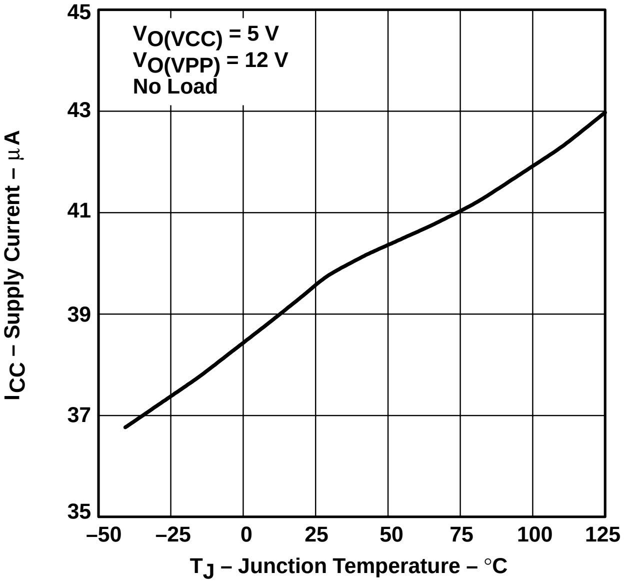


Figure 14

SUPPLY CURRENT vs JUNCTION TEMPERATURE

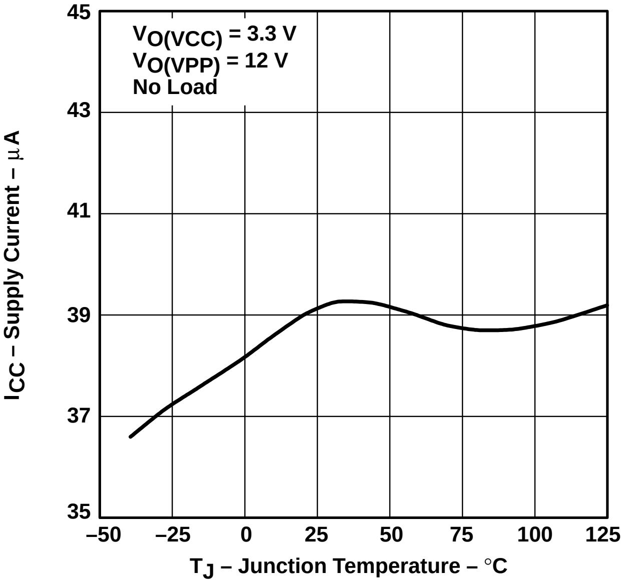


Figure 15

5-V VCC SWITCH

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE

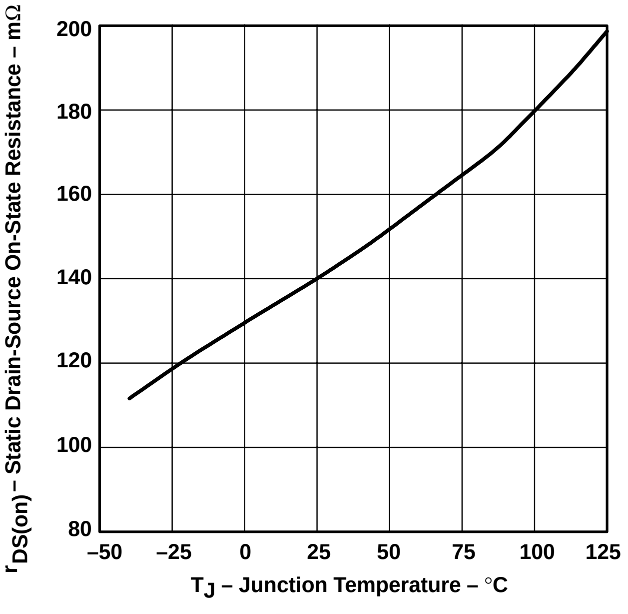


Figure 16

3.31–V VCC SWITCH

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE

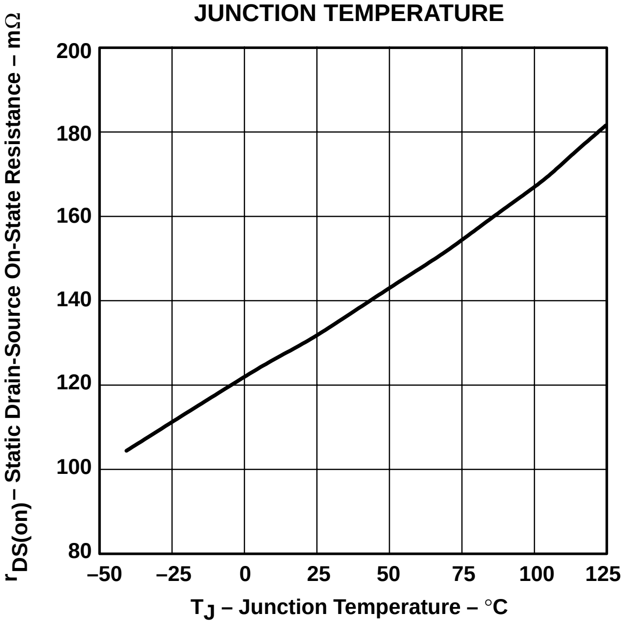


Figure 17

TYPICAL CHARACTERISTICS

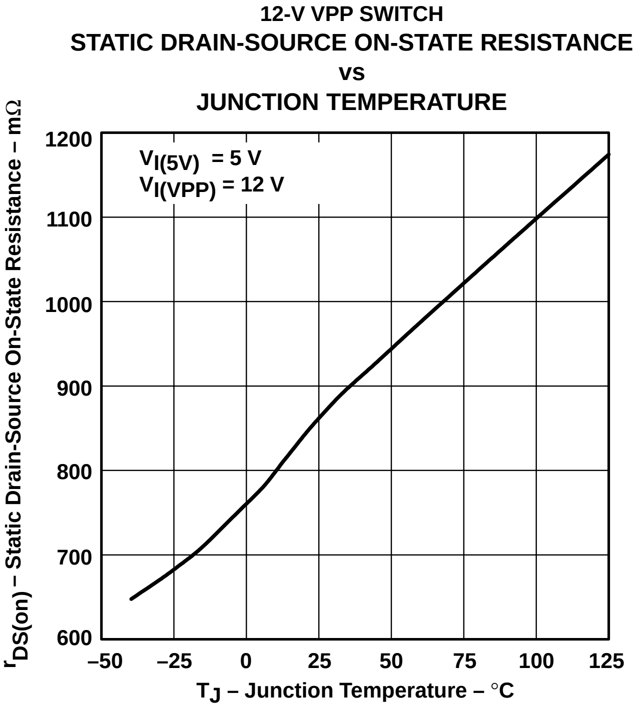


Figure 18

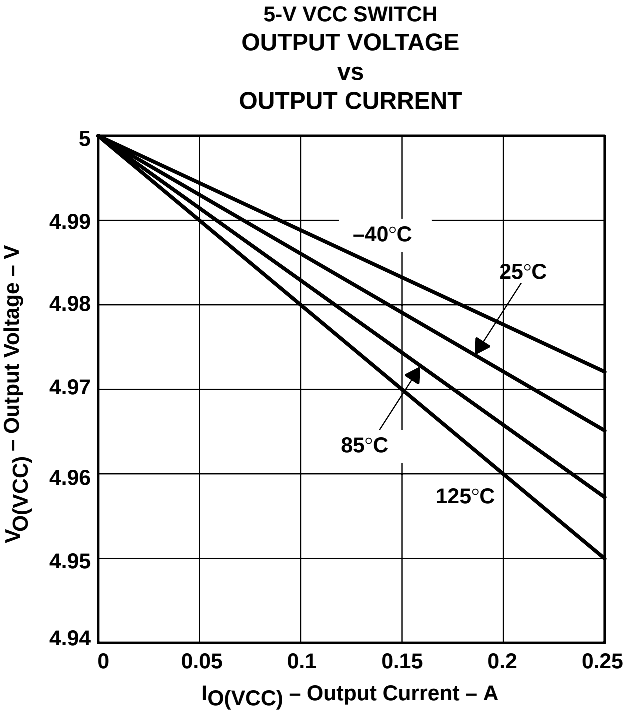


Figure 19

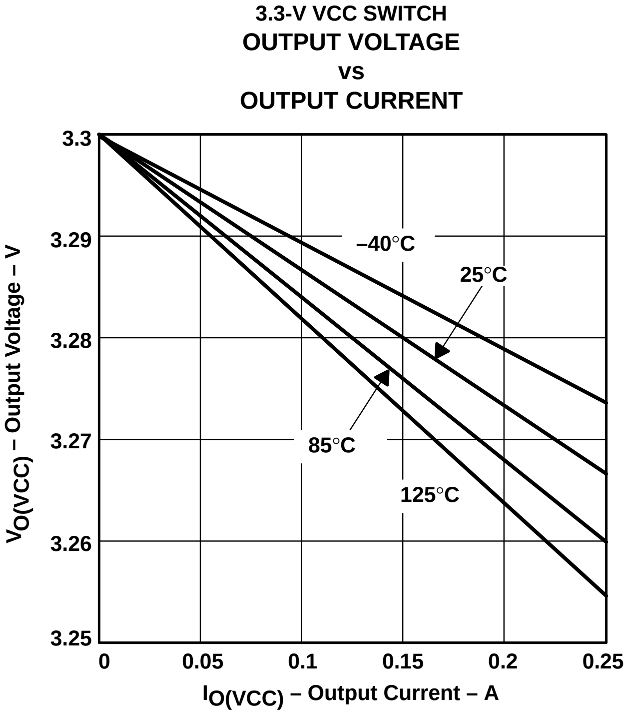


Figure 20

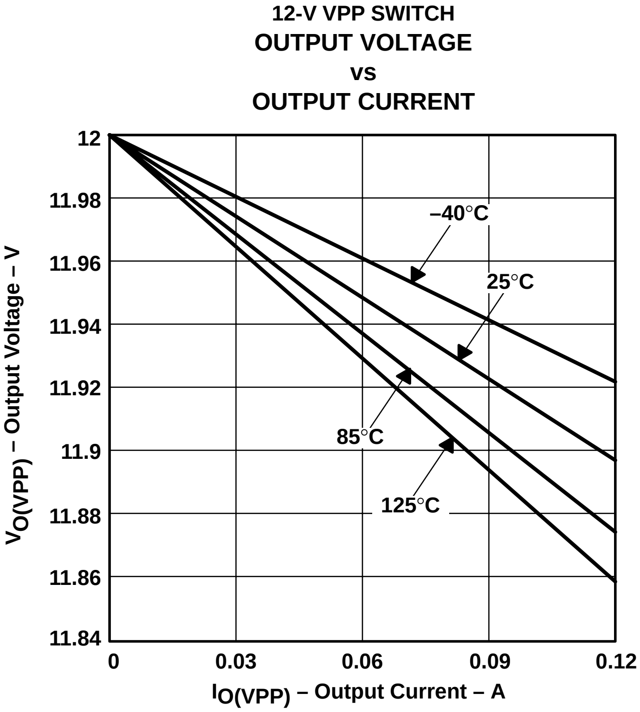


Figure 21

TYPICAL CHARACTERISTICS

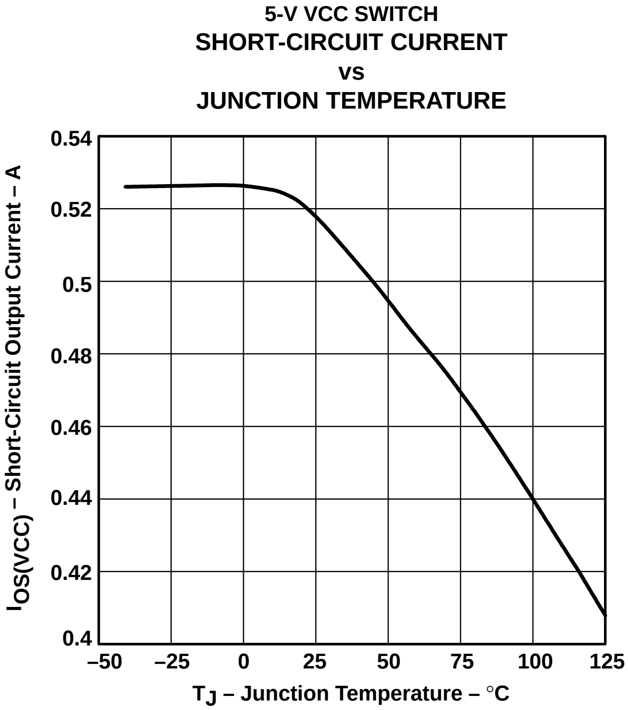


Figure 22

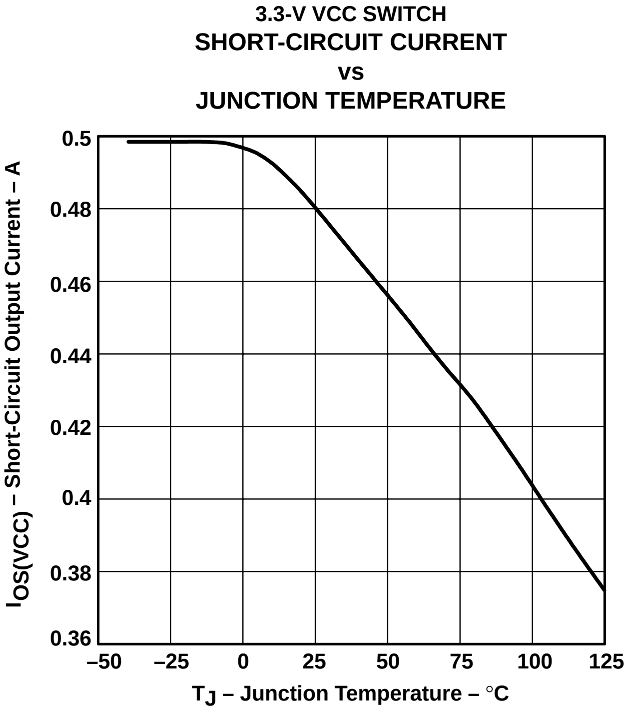


Figure 23

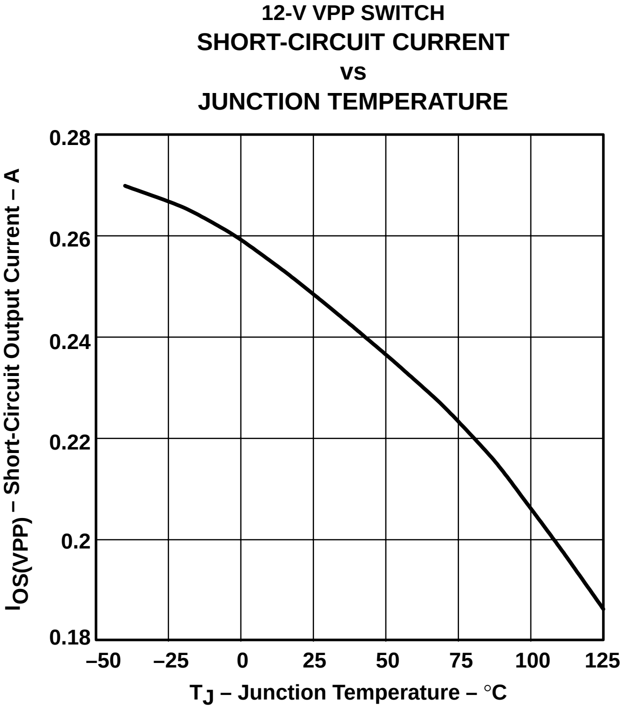


Figure 24

APPLICATION INFORMATION

overview

PC Cards were initially introduced as a means to add EEPROM (flash memory) to portable computers with limited on-board memory. The idea of add-in cards quickly took hold; modems, wireless LANs, GPS systems, multimedia, and hard-disk versions were soon available. As the number of PC Card applications grew, the engineering community quickly recognized the need for a standard to ensure compatibility across platforms. To this end, the PCMCIA (Personal Computer Memory Card International Association) was established, comprised of members from leading computer, software, PC Card, and semiconductor manufacturers. One key goal was to realize the *plug-and-play* concept, i.e. cards and hosts from different vendors should be compatible.

PC Card power specification

System compatibility also means power compatibility. The most current set of specifications (PC Card Standard) set forth by the PCMCIA committee states that power is to be transferred between the host and the card through eight of the 68 terminals of the PC Card connectors. This power interface consists of two VCC, two VPP, and four ground terminals. Multiple VCC and ground terminals minimize connector-terminal and line resistance. The two VPP terminals were originally specified as separate signals, but are commonly tied together in the host to form a single node to minimize voltage losses. Card primary power is supplied through the VCC terminals; flash-memory programming and erase voltage is supplied through the VPP terminals.

designing for voltage regulation

The current PCMCIA specification for output voltage regulation of the 5-V output is 5% (250 mV). In a typical PC power-system design, the power supply will have an output voltage regulation ($V_{PS(reg)}$) of 2% (100 mV). Also, a voltage drop from the power supply to the PC Card will result from resistive losses (V_{PCB}) in the PCB traces and the PCMCIA connector. A typical design would limit the total of these resistive losses to less than 1% (50 mV) of the output voltage. Therefore the allowable voltage drop (V_{DS}) for the TPS2212 is the PCMCIA voltage regulation less the power supply regulation and less the PCB and connector resistive drops:

$$V_{DS} = V_{O(reg)} - V_{PS(reg)} - V_{PCB}$$

Typically, this would leave 100 mV for the allowable voltage drop across the TPS2212. The voltage drop is the output current multiplied by the switch resistance of the TPS2212. Therefore, the maximum output current that can be delivered to the PC Card in regulation is the allowable voltage drop across the TPS2212 divided by the output switch resistance.

$$I_O\text{max} = \frac{V_{DS}}{r_{DS(on)}}$$

The VCC outputs deliver 250 mA continuous at 5 V and 3.3 V within regulation over the operating temperature range. Using the same equations, the PCMCIA specification for output voltage regulation of the 3.3 V output is 300 mV. Using the voltage drop percentages for power supply regulation (2%) and PCB resistive loss (1%), the allowable voltage drop for the 3.3 V switch is 200 mV. The 12-V outputs (VPP) of the TPS2212 can deliver 150 mA continuously.

APPLICATION INFORMATION

overcurrent and overtemperature protection

PC Cards are inherently subject to damage from mishandling. Host systems require protection against short-circuited cards that could lead to power supply or PCB trace damage. Even systems sufficiently robust to withstand a short circuit would still undergo rapid battery discharge into the damaged PC Card, resulting in a sudden loss of system power. Most hosts include fuses for protection. The reliability of fused systems is poor and requires troubleshooting and repair, usually by the manufacturer, when fuses are blown.

The TPS2212 uses sense FETs to check for overcurrent conditions in each of the VCC and VPP outputs. Unlike sense resistors or polyfuses, these FETs do not add to the series resistance of the switch; therefore voltage and power losses are reduced. Overcurrent sensing is applied to each output separately. When an overcurrent condition is detected, only the power output affected is limited; all other power outputs continue to function normally. The $\overline{\text{OC}}$ indicator, normally a logic high, is a logic low when an overcurrent condition is detected providing for initiation of system diagnostics and/or sending a warning message to the user.

During power up, the TPS2212 controls the rise time of the VCC and VPP outputs and limits the current into a faulty card or connector. If a short circuit is applied after power is established (e.g., hot insertion of a bad card), current is initially limited only by the impedance between the short and the power supply. In extreme cases, as much as 5 A to 10 A may flow into the short before the current limiting of the TPS2212 engages. If the VCC or VPP outputs are driven below ground, the TPS2212 may latch nondestructively in an off state. Cycling power will reestablish normal operation.

Overcurrent limiting for the VCC outputs is designed to activate if powered up into a short in the range of 300 mA to 600 mA, typically at about 450 mA. The VPP outputs limit from 120 mA to 400 mA, typically around 280 mA. The protection circuitry acts by linearly limiting the current passing through the switch rather than initiating a full shutdown of the supply. Shutdown occurs only during thermal limiting.

Thermal limiting prevents destruction of the IC from overheating if the package power dissipation ratings are exceeded. Thermal limiting disables power output until the device has cooled.

12-V supply not required

Most PC Card switches use the externally supplied 12 V to power gate drive and other chip functions, which requires that power be present at all times. The TPS2212 offers considerable power savings by using an internal charge pump to generate the required higher voltages from the 5-V input. Therefore, the external 12-V supply can be disabled except when needed for flash-memory functions, thereby extending battery lifetime. Do not ground the VPPI switch input when the VPPI input is not used. Additional power savings are realized by the TPS2212 during a software shutdown in which quiescent current drops to a maximum of 1 µA.

3.3-V low-voltage mode

The TPS2212 will operate in a 3.3-V low-voltage mode when 3.3 V is the only available input voltage ($V_{I(5V)}$ = 0). This allows host and PC Cards to be operated in low-power 3.3-volts-only modes such as sleep or pager modes. Note that in these operation modes, the TPS2212 will derive its bias current from the 3.3-V input pin and only 3.3 V can be delivered to the PC Card.

APPLICATION INFORMATION

voltage transitioning requirement

PC Cards are migrating from 5 V to 3.3 V to minimize power consumption, optimize board space, and increase logic speeds. The TPS2212 meets all combinations of power delivery as currently defined in the PCMCIA standard. The latest protocol accommodates mixed 3.3-V/5-V systems by first powering the card with 5 V, then polling it to determine its 3.3-V compatibility. The PCMCIA specification requires that the capacitors on 3.3-V compatible cards be discharged to below 0.8 V before applying 3.3-V power. This functions as a power reset and ensures that sensitive 3.3-V circuitry is not subjected to any residual 5-V charge. The TPS2212 offers a selectable VCC and VPP ground state, in accordance with PCMCIA 3.3-V/5-V switching specifications.

output ground switches

PC Card specification requires that V_{CC} be discharged within 100 ms. PC Card resistance can not be relied on to provide a discharge path for voltages stored on PC Card capacitance because of possible high-impedance isolation by power-management schemes.

power-supply considerations

The TPS2212 has multiple pins for each of its 3.3-V and 5-V power inputs and for the switched VCC outputs. Any individual pin can conduct the rated input or output current. Unless all pins are connected in parallel, the series resistance is significantly higher than that specified, resulting in increased voltage drops and lost power. It is recommended that all input and output power pins be paralleled for optimum operation.

To increase the noise immunity of the TPS2212, the power supply inputs should be bypassed with a 1-µF electrolytic or tantalum capacitor paralleled by a 0.047-µF to 0.1-µF ceramic capacitor. It is strongly recommended that the switched outputs be bypassed with a 0.1-µF, or larger, ceramic capacitor; doing so improves the immunity of the TPS2212 to electrostatic discharge (ESD). Care should be taken to minimize the inductance of PCB traces between the TPS2212 and the load. High switching currents can produce large negative voltage transients, which forward biases substrate diodes, resulting in unpredictable performance. Similarly, no pin should be taken below –0.3 V.

calculating junction temperature

The switch resistance, $r_{DS(on)}$, is dependent on the junction temperature, T_J, of the die and the current through the switch. To calculate T_J, first find $r_{DS(on)}$ from Figures 16 through 18 using an initial temperature estimate about 50°C above ambient. Then calculate the power dissipation for each switch, using the formula:

$$P_D = r_{DS(on)} \times I^2$$

Next, sum the power dissipation and calculate the junction temperature:

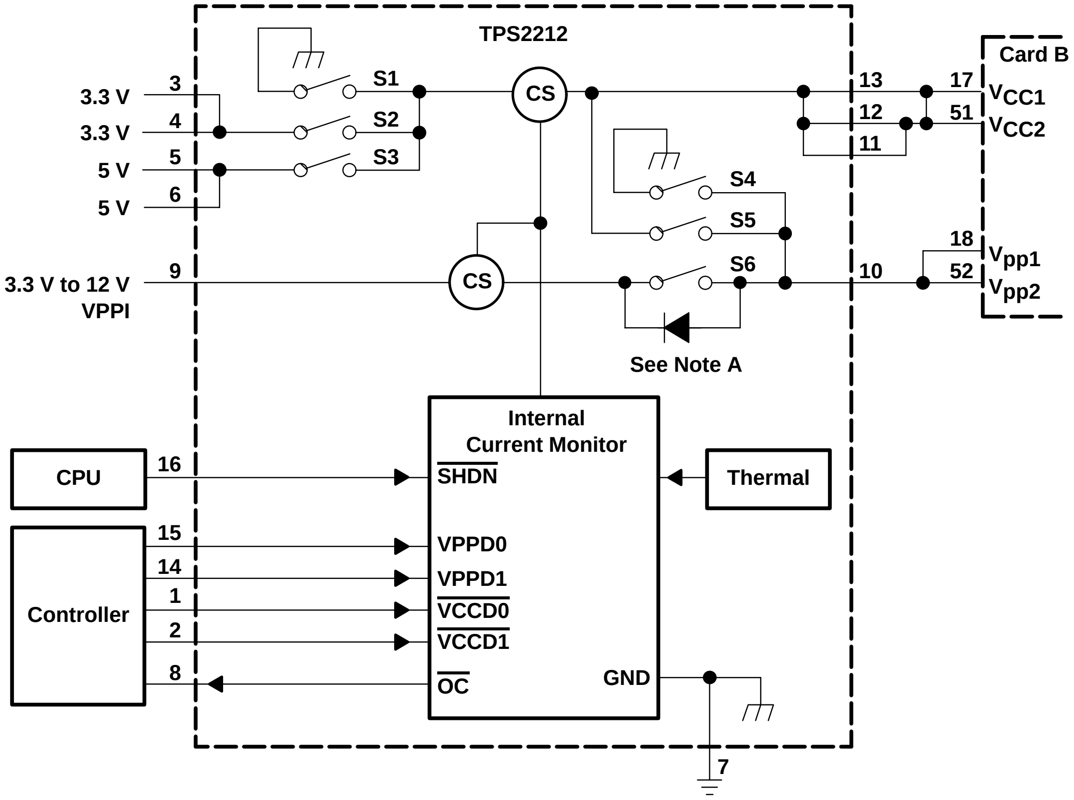
$$T_J = \left(\sum P_D \times R_{\theta JA}\right) + T_A,\ R_{\theta JA} = 108°C/W$$

Compare the calculated junction temperature with the initial temperature estimate. If the temperatures are not within a few degrees of each other, recalculate using the calculated temperature as the initial estimate.

APPLICATION INFORMATION

ESD protection

All TPS2212 inputs and outputs incorporate ESD-protection circuitry designed to withstand a 2-kV human-body-model discharge as defined in MIL-STD-883C, Method 3015. The VCC and VPP outputs can be exposed to potentially higher discharges from the external environment through the PC Card connector. Bypassing the outputs with 0.1-µF capacitors protects the devices from discharges up to 10 kV.



NOTE A: MOSFET switch S6 has a back-gate diode from the source to the drain. Unused switch inputs should never be grounded.

Figure 25. Internal Switching Matrix, TPS2212 Control Logic

APPLICATION INFORMATION

TPS2212 control logic

VPP

CONTROL SIGNALS			INTERNAL SWITCH SETTINGS			OUTPUT
$\overline{\text{SHDN}}$	**VPPD0**	**VPPD1**	**S4**	**S5**	**S6**	**VPP**
1	0	0	CLOSED	OPEN	OPEN	0 V
1	0	1	OPEN	CLOSED	OPEN	VCC†
1	1	0	OPEN	OPEN	CLOSED	VPPI
1	1	1	OPEN	OPEN	OPEN	Hi-Z
0	X	X	OPEN	OPEN	OPEN	Hi-Z

† Output depends on AVCC

VCC

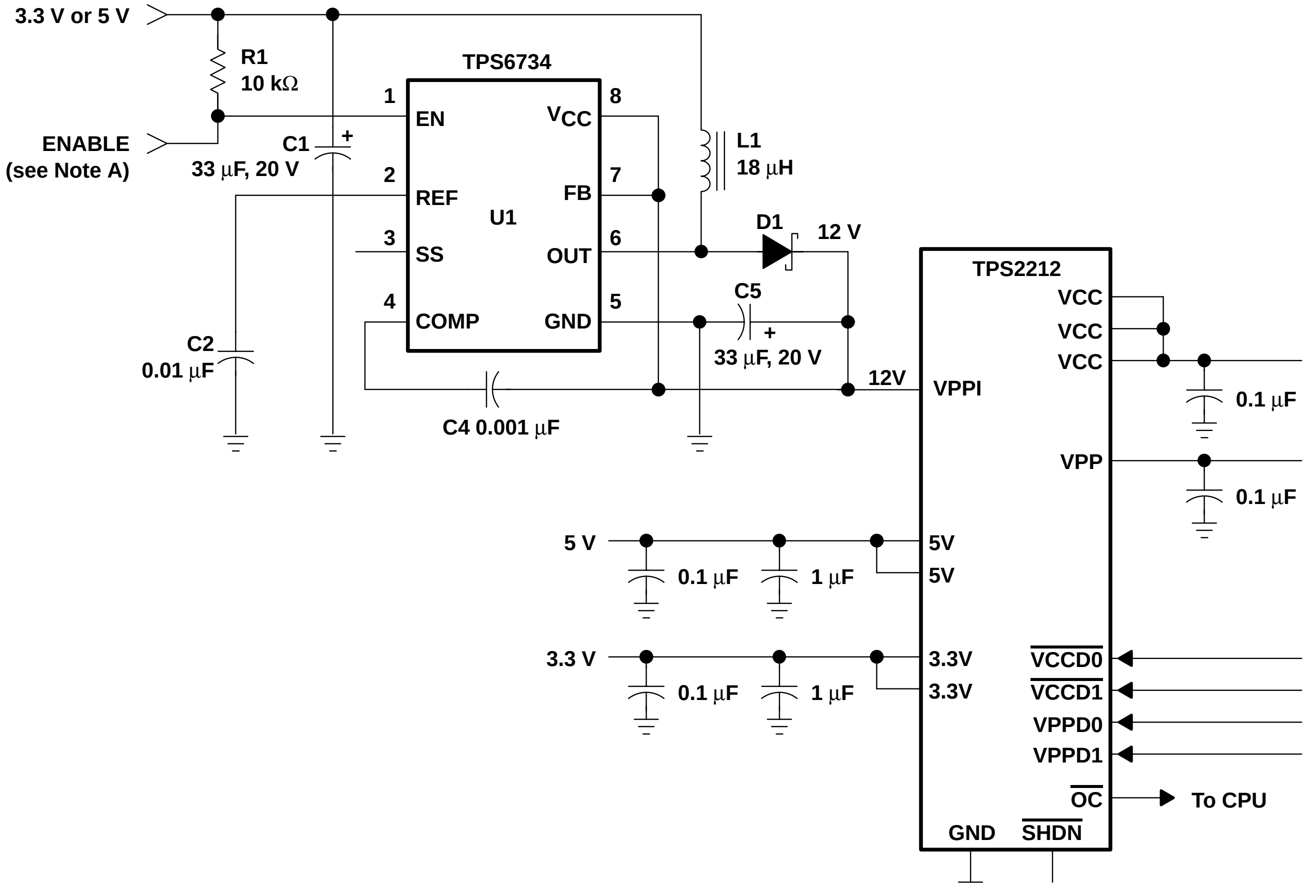
CONTROL SIGNALS			INTERNAL SWITCH SETTINGS			OUTPUT
$\overline{\text{SHDN}}$	**$\overline{\text{VCCD1}}$**	**$\overline{\text{VCCD0}}$**	**S1**	**S2**	**S3**	**VCC**
1	0	0	CLOSED	OPEN	OPEN	0 V
1	0	1	OPEN	CLOSED	OPEN	3.3 V
1	1	0	OPEN	OPEN	CLOSED	5 V
1	1	1	CLOSED	OPEN	OPEN	0 V
0	X	X	OPEN	OPEN	OPEN	Hi-Z

APPLICATION INFORMATION

12-V flash memory supply

The TPS6734 is a fixed 12-V output boost converter capable of delivering 120 mA from inputs as low as 2.7 V. The device is pin-for-pin compatible with the MAX734 regulator and offers the following advantages: lower supply current, wider operating input-voltage range, and higher output currents. As shown in Figure 26, the only external components required are: an inductor, a Schottky rectifier, an output filter capacitor, an input filter capacitor, and a small capacitor for loop compensation. The entire converter occupies less than 0.7 in^2 of PCB space when implemented with surface-mount components. An enable input is provided to shut the converter down and reduce the supply current to 3 µA when 12 V is not needed.

The TPS6734 is a 170-kHz current-mode PWM (pulse-width modulation) controller with an n-channel MOSFET power switch. Gate drive for the switch is derived from the 12-V output after start-up to minimize the die area needed to realize the 0.7-Ω MOSFET and improve efficiency at input voltages below 5 V. Soft start is accomplished with the addition of one small capacitor. A 1.22-V reference (pin 2) is brought out for external use. For additional information, see the TPS6734 data sheet (SLVS127).



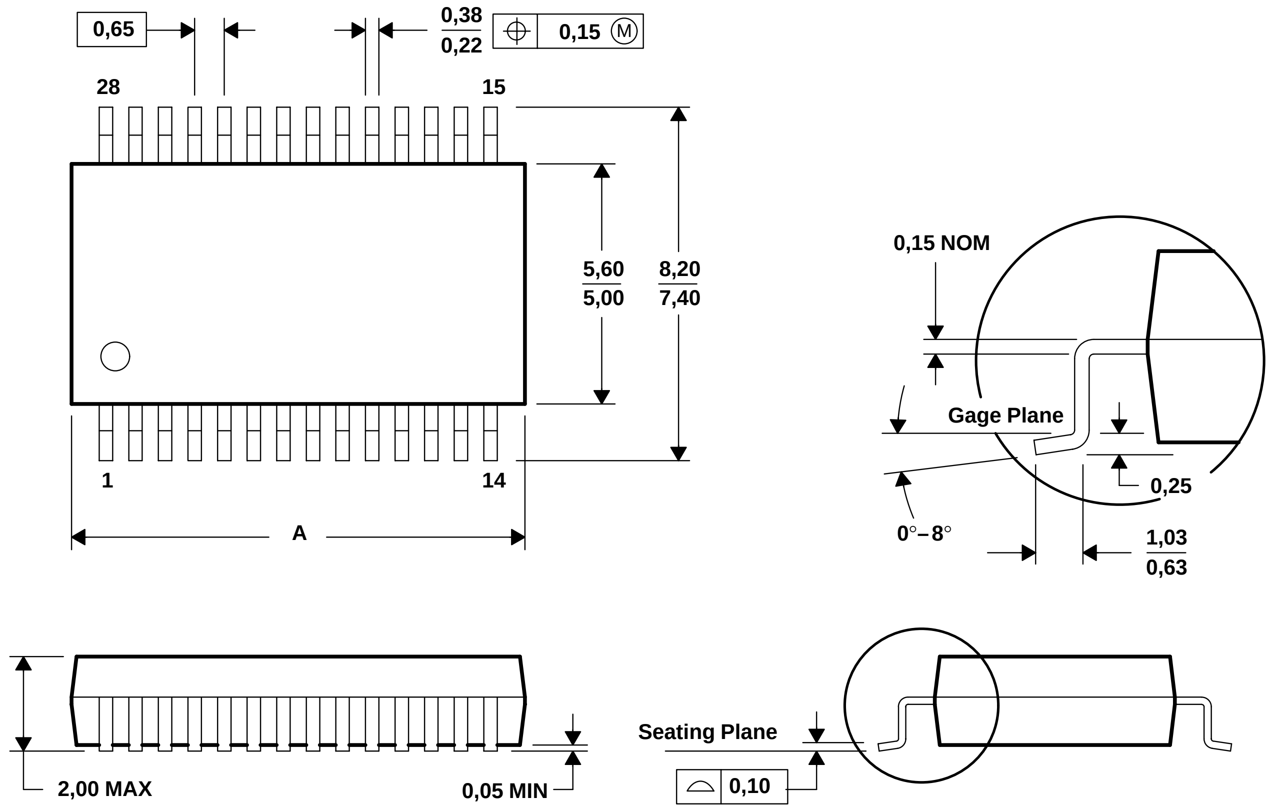
NOTE A: The enable terminal can be tied to a generall purpose I/O terminal on the PCMCIA controller or tied high.

Figure 26. TPS2212 With TPS6734 12-V, 120-mA Supply

MECHANICAL DATA

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

28 PIN SHOWN



DIM \ PINS **	8	14	16	20	24	28	30	38
A MAX	3,30	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	2,70	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 / C 10/95

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-150

PACKAGE OPTION ADDENDUM

27-Feb-2006

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TPS2212IDB	ACTIVE	SSOP	DB	16	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2212IDBG4	ACTIVE	SSOP	DB	16	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2212IDBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2212IDBRG4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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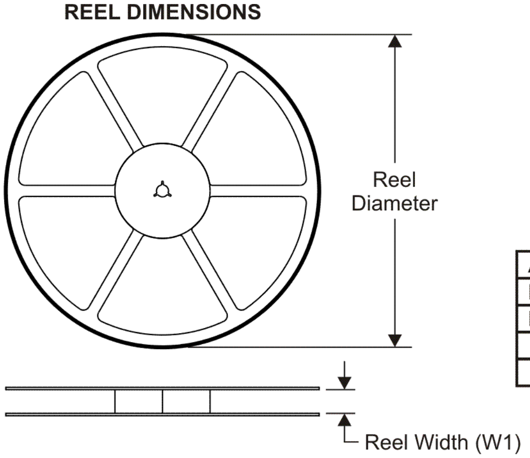
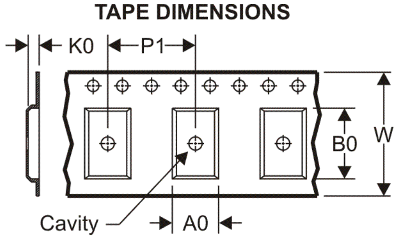
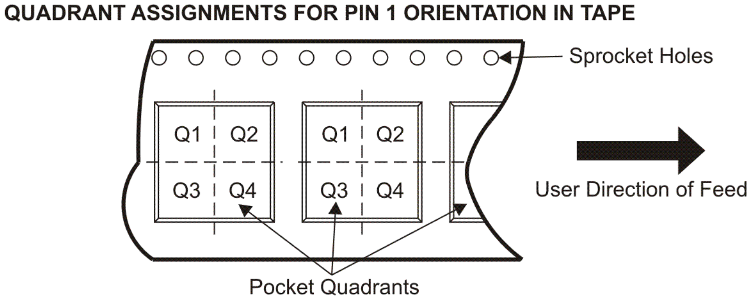




A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

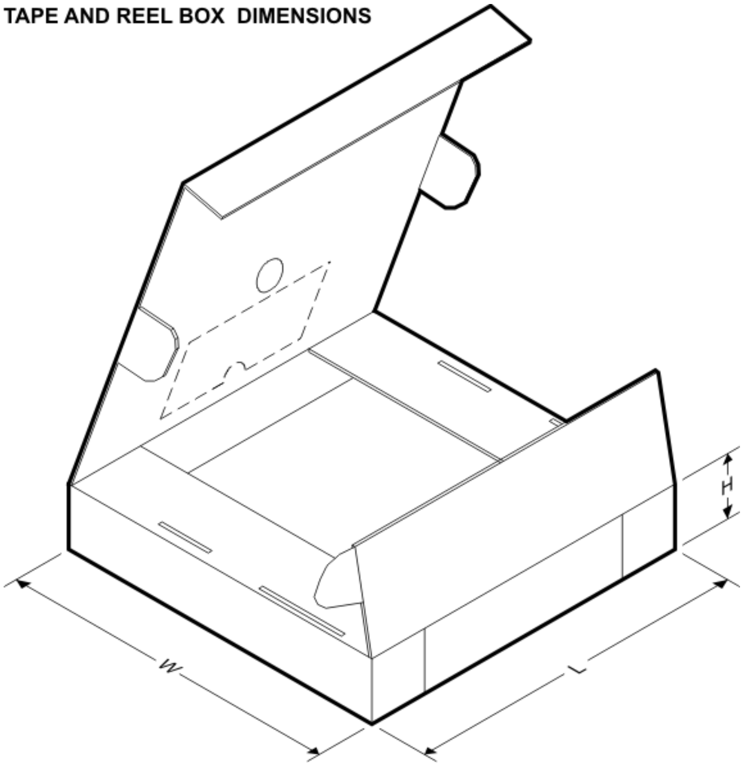


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2212IDBR	SSOP	DB	16	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2212IDBR	SSOP	DB	16	2000	346.0	346.0	33.0

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