

MOSFET

Metal Oxide Semiconductor Field Effect Transistor

CFDA Automotive

650V CoolMOS™ CFDA Power Transistor
IPD65R420CFDA

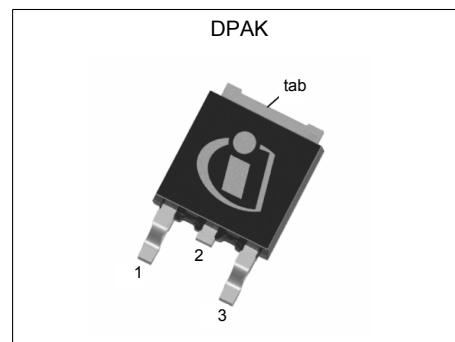
Data Sheet

Rev. 2.1
Final

Automotive

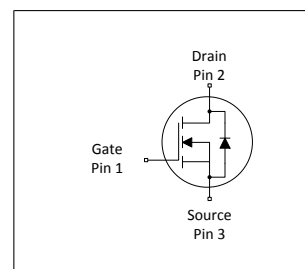
1 Description

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. 650V CoolMOS™ CFDA series combines the experience of the leading SJ MOSFET supplier with high class innovation. The resulting devices provide all benefits of a fast switching SJ MOSFET while offering an extremely fast and robust body diode. This combination of extremely low switching, commutation and conduction losses together with highest robustness make especially resonant switching applications more reliable, more efficient, lighter, and cooler.



Features

- Ultra-fast body diode
- Very high commutation ruggedness
- Extremely low losses due to very low FOM $R_{ds(on)} \cdot Q_g$ and E_{oss}
- Easy to use/drive
- Qualified according to AEC Q101
- Green package (RoHS compliant), Pb-free plating, halogen free for mold compound



Applications

650V CoolMOS™ CFDA is designed for switching applications.



Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	650	V
$R_{DS(on),max}$	0.42	Ω
Q_g,typ	90	nC
$I_D,pulse$	80	A
$E_{oss @ 400V}$	2.8	μJ
Body diode di/dt	500	A/ μs
Q_{rr}	0.7	μC
t_{rr}	140	ns
I_{rrm}	8.8	A

Type / Ordering Code	Package	Marking	Related Links
IPD65R420CFDA	PG-TO 252	65F420A	-

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2 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D			8.7	A	$T_C = 25^\circ\text{C}$
				5.5		$T_C = 100^\circ\text{C}$
Pulsed drain current ²⁾	$I_{D,pulse}$			27	A	$T_C = 25^\circ\text{C}$
Avalanche energy, single pulse	E_{AS}			227	mJ	$I_D = 1.8\text{A}$, $V_{DD} = 50\text{V}$
Avalanche energy, repetitive	E_{AR}			0.34	mJ	$I_D = 1.8\text{A}$, $V_{DD} = 50\text{V}$
Avalanche current, repetitive	I_{AR}			1.8	A	
MOSFET dv/dt ruggedness	dv/dt			50	V/ns	$V_{DS} = 0 \dots 400\text{V}$
Gate source voltage	V_{GS}	-20		20	V	static
		-30		30		AC ($f > 1\text{ Hz}$)
Power dissipation (SMD) DPAK	P_{tot}			83.3	W	$T_C = 25^\circ\text{C}$
Operating and storage temperature	T_j, T_{stg}	-40		150	$^\circ\text{C}$	
Continuous diode forward current	I_S			8.7	A	$T_C = 25^\circ\text{C}$
Diode pulse current	$I_{S,pulse}$			27	A	$T_C = 25^\circ\text{C}$
Reverse diode dv/dt ³⁾	dv/dt			50	V/ns	$V_{DS} = 0 \dots 400\text{V}$, $I_{SD} \leq I_D$, $T_j = 25^\circ\text{C}$
Maximum diode commutation speed	di/dt			900	A/ μs	

¹⁾ Limited by $T_{j,max}$

²⁾ Pulse width t_p limited by $T_{j,max}$

³⁾ Identical low side and high side switch with identical R_G

3 Thermal characteristics

Table 3 Thermal characteristics DPAK

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}			1.5	K/W	
Thermal resistance, junction - ambient ¹⁾	R_{thJA}			62	K/W	SMD version, device on PCB, minimal footprint
			35			SMD version, device on PCB, 6cm ² cooling area
Soldering temperature, wave- & reflowsoldering allowed	T_{sold}			260	°C	reflow MSL

¹⁾ Device on 40mm*40mm*1.5mm one layer epoxy PCB FR4 with 6cm² copper area (thickness 70µm) for drain connection. PCB is vertical without air stream cooling.

4 Electrical characteristics

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	650			V	$V_{GS} = 0V, I_D = 1mA$
Gate threshold voltage	$V_{GS(th)}$	3.5	4	4.5	V	$V_{DS} = V_{GS}, I_D = 0.3445mA$
Zero gate voltage drain current	I_{DSS}			5	μA	$V_{DS} = 650V, V_{GS} = 0V, T_j = 25^\circ\text{C}$
			600			$V_{DS} = 650V, V_{GS} = 0V, T_j = 150^\circ\text{C}$
Gate-source leakage current	I_{GSS}			100	nA	$V_{GS} = 20V, V_{DS} = 0V$
Drain-source on-state resistance	$R_{DS(on)}$		0.378	0.42	Ω	$V_{GS} = 10V, I_D = 3.4A, T_j = 25^\circ\text{C}$
			0.983			$V_{GS} = 10V, I_D = 3.4A, T_j = 150^\circ\text{C}$
Gate resistance	R_G		4		Ω	$f = 1MHz$, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}		870		pF	$V_{GS} = 0V, V_{DS} = 100V, f = 1MHz$
Output capacitance	C_{oss}		45		pF	
Effective output capacitance, energy related ¹⁾	$C_{o(er)}$		36		pF	$V_{GS} = 0V, V_{DS} = 0 \dots 400V$
Effective output capacitance, time related ²⁾	$C_{o(tr)}$		161		pF	$I_D = \text{constant}, V_{GS} = 0V, V_{DS} = 0 \dots 400V$
Turn-on delay time	$t_{d(on)}$		10		ns	$V_{DD} = 400V, V_{GS} = 13V, I_D = 5.2A, R_G = 3.4\Omega$
Rise time	t_r		7		ns	
Turn-off delay time	$t_{d(off)}$		38		ns	
Fall time	t_f		8		ns	

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}		5.5		nC	$V_{DD} = 480V, I_D = 5.2A, V_{GS} = 0 \text{ to } 10V$
Gate to drain charge	Q_{gd}		17.5		nC	
Gate charge total	Q_g		32		nC	
Gate plateau voltage	$V_{plateau}$		6.4		V	

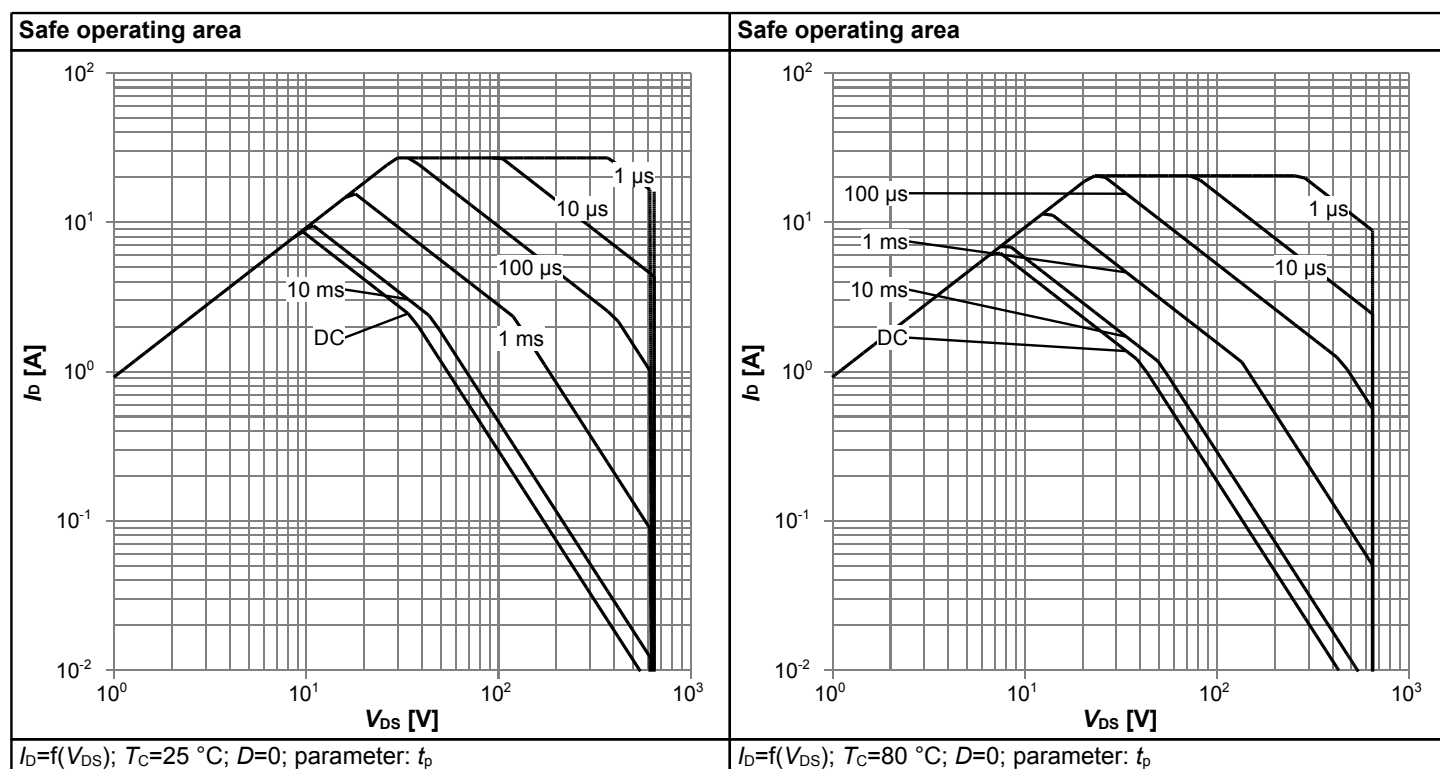
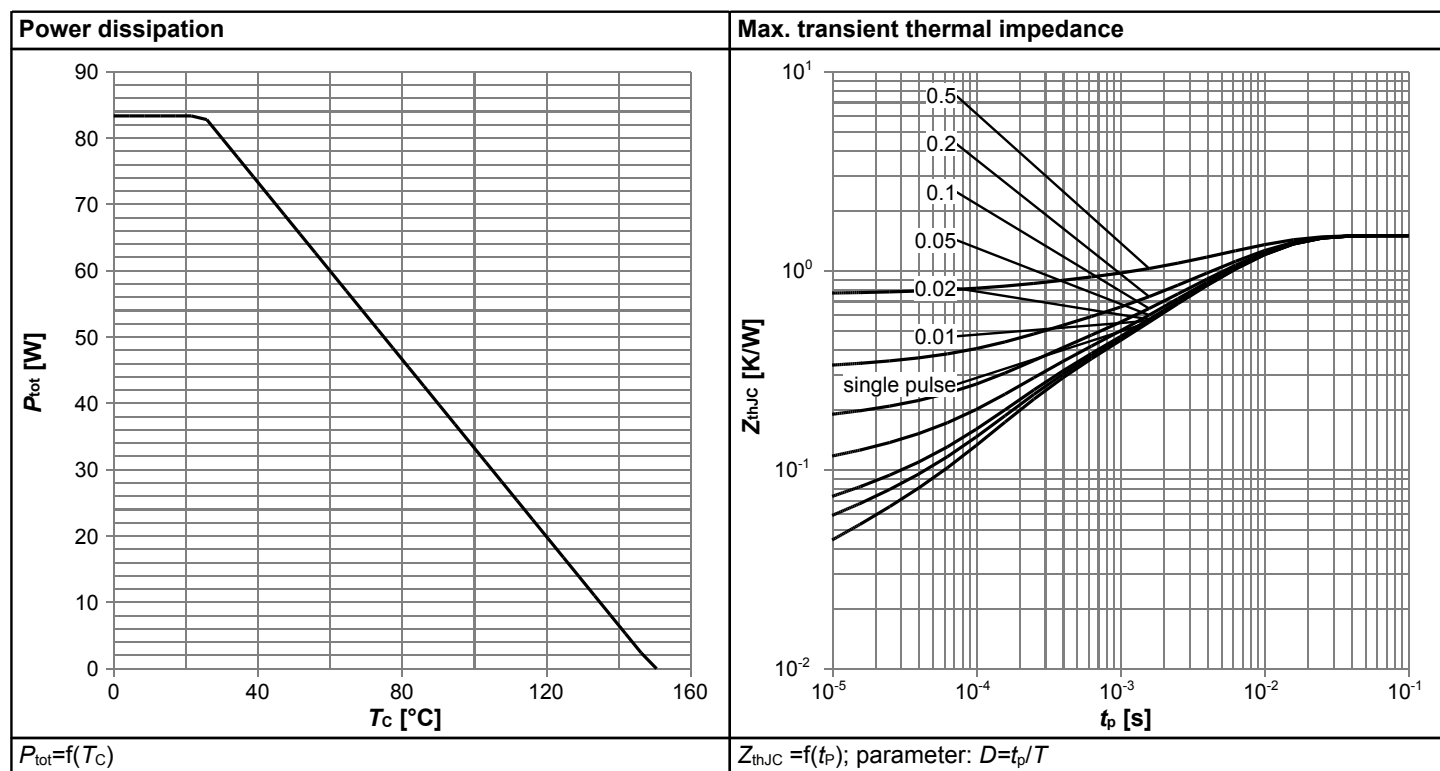
¹⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V

²⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

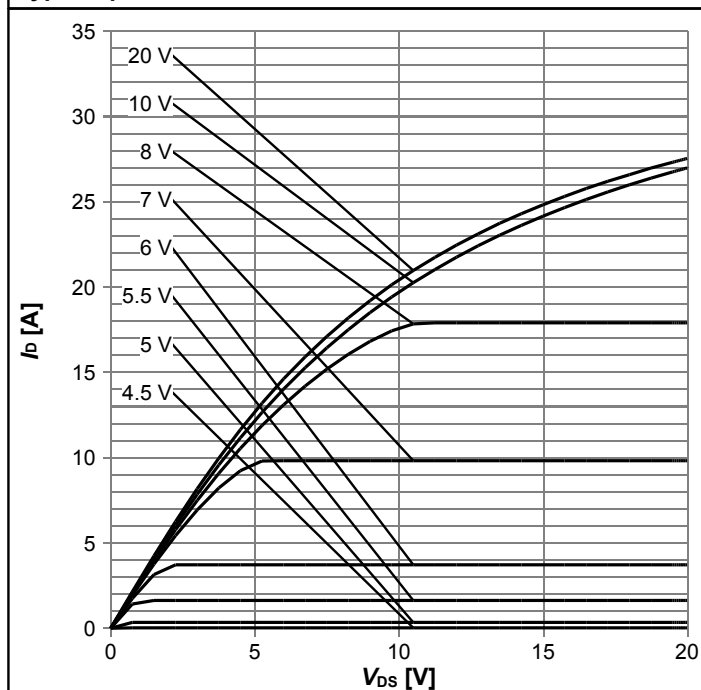
Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}		0.9		V	$V_{GS} = 0V$, $I_F = 5.2A$, $T_J = 25^\circ C$
Reverse recovery time	t_{rr}		90		ns	$V_R = 400V$, $I_F = 5.2A$, $di_F/dt = 100A/\mu s$ (see table 8)
Reverse recovery charge	Q_{rr}		0.3		μC	
Peak reverse recovery current	I_{rrm}		6.2		A	

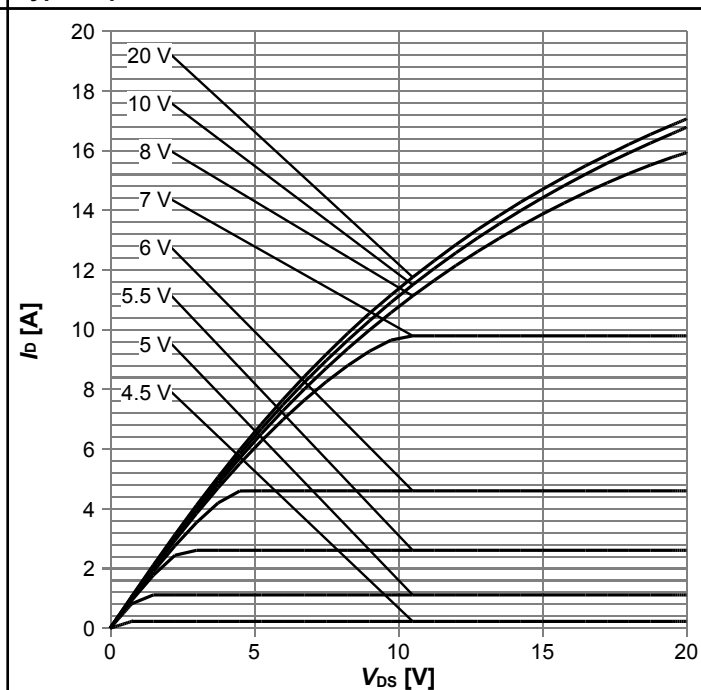
5 Electrical characteristics diagrams



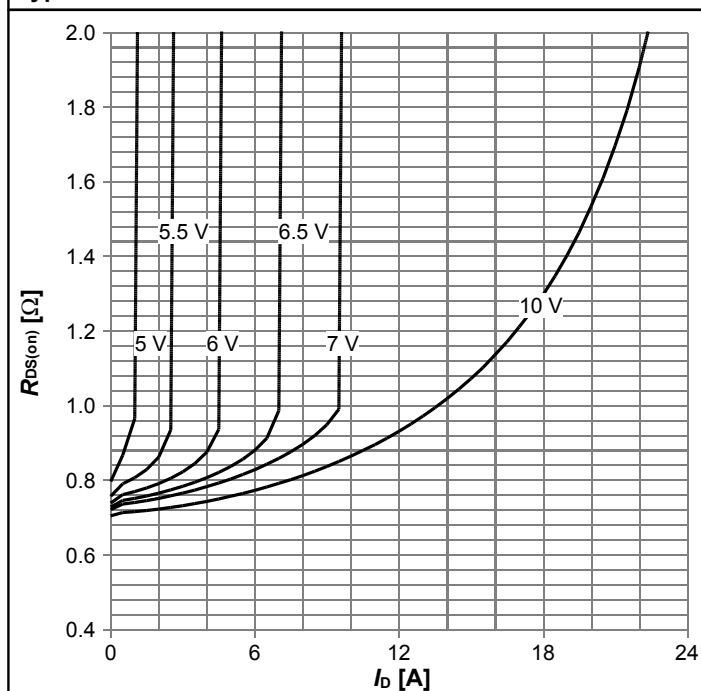
Typ. output characteristics


 $I_D = f(V_{DS})$; $T_j = 25^\circ\text{C}$; parameter: V_{GS}

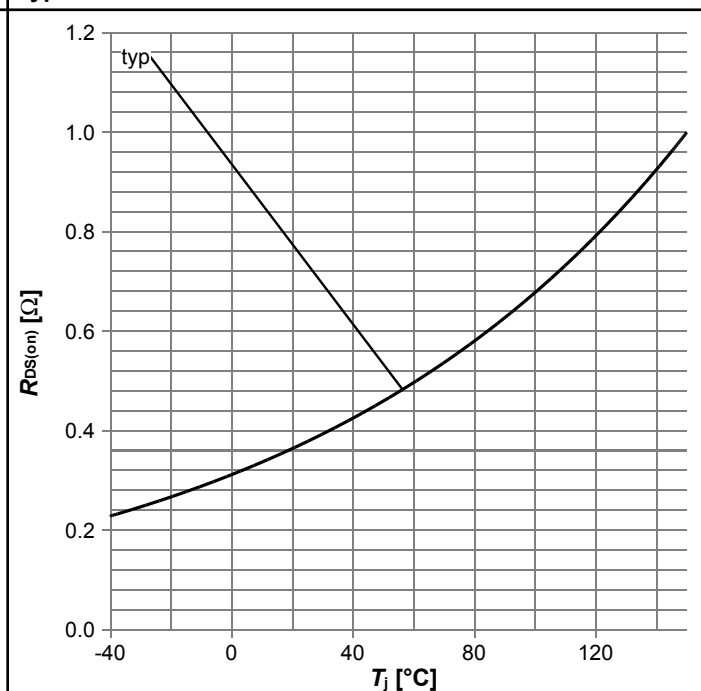
Typ. output characteristics


 $I_D = f(V_{DS})$; $T_j = 125^\circ\text{C}$; parameter: V_{GS}

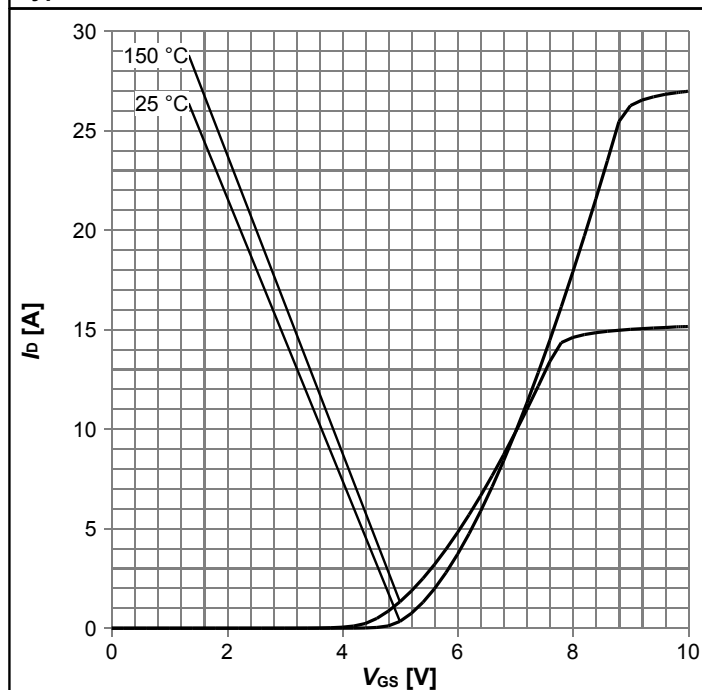
Typ. drain-source on-state resistance


 $R_{DS(on)} = f(I_D)$; $T_j = 125^\circ\text{C}$; parameter: V_{GS}

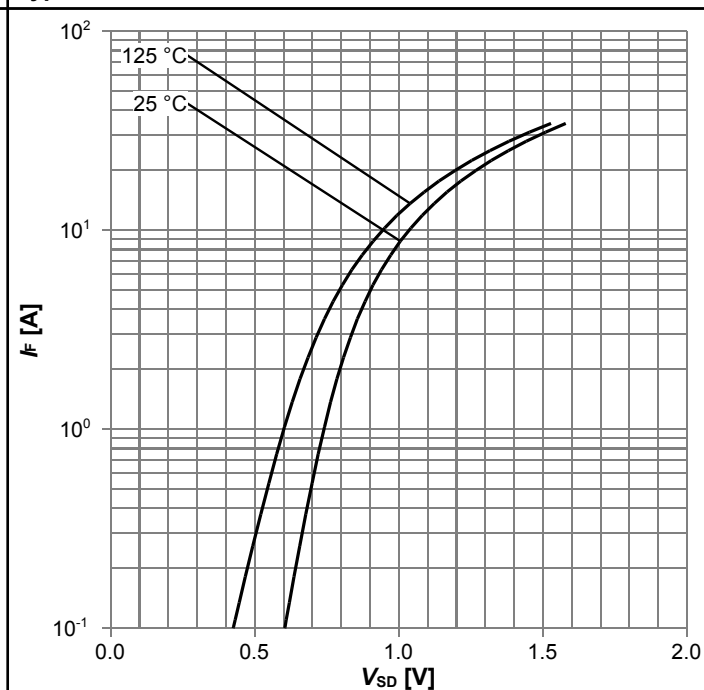
Typ. drain-source on-state resistance


 $R_{DS(on)} = f(T_j)$; $I_D = 18.1$ A; $V_{GS} = 10$ V

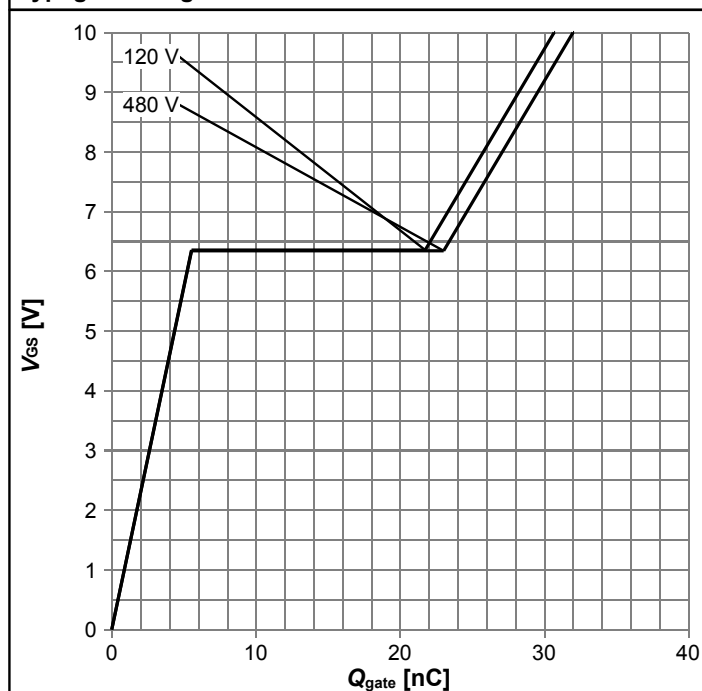
Typ. transfer characteristics


 $I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}; \text{parameter: } T_j$

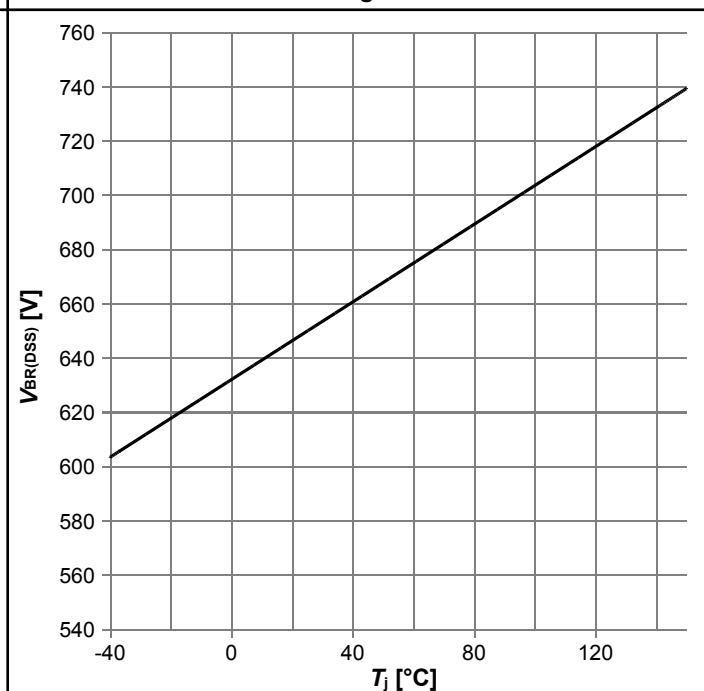
Typ. forward characteristics of reverse diode


 $I_F = f(V_{SD}); \text{parameter: } T_j$

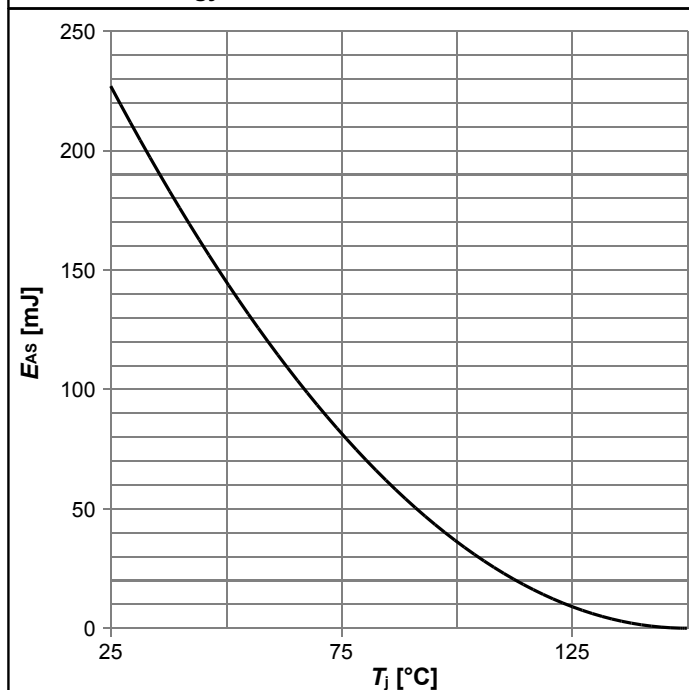
Typ. gate charge


 $V_{GS} = f(Q_{gate}); I_D = 5.1 \text{ A pulsed}; \text{parameter: } V_{DD}$

Drain-source breakdown voltage

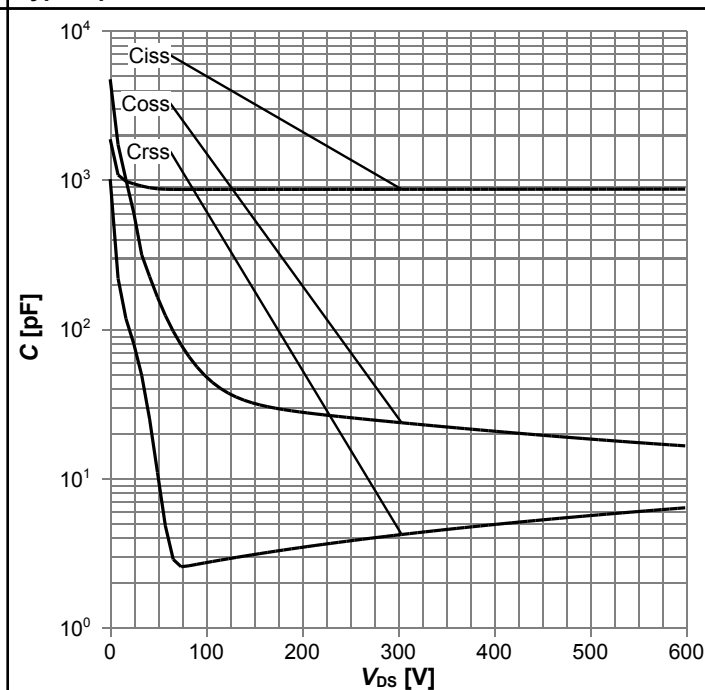

 $V_{BR(DSS)} = f(T_j); I_D = 0.25 \text{ mA}$

Avalanche energy



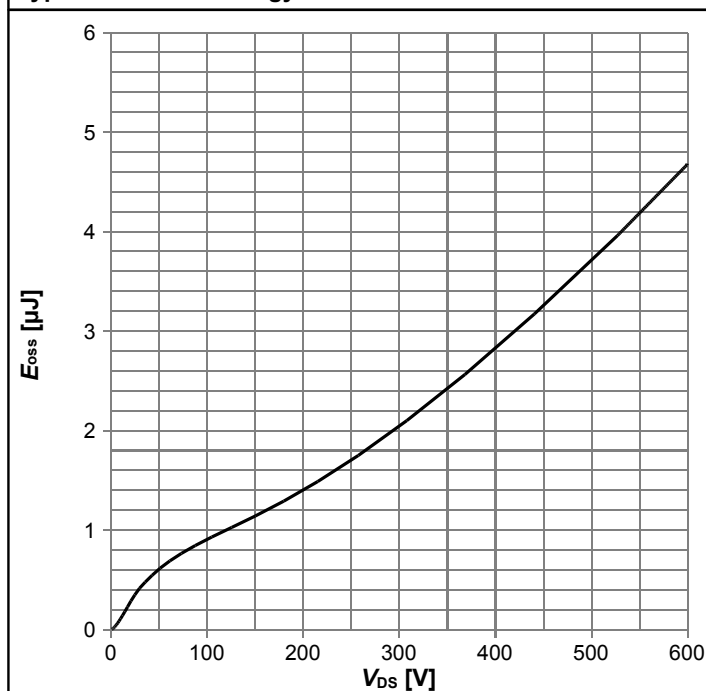
$$E_{AS}=f(T_J); I_D=1.8 \text{ A}; V_{DD}=50 \text{ V}$$

Typ. capacitances



$$C=f(V_{DS}); V_{GS}=0 \text{ V}; f=1 \text{ MHz}$$

Typ. Coss stored energy



$$E_{Coss}=f(V_{DS})$$

6 Test Circuits

Table 8 Diode characteristics

Test circuit for diode characteristics

$R_{g1} = R_{g2}$

Diode recovery waveform

$t_{rr} = t_F + t_S$
 $Q_{rr} = Q_F + Q_S$

Table 9 Switching times

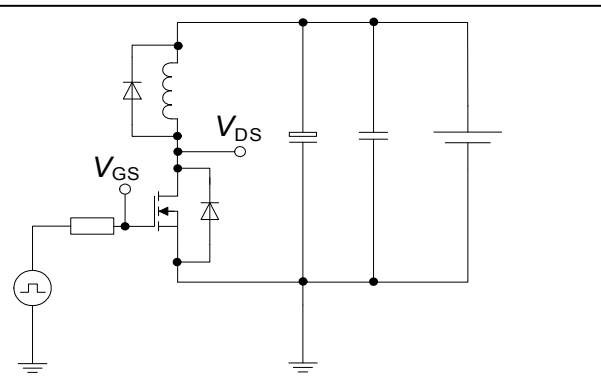
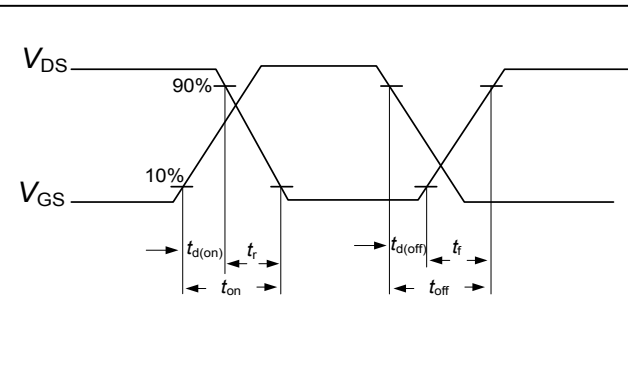
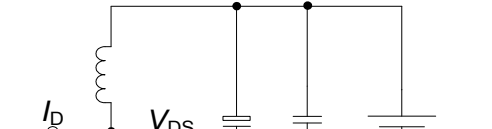
Switching times test circuit for inductive load	Switching times waveform
 The circuit diagram illustrates a MOSFET switching an inductive load. A pulse generator is connected to the gate of the MOSFET through a resistor. The drain of the MOSFET is connected to a load consisting of an inductor and a diode in parallel, which is then connected to a DC voltage source. The drain-source voltage V_{DS} is measured across the load. The MOSFET's body diode is also shown.	 The waveform diagram shows the switching transitions of the MOSFET. The top trace represents the drain-source voltage V_{DS}, and the bottom trace represents the gate-source voltage V_{GS}. The transitions are marked at 10% and 90% of the voltage levels. The timing parameters are defined as follows: $t_{d(on)}$: Delay time from the 10% V_{GS} level to the 90% V_{DS} level during turn-on. t_r: Rise time from the 90% V_{DS} level to the plateau during turn-on. t_{on}: Total turn-on time from the 10% V_{GS} level to the plateau. $t_{d(off)}$: Delay time from the 90% V_{DS} level to the 10% V_{GS} level during turn-off. t_f: Fall time from the plateau to the 90% V_{DS} level during turn-off. t_{off}: Total turn-off time from the plateau to the 10% V_{GS} level.

Table 10 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform
	

7 Package Outlines

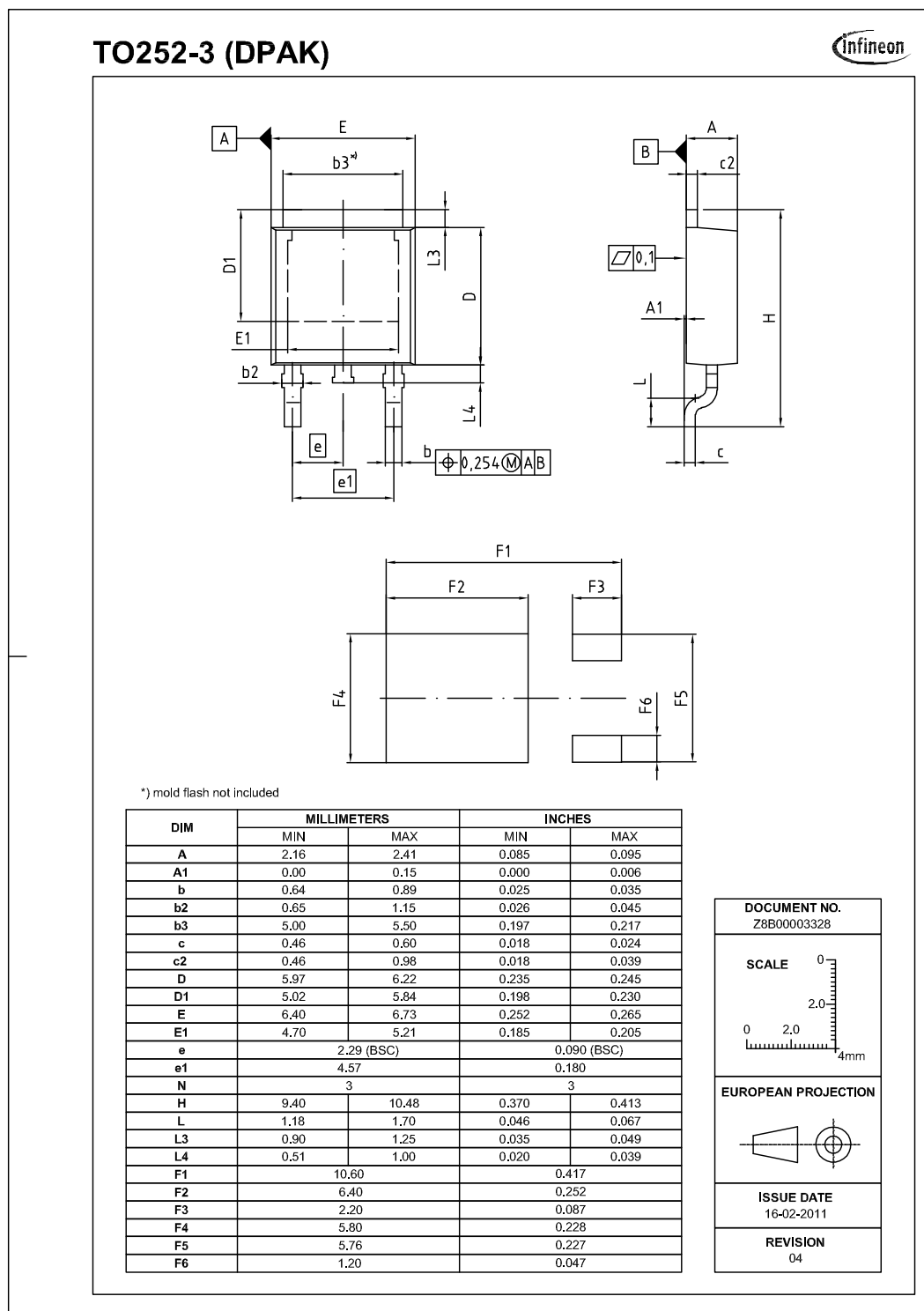


Figure 1 Outline PG-TO 252, dimensions in mm/inches

Revision History

IPD65R420CFDA

Revision: 2015-02-11, Rev. 2.1

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2012-07-12	Preliminary
2.1	2015-02-11	Correction of Marking Code

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