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July 2014

FDFMA2P853

Integrated P-Channel PowerTrench[®] MOSFET and Schottky Diode[®]

General Description

This device is designed specifically as a single package solution for the battery charge switch in cellular handset and other ultra-portable applications. It features a MOSFET with low on-state resistance and an independently connected low forward voltage schottky diode for minimum conduction losses.

The MicroFET 2x2 package offers exceptional thermal performance for its size and is well suited to linear mode applications.

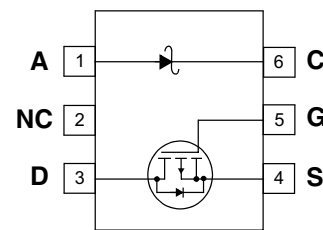
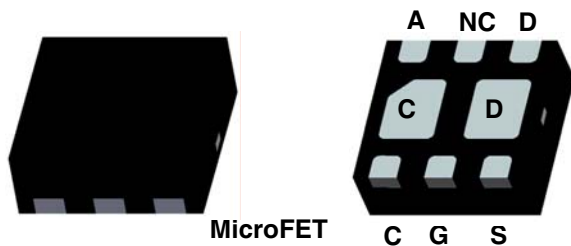
Features

MOSFET:

- -3.0 A, -20V. $R_{DS(ON)} = 120\text{ m}\Omega @ V_{GS} = -4.5\text{ V}$
- $R_{DS(ON)} = 160\text{ m}\Omega @ V_{GS} = -2.5\text{ V}$
- $R_{DS(ON)} = 240\text{ m}\Omega @ V_{GS} = -1.8\text{ V}$

Schottky:

- $V_F < 0.46\text{ V @ } 500\text{ mA}$
- Low Profile - 0.8 mm maximum - in the new package MicroFET 2x2 mm
- RoHS Compliant



Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	MOSFET Drain-Source Voltage	-20	V
V_{GSS}	MOSFET Gate-Source Voltage	± 8	V
I_D	Drain Current -Continuous (Note 1a)	-3.0	A
		-6	
V_{RRM}	Schottky Repetitive Peak Reverse voltage	30	V
I_O	Schottky Average Forward Current (Note 1a)	1	A
P_D	Power dissipation for Single Operation (Note 1a)	1.4	W
		0.7 (Note 1b)	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	Units
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	86
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1b)	173
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1c)	86
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1d)	140

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape Width	Quantity
.853	FDFMA2P853	7inch	8mm	3000 units

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$, Referenced to 25°C		-12		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -16\text{ V}, V_{GS} = 0\text{ V}$			-1	μA
I_{GSS}	Gate-Body Leakage	$V_{GS} = \pm 8\text{ V}, V_{DS} = 0\text{ V}$			± 100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-0.4	-0.7	-1.3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$, Referenced to 25°C		2		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -4.5\text{ V}, I_D = -3.0\text{ A}$ $V_{GS} = -2.5\text{ V}, I_D = -2.5\text{ A}$ $V_{GS} = -1.8\text{ V}, I_D = -1.0\text{ A}$ $V_{GS} = -4.5\text{ V}, I_D = -3.0\text{ A}, T_J = 125^\circ\text{C}$		90 120 172 118	120 160 240 160	m Ω
$I_{D(on)}$	On-State Drain Current	$V_{GS} = -4.5\text{ V}, V_{DS} = -5\text{ V}$	-20			A
g_{FS}	Forward Transconductance	$V_{DS} = -5\text{ V}, I_D = -3.0\text{ A}$		7		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		435		pF
C_{oss}	Output Capacitance			80		pF
C_{rss}	Reverse Transfer Capacitance			45		pF
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -10\text{ V}, I_D = -1\text{ A},$ $V_{GS} = -4.5\text{ V}, R_{GEN} = 6\ \Omega$		9	18	ns
t_r	Turn-On Rise Time			11	19	ns
$t_{d(off)}$	Turn-Off Delay Time			15	27	ns
t_f	Turn-Off Fall Time			6	12	ns
Q_g	Total Gate Charge	$V_{DS} = -10\text{ V}, I_D = -3.0\text{ A},$ $V_{GS} = -4.5\text{ V}$		4	6	nC
Q_{gs}	Gate-Source Charge			0.8		nC
Q_{gd}	Gate-Drain Charge			0.9		nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current				-1.1	A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -1.1\text{ A}$ (Note 2)		-0.8	-1.2	V
t_{rr}	Diode Reverse Recovery Time	$I_F = -3.0\text{ A},$ $dI_F/dt = 100\text{ A}/\mu\text{s}$		17		ns
Q_{rr}	Diode Reverse Recovery Charge			6		nC
Schottky Diode Characteristics						
I_R	Reverse Leakage	$V_R = 5\text{ V}$	$T_J = 25^\circ\text{C}$ $T_J = 125^\circ\text{C}$	9.9 2.3	50 10	μA mA
I_R	Reverse Leakage	$V_R = 20\text{ V}$	$T_J = 25^\circ\text{C}$ $T_J = 85^\circ\text{C}$ $T_J = 125^\circ\text{C}$	9.9 0.3 2.3	100 1 10	μA mA mA
V_F	Forward Voltage	$I_F = 500\text{ mA}$	$T_J = 25^\circ\text{C}$ $T_J = 125^\circ\text{C}$	0.4 0.3	0.46 0.35	V
V_F	Forward Voltage	$I_F = 1\text{ A}$	$T_J = 25^\circ\text{C}$ $T_J = 125^\circ\text{C}$	0.5 0.49	0.55 0.54	V

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

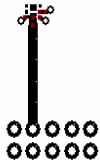
Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² oz. copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.

- (a) MOSFET $R_{\theta JA} = 86^\circ\text{C/W}$ when mounted on a 1 in² pad of 2 oz copper, 1.5" x 1.5" x 0.062" thick PCB
- (b) MOSFET $R_{\theta JA} = 173^\circ\text{C/W}$ when mounted on a minimum pad of 2 oz copper
- (c) Schottky $R_{\theta JA} = 86^\circ\text{C/W}$ when mounted on a 1 in² pad of 2 oz copper, 1.5" x 1.5" x 0.062" thick PCB
- (d) Schottky $R_{\theta JA} = 140^\circ\text{C/W}$ when mounted on a minimum pad of 2 oz copper



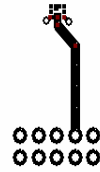
a) 86°C/W when mounted on a 1 in² pad of 2 oz copper



b) 173°C/W when mounted on a minimum pad of 2 oz copper



c) 86°C/W when mounted on a 1 in² pad of 2 oz copper



d) 140°C/W when mounted on a minimum pad of 2 oz copper

Scale 1: 1 on letter size paper

2. Pulse Test: Pulse Width < 300 μs , Duty Cycle < 2.0%

Typical Characteristics

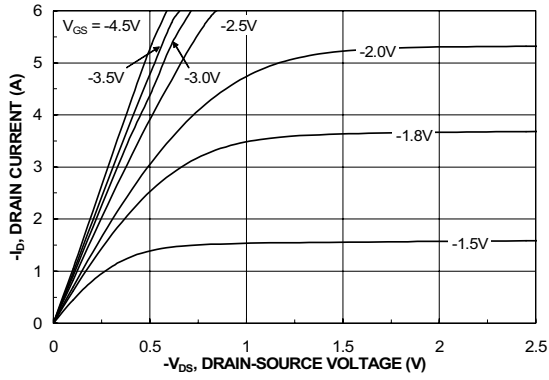


Figure 1. On-Region Characteristics

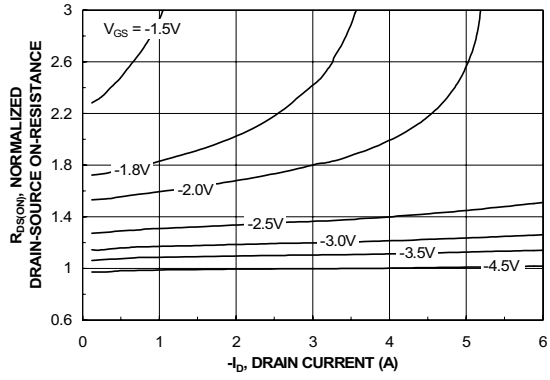


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

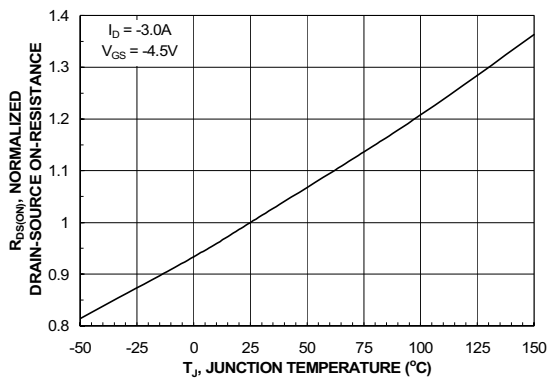


Figure 3. On-Resistance Variation with Temperature

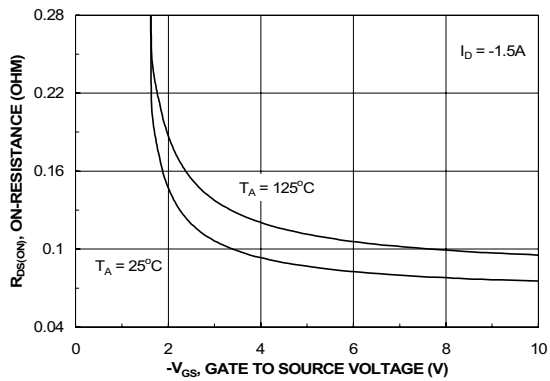


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

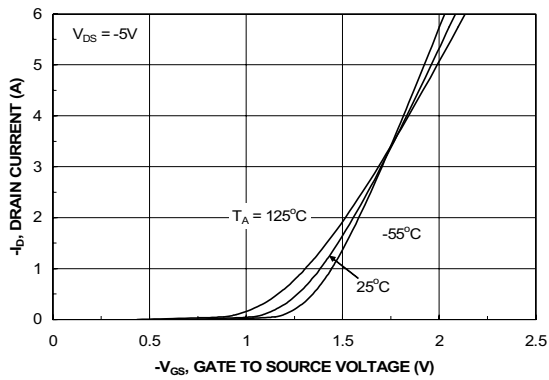


Figure 5. Transfer Characteristics

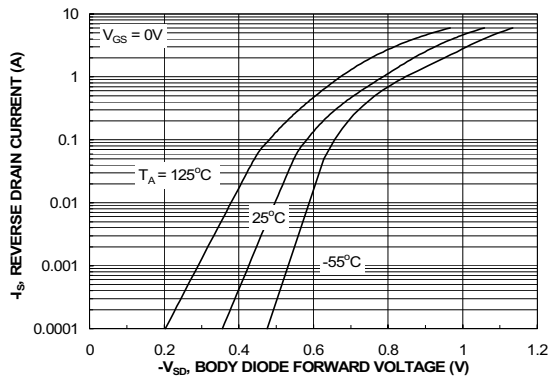


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

Typical Characteristics

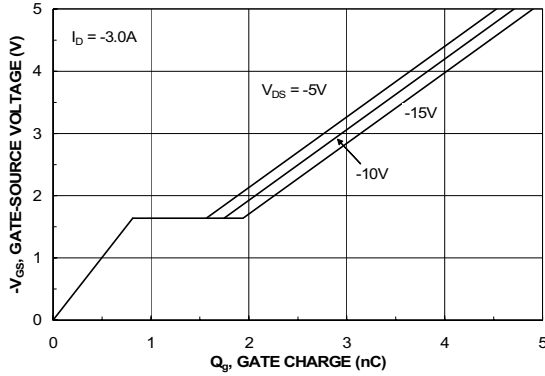


Figure 7. Gate Charge Characteristics

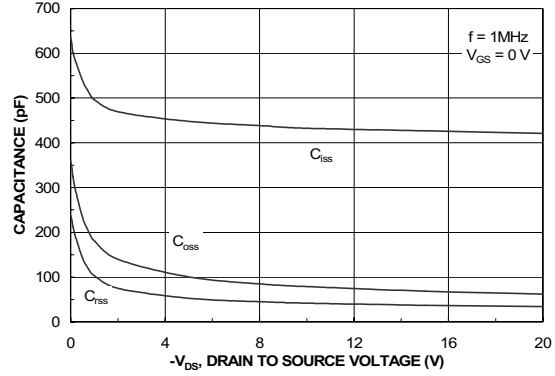


Figure 8. Capacitance Characteristics

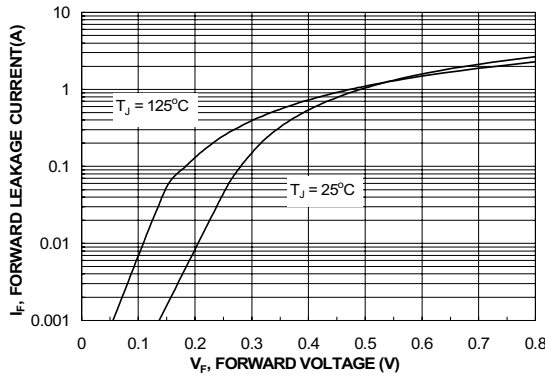


Figure 9. Schottky Diode Forward Voltage

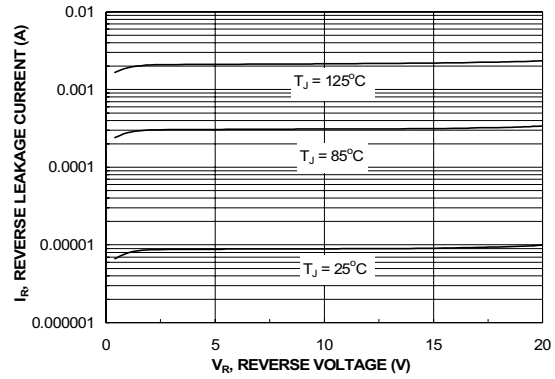


Figure 10. Schottky Diode Reverse Current

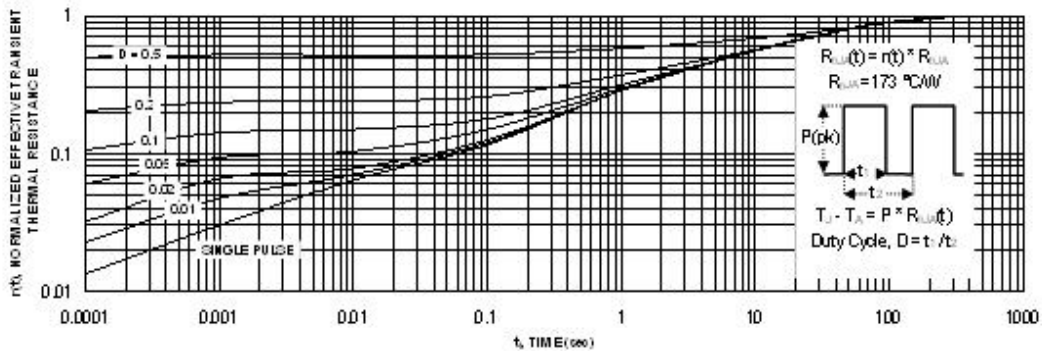
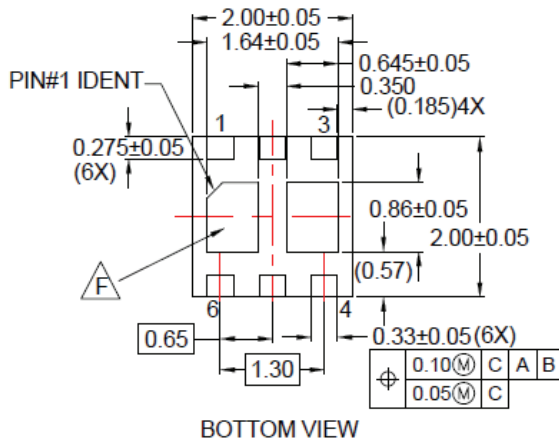
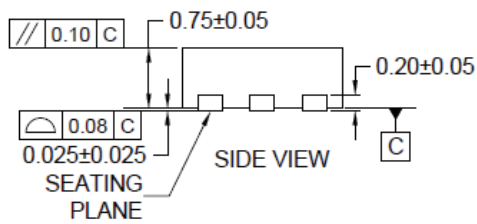
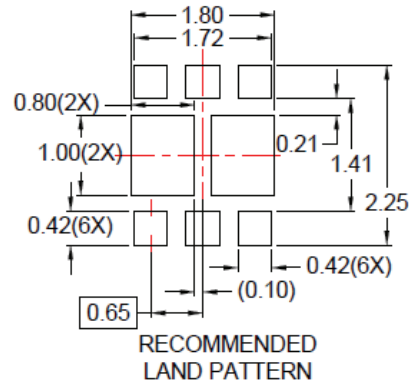
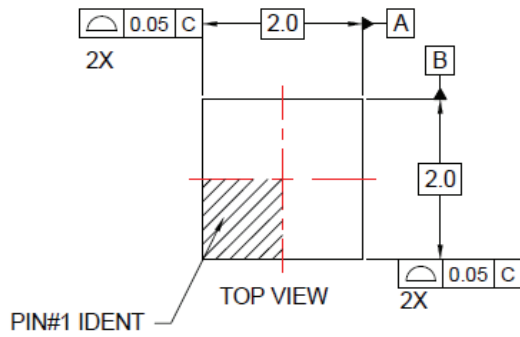


Figure 11. Transient Thermal Response Curve

Thermal characterization performed using the conditions described in Note 1c.
 Transient thermal response will change depending on the circuit board design.

Dimensional Outline and Pad Layout



NOTES:

- A. CONFORM TO JADEC REGISTRATIONS MO-229, VARIATION VCCC, EXCEPT WHERE NOTED.
 - B. DIMENSIONS ARE IN MILLIMETERS.
 - C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
 - D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.
 - E. DRAWING FILENAME: MKT-UMLP16Erev4
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