

**FOUR OUTPUT DIFFERENTIAL BUFFER FOR PCIe GEN1-3**
**9DB433**
**Description**

The 9DB433 zero-delay buffer supports PCIe Gen3 requirements, while being backwards compatible to PCIe Gen2 and Gen1. The 9DB433 is driven by a differential SRC output pair from an IDT 932S421 or 932SQ420 or equivalent main clock generator.

**Typical Applications**

4 output PCIe Gen1-3 zero-delay/fanout buffer

**Key Specifications**

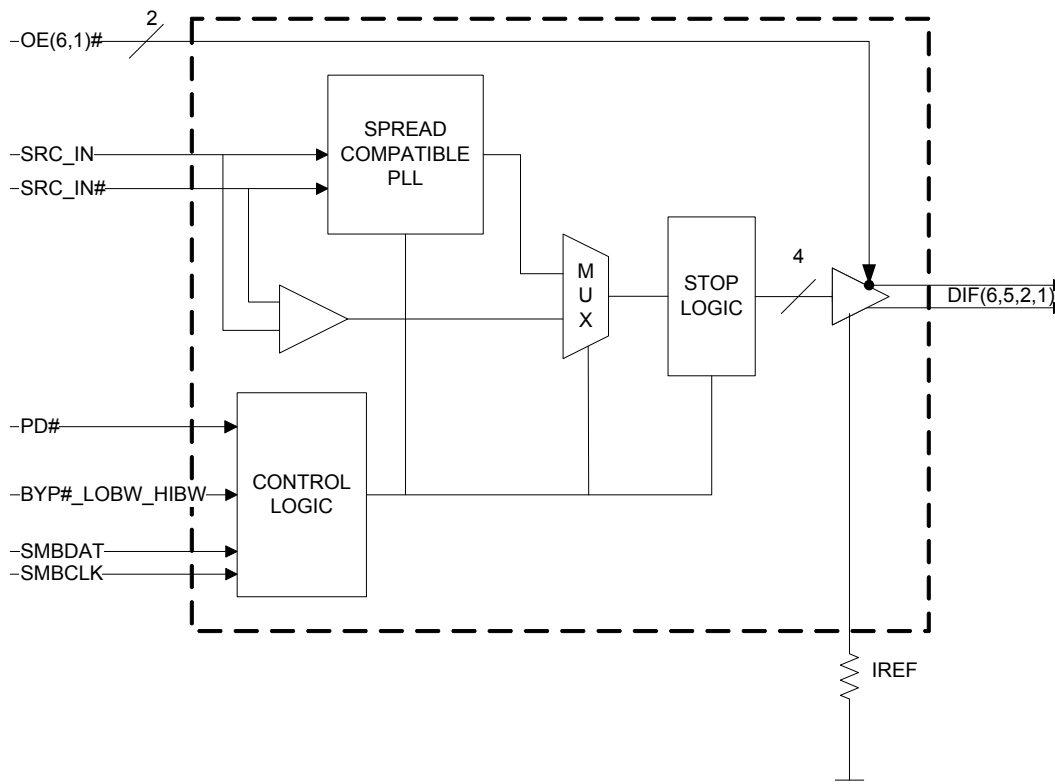
- Output cycle-cycle jitter <50ps
- Output to Output skew <50ps
- Phase jitter: PCIe Gen3 <1.0ps rms

**Features**

- 3 selectable SMBus addresses; multiple devices can share the same SMBus segment
- OE# pins; suitable for Express Card applications
- PLL or bypass mode; PLL can dejitter incoming clock
- Selectable PLL bandwidth; minimizes jitter peaking in downstream PLLs
- Spread spectrum compatible; tracks spreading input clock for low EMI
- SMBus interface; unused outputs can be disabled
- Supports undriven differential outputs in Power Down mode for power management

**Output Features**

- 4 0.7V current-mode differential HCSL output pairs
- Supports zero delay buffer mode and fanout mode
- Selectable bandwidth
- 50-110MHz operation in PLL mode
- 5-166MHz operation in Bypass mode

**Block Diagram**


## Pin Configuration

|                |    |        |    |             |
|----------------|----|--------|----|-------------|
| VDDR           | 1  | 9DB433 | 28 | VDDA        |
| SRC_IN         | 2  |        | 27 | GNDA        |
| SRC_IN#        | 3  |        | 26 | IREF        |
| GND            | 4  |        | 25 | PD#         |
| VDD            | 5  |        | 24 | VDD         |
| DIF_1          | 6  |        | 23 | DIF_6       |
| DIF_1#         | 7  |        | 22 | DIF_6#      |
| OE1#           | 8  |        | 21 | OE6#        |
| DIF_2          | 9  |        | 20 | DIF_5       |
| DIF_2#         | 10 |        | 19 | DIF_5#      |
| VDD            | 11 |        | 18 | VDD         |
| BYP#_HIBW_LOBW | 12 |        | 17 | SMB_ADR_tri |
| SMBCLK         | 13 |        | 16 | VDD         |
| SMBDAT         | 14 |        | 15 | GND         |

### Notes:

Highlighted Pins are the differences between 9DB403 and 9DB433.

Pin 12 and Pin 17 are latched on power up. Please make sure that the power supply to the pullup/pulldown resistors ramps at the same time as the main supply to the chip.

## SMBus Address Selection and Readback

| SMB_ADR_tri | Address |
|-------------|---------|
| Low         | DA/DB   |
| Mid         | DC/DD   |
| High        | D8/D9   |

## PLL Operating Mode Readback Table

| BYP#_LOBW_HIBW | MODE            | Byte0, bit 3 | Byte 0 bit 1 |
|----------------|-----------------|--------------|--------------|
| Low            | Bypass          | 0            | 0            |
| Mid            | PLL 100M Hi BW  | 1            | 0            |
| High           | PLL 100M Low BW | 0            | 1            |

## Power Groups

| Pin Number  |     | Description                    |
|-------------|-----|--------------------------------|
| VDD         | GND |                                |
| 1           | 4   | SRC_IN/SRC_IN#                 |
| 5,11,18, 24 | 4   | DIF(1,2,5,6)                   |
| 16          | 15  | DIGITAL VDD/GND                |
| 28          | 27  | Analog VDD/GND for PLL in IREF |

For best results, treat pin 1 as analog VDD.

## Tri-Level Input Logic Pins

| State of Pin | Voltage      |
|--------------|--------------|
| Low          | <0.8V        |
| Mid          | 1.2<Vin<1.8V |
| High         | Vin > 2.0V   |

## Pin Descriptions

| PIN # | PIN NAME       | PIN TYPE | DESCRIPTION   |
|-------|----------------|----------|---|
| 1     | VDDR           | PWR      | 3.3V power for differential input clock (receiver). This VDD should be treated as an analog power rail and filtered appropriately.  |
| 2     | SRC_IN         | IN       | 0.7 V Differential SRC TRUE input   |
| 3     | SRC_IN#        | IN       | 0.7 V Differential SRC COMPLEMENTARY input  |
| 4     | GND            | PWR      | Ground pin.   |
| 5     | VDD            | PWR      | Power supply, nominal 3.3V  |
| 6     | DIF_1          | OUT      | 0.7V differential true clock output   |
| 7     | DIF_1#         | OUT      | 0.7V differential Complementary clock output  |
| 8     | OE1#           | IN       | Active low input for enabling DIF pair 1.<br>1 =disable outputs, 0 = enable outputs   |
| 9     | DIF_2          | OUT      | 0.7V differential true clock output   |
| 10    | DIF_2#         | OUT      | 0.7V differential Complementary clock output  |
| 11    | VDD            | PWR      | Power supply, nominal 3.3V  |
| 12    | BYP#_HIBW_LOBW | IN       | Tri-level input to select bypass mode, Hi BW PLL, or Lo BW PLL mode   |
| 13    | SMBCLK         | IN       | Clock pin of SMBUS circuitry, 5V tolerant   |
| 14    | SMBDAT         | I/O      | Data pin of SMBUS circuitry, 5V tolerant  |
| 15    | GND            | PWR      | Ground pin.   |
| 16    | VDD            | PWR      | Power supply, nominal 3.3V  |
| 17    | SMB_ADR_tri    | IN       | SMBus address select bit. This is a tri-level input that decodes 1 of 3 SMBus Addresses.  |
| 18    | VDD            | PWR      | Power supply, nominal 3.3V  |
| 19    | DIF_5#         | OUT      | 0.7V differential Complementary clock output  |
| 20    | DIF_5          | OUT      | 0.7V differential true clock output   |
| 21    | OE6#           | IN       | Active low input for enabling DIF pair 6.<br>1 =disable outputs, 0 = enable outputs   |
| 22    | DIF_6#         | OUT      | 0.7V differential Complementary clock output  |
| 23    | DIF_6          | OUT      | 0.7V differential true clock output   |
| 24    | VDD            | PWR      | Power supply, nominal 3.3V  |
| 25    | PD#            | IN       | Asynchronous active low input pin used to power down the device. The internal clocks are disabled and the VCO and the crystal osc. (if any) are stopped.  |
| 26    | IREF           | OUT      | This pin establishes the reference for the differential current-mode output pairs. It requires a fixed precision resistor to ground. 475ohm is the standard value for 100ohm differential impedance. Other impedances require different values. See data sheet. |
| 27    | GND_A          | PWR      | Ground pin for the PLL core.  |
| 28    | VDD_A          | PWR      | 3.3V power for the PLL core.  |

## Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 9DB433. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| PARAMETER                 | SYMBOL             | CONDITIONS                 | MIN     | TYP | MAX                   | UNITS | NOTES |
|---------------------------|--------------------|----------------------------|---------|-----|-----------------------|-------|-------|
| 3.3V Core Supply Voltage  | VDDA/R             |                            |         |     | 4.6                   | V     | 1,2   |
| 3.3V Logic Supply Voltage | VDD                |                            |         |     | 4.6                   | V     | 1,2   |
| Input Low Voltage         | V <sub>IL</sub>    |                            | GND-0.5 |     |                       | V     | 1     |
| Input High Voltage        | V <sub>IH</sub>    | Except for SMBus interface |         |     | V <sub>DD</sub> +0.5V | V     | 1     |
| Input High Voltage        | V <sub>IHSMB</sub> | SMBus clock and data pins  |         |     | 5.5V                  | V     | 1     |
| Storage Temperature       | T <sub>s</sub>     |                            | -65     |     | 150                   | °C    | 1     |
| Junction Temperature      | T <sub>j</sub>     |                            |         |     | 125                   | °C    | 1     |
| Input ESD protection      | ESD prot           | Human Body Model           | 2000    |     |                       | V     | 1     |

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup>Operation under these conditions is neither implied nor guaranteed.

## Electrical Characteristics—DIF 0.7V Current Mode Differential Outputs

T<sub>A</sub> = T<sub>COM</sub> or T<sub>IND</sub>; Supply Voltage VDD = 3.3 V +/-5%

| PARAMETER              | SYMBOL                 | CONDITIONS  | MIN  | TYP    | MAX  | UNITS | NOTES   |
|------------------------|------------------------|---|------|--------|------|-------|---------|
| Slew rate              | Trf                    | Scope averaging on  | 1.5  | 2.8    | 4    | V/ns  | 1, 2, 3 |
| Slew rate matching     | ΔTrf                   | Slew rate matching, Scope averaging on  |      | 8      | 20   | %     | 1, 2, 4 |
| Voltage High           | V <sub>High</sub>      | Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on) | 660  | 797    | 850  | mV    | 1       |
| Voltage Low            | V <sub>Low</sub>       |   | -150 | 14     | 150  |       | 1       |
| Max Voltage            | V <sub>max</sub>       | Measurement on single ended signal using absolute value. (Scope averaging off)                        |      | 813    | 1150 | mV    | 1       |
| Min Voltage            | V <sub>min</sub>       |   | -300 | -1     |      |       | 1       |
| V <sub>swing</sub>     | V <sub>swing</sub>     | Scope averaging off (Differential)  | 300  | 1596.9 |      | mV    | 1, 2    |
| Crossing Voltage (abs) | V <sub>cross_abs</sub> | Scope averaging off   | 250  | 378    | 550  | mV    | 1, 5    |
| Crossing Voltage (var) | Δ-V <sub>cross</sub>   | Scope averaging off   |      | 16     | 140  | mV    | 1, 6    |

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production. I<sub>REF</sub> = VDD/(3xR<sub>R</sub>). For R<sub>R</sub> = 475Ω (1%), I<sub>REF</sub> = 2.32mA.

I<sub>OH</sub> = 6 x I<sub>REF</sub> and V<sub>OH</sub> = 0.7V @ Z<sub>O</sub>=50Ω (100Ω differential impedance).

<sup>2</sup> Measured from differential waveform

<sup>3</sup> Slew rate is measured through the V<sub>swing</sub> voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

<sup>4</sup> Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

<sup>5</sup> V<sub>cross</sub> is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

<sup>6</sup> The total variation of all V<sub>cross</sub> measurements in any particular system. Note that this is a subset of V<sub>cross\_min/max</sub> (V<sub>cross</sub> absolute) allowed. The intent is to limit V<sub>cross</sub> induced modulation by setting V<sub>cross\_delta</sub> to be smaller than V<sub>cross</sub> absolute.

## Electrical Characteristics–Input/Supply/Common Parameters

TA = T<sub>COM</sub> or T<sub>IND</sub>; Supply Voltage VDD = 3.3 V +/-5%

| PARAMETER                     | SYMBOL                | CONDITIONS  | MIN       | TYP   | MAX                   | UNITS  | NOTES |
|-------------------------------|-----------------------|---|-----------|-------|-----------------------|--------|-------|
| Ambient Operating Temperature | T <sub>COM</sub>      | Commercial range  | 0         |       | 70                    | °C     | 1     |
|                               | T <sub>IND</sub>      | Industrial range  | -40       |       | 85                    | °C     | 1     |
| Input High Voltage            | V <sub>IH</sub>       | Single-ended inputs, except SMBus, low threshold and tri-level inputs   | 2         |       | V <sub>DD</sub> + 0.3 | V      | 1     |
| Input Low Voltage             | V <sub>IL</sub>       | Single-ended inputs, except SMBus, low threshold and tri-level inputs   | GND - 0.3 |       | 0.8                   | V      | 1     |
| Input Current                 | I <sub>IN</sub>       | Single-ended inputs, V <sub>IN</sub> = GND, V <sub>IN</sub> = VDD   | -5        | -0.02 | 5                     | uA     | 1     |
|                               | I <sub>INP</sub>      | Single-ended inputs<br>V <sub>IN</sub> = 0 V; Inputs with internal pull-up resistors<br>V <sub>IN</sub> = VDD; Inputs with internal pull-down resistors | -50       |       | 50                    | uA     | 1     |
| Input Frequency               | F <sub>ibyp</sub>     | V <sub>DD</sub> = 3.3 V, Bypass mode  | 5         |       | 166                   | MHz    | 2     |
|                               | F <sub>ipll</sub>     | V <sub>DD</sub> = 3.3 V, 100MHz PLL mode  | 50        | 100   | 110                   | MHz    | 2     |
| Pin Inductance                | L <sub>pin</sub>      |   |           |       | 7                     | nH     | 1     |
| Capacitance                   | C <sub>IN</sub>       | Logic Inputs, except DIF_IN   | 1.5       |       | 5                     | pF     | 1     |
|                               | C <sub>INDIF_IN</sub> | DIF_IN differential clock inputs  | 1.5       |       | 2.7                   | pF     | 1,4   |
|                               | C <sub>OUT</sub>      | Output pin capacitance  |           |       | 6                     | pF     | 1     |
| Clk Stabilization             | T <sub>STAB</sub>     | From V <sub>DD</sub> Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock   |           |       | 1                     | ms     | 1,2   |
| Input SS Modulation Frequency | f <sub>MODIN</sub>    | Allowable Frequency (Triangular Modulation)   | 30        | 31.5  | 33                    | kHz    | 1     |
| OE# Latency                   | t <sub>LATOE#</sub>   | DIF start after OE# assertion<br>DIF stop after OE# deassertion   | 1         | 2     | 3                     | cycles | 1,3   |
| Tdrive_PD#                    | t <sub>DRVPD</sub>    | DIF output enable after PD# de-assertion  |           | 13    | 300                   | us     | 1,3   |
| Tfall                         | t <sub>F</sub>        | Fall time of control inputs   |           |       | 5                     | ns     | 1,2   |
| Trise                         | t <sub>R</sub>        | Rise time of control inputs   |           |       | 5                     | ns     | 1,2   |
| SMBus Input Low Voltage       | V <sub>ILSMB</sub>    |   |           |       | 0.8                   | V      | 1     |
| SMBus Input High Voltage      | V <sub>IHSMB</sub>    |   | 2.1       |       | V <sub>DD</sub> SMB   | V      | 1     |
| SMBus Output Low Voltage      | V <sub>OLSMB</sub>    | @ I <sub>PULLUP</sub>   |           |       | 0.4                   | V      | 1     |
| SMBus Sink Current            | I <sub>PULLUP</sub>   | @ V <sub>OL</sub>   | 4         |       |                       | mA     | 1     |
| Nominal Bus Voltage           | V <sub>DD</sub> SMB   | 3V to 5V +/- 10%  | 2.7       |       | 5.5                   | V      | 1     |
| SCLK/SDATA Rise Time          | t <sub>RSMB</sub>     | (Max VIL - 0.15) to (Min VIH + 0.15)  |           |       | 1000                  | ns     | 1     |
| SCLK/SDATA Fall Time          | t <sub>FSMB</sub>     | (Min VIH + 0.15) to (Max VIL - 0.15)  |           |       | 300                   | ns     | 1     |
| SMBus Operating Frequency     | f <sub>MAXSMB</sub>   | Maximum SMBus operating frequency   |           |       | 440                   | kHz    | 1,5   |

<sup>1</sup> Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup> Control input must be monotonic from 20% to 80% of input swing.

<sup>3</sup> Time from deassertion until outputs are >200 mV.

<sup>4</sup> DIF\_IN input.

<sup>5</sup> The differential input clock must be running for the SMBus to be active.

## Electrical Characteristics–DIF\_IN Clock Input Parameters

$T_{AMB}=T_{COM}$  or  $T_{IND}$  unless otherwise indicated, supply voltages per normal operation conditions; see Test Loads for Loading Conditions

| PARAMETER                        | SYMBOL      | CONDITIONS                             | MIN | TYP | MAX | UNITS | NOTES |
|----------------------------------|-------------|--|-----|-----|-----|-------|-------|
| Input Crossover Voltage - DIF_IN | $V_{CROSS}$ | Cross Over Voltage                     | 150 | 375 | 900 | mV    | 1     |
| Input Swing - DIF_IN             | $V_{SWING}$ | Differential value                     | 300 |     |     | mV    | 1     |
| Input Slew Rate - DIF_IN         | $dv/dt$     | Measured differentially                | 0.6 |     | 8   | V/ns  | 1,2   |
| Input Leakage Current            | $I_{IN}$    | $V_{IN} = V_{DD}$ , $V_{IN} = GND$     | -5  |     | 5   | uA    |       |
| Input Duty Cycle                 | $d_{tin}$   | Measurement from differential waveform | 45  |     | 55  | %     | 1     |
| Input Jitter - Cycle to Cycle    | $J_{DIFin}$ | Differential measurement               | 0   |     | 125 | ps    | 1     |

<sup>1</sup> Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup> Slew rate measured through +/-75mV window centered around differential zero.

## Electrical Characteristics–Current Consumption

$T_A = T_{COM}$  or  $T_{IND}$ ; Supply Voltage  $V_{DD} = 3.3 V \pm 5\%$

| PARAMETER                | SYMBOL         | CONDITIONS   | MIN | TYP | MAX | UNITS | NOTES |
|--------------------------|----------------|--|-----|-----|-----|-------|-------|
| Operating Supply Current | $I_{DD3.3OP}$  | All outputs active @100MHz, $C_L = \text{Full load}$ ; |     | 93  | 120 | mA    | 1     |
| Powerdown Current        | $I_{DD3.3PD}$  | All diff pairs driven                                  |     | 30  | 40  | mA    | 1     |
|                          | $I_{DD3.3PDZ}$ | All differential pairs tri-stated                      |     | 3   | 6   | mA    | 1     |

<sup>1</sup> Guaranteed by design and characterization, not 100% tested in production.

## Electrical Characteristics–Output Duty Cycle, Jitter, Skew and PLL Characteristics

$T_A = T_{COM}$  or  $T_{IND}$ ; Supply Voltage  $V_{DD} = 3.3 V \pm 5\%$

| PARAMETER              | SYMBOL        | CONDITIONS                                   | MIN  | TYP  | MAX   | UNITS | NOTES |
|------------------------|---------------|--|------|------|-------|-------|-------|
| PLL Bandwidth          | BW            | -3dB point in High BW Mode ( $T_{IND}$ )     | 1.5  | 2.8  | 4.1   | MHz   | 1     |
|                        |               | -3dB point in High BW Mode ( $T_{COM}$ )     | 2    | 2.8  | 4     | MHz   | 1     |
|                        |               | -3dB point in Low BW Mode                    | 0.7  | 1.1  | 1.4   | MHz   | 1     |
| PLL Jitter Peaking     | $t_{JPEAK}$   | Peak Pass band Gain                          |      | 1.5  | 2     | dB    | 1     |
| Duty Cycle             | $t_{DC}$      | Measured differentially, PLL Mode            | 45   | 49.2 | 55    | %     | 1     |
| Duty Cycle Distortion  | $t_{DCD}$     | Measured differentially, Bypass Mode @100MHz | -2   | -0.4 | 2     | %     | 1,4   |
| Skew, Input to Output  | $t_{pdBYP}$   | Bypass Mode, $V_T = 50\%$ ( $T_{IND}$ )      | 3500 | 4263 | 4900  | ps    | 1     |
|                        |               | Bypass Mode, $V_T = 50\%$ ( $T_{COM}$ )      | 3500 | 4115 | 4500  | ps    | 1,5   |
|                        | $t_{pdPLL}$   | PLL Mode $V_T = 50\%$                        | -250 | -45  | 250   | ps    | 1     |
| Skew, Output to Output | $t_{sk3}$     | $V_T = 50\%$                                 |      | 40.0 | 50/60 | ps    | 1,5   |
| Jitter, Cycle to cycle | $t_{jyc-cyc}$ | PLL mode                                     |      | 21   | 50    | ps    | 1,3   |
|                        |               | Additive Jitter in Bypass Mode               |      | 3    | 10    | ps    | 1,3   |

<sup>1</sup> Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup>  $I_{REF} = V_{DD}/(3 \times R_R)$ . For  $R_R = 475\Omega$  (1%),  $I_{REF} = 2.32\text{mA}$ .  $I_{OH} = 6 \times I_{REF}$  and  $V_{OH} = 0.7V$  @  $Z_O=50\Omega$ .

<sup>3</sup> Measured from differential waveform

<sup>4</sup> Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in bypass mode.

<sup>5</sup> First number is commercial temp, second number is industrial temp.

## Electrical Characteristics–PCIe Phase Jitter Parameters

TA = T<sub>COM</sub> or T<sub>IND</sub>; Supply Voltage VDD = 3.3 V +/-5%

| PARAMETER                             | SYMBOL                 | CONDITIONS   | MIN | TYP  | MAX | INDUSTRY LIMIT | UNITS    | Notes    |
|---------------------------------------|------------------------|--|-----|------|-----|----------------|----------|----------|
| Phase Jitter, PLL Mode                | t <sub>jphPCIeG1</sub> | PCIe Gen 1   |     | 26   | 40  | 86             | ps (p-p) | 1,2,3    |
|                                       | t <sub>jphPCIeG2</sub> | PCIe Gen 2 Lo Band<br>10kHz < f < 1.5MHz             |     | 0.8  | 1.2 | 3              | ps (rms) | 1,2      |
|                                       |                        | PCIe Gen 2 High Band<br>1.5MHz < f < Nyquist (50MHz) |     | 1.6  | 1.8 | 3.1            | ps (rms) | 1,2      |
|                                       | t <sub>jphPCIeG3</sub> | PCIe Gen 3<br>(PLL BW of 2-4MHz, CDR = 10MHz)        |     | 0.48 | 0.6 | 1              | ps (rms) | 1,2,4    |
| Additive Phase Jitter,<br>Bypass Mode | t <sub>jphPCIeG1</sub> | PCIe Gen 1   |     | 2.6  | 5   | N/A            | ps (p-p) | 1,2,3    |
|                                       | t <sub>jphPCIeG2</sub> | PCIe Gen 2 Lo Band<br>10kHz < f < 1.5MHz             |     | 0.06 | 0.2 | N/A            | ps (rms) | 1,2      |
|                                       |                        | PCIe Gen 2 High Band<br>1.5MHz < f < Nyquist (50MHz) |     |      |     | 0.3            | N/A      | ps (rms) |
|                                       | t <sub>jphPCIeG3</sub> | PCIe Gen 3<br>(PLL BW of 2-4MHz, CDR = 10MHz)        |     |      | 0.1 | N/A            | ps (rms) | 1,2      |

<sup>1</sup> Applies to all outputs.

<sup>2</sup> See <http://www.pcisig.com> for complete specs

<sup>3</sup> Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.

## Clock Periods–Differential Outputs Tracking Spread Spectrum

| Measurement Window | 1 Clock                 | 1us                     | 0.1s                    | 0.1s    | 0.1s              | 1us                | 1 Clock |       |       |
|--------------------|-------------------------|-------------------------|-------------------------|---------|-------------------|--------------------|---------|-------|-------|
| Symbol             | Lg-                     | -SSC                    | -ppm error              | 0ppm    | + ppm error       | +SSC               | Lg+     |       |       |
| Definition         | Absolute Period         | Short-term Average      | Long-Term Average       | Period  | Long-Term Average | Short-term Average | Period  |       |       |
|                    | Minimum Absolute Period | Minimum Absolute Period | Minimum Absolute Period | Nominal | Maximum           | Maximum            | Maximum | Units | Notes |
| <b>DIF 100</b>     | 9.949                   | 9.999                   | 10.024                  | 10.025  | 10.026            | 10.051             | 10.101  | ns    | 1,2,3 |

| Output Termination and Layout Information       |                    |      |        |
|---|--------------------|------|--------|
| Common Recommendations for Differential Routing | Dimension or Value | Unit | Figure |
| L1 length, route as non-coupled 50ohm trace     | 0.5 max            | inch | 1      |
| L2 length, route as non-coupled 50ohm trace     | 0.2 max            | inch | 1      |
| L3 length, route as non-coupled 50ohm trace     | 0.2 max            | inch | 1      |
| $R_s$   | 33                 | ohm  | 1      |
| $R_t$   | 49.9               | ohm  | 1      |

| Down Device Differential Routing                                 |                     |      |   |
|--|---------------------|------|---|
| L4 length, route as coupled microstrip 100ohm differential trace | 2 min to 16 max     | inch | 1 |
| L4 length, route as coupled stripline 100ohm differential trace  | 1.8 min to 14.4 max | inch | 1 |

| Differential Routing to PCI Express Connector                    |                       |      |   |
|--|-----------------------|------|---|
| L4 length, route as coupled microstrip 100ohm differential trace | 0.25 to 14 max        | inch | 2 |
| L4 length, route as coupled stripline 100ohm differential trace  | 0.225 min to 12.6 max | inch | 2 |

Figure 1: Down Device Routing

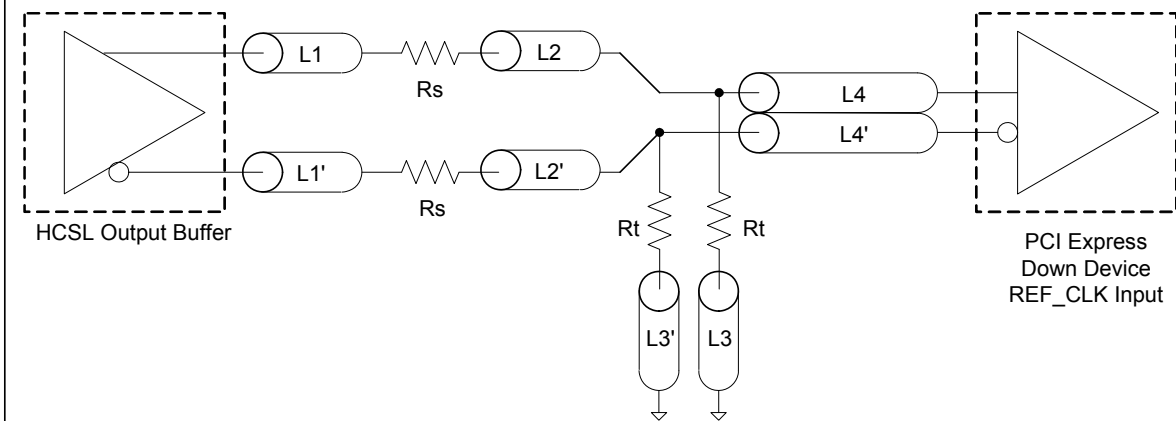
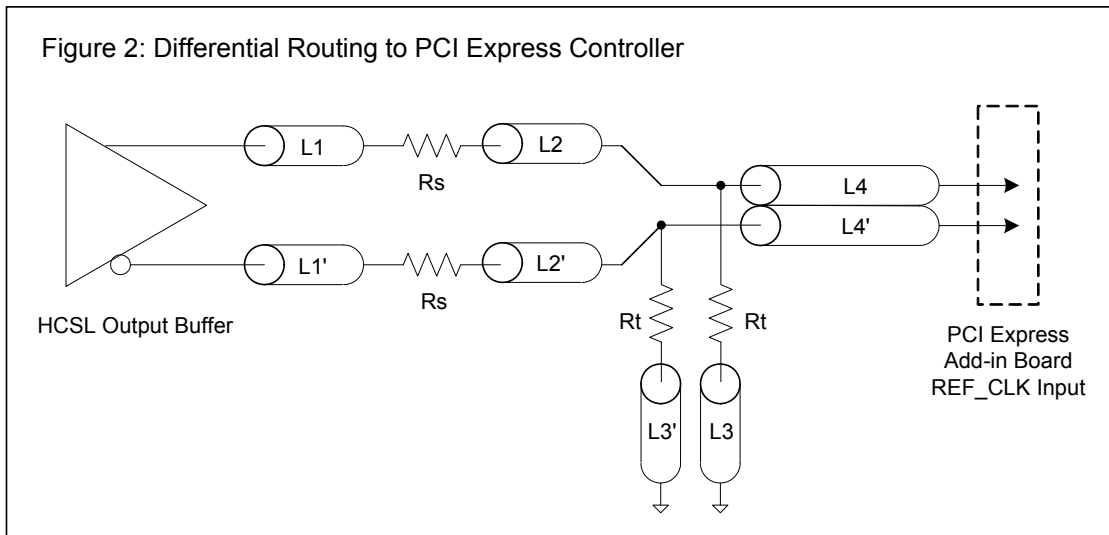


Figure 2: Differential Routing to PCI Express Controller





| Termination for LVDS and other Common Differential Signals (figure 3) |                  |                 |    |      |      |     |                                |
|---|------------------|-----------------|----|------|------|-----|--------------------------------|
| V <sub>diff</sub>   | V <sub>p-p</sub> | V <sub>cm</sub> | R1 | R2   | R3   | R4  | Note                           |
| 0.45v   | 0.22v            | 1.08            | 33 | 150  | 100  | 100 |                                |
| 0.58  | 0.28             | 0.6             | 33 | 78.7 | 137  | 100 |                                |
| 0.80  | 0.40             | 0.6             | 33 | 78.7 | none | 100 | ICS874003i-02 input compatible |
| 0.60  | 0.3              | 1.2             | 33 | 174  | 140  | 100 | Standard LVDS                  |

R1a = R1b = R1

R2a = R2b = R2



| Termination for Cable AC Coupled Application (figure 4) |             |      |
|---|-------------|------|
| Component   | Value       | Note |
| R5a, R5b  | 8.2K 5%     |      |
| R6a, R6b  | 1K 5%       |      |
| Cc  | 0.1 $\mu$ F |      |
| V <sub>cm</sub>   | 0.350 volts |      |



## General SMBus Serial Interface Information for 9DB433

### How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending Byte N through Byte N+X-1
- IDT clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

| Index Block Write Operation |           |        |                      |
|-----------------------------|-----------|--------|----------------------|
| Controller (Host)           |           |        | IDT (Slave/Receiver) |
| T                           | starT bit |        |                      |
| Slave Address               |           |        |                      |
| WR                          | WRite     |        |                      |
|                             |           |        | ACK                  |
| Beginning Byte = N          |           |        |                      |
|                             |           |        | ACK                  |
| Data Byte Count = X         |           |        |                      |
|                             |           |        | ACK                  |
| Beginning Byte N            |           | X Byte |                      |
|                             |           |        | ACK                  |
| O                           |           |        | O                    |
| O                           |           |        | O                    |
| Byte N + X - 1              |           |        | O                    |
|                             |           |        | ACK                  |
| P                           | stoP bit  |        |                      |

| Read Address       | Write Address      |
|--------------------|--------------------|
| DD* <sub>(H)</sub> | DC* <sub>(H)</sub> |

\* Assuming SMB\_ADR\_tri is at mid-level

### How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends Byte N+X-1
- IDT clock sends **Byte 0 through Byte X (if X<sub>(H)</sub> was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Index Block Read Operation |                 |        |                      |
|----------------------------|-----------------|--------|----------------------|
| Controller (Host)          |                 |        | IDT (Slave/Receiver) |
| T                          | starT bit       |        |                      |
| Slave Address              |                 |        |                      |
| WR                         | WRite           |        |                      |
|                            |                 |        | ACK                  |
| Beginning Byte = N         |                 |        |                      |
|                            |                 |        | ACK                  |
| RT                         | Repeat starT    |        |                      |
| Slave Address              |                 |        |                      |
| RD                         | ReaD            |        |                      |
|                            |                 |        | ACK                  |
|                            |                 |        |                      |
| ACK                        |                 |        | Data Byte Count=X    |
|                            |                 |        |                      |
| ACK                        |                 | X Byte | Beginning Byte N     |
| O                          |                 |        | O                    |
| O                          |                 |        | O                    |
| O                          |                 |        | O                    |
|                            |                 |        |                      |
|                            |                 |        | Byte N + X - 1       |
| N                          | Not acknowledge |        |                      |
| P                          | stoP bit        |        |                      |

SMBus Table: Frequency Select Register, READ/WRITE ADDRESS (Selectable)

| Byte 0 | Pin # | Name     | Control Function       | Type | 0                                 | 1    | Default |
|--------|-------|----------|------------------------|------|-----------------------------------|------|---------|
| Bit 7  | -     | PD_Mode  | PD# drive mode         | RW   | driven                            | Hi-Z | 1       |
| Bit 6  | -     | OE_Mode  | OE#_Stop drive mode    | RW   | driven                            | Hi-Z | 0       |
| Bit 5  | -     |          | Reserved               |      |                                   |      | 0       |
| Bit 4  | -     |          | Reserved               |      |                                   |      | X       |
| Bit 3  | -     | MODE1    | BYPASS#/PLL1           | RW   | See Operating Mode Readback Table |      | Latched |
| Bit 2  | -     |          | Reserved               |      |                                   |      | 1       |
| Bit 1  | -     | MODE0    | BYPASS#/PLL0           | RW   | See Operating Mode Readback Table |      | Latched |
| Bit 0  | -     | SRC_DIV# | SRC Divide by 2 Select | RW   | x/2                               | x/1  | 1       |

SMBus Table: Output Control Register

| Byte 1 | Pin # | Name  | Control Function | Type | 0       | 1      | Default |
|--------|-------|-------|------------------|------|---------|--------|---------|
| Bit 7  |       |       | Reserved         |      |         |        | 1       |
| Bit 6  | 22,23 | DIF_6 | Output Enable    | RW   | Disable | Enable | 1       |
| Bit 5  | 19,20 | DIF_5 | Output Enable    | RW   | Disable | Enable | 1       |
| Bit 4  |       |       | Reserved         |      |         |        | 1       |
| Bit 3  |       |       | Reserved         |      |         |        | 1       |
| Bit 2  | 9,10  | DIF_2 | Output Enable    | RW   | Disable | Enable | 1       |
| Bit 1  | 6,7   | DIF_1 | Output Enable    | RW   | Disable | Enable | 1       |
| Bit 0  |       |       | Reserved         |      |         |        | 1       |

NOTE: The SMBus Output Enable Bit must be '1' AND the respective OE pin must be active for the output to run!

SMBus Table: OE Pin Control Register

| Byte 2 | Pin # | Name  | Control Function          | Type | 0        | 1         | Default |
|--------|-------|-------|---------------------------|------|----------|-----------|---------|
| Bit 7  |       |       | Reserved                  |      |          |           | 0       |
| Bit 6  | 22,23 | DIF_6 | DIF_6 Stoppable with OE6# | RW   | Free-run | Stoppable | 0       |
| Bit 5  | 19,20 | DIF_5 | DIF_5 Stoppable with OE5# | RW   | Free-run | Stoppable | 0       |
| Bit 4  |       |       | Reserved                  |      |          |           | 0       |
| Bit 3  |       |       | Reserved                  |      |          |           | 0       |
| Bit 2  | 9,10  | DIF_2 | DIF_2 Stoppable with OE2# | RW   | Free-run | Stoppable | 0       |
| Bit 1  | 6,7   | DIF_1 | DIF_1 Stoppable with OE1# | RW   | Free-run | Stoppable | 0       |
| Bit 0  |       |       | Reserved                  |      |          |           | 0       |

NOTE: Only OE1# and OE6# are available on 28-TSSOP/SSOP packages. If you wish the default to be "Stoppable" see the 9DB434.

SMBus Table: Reserved Register

| Byte 3 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|------------------|------|---|---|---------|
| Bit 7  |       |      | Reserved         |      |   |   | X       |
| Bit 6  |       |      | Reserved         |      |   |   | X       |
| Bit 5  |       |      | Reserved         |      |   |   | X       |
| Bit 4  |       |      | Reserved         |      |   |   | X       |
| Bit 3  |       |      | Reserved         |      |   |   | X       |
| Bit 2  |       |      | Reserved         |      |   |   | X       |
| Bit 1  |       |      | Reserved         |      |   |   | X       |
| Bit 0  |       |      | Reserved         |      |   |   | X       |

SMBus Table: Vendor &amp; Revision ID Register

| Byte 4 | Pin # | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------|------|------------------|------|---|---|---------|
| Bit 7  | -     | RID3 | REVISION ID      | R    | - | - | 0       |
| Bit 6  | -     | RID2 |                  | R    | - | - | 0       |
| Bit 5  | -     | RID1 |                  | R    | - | - | 0       |
| Bit 4  | -     | RID0 |                  | R    | - | - | 1       |
| Bit 3  | -     | VID3 | VENDOR ID        | R    | - | - | 0       |
| Bit 2  | -     | VID2 |                  | R    | - | - | 0       |
| Bit 1  | -     | VID1 |                  | R    | - | - | 0       |
| Bit 0  | -     | VID0 |                  | R    | - | - | 1       |

SMBus Table: DEVICE ID

| Byte 5 | Pin # | Name | Control Function  | Type | 0                                 | 1 | Default |
|--------|-------|------|-------------------|------|-----------------------------------|---|---------|
| Bit 7  | -     | DID7 | Device ID 7 (MSB) | R    | Device ID is 43 Hex for<br>9DB433 |   | 0       |
| Bit 6  | -     | DID6 | Device ID 6       | R    |                                   |   | 1       |
| Bit 5  | -     | DID5 | Device ID 5       | R    |                                   |   | 0       |
| Bit 4  | -     | DID4 | Device ID 4       | R    |                                   |   | 0       |
| Bit 3  | -     | DID3 | Device ID 3       | R    |                                   |   | 0       |
| Bit 2  | -     | DID2 | Device ID 2       | R    |                                   |   | 0       |
| Bit 1  | -     | DID1 | Device ID 1       | R    |                                   |   | 1       |
| Bit 0  | -     | DID0 | Device ID 0       | R    |                                   |   | 1       |

SMBus Table: Byte Count Register

| Byte 6 | Pin # | Name | Control Function   | Type | 0 | 1 | Default |
|--------|-------|------|--|------|---|---|---------|
| Bit 7  | -     | BC7  | Writing to this register configures how<br>many bytes will be read back. | RW   | - | - | 0       |
| Bit 6  | -     | BC6  |  | RW   | - | - | 0       |
| Bit 5  | -     | BC5  |  | RW   | - | - | 0       |
| Bit 4  | -     | BC4  |  | RW   | - | - | 0       |
| Bit 3  | -     | BC3  |  | RW   | - | - | 0       |
| Bit 2  | -     | BC2  |  | RW   | - | - | 1       |
| Bit 1  | -     | BC1  |  | RW   | - | - | 1       |
| Bit 0  | -     | BC0  |  | RW   | - | - | 1       |

### PD#, Power Down

The PD# pin cleanly shuts off all clocks and places the device into a power saving mode. PD# must be asserted before shutting off the input clock or power to insure an orderly shutdown. PD is asynchronous active-low input for both powering down the device and powering up the device. When PD# is asserted, all clocks will be driven high, or tri-stated (depending on the PD# drive mode and Output control bits) before the PLL is shut down.

### PD# Assertion

When PD# is sampled low by two consecutive rising edges of DIF#, all DIF outputs must be held High, or tri-stated (depending on the PD# drive mode and Output control bits) on the next High-Low transition of the DIF# outputs. When the PD# drive mode bit is set to '0', all clock outputs will be held with DIF driven High with 2 x IREF and DIF# tri-stated. If the PD# drive mode bit is set to '1', both DIF and DIF# are tri-stated.



### PD# De-assertion

Power-up latency is less than 1 ms. This is the time from de-assertion of the PD# pin, or VDD reaching 3.3V, or the time from valid SRC\_IN clocks until the time that stable clocks are output from the device (PLL Locked). If the PD# drive mode bit is set to '1', all the DIF outputs must be driven to a voltage of >200mV within 300μs of PD# de-assertion.



### Package Outline Drawings (28-pin SSOP)



209 mil SSOP

| SYMBOL   | In Millimeters    |                   | In Inches         |                   |
|----------|-------------------|-------------------|-------------------|-------------------|
|          | COMMON DIMENSIONS | COMMON DIMENSIONS | COMMON DIMENSIONS | COMMON DIMENSIONS |
| A        | --                | 2.00              | --                | .079              |
| A1       | 0.05              | --                | .002              | --                |
| A2       | 1.65              | 1.85              | .065              | .073              |
| b        | 0.22              | 0.38              | .009              | .015              |
| c        | 0.09              | 0.25              | .0035             | .010              |
| D        | SEE VARIATIONS    |                   | SEE VARIATIONS    |                   |
| E        | 7.40              | 8.20              | .291              | .323              |
| E1       | 5.00              | 5.60              | .197              | .220              |
| e        | 0.65 BASIC        |                   | 0.0256 BASIC      |                   |
| L        | 0.55              | 0.95              | .022              | .037              |
| N        | SEE VARIATIONS    |                   | SEE VARIATIONS    |                   |
| $\alpha$ | 0°                | 8°                | 0°                | 8°                |

VARIATIONS

| N  | D mm. |       | D (inch) |      |
|----|-------|-------|----------|------|
|    | MIN   | MAX   | MIN      | MAX  |
| 28 | 9.90  | 10.50 | .390     | .413 |

Reference Doc.: JEDEC Publication 95, MO-150



## Package Outline Drawings (28-pin TSSOP)



## Ordering Information

| Part / Order Number | Shipping Packaging | Package      | Temperature  |
|---------------------|--------------------|--------------|--------------|
| 9DB433AFLF          | Tubes              | 28-pin SSOP  | 0 to +70°C   |
| 9DB433AFLFT         | Tape and Reel      | 28-pin SSOP  | 0 to +70°C   |
| 9DB433AGLF          | Tubes              | 28-pin TSSOP | 0 to +70°C   |
| 9DB433AGLFT         | Tape and Reel      | 28-pin TSSOP | 0 to +70°C   |
| 9DB433AFILF         | Tubes              | 28-pin SSOP  | -40 to +85°C |
| 9DB433AFILFT        | Tape and Reel      | 28-pin SSOP  | -40 to +85°C |
| 9DB433AGILF         | Tubes              | 28-pin TSSOP | -40 to +85°C |
| 9DB433AGILFT        | Tape and Reel      | 28-pin TSSOP | -40 to +85°C |

“LF” suffix to the part number denotes Pb-Free configuration, RoHS compliant.

“A” is the device revision designator (will not correlate with the datasheet revision).

## Revision History

| Issue Date | Description  | Page #  |
|------------|--|---------|
| 6/30/2010  | Released to final  |         |
| 5/9/2011   | 1. Update pin 1 pin-name and pin description from VDD to VDDR. This highlights that optimal performance is obtained by treating VDDR as in analog pin. This is a document update only, there is no silicon change.   | Various |
| 3/13/2012  | 1. Added additional line to PLL Bandwidth "-3dB point in High BW Mode" conditions for industrial mode (min1.5, typ 2.7, max 4.1 MHz)<br>2. Added additional line to Skew, Input to Output "Bypass Mode" conditions for industrial mode (min 2500, max 4900 ps) | 6       |
| 7/5/2012   | 1. Changed references of PCIe Gen3 to PCIe Gen1,2,3  | 1       |
| 7/12/2012  | 1. Added missing typical values to DS.   | Various |
| 9/18/2012  | Updated Byte 2, bits 1, 2, 5 and 6 per char review. Outputs can be programmed with Byte 2 to be Stoppable or Free-Run with DIF_Stop pin, not the OE pins.  | Various |
| 9/30/2013  | Corrected typo in ordering information for 28-SSOP I-temp device.  | 15      |
| 8/14/2015  | 1. Corrected default value of Byte 2 to 00hex. Added note referring to 9DB434 if FFhex is the desired default.   | 11      |
| 6/7/2016   | 1. Corrected Idd values for 9DB433.<br>2. Updated typical values in electrical tables.<br>3. Updated clock input electrical table to latest format.<br>4. Updated SMBus operating frequency to 440KHz.<br>5. Corrected typo in Byte 0, bit 6 defaults to 0.    | Various |
| 5/25/2018  | 1. Updated the minimum input slew rate from 1 V/ns to 0.6V/ns.   | 6       |



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