

200 mA LOAD SWITCH FEATURING PRE-BIASED PNP TRANSISTOR AND N-MOSFET WITH PULL DOWN RESISTOR

General Description

- LMN200B01 is best suited for applications where the load needs to be turned on and off using control circuits like micro-controllers, comparators, etc., particularly at a point of load. It features a discrete pass transistor with stable $V_{CE(SAT)}$ which does not depend on the input voltage and can support continuous maximum current of 200 mA. It also contains a discrete N-MOSFET that can be used as control. This N-MOSFET also has a built-in pull down resistor at its gate. The component can be used as a part of a circuit or as a stand alone discrete device.

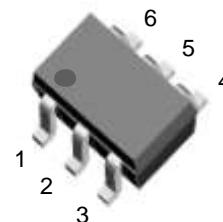


Fig. 1: SOT-26

Features

- Voltage Controlled Small Signal Switch
- N-MOSFET with Gate Pull-Down Resistor
- Surface Mount Package
- Ideally Suited for Automated Assembly Processes
- Lead Free By Design/ROHS Compliant (Note 1)**
- "Green" Device (Note 2)

Mechanical Data

- Case: SOT-26
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture sensitivity: Level 1 per J-STD-020C
- Terminal Connections: See Diagram
- Terminals: Finish - Matte Tin annealed over Copper leadframe. Solderable per MIL-STD-202, Method 208
- Marking & Type Code Information: See Last Page
- Ordering Information: See Last Page
- Weight: 0.016 grams (approximate)

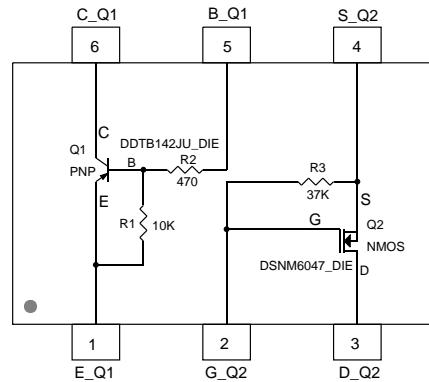


Fig. 2 Schematic and Pin Configuration

Sub-Components	Reference	Device Type	R1 (NOM)	R2 (NOM)	R3 (NOM)	Figure
DDTB142JU_DIE	Q1	PNP Transistor	10K	470		2
DSNM6047_DIE	Q2	N-MOSFET			37K	2

Maximum Ratings, Total Device @ $T_A = 25^\circ\text{C}$ unless otherwise specified

Characteristic	Symbol	Value	Unit
Power Dissipation (Note 3)	P_d	300	mW
Power Derating Factor above 125°C	P_{der}	2.4	$\text{mW}/^\circ\text{C}$
Output Current	I_{out}	200	mA

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Junction Operation and Storage Temperature Range	T_j, T_{stg}	-55 to +150	°C
Thermal Resistance, Junction to Ambient Air (Note 3) (Equivalent to one heated junction of PNP transistor)	R_{JA}	417	°C/W

- Notes:
1. No purposefully added lead.
 2. Diodes Inc.'s "Green" policy can be found on our website at http://www.diodes.com/products/lead_free/index.php.
 3. Device mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inch; pad layout as shown on Diodes Inc. suggested pad layout document AP02001, which can be found on our website at <http://www.diodes.com/datasheets/ap02001.pdf>.

Maximum Ratings:
Sub-Component Device: Pre-Biased PNP Transistor (Q1)

 @ $T_A = 25^\circ\text{C}$ unless otherwise specified

Characteristic	Symbol	Value	Unit
Collector-Base Voltage	V_{CBO}	-50	V
Collector-Emitter Voltage	V_{CEO}	-50	V
Supply Voltage	V_{cc}	-50	V
Input Voltage	V_{in}	+5 to -6	V
Output Current	I_C	-200	mA

Sub-Component Device:
N-MOSFET with Gate Pull-Down Resistor (Q2)

 @ $T_A = 25^\circ\text{C}$ unless otherwise specified

Characteristic	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	60	V
Drain Gate Voltage ($R_{GS} = 1\text{M}\Omega$)	V_{DGR}	60	V
Gate-Source Voltage	V_{GSS}	+/-20	V
Pulsed ($t_p < 50\text{ }\mu\text{s}$)		+/-40	
Drain Current (Page 1: Note 3)	I_D	115	mA
Pulsed ($t_p < 10\text{ }\mu\text{s}$, Duty Cycle <1%)		800	
Continuous Source Current	I_S	115	mA

Electrical Characteristics: Pre-Biased PNP Transistor (Q1) @ $T_A = 25^\circ\text{C}$ unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS						
Collector-Base Cut Off Current	I_{CBO}			-100	nA	$V_{CB} = -50\text{V}$, $I_E = 0$
Collector-Emitter Cut Off Current	I_{CEO}			-500	nA	$V_{CE} = -50\text{V}$, $I_B = 0$
Emitter-Base Cut Off Current	I_{EBO}		-0.5	-1	mA	$V_{EB} = -5\text{V}$, $I_C = 0$
Emitter-Base Cut Off Current	$V_{(BR)CBO}$	-50			V	$I_C = -10\mu\text{A}$, $I_E = 0$
Collector-Base Breakdown Voltage	$V_{(BR)CEO}$	-50			V	$I_C = -2 \text{ mA}$, $I_B = 0$
Collector-Emitter Breakdown Voltage	$V_{I(OFF)}$		-0.55	-0.3	V	$V_{CE} = -5\text{V}$, $I_C = -100\mu\text{A}$
Output Voltage	V_{OH}	-4.9			V	$V_{CC} = -5\text{V}$, $V_B = -0.05\text{V}$, $R_L = 1\text{K}$
Output Current (leakage current same as I_{CEO})	$I_{O(OFF)}$			-500	nA	$V_{CC} = -50\text{V}$, $V_I = 0\text{V}$
ON CHARACTERISTICS						
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$			-0.15	V	$I_C = -10 \text{ mA}$, $I_B = -0.5 \text{ mA}$
				-0.2	V	$I_C = -50\text{mA}$, $I_B = -5\text{mA}$
				-0.2	V	$I_C = -20\text{mA}$, $I_B = -1\text{mA}$
				-0.25	V	$I_C = -100\text{mA}$, $I_B = -10\text{mA}$
				-0.25	V	$I_C = -200\text{mA}$, $I_B = -10\text{mA}$
				-0.3	V	$I_C = -200\text{mA}$, $I_B = -20\text{mA}$
Equivalent on-resistance*	$R_{CE(SAT)}$			1.5		$I_C = -200\text{mA}$, $I_B = -10\text{mA}$
DC Current Gain	h_{FE}	60	150			$V_{CE} = -5\text{V}$, $I_C = -20 \text{ mA}$
		60	215			$V_{CE} = -5\text{V}$, $I_C = -50 \text{ mA}$
		60	245			$V_{CE} = -5\text{V}$, $I_C = -100 \text{ mA}$
		60	250			$V_{CE} = -5\text{V}$, $I_C = -200 \text{ mA}$
Input On Voltage	$V_{I(ON)}$	-2.45	-0.7		V	$V_O = -0.3\text{V}$, $I_C = -2 \text{ mA}$
Output Voltage (equivalent to $V_{CE(SAT)}$ or $V_{O(on)}$)	V_{OL}		-0.065	-0.15	V	$V_{CC} = -5\text{V}$, $V_B = -2.5\text{V}$, $I_o/I_i = -50\text{mA} / -2.5\text{mA}$
Input Current	I_i		-9.2	-13	mA	$V_I = -5\text{V}$
Base-Emitter Turn-on Voltage	$V_{BE(ON)}$		-1.125	-1.3	V	$V_{CE} = -5\text{V}$, $I_C = -200\text{mA}$
Base-Emitter Saturation Voltage	$V_{BE(SAT)}$		-3.2	-3.6	V	$I_C = -50\text{mA}$, $I_B = -5\text{mA}$
			-4.55	-5.5		$I_C = -80\text{mA}$, $I_B = -8\text{mA}$
Input Resistor (Base), +/- 30%	R2		0.47		K	
Pull-up Resistor (Base to Vcc supply), +/- 30%	R1		10		K	
Resistor Ratio (Input Resistor/Pullup resistor), +/- 20%	R1/R2		21			
SMALL SIGNAL CHARACTERISTICS						
Transition Frequency (gain bandwidth product)	f_T		200		MHz	$V_{CE} = -10\text{V}$, $I_E = -5\text{mA}$, $f = 100\text{MHz}$
Collector capacitance, (Ccbo-Output Capacitance)	C_C		20		pF	$V_{CB} = -10\text{V}$, $I_E = 0\text{A}$, $f = 1\text{MHz}$

 * Pulse Test: Pulse width, $t_p < 300 \mu\text{s}$, Duty Cycle, $d \leq 0.02$.

Electrical Characteristics:**N-MOSFET with Gate Pull-Down Resistor (Q2)** @ $T_A = 25^\circ\text{C}$ unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 4)						
Drain-Source Breakdown Voltage, $BVDSS$	$V_{(\text{BR})\text{DSS}}$	60			V	$V_{GS} = 0\text{V}, I_D = 10\mu\text{A}$
Zero Gate Voltage Drain Current (Drain Leakage Current)	I_{DSS}			1	μA	$V_{GS} = 0\text{V}, V_{DS} = 60\text{V}$
Gate-Body Leakage Current, Forward	I_{GSSF}			0.95	mA	$V_{GS} = 20\text{V}, V_{DS} = 0\text{V}$
Gate-Body Leakage Current, Reverse	I_{GSSR}			-0.95	mA	$V_{GS} = -20\text{V}, V_{DS} = 0\text{V}$
ON CHARACTERISTICS (Note 4)						
Gate Source Threshold Voltage (Control Supply Voltage)	$V_{GS(\text{th})}$	1	1.86	2.2	V	$V_{DS} = V_{GS}, I_D = 0.25\text{mA}$
Static Drain-Source On-State Voltage	$V_{DS(\text{on})}$		0.08	1.5	V	$V_{GS} = 5\text{V}, I_D = 50\text{mA}$
			0.15	3.75		$V_{GS} = 10\text{V}, I_D = 115\text{mA}$
On-State Drain Current	$I_{D(\text{on})}$	500			mA	$V_{GS} = 10\text{V}, V_{DS} = 2 V_{DS(\text{ON})}$
Static Drain-Source On Resistance	$R_{DS(\text{on})}$		1.55	3		$V_{GS} = 5\text{V}, I_D = 50\text{mA}$
			1.4	2		$V_{GS} = 10\text{V}, I_D = 500\text{mA}$
Forward Transconductance	g_{FS}	80	240		mS	$V_{DS} = 2 V_{DS(\text{ON})}, I_D = 115\text{ mA}$
		80	350			$V_{DS} = 2 V_{DS(\text{ON})}, I_D = 200\text{ mA}$
Gate Pull-Down Resistor, +/- 30%	R_3		37		K	
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{iss}			50	pF	$V_{DS} = -25\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$
Output Capacitance	C_{oss}			25	pF	
Reverse Transfer Capacitance	C_{rss}			5	pF	
SWITCHING CHARACTERISTICS*						
Turn-On Delay Time	$t_{d(on)}$			20	ns	$V_{DD} = 30\text{V}, V_{GS} = 10\text{V}, I_D = 200\text{mA}, R_G = 25 \Omega, R_L = 150 \Omega$
Turn-Off Delay Time	$t_{d(off)}$			40	ns	
SOURCE-DRAIN (BODY) DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
Drain-Source Diode Forward On-Voltage	V_{SD}		0.88	1.5	V	$V_{GS} = 0\text{V}, I_S = 115\text{ mA}^*$
Maximum Continuous Drain-Source Diode Forward Current (Reverse Drain Current)	I_S			115	mA	
Maximum Pulsed Drain-Source Diode Forward Current	I_{SM}			800	mA	

* Pulse Test: Pulse width, $tp < 300 \mu\text{s}$, Duty Cycle, $d \leq 0.02$.

Notes: 4. Short duration test pulse used to minimize self-heating effect.

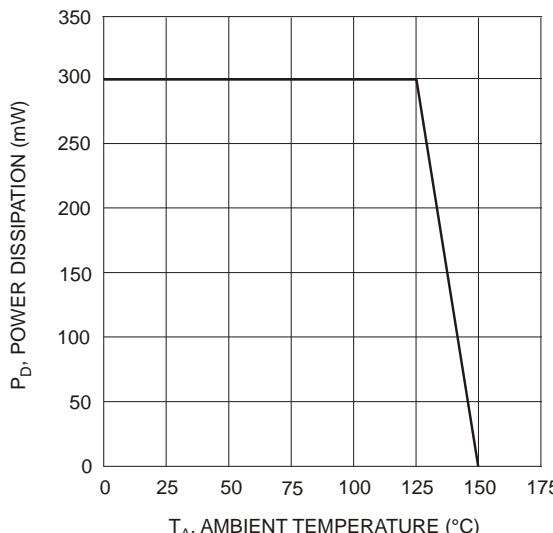
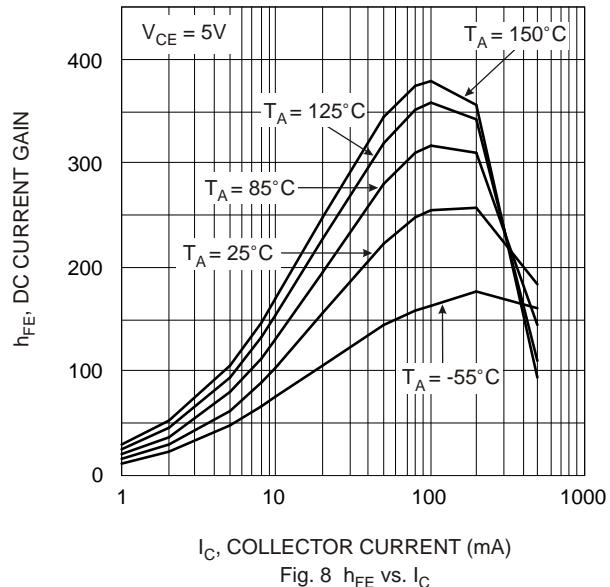
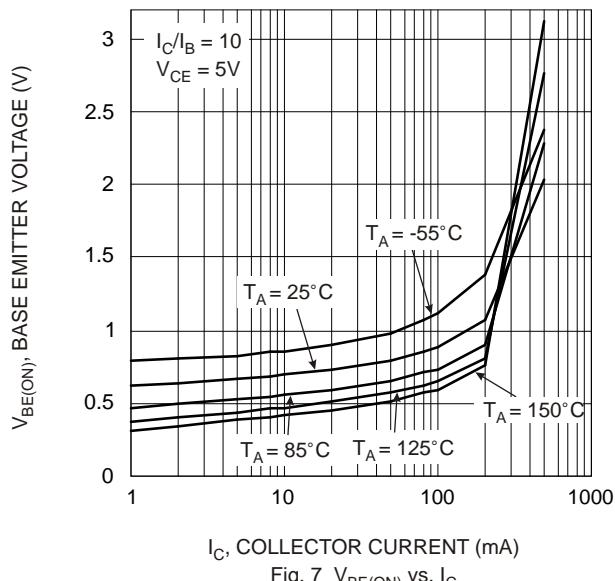
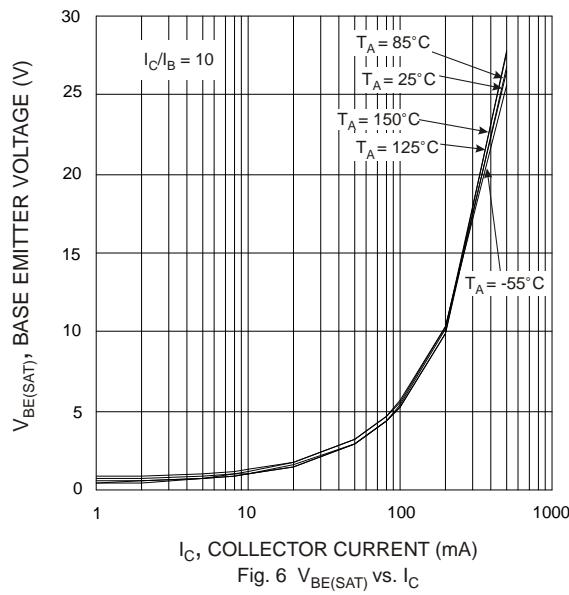
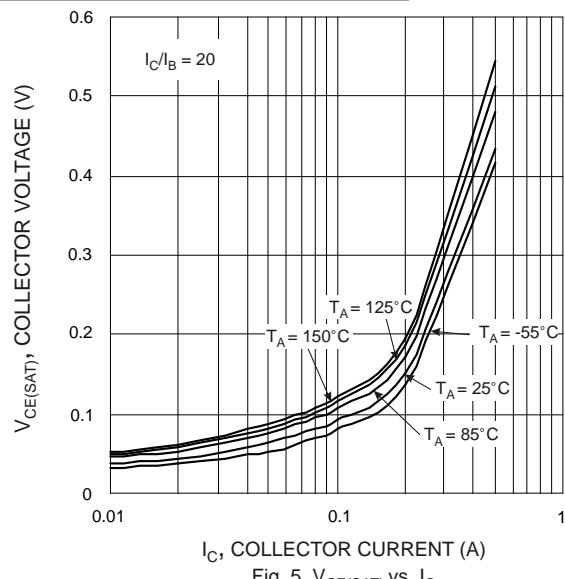
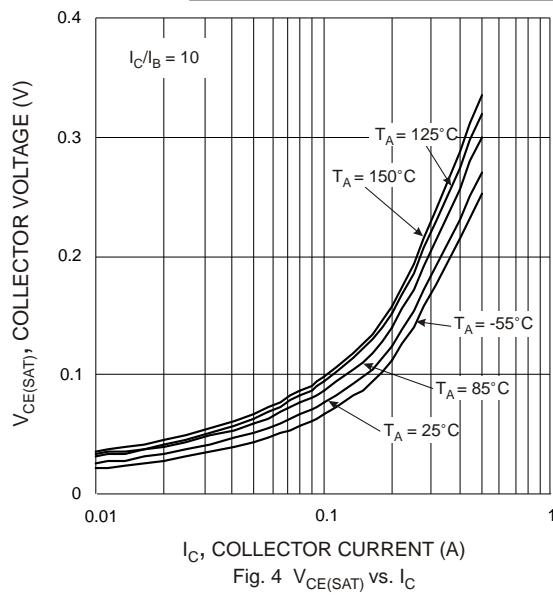
Typical Characteristics T_A , AMBIENT TEMPERATURE (°C)

Fig. 3, Max Power Dissipation vs Ambient Temperature

Typical Pre-Biased PNP Transistor (Q1) Characteristics



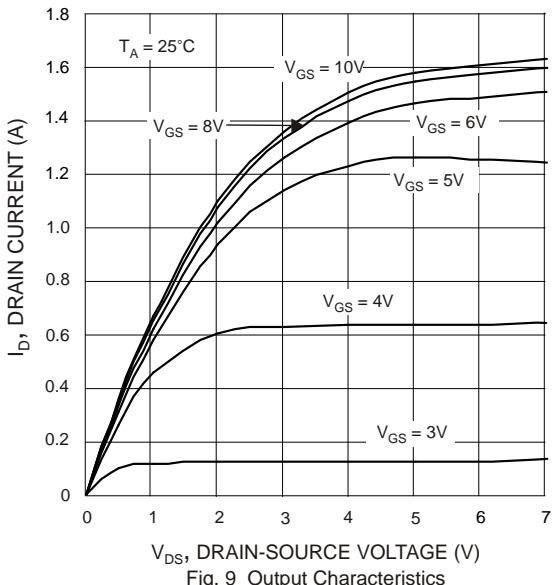


Fig. 9 Output Characteristics

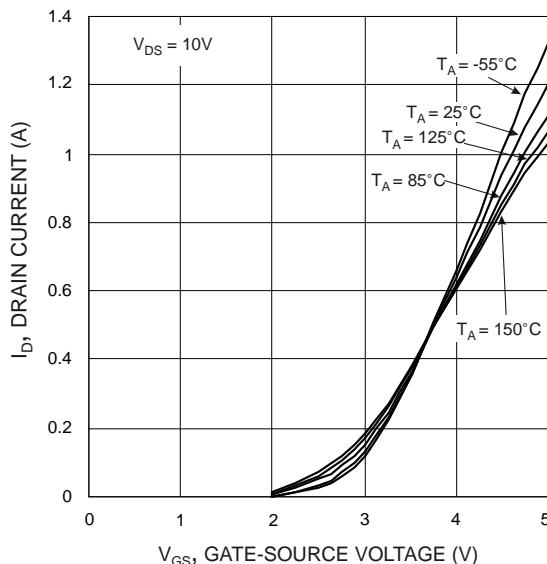
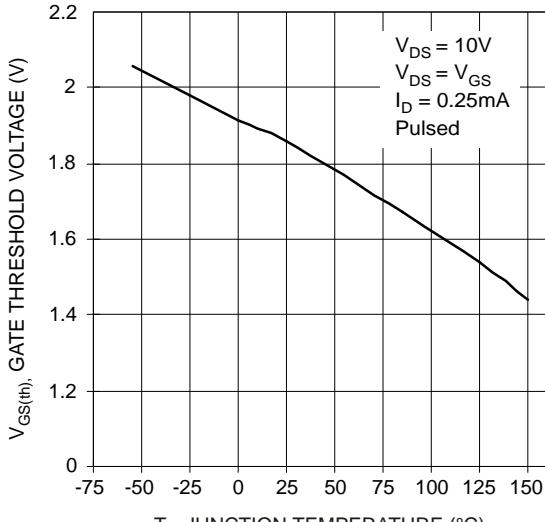
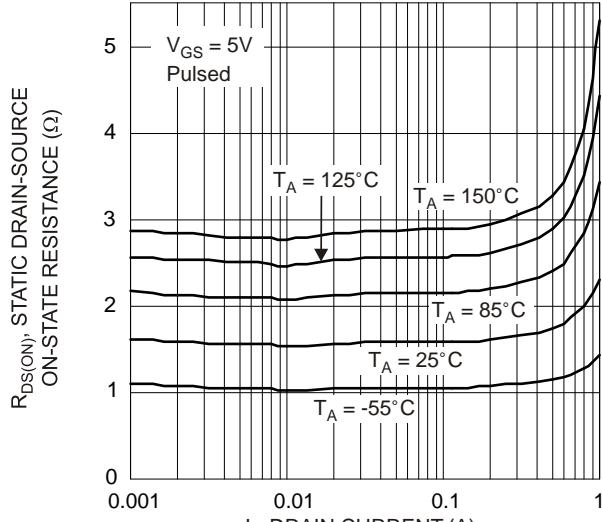
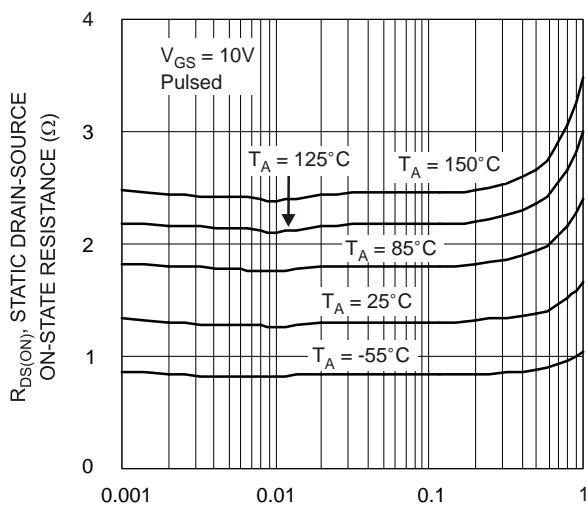
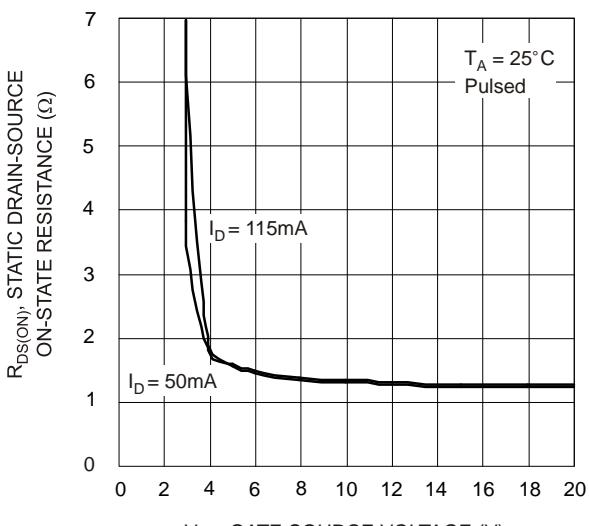


Fig. 10 Transfer Characteristics


 Fig. 11 Gate Threshold Voltage
vs. Junction Temperature

 Fig. 12 Static Drain-Source On-Resistance
vs. Drain Current

 Fig. 13 Static Drain-Source On-Resistance
vs. Drain Current

 Fig. 14 Static Drain-Source On-Resistance
vs. Gate-Source Voltage

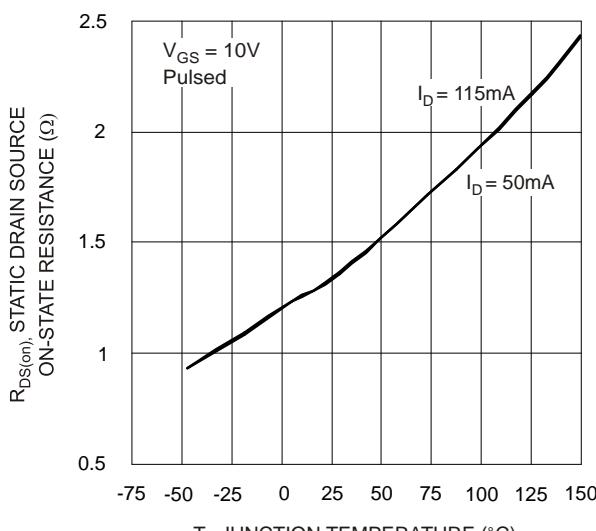


Fig. 15 Static Drain-Source On-State Resistance
vs. Junction Temperature

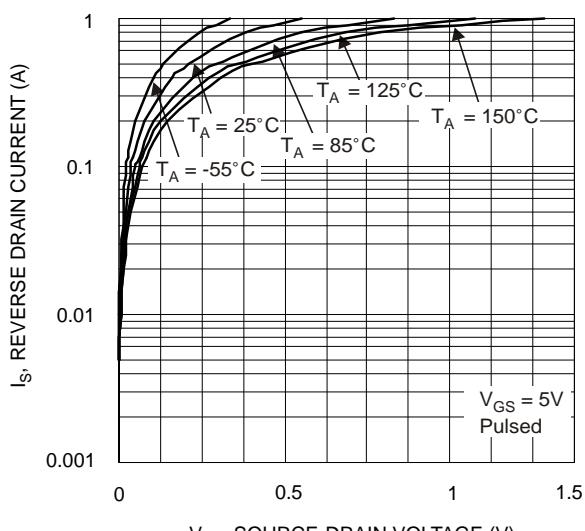


Fig. 16 Reverse Drain Current
vs. Source-Drain Voltage

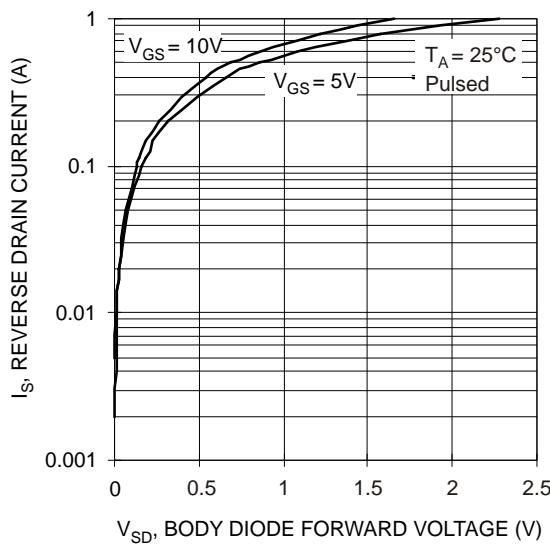


Fig. 17 Reverse Drain Current
vs. Body Diode Forward Voltage

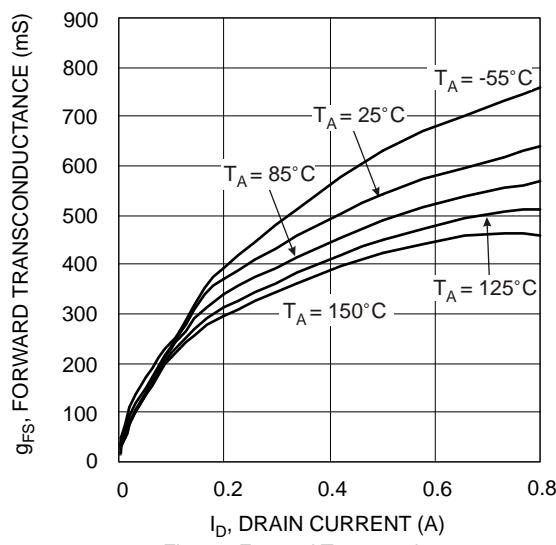


Fig. 18 Forward Transconductance
vs. Drain Current ($V_{DS} > I_D R_{DS(\text{ON})}$)

Application Details

- PNP Transistor (DDTB142JU) and N-MOSFET (DSNM6047) with gate pull-down resistor integrated as one in LMN200B01 can be used as a discrete entity for general purpose applications or as an integrated circuit to function as a Load Switch. When it is used as the latter as shown in Fig 19, various input voltage sources can be used as long as it does not exceed the maximum ratings of the device. These devices are designed to deliver continuous output load current up to a maximum of 200 mA. The MOSFET Switch draws no current, hence loading of control circuit is prevented. Care must be taken for higher levels of dissipation while designing for higher load conditions. These devices provide high power and also consume less space. The product mainly helps in optimizing power usage, thereby conserving battery life in a controlled load system like portable battery powered applications. (Please see Fig. 20 for one example of a typical application circuit used in conjunction with voltage regulator as a part of a power management system)

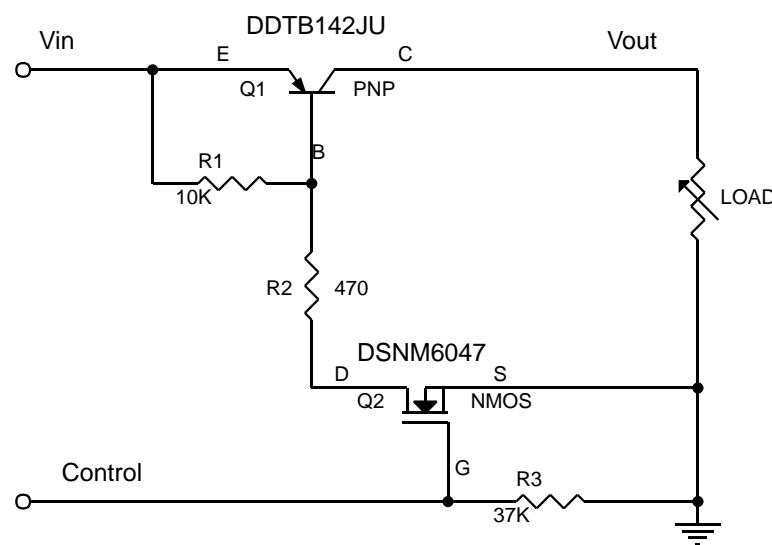


Fig. 19 Circuit Diagram

Typical Application Circuit

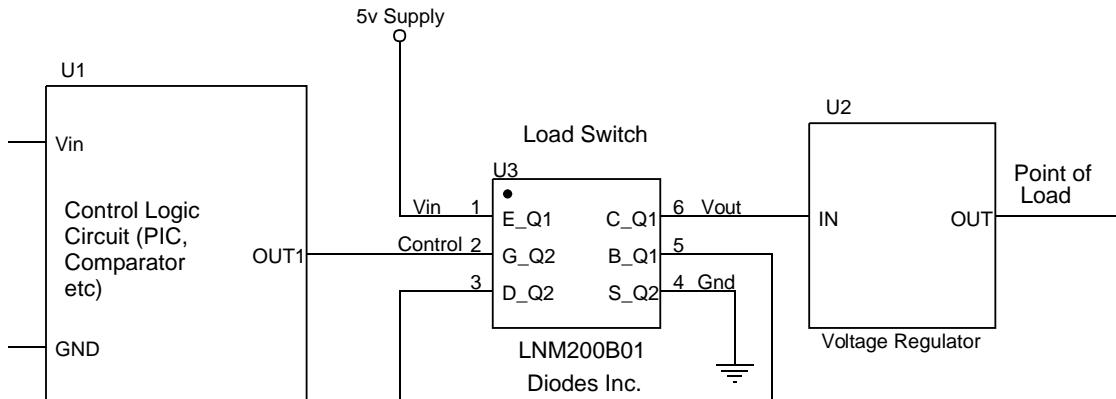
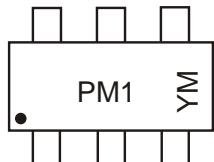


Fig. 20

Ordering Information (Note 5)

Device	Marking Code	Packaging	Shipping
LMN200B01-7	PM1	SOT-26	3000/Tape & Reel

Note: 5. For Packaging Details, go to our website at <http://www.diodes.com/datasheets/ap02007.pdf>.

Marking Information

PM1 = Product Type Marking Code,
 YM = Date Code Marking
 Y = Year ex: T = 2006
 M = Month ex: 9 = September

Fig. 21

Date Code Key

Year							2006	2007	2008	2009
Code							T	U	V	W

Month	Jan	Feb	March	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Mechanical Details

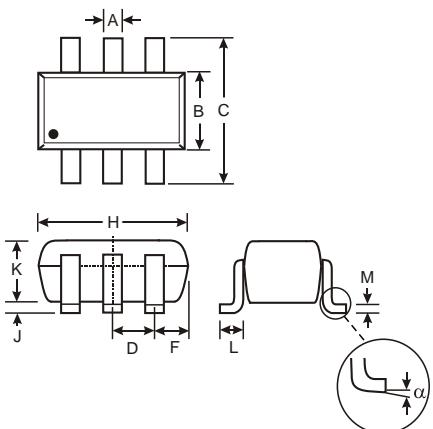


Fig. 22

SOT-26			
Dim	Min	Max	Typ
A	0.35	0.5	0.38
B	1.5	1.7	1.6
C	2.7	3	2.8
D	-	-	0.95
F	-	-	0.55
H	2.9	3.1	3
J	0.013	0.1	0.05
K	1	1.3	1.1
L	0.35	0.55	0.4
M	0.1	0.2	0.15
	0°	8°	-

All Dimensions in mm

Suggested Pad Layout: (Based on IPC-SM-782)

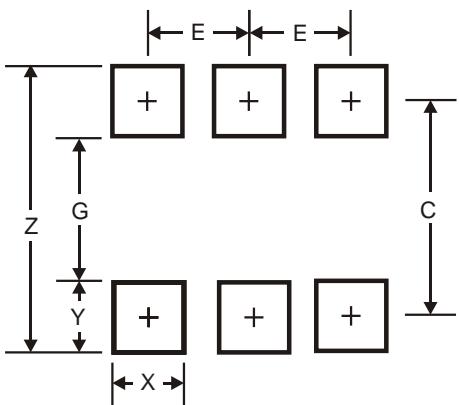


Fig. 23

Figure 23 Dimensions	SOT-26*
Z	3.2
G	1.6
X	0.55
Y	0.8
C	2.4
E	0.95

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